A 55 nm HV-CMOS Pixel Sensor Design for High-Energy Particle Tracking with High Hit Rate and Precise Time Resolution

Leyi Li[1,6], Xiaomin Wei[2], Xiaoxu Zhang[1,4], Yang Zhou[1], Mei Zhao[1], WeiGuo Lu[1], Zexuan Zhao[2], Huimin Wu[2], Yue Zhao[2], Zheng Wei[2], Yang Chen[5], Yujie Wang[5], Zhan Shi[5], Jianpeng Deng[3], Pengxu Li[3], Hongbo Zhu[3], Meng Wang[6], Jianchun Wang[1], Yiming Li[1]

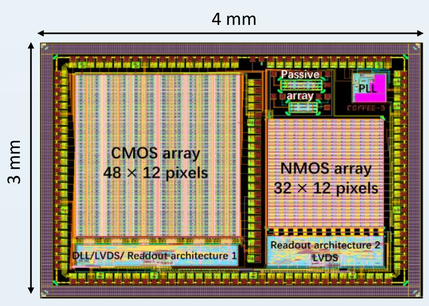
[1]Insitute of High Energy Physics, CAS, Beijing, China [2]Northwestern Polytechnical University, Xi'an, China
[3]Zhejiang University [4]Nanjing University, Nanjing, China [5]Dalian Minzu University, Dalian, China [6]Shandong University, Qingdao, China

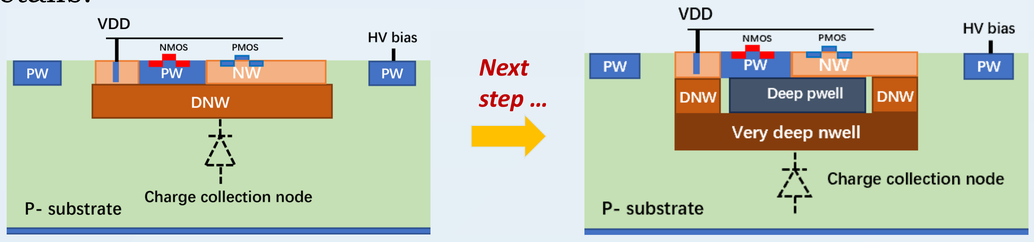
Introduction

This work presents a design framework of a High-Voltage CMOS pixel sensor for high energy particle tracking, which can provide a time resolution of few nanosecond order under the hit rate exceeding 100 MHz/cm^2. The design is based on a **55nm** CMOS process and implemented in the **COFFEE3** prototype. A complete readout architecture has been integrated into a 40 × 145 μm^2 pixel to account for potential process modifications and to prepare for large-scale ASIC development.

Process and Prototype

The COFFEE3 prototype incorporates two architectures: The CMOS array based on modified quintuple-well process , for applications requiring high-precision time resolution under high hit density; The NOMS array based on triple-well process for low power consumption application, please refer to *Bingchen's* poster for more details.





Current process: triple-well, low resistivity ~ 10 Ω•cm (Now)
Large equivalent capacitance
Depletion zone ~ 10 um

Modified process: quintuple-well, high resistivity ~ 1-4k Ω•cm (Future)
↓ Equivalent capacitance ~ 200 fF
↑ Thick depletion zone > 100 um

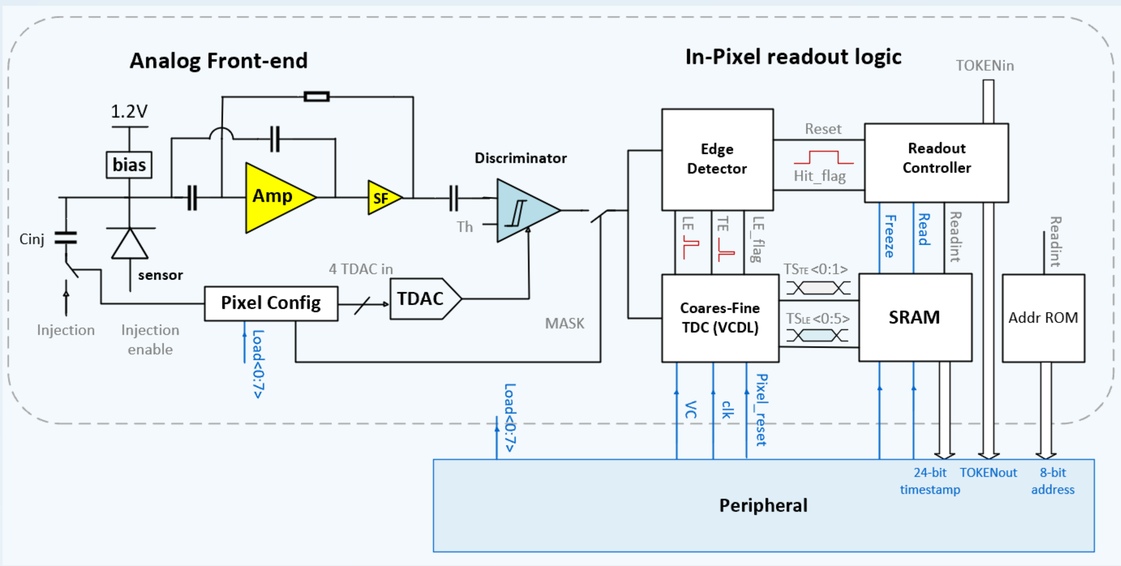


Fig 1. The in-pixel schematic of the CMOS array, including the periphery. Signal collection, amplification, and digitization are all implemented within each individual pixel. Furthermore, a pixel-level coarse-fine **Time-to-Digital Converter (TDC)** is also integrated into each pixel; the **leading edge (LE)** and **trailing edge (TE)** time information of particle hits is first stored locally within the pixel, then transmitted along with the address of the activated pixel to the bottom of the array in priority order.

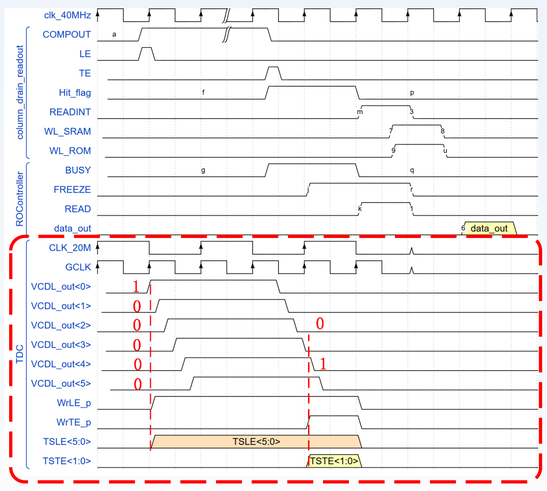


Fig 2. The timing diagram of the in-pixel readout circuitry, illustrating the complete process from the discriminator output to the data packet output and the working principle of in-pixel coarse-fine TDC.

Delay line Coarse-fine TDC

- A 20 MHz Gray-coded clock as input
- A 40 MHz coarse timestamp (25 ns) is internally generated
- Only hit pixels generate fine timestamp from their discriminator output

✓ **Reduce power consumption**

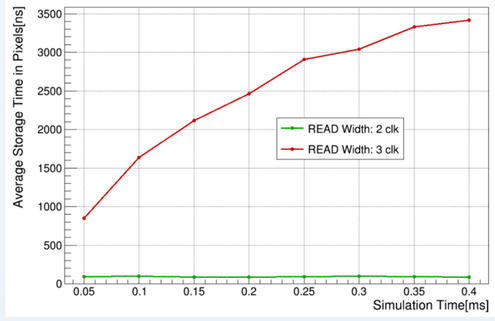
- **Timestamp of LE: 6 bins ~ 4.17 ns**
- Refer to *Yuman's* poster for the related test results

✓ **TDC quantization noise contribution to the time resolution uncertainty is < 2 ns**

Simulation

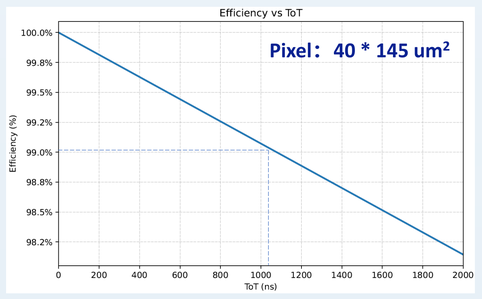
1. Hit Density

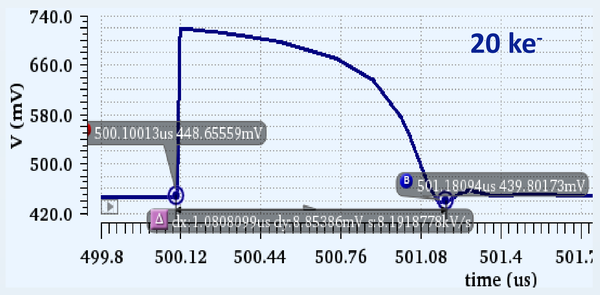
☐ Digital pile-up



- READ = 3 clock cycles → longer in-pixel storage before readout; Causing digital pile-up
- READ = 2 clock cycles → near-zero storage
- In this design, the width of READ signal designed to be adjustable

☐ Analog pile-up

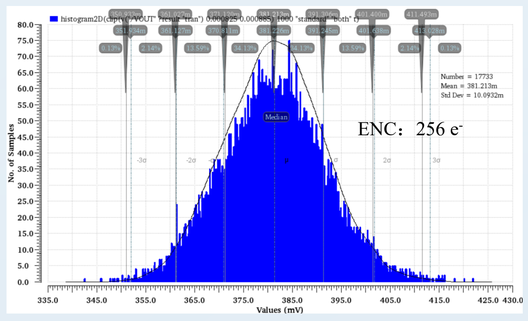




The CSA output waveform width for a 20 ke$^-$ input charge is limited to 1 μs, ensuring a <1% detection efficiency lost due to analogue pile-up while the hit density reach ~100Mhz/cm^2.

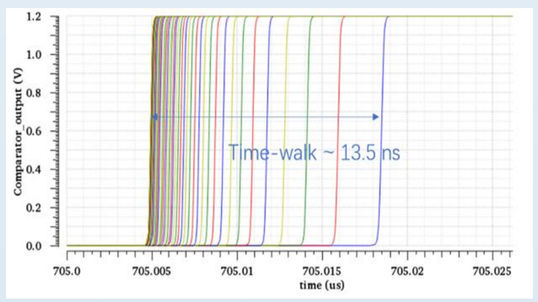
✓ **High hit rate processing capability**

2. Noise



- Based on the modified high resistivity process, **Cd ~ 200 fF**
- ENC ~ 256 e$^-$
- Each pixel integrates a 4-bit DAC for individual threshold configuration

3. Time-walk



- Cd ~ 200 fF
- Signal range: 1.8k - 16 ke$^-$, time-walk ~ 13.5 ns

$$\sigma_{TW}^2 \ contribution < (4\ ns)^2$$

✓ **The time-walk contribution to the time resolution uncertainty is < 4 ns**

Conclusion & outlook

The CMOS array in COFFEE3 prototype for high hit density and time precision was developed in a 55nm CMOS process. We have also achieved the improved column readout and TDC integration within the pixels, laying the research foundation for future expansion to larger chips. The total time accuracy is expected to be less than 5ns, including contributions from signal collection time, time-walk effects, jitter and the quantization noise of the TDC. The testing work for evaluating the readout architecture final performances are still actively in progress.

Email: lyli@ihep.ac.cn