

A low-power 55 nm HV-CMOS pixel sensor readout architecture for the CEPC Inner Tracker

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Introduction

The HV-CMOS pixel sensor has been confirmed as the baseline technical solution for the inner tracking (ITK) detector of the CEPC. It needs to provide ~ns time resolution and <10 μm position under the condition of <200 mW/cm² power consumption.

On the basis of meeting the requirements of CEPC, two different readout architectures are proposed. The first one aims to further increase the upper limit of hit density (>100 MHz/cm²) that HV-CMOS technology can handle (refer to Leyi Li's Poster). The other one target to further reduce the average power consumption of the HV-CMOS pixel sensor to simplify the requirements of the cooling system; this readout concept could also be used to further reduce the position resolution and improve data accuracy. (This Poster)

The power consumption theory

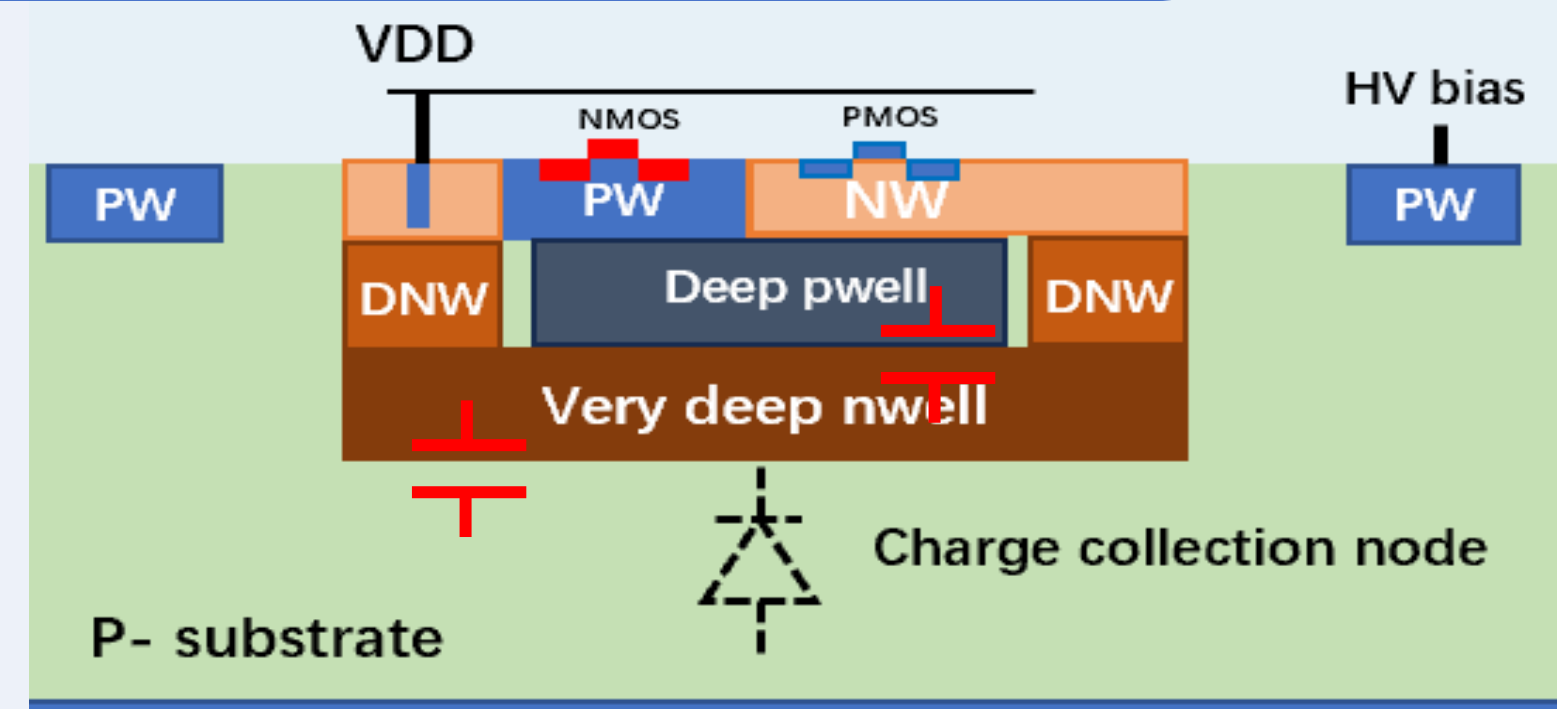


Fig 1. The pixel cross section view of a typical HV-CMOS sensor. The very deep N-well (VDNW) and P-type substrate formed the charge collection electrode. Charge-sensitive amplifiers (CSA) and readout electronics can be integrated nearby within the pixel

Working principle:

- The power consumption of a HV-CMOS pixel sensor (typically contains ~100000 pixel unit) mainly from the in-pixel electronics.
- The response time of a CSA proportional to the capacitance of the sensor diode (C_d) and inversely proportional to the transconductances of the transistor used for the amplifier (g_m), as given by:

$$\tau_{CSA} \propto \frac{1}{g_m} \frac{C_d}{C_f}$$

- g_m is normally proportional to the consumed current. The relationship is:

$$g_m = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_{DS}}$$

- Time walk is the main contributing source to time resolution. It is proportional to the time response of the CSA and the threshold (V_{TH}) of the comparator, and inversely proportional to the minimum signal quantity, which can be expressed as:

$$TW \propto \tau_{CSA} \frac{V_{TH}}{V_{sig,min}}$$

Conclusion:

For a determined temporal response, a smaller C_d and large signal are crucial to reduce the power consumption of the pixel sensor.

The C_d theory

The main contributions of C_d :

- The capacitance between Deep pwell (DPW) and VDNW;
- The capacitance between the signal collection electrode VDNW and P-sub;

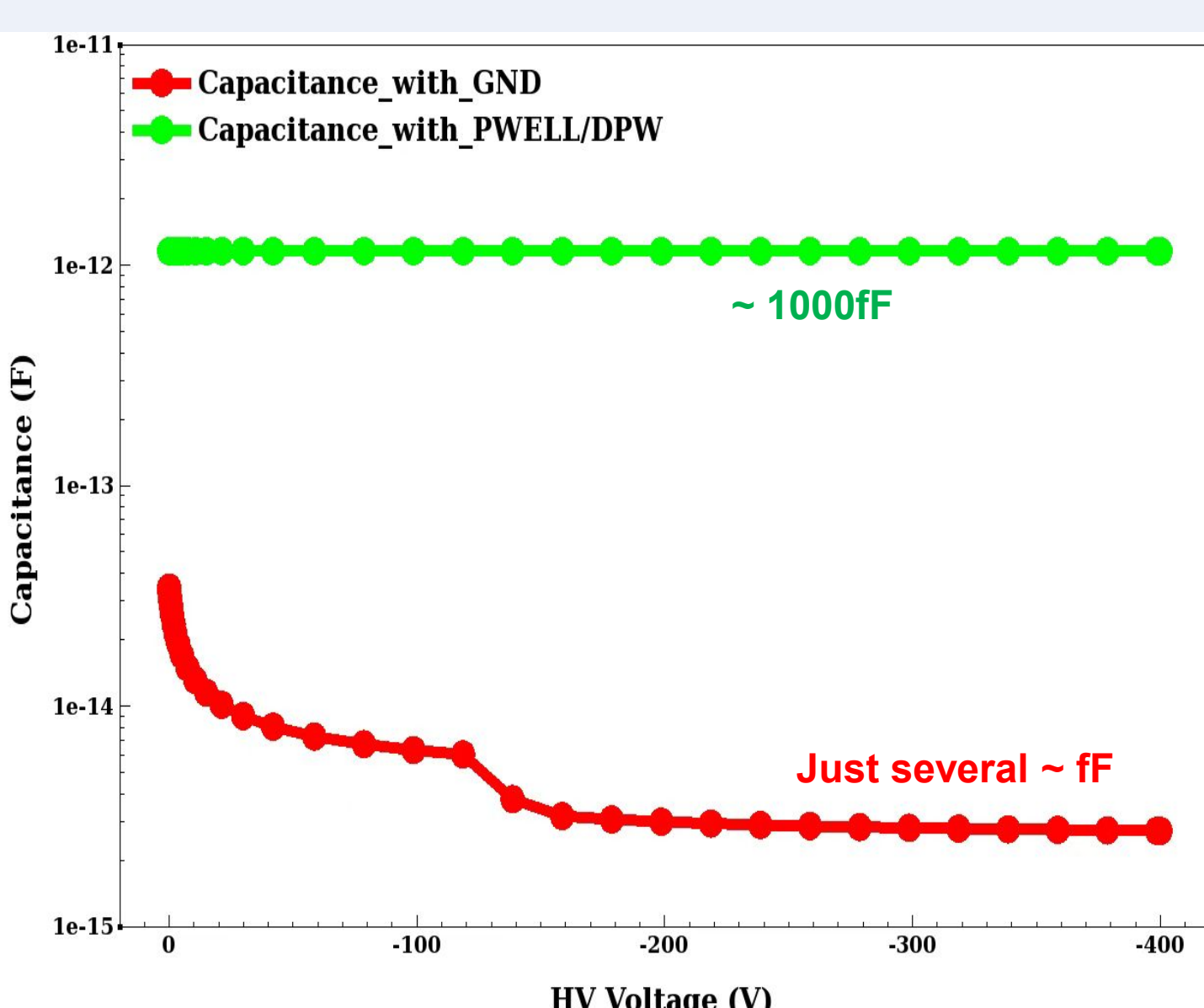
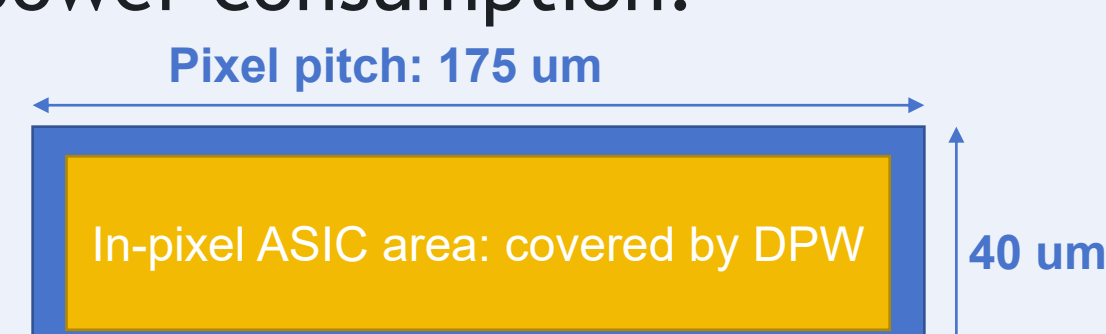


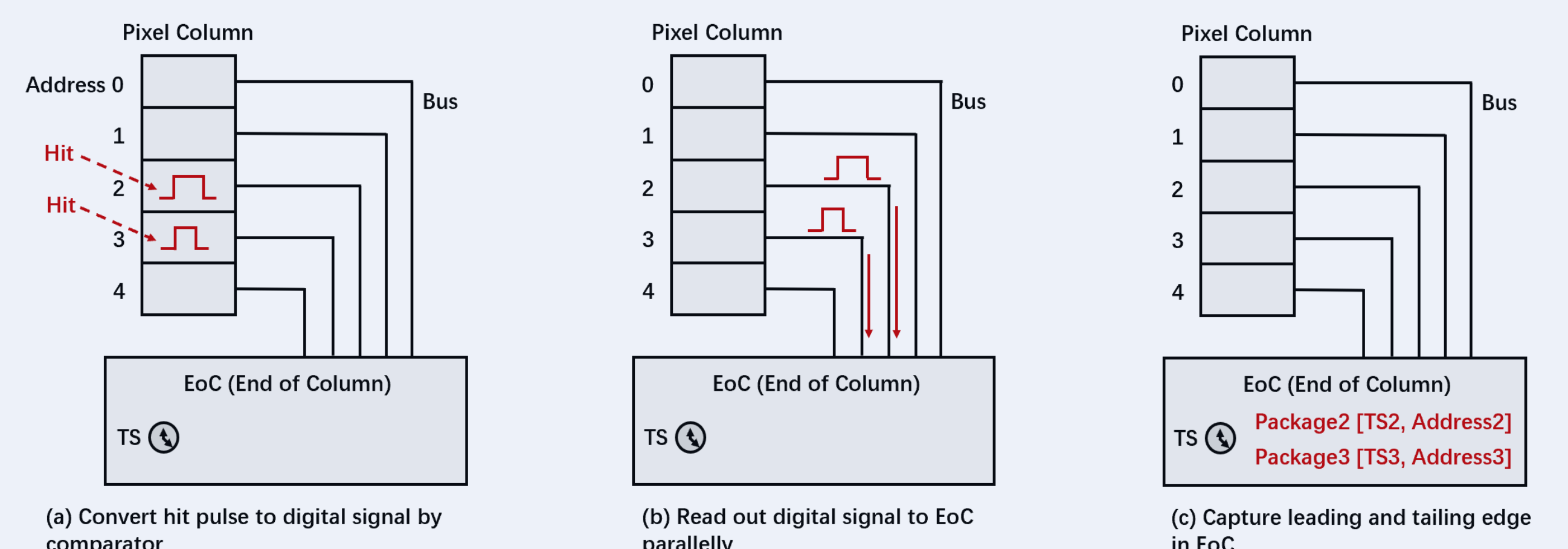
Fig. TCAD simulation results of the relationship between the C_d value and bias voltage of a typical HV-CMOS pixel. The pixel size is set at 40*175μm², most of the size is covered by DPW. The doping conditions are derived from speculation. Only the changing trends and proportions of the two capacitance sources are referenced.

Conclusion:

- Small in-pixel ASIC layout size is most important for less C_d ; After the high-voltage reaches 200V, it is also the main source of C_d ;
- A simple in-pixel electronic structure is very beneficial for low power consumption.

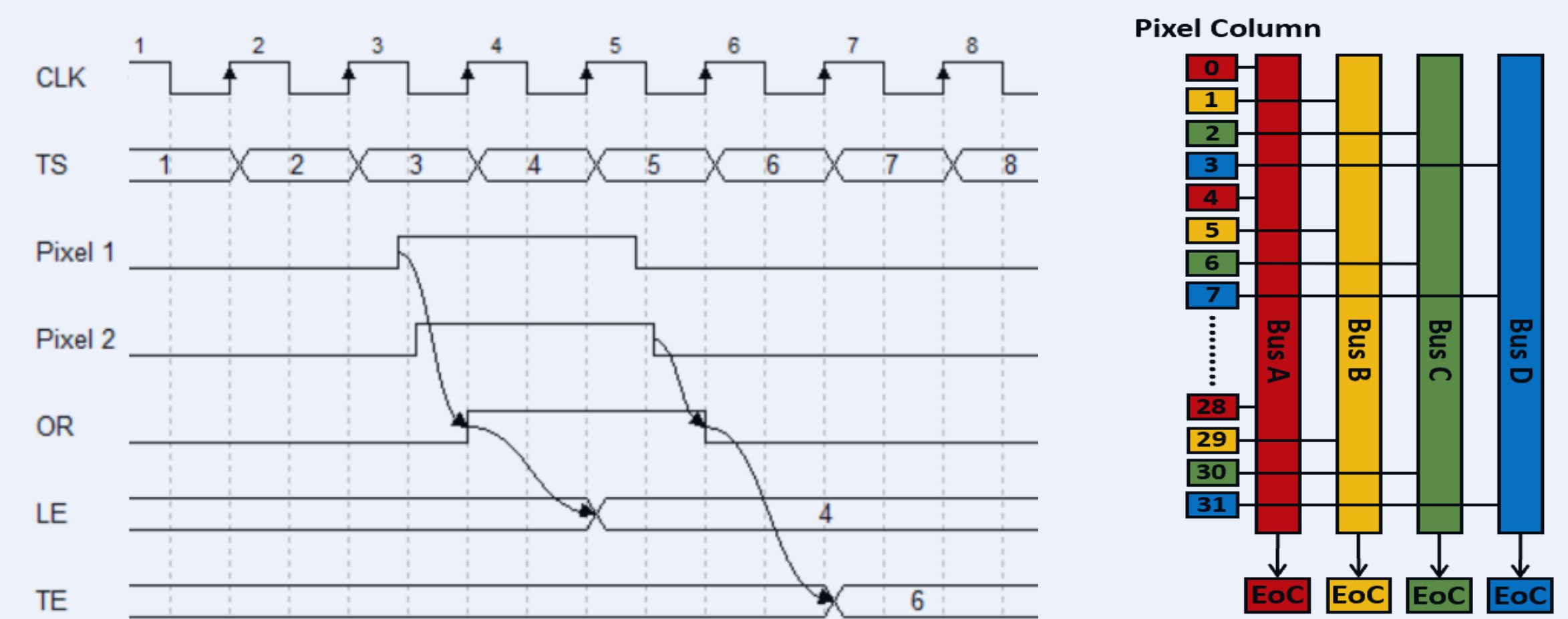


The low-power readout architecture



Read out concept of the pixel matrix: The signal output of each pixel is transmitted in parallel to the bottom of the column for further processing. It is characterized by the fact that the pixel can only contain an amplifier and a comparator, occupying very little area to achieve a smaller C_d value.

Multiple pixels simultaneously fired in a column, may lead to inaccuracies in time stamps.



To overcome such issues. Each column of pixels can be divided into 4 groups, input to 4 distinct EoC modules. Each EoC module contains two separate state machines and time-stamp counters, ensuring accurate time information even when particles hit adjacent pixels (charge sharing effect) or multiple pixels in the same column fired simultaneously.

Implementation of the readout architecture

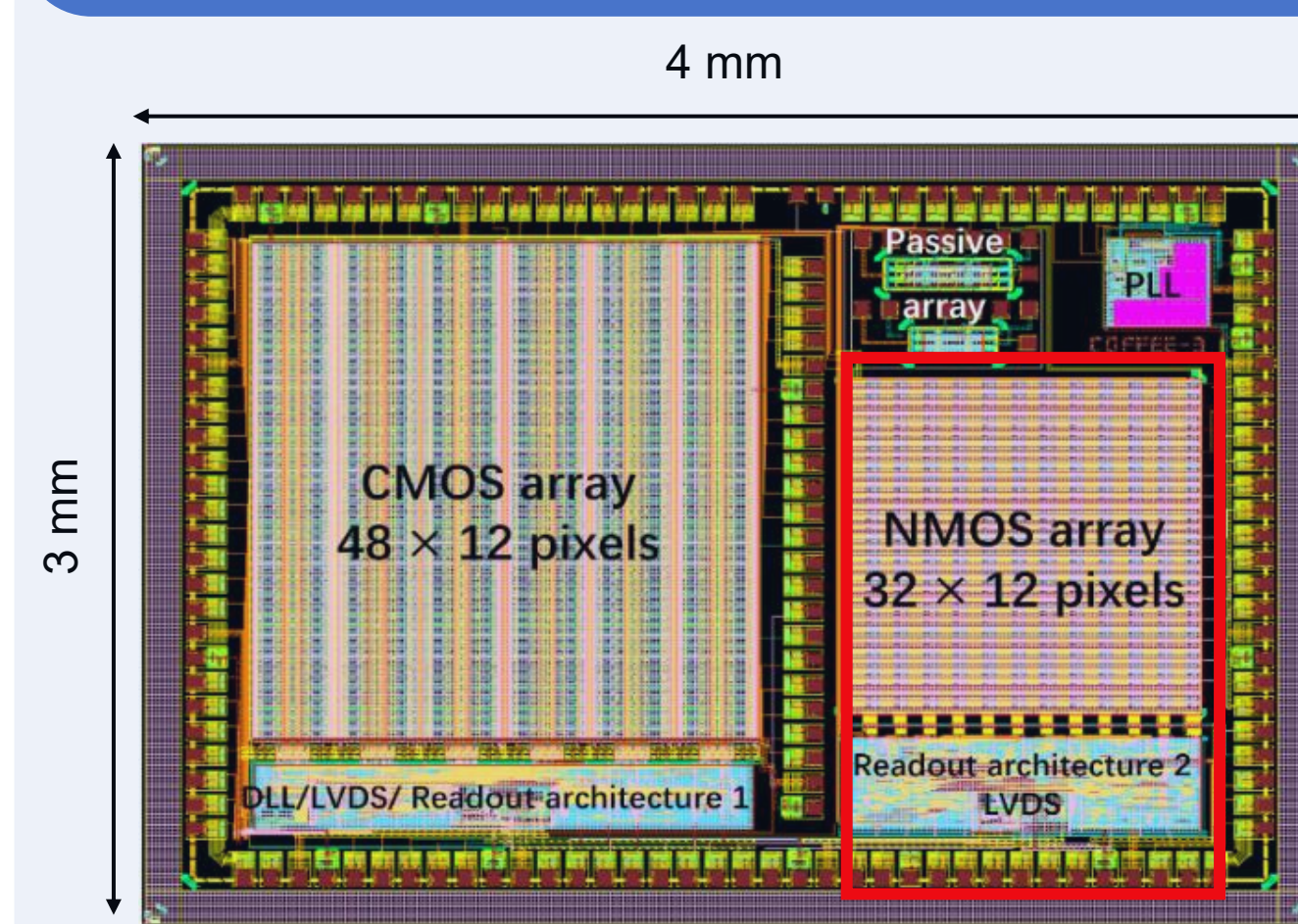


Fig. Layout of the COFFEE3, submitted Jan. 2025. The proposed architecture have implemented in the area circled in red in the above figure. The current process substrate resistivity is 10 Ω·cm, breakdown voltage is ~70V, depletion depth is ~10 μm.



Fig. Response of full readout chain with laser test: Sensing diode → in-pixel (CSA/comparator/TDC) → EoC (digital peripheral) → data link → DAQ (refer to Boxin Wang's Poster)

Summary & outlook

On the basis of meeting the requirements of CEPC, we have proposed and preliminarily verified an 55nm HV-CMOS pixel sensor readout architecture on that has the potential to further reduce power consumption or improve position resolution accuracy.

The next step will focus on optimizing the process, increasing the breakdown voltage, and reducing the contribution of VDNW and P-substrate capacitance to C_d . High-resistivity wafers will be adopted to increase the total signal (from the current ~1000e- to ~16000e-), thereby simplifying the design and power consumption of the in-pixel CSA and further reducing the overall chip power consumption.

A simplified in-pixel design could also be used to further reduce the pixel size to improve position resolution, while this requires more discussions starting from the physical requirements to determine.