ATLAS High Granularity Timing Detector

Zhijun Liang

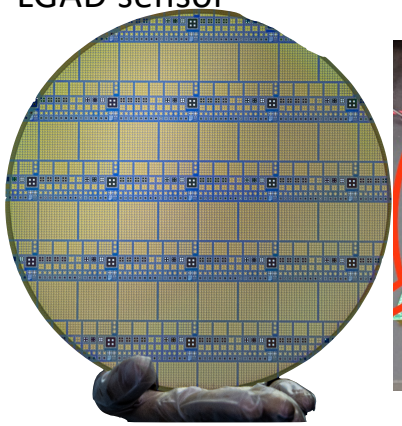
(The Institute of High Energy Physics, the Chinese Academy of Sciences)

梁志均（中国科学院高能物理研究所）

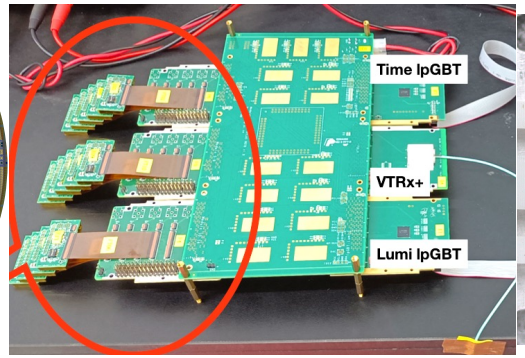
Research Content, Assessment Index (考核指标，研究内容)

- 研究内容： Develop all key components for the Timing Detector
  - Developed radiation hard LGAD silicon sensor
  - Build large-area ASIC+Sensor Module with robot
  - Develop Front-end electronics, high voltage system, flexible cable
- Assessment index （考核指标）:
  - Sensor and detector module time resolution reach 30-50 ps

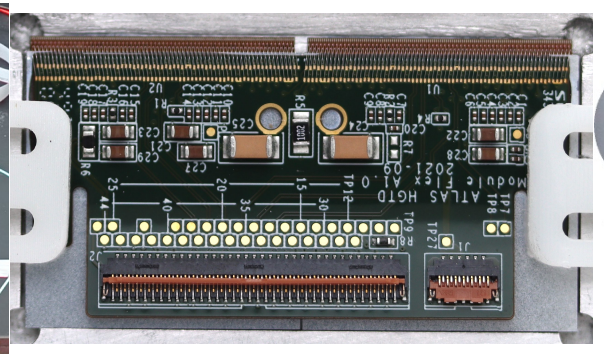
LGAD sensor



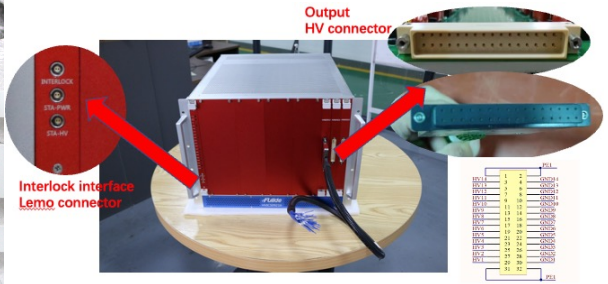
Electronics



Modules



High Voltage supply



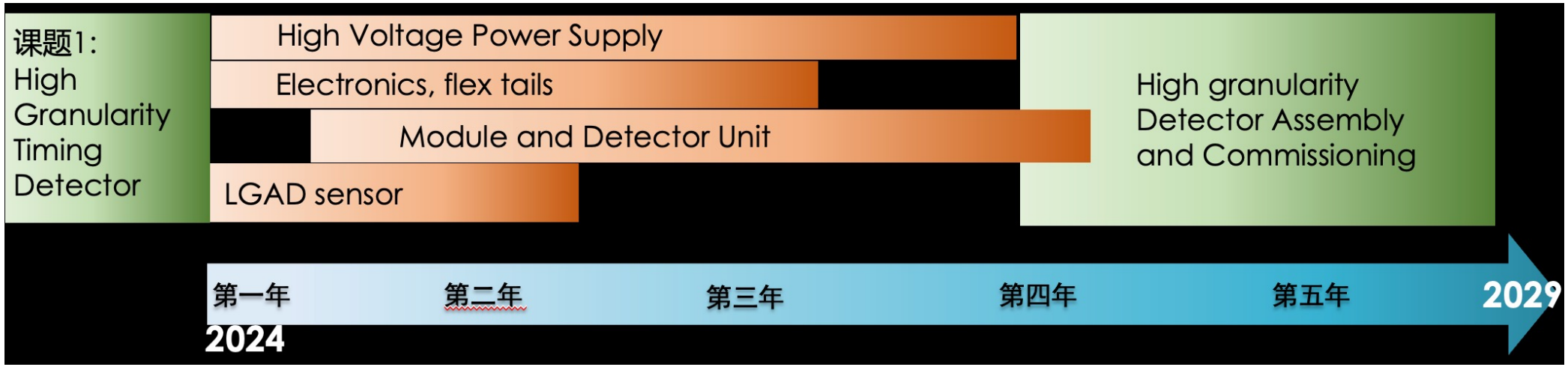
Assessment index status （考核指标）：

- Final goal:
  - Final production sensor and detector module time resolution 30-50 ps
- This year (2nd year or midterm):
  - pre-production sensor and hybrids resolution better than 50ps
    - Irradiated sensor +ASIC hybrids can reach 43ps in test beam

课题目标[1]	预期成果				考核指标[2]				考核方式（方法）及评价手段[4]	本年度指标状态
	预期成果名称			预期成果类型	指标名称	立项时已有指标值/状态	中期指标值/状态[3]	完成时指标值/状态		
在高颗粒度时间探测器方面，研发硅传感器、前端电子学、探测器模块组装等，研制出高时间分辨率的探测器模块与前端读出电路板，其时间分辨率好于 50 皮秒。	**主要成果**	1	高精度时间探测器	□新理论 □新原理 □新产品 ■新技术 □新方法 □关键部件 □数据库 □软件 □应用解决方案 □实验装置/系统 □临床指南/规范 □工程工艺 □标准 □论文 □发明专利 □其他____	时间分辨率（关键核心指标）	小面积原型硅传感器时间分辨率好于 50 皮秒	为 ATLAS 升级研制出正式的硅传感器，时间分辨率达到 30-50 皮秒	探测器模块时间分辨率达到 30-50 皮秒	测试报告、同行评审。	为 ATLAS 升级项目研制出预生产的硅传感器，以及传感器倒装焊后做出裸模块，时间分辨好于 50 皮秒

Status

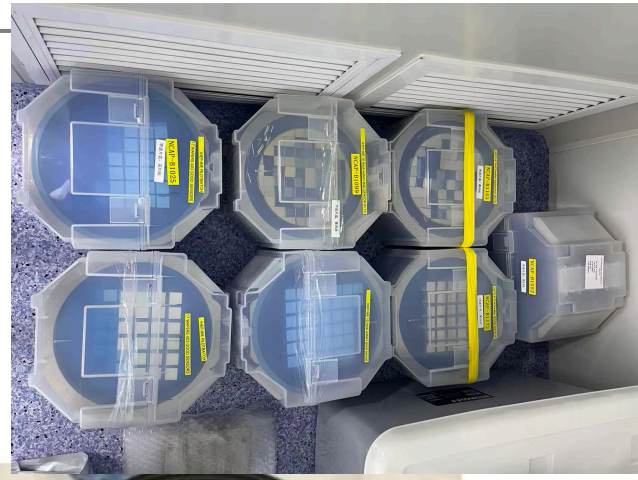
	Prototyping	Pre-production	Production	Delay wrt to task book
Sensor	Done	Done	~15% produced	No delay in general, but In-kind Delayed
ASIC	Done	50% tested	~11% delivered	10 months delayed
Module	Done	Starting	Expected Q3 2025	~10 months delayed
PEB	1/6 prototyped 2/6 designed	Early 2025		~1 year delayed
Flex tails	Done	To be started		~1 year delayed
High voltage power supply	Done	Done	Q2 2025	10 months delayed

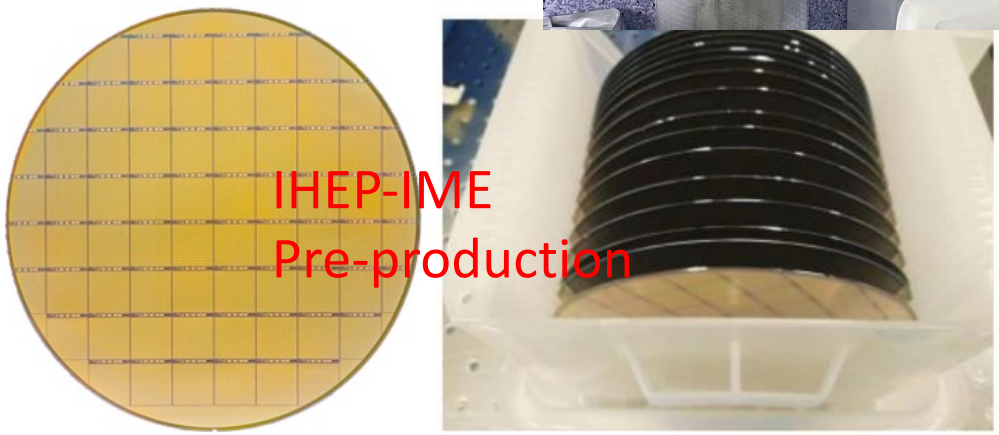


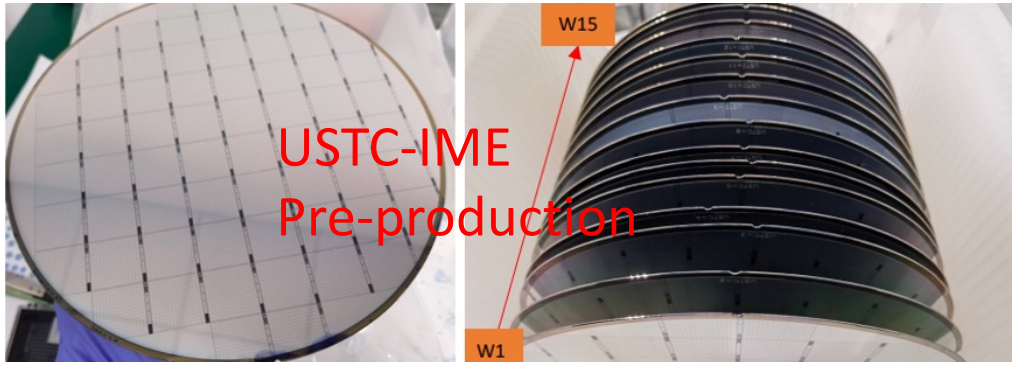
LGAD sensors pre-production and pre

- CERN chosen IHEP-IME sensor in tendering, contract signed in Feb 2025
- The sensor production will be 100% done by China
  - First time domestic silicon sensor was used by CERN
  - IHEP-IME: 90% (66% from CERN tendering+24% in-kind): ~8 m^2
  - USTC-IME: 10% in-kind contribution (~0.8 m^2)
- Production status
  - IHEP
    - pre-production: ~1700 sensor fabricated
    - Production: ~3000 sensor fabricated (~15%)
    - In-kind
  - USTC
    - pre-production: ~270 sensor fabricated

IHEP-IME production



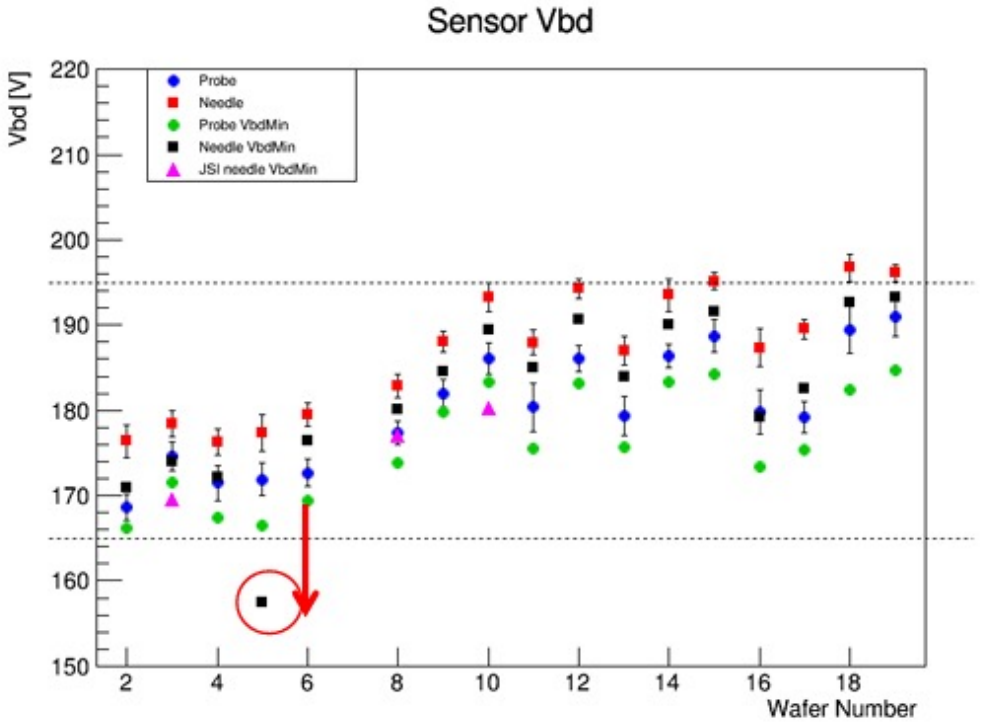




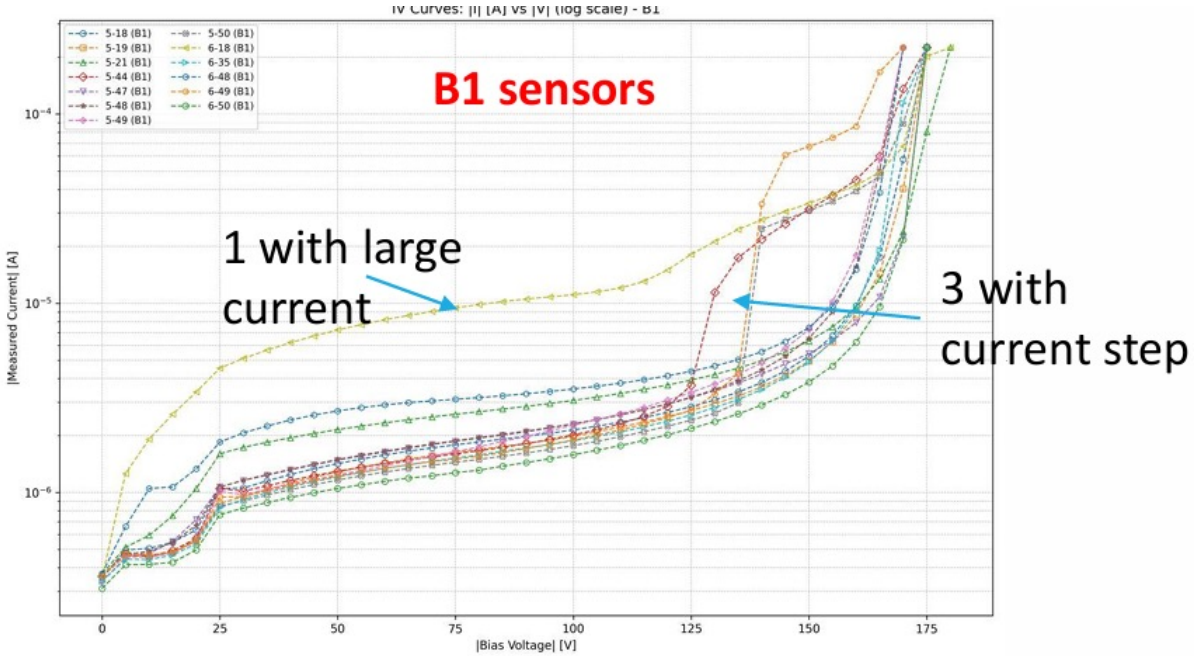
LGAD sensors pre-production and pre

- Critical items: signing of in-kind contributions for China (IHEP + USTC), one year delayed
  - Need to find method to reliably pick ‘good’ cateogory B1 (more in Mei Zhao’s talk)
    - Category A: breakdown voltage (VBD) in range (165V, 195V)
    - Category B1: VBD in range (150V, 165V)

Sensor qualification tests in production

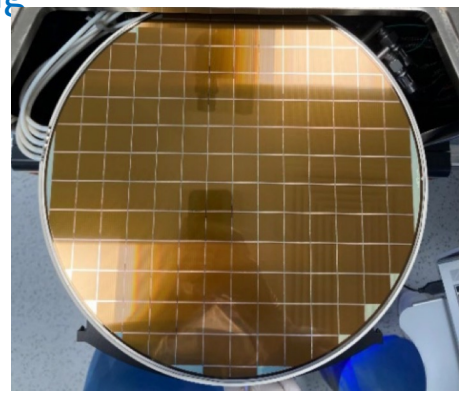


Hybrids I-V curve with Category B1 sensors

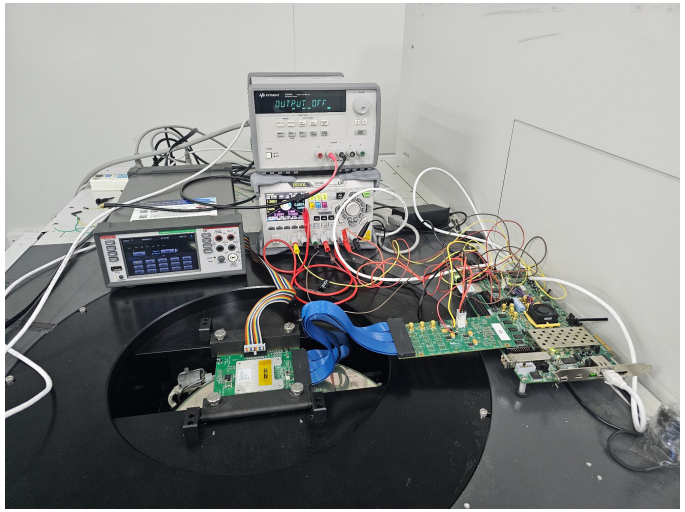


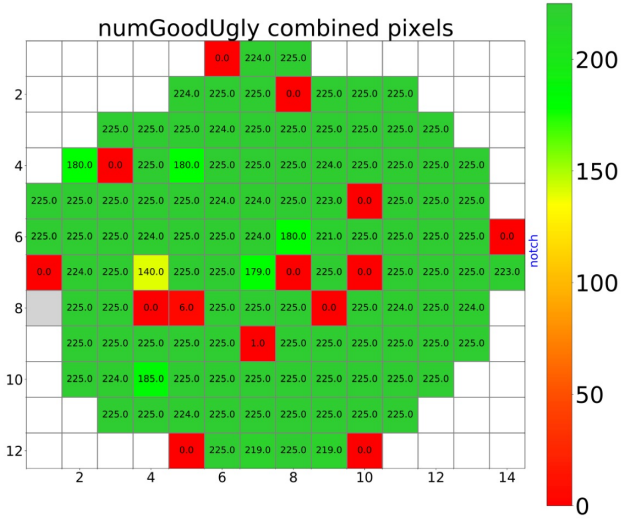
ASIC production and testing

- China and IJClab/Omega share 50% of wafer probe test （~225 wafers)
  - Agreements was probe cards, and evaluation criteria should have been defined by IJCLab
  - IHEP is now much advanced, IJClab recently gave up testing in France, will move to China for testing
- Issue:
  - ASIC wafer testing has been the bottle neck for the project for sometime (in critical path)
    - PRR was scheduled at Oct 2024, now passed PRR July 2025 (delayed by ~10 months)
    - TSMC finished production, 25 wafer (11%) delivered to CERN.
  - ~10% ASIC short issue → use new dicing scheme. (technical risk)
  - We still working on Tax free import ASIC wafers to China (policy risk)
    - Contract with CERN signed, iterating with Chinese custom, expect green light at the end of 2025.

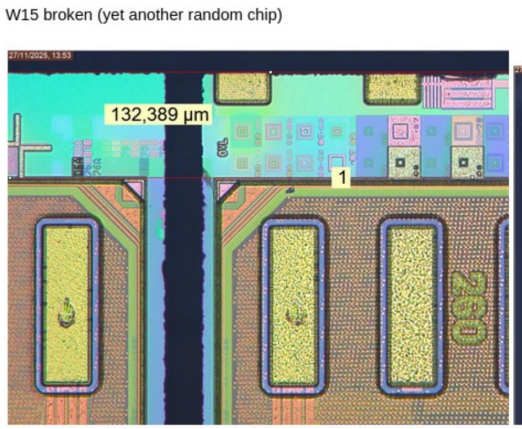


ASIC Yield is 70 ~ 80%

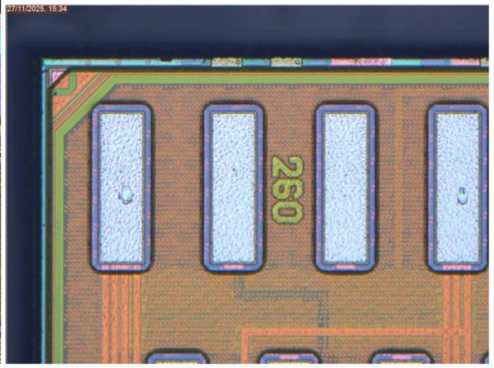




new dicing scheme



old dicing scheme



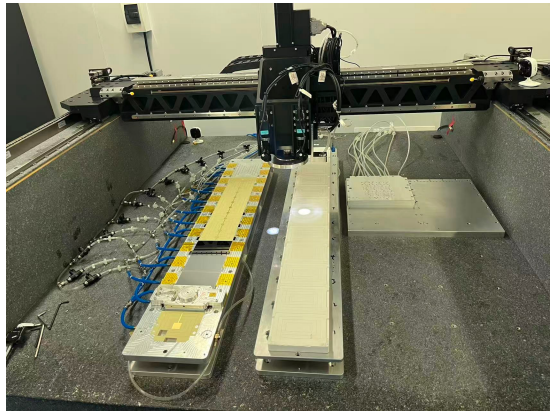
Module and detector units

- 5 production site at HGTD (China, Mainz (Germany), France, IFAE(Spain), Morocco)
  - China is largest site, will assemble 44% of the module (~4000 modules)
    - China module team included IHEP/USTC/SDU/SJTU/Naikai, assembly lab is in IHEP
- Latest update :
  - IHEP and USTC sites merged (some issue for site merging covered by Lailin)
    - Has explored using AMS gantry in IHEP hall 3 for module loading
  - 150 ALTIROC-A Hybrids fabricated (16% of pre-production)
  - Module flex finished pre-production (480 flexes)
  - Supported unit prototyped, ready for pre-production

ALTIROC-A Hybrids

Support units

Gantry robot @IHEP hall 3

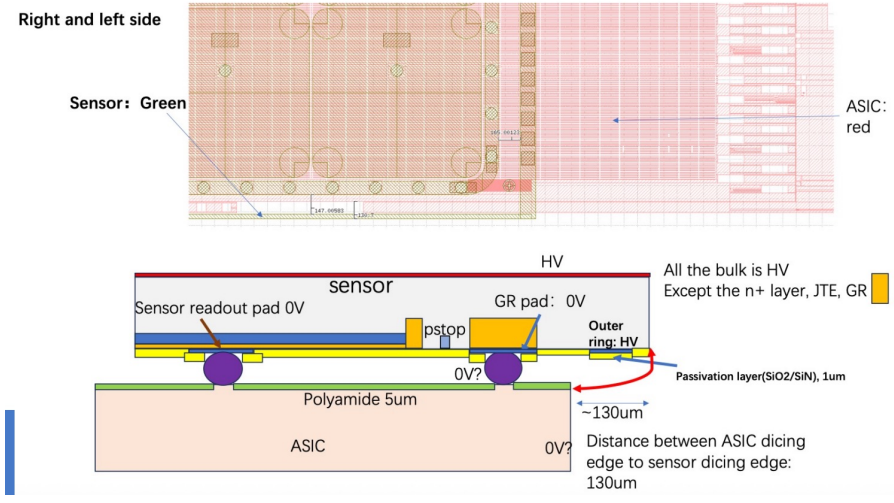


Module flex pre-production

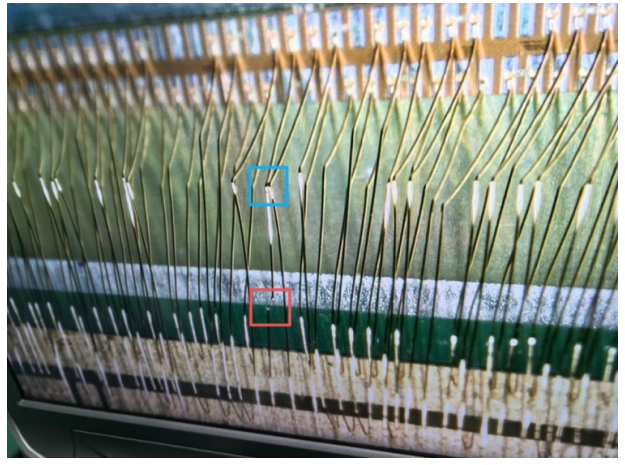
Module and detector units: issue

- Not enough study for Irradiated Hybrids performance (technical risk: high voltage sparking)
  - Only 10 hybrids irradiated, 2 hybrids showed anomalies at -650V
- Module wire bonds touching issue after 120+ thermal cycles (technical risk)
- Slow in setting up for pre-production
  - Finalizing final tooling and algorithm, defining standard procedure
  - Documentation (paper documents traveler) , and records in production database
- Manpower issue for production
  - Need shifters for module assembly/testing/metrology/loading

Hybrids high voltage sparking risk



Module wire bonds issue after thermal cycles

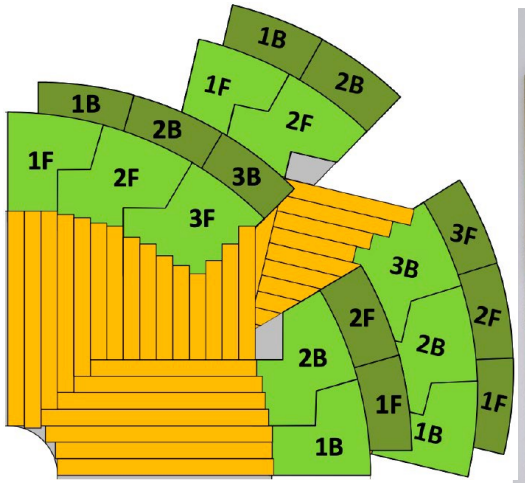


Module	Assembly time	Flex type	120 cycles	150 cycles	180 cycles	210 cycles	225 cycles	Note
FM-A-09	2025.6.10	Prototype	×	√	√	√	-	Wire boding touching at 120, fixed after re-wirebonding
FM-A-10	2025.6.10	Prototype	√	√	√	√	√	-
FM-A-12	2025.9.2	20WMFHP 1A01162	√	×	√	√	-	Wire boding touching at 150, fixed after re-wirebonding
FM-A-13	2025.9.2	20WMFHP 1A02391	√	√	×			Wire boding touching at 180, still not functional after re-wirebonding

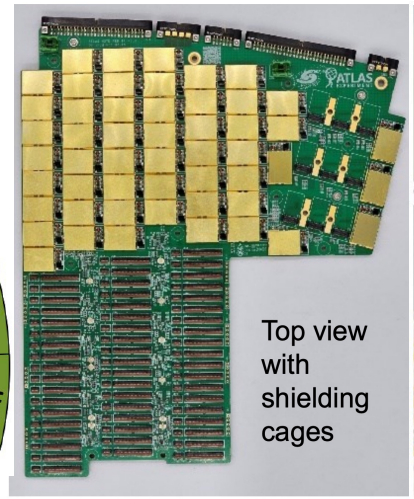
Peripheral Electronics Board (PEB)

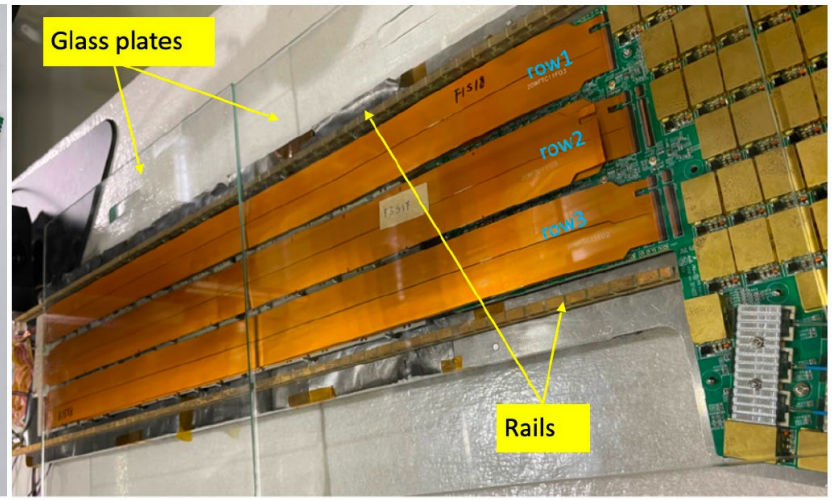
- China (IHEP/NJU) will design and produce 100% PEB (6 PCB boards)
- Challenge: fast communication with 55 modules, 24 metal layers in PCB
- Update:
  - IHEP and NJU developed 1st Peripheral Electronics Boards at early 2024
  - 2nd Peripheral Electronics Boards (PEB 3F) designed in 2025
    - Fabrication Stuck due to CERN BPOL chip irradiation hardness issue

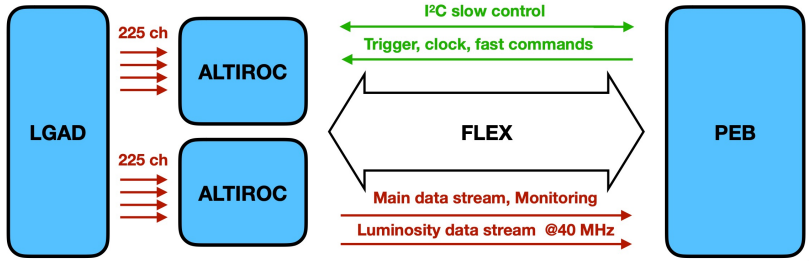
6 types of PEB



PEB1F prototype

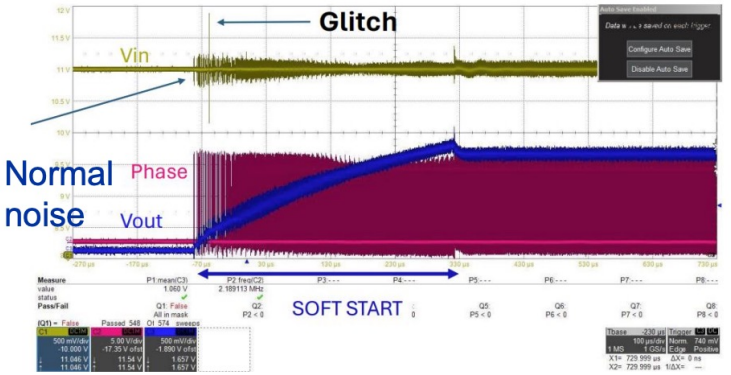




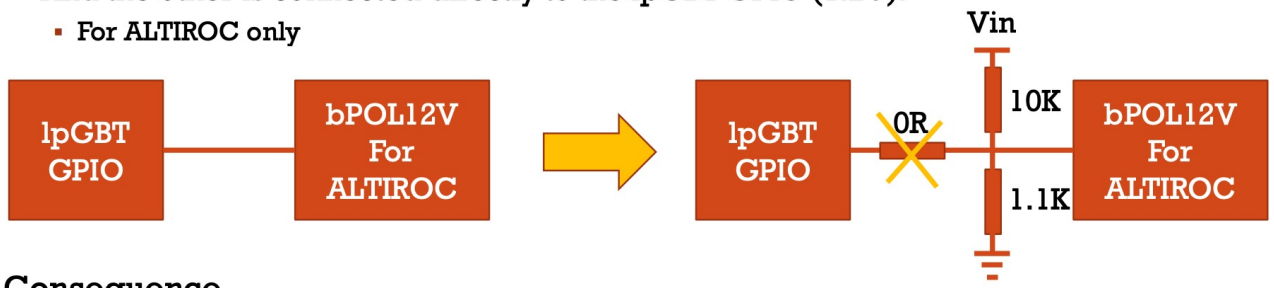


Peripheral Electronics Board (PEB): issue

- Lack of manpower in testing and design
  - Eg: PEB1F testing with ALTIROC-A, low temperature testing
  - Need these data to finalize the rest of PEB design
- CERN BPOL chip irradiation hardness issue
  - Impact to LHC upgrade project
  - Output voltage is too high (glitch) after irradiation
  - Voltage divider solution may not work for HGTD
    - Due to LV current limit (need to iterate with foundry)



- There are two enable configurations (self-starting and controlled start-up):
  - One is implemented via a voltage divider (10kΩ and 1.1kΩ)
    - No impact
  - And the other is connected directly to the lpGBT GPIO (1.2V).
    - For ALTIROC only

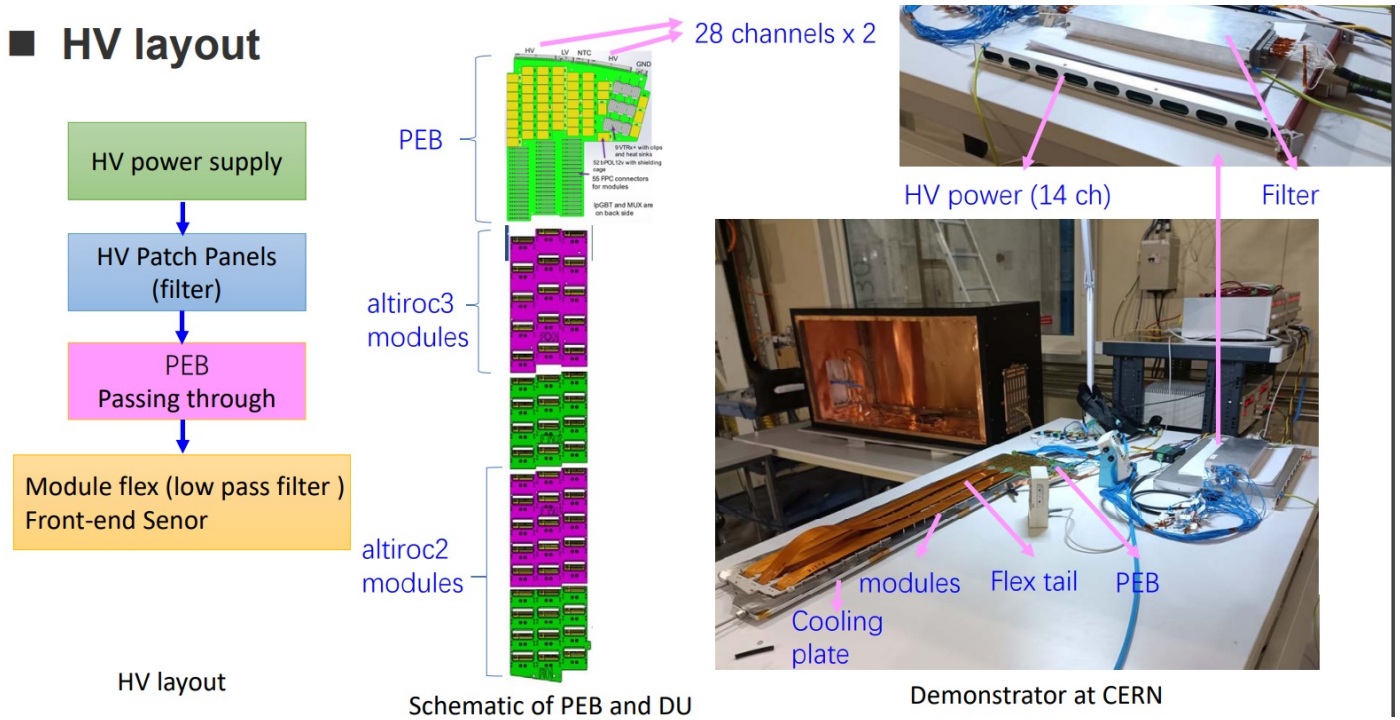


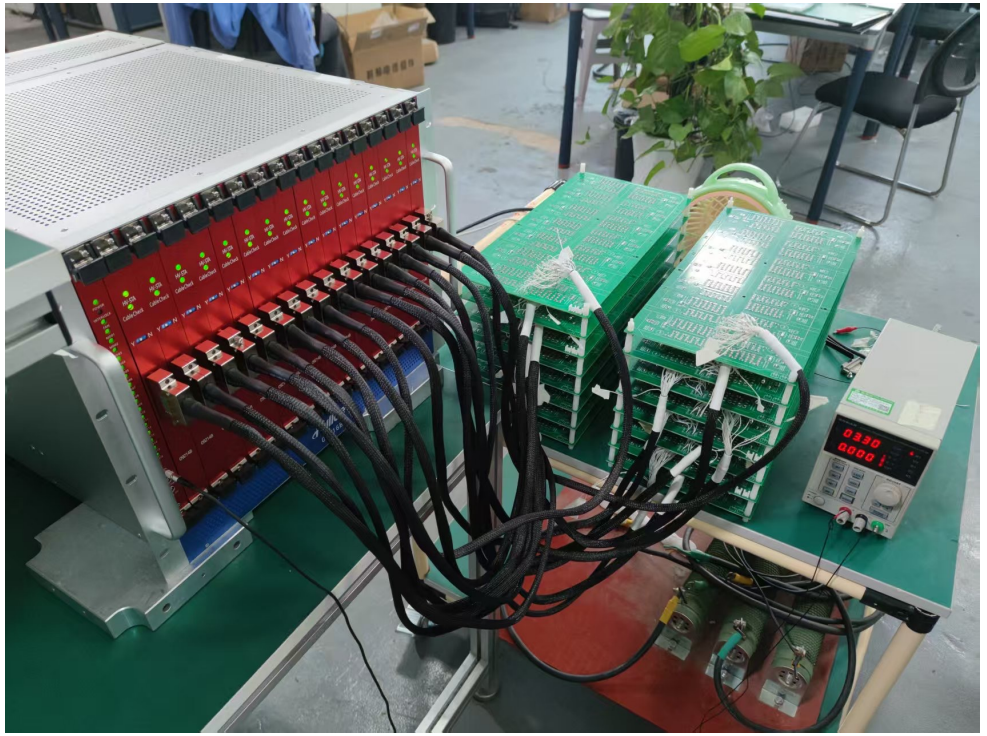
- Consequence
  - Give up VDDD on first, and then config ALTIROC, at last VDDA on
  - All On at the same time, the inrush/surge current is huge, may be x2 larger than normal. LV system will over-current trip.

High voltage (HV) power supply

- China (IHEP/SDU) prototyped and oversee HV supply production and do quality tests
- Challenge: 1000V voltage, 100nA precision in current measurement
- Latest update : pre-production finished in 2025.
  - IHEP/SDU team went to FULLDE this summer for quality assurance tests
  - Two HV crates delivered to CERN in Sep. SDU student doing reception tests.

HV pre-production quality tests





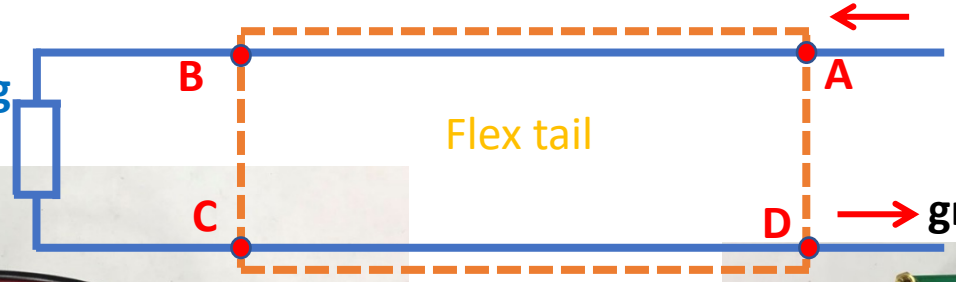
Flex tails（柔性电子学尾板）

- SDU is responsible for 33% of flex tails production
- Prototype has been made, and satisficed the requirement, Ready for pre-production
- Issue: waiting for flex tails length final calculation. one year delayed in pre-production

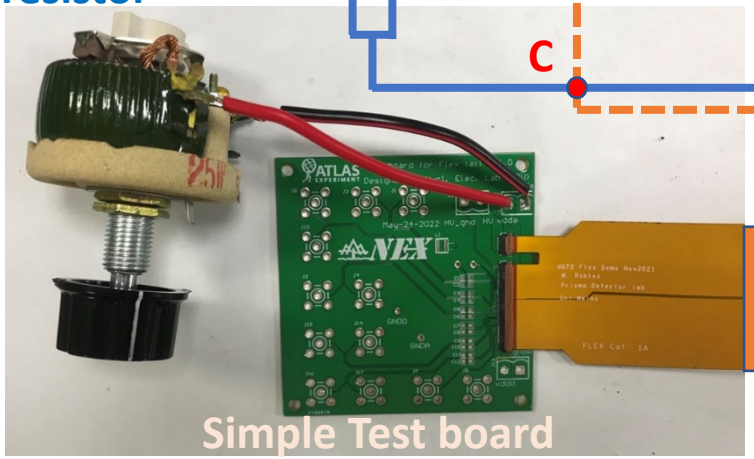
caliper

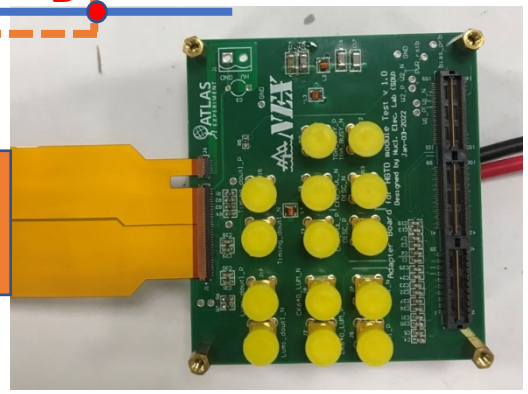
micrometer

High power BC1 adjustable sliding resistor



~ 46 mΩ for vdda and ~22 mΩ for gnda.





Adapter board v1

Summary

- Significant Progress in last 6 months, eg:
  - HV power supply pre-production done
  - LGAD Sensor production (CERN contract) progressed well
- Major Issue
  - Sensor: Signing of in-kind contributions for China (IHEP + USTC)
  - PEB: need solution for BPOL issue, need manpower for more PEB1F testing
  - Module: site qualification, pre-production
    - Need standard procedure and documentation, manpower and training

ATLAS Outstanding Achievement Award

- IHEP and USTC members won the 2025 Outstanding Achievement Award
  - for their development of the LGAD sensor in HGTD project
  - The list of ATLAS award for HGTD project: Bojan Hiti (Ljubljana), Alissa Howard (Ljubljana), Xuewei Jia (Munich MPI), Mengzhao Li (Beijing IHEP), Chihao Li (Michigan), Kuo Ma (Hefei), Theodoros Manoussos (CERN), Weiyi Sun (Beijing IHEP), Guilherme Tomio Saito (Sao Paulo), Iskra Velkovska (Ljubljana), Xiao Yang (CERN), Mei Zhao (Beijing IHEP)

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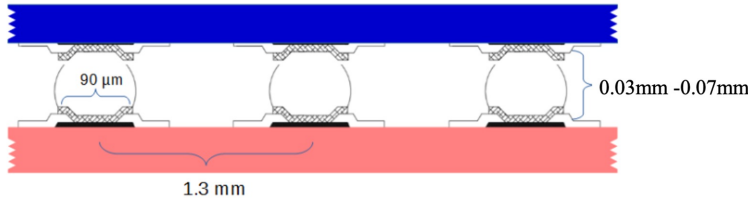
Voir en français

Celebrating the outstanding achievements of the ATLAS collaboration

The ATLAS collaboration celebrated the dedication, ingenuity and collaborative spirit of its members at the 8th Outstanding Achievement Awards

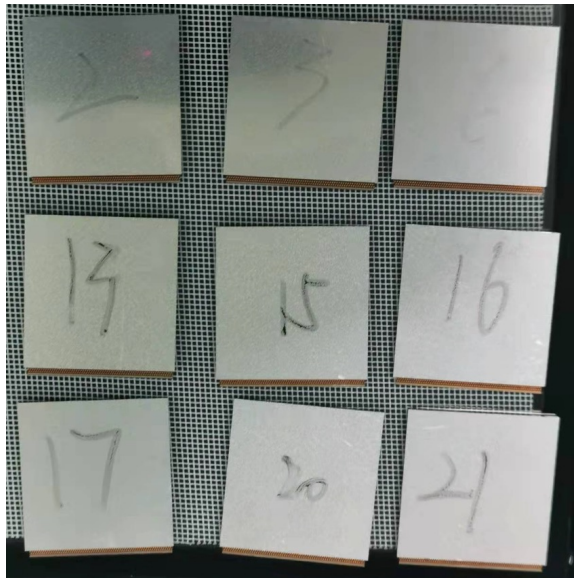
8 JULY, 2025 | By ATLAS collaboration

Sensor+ASIC Hybrid

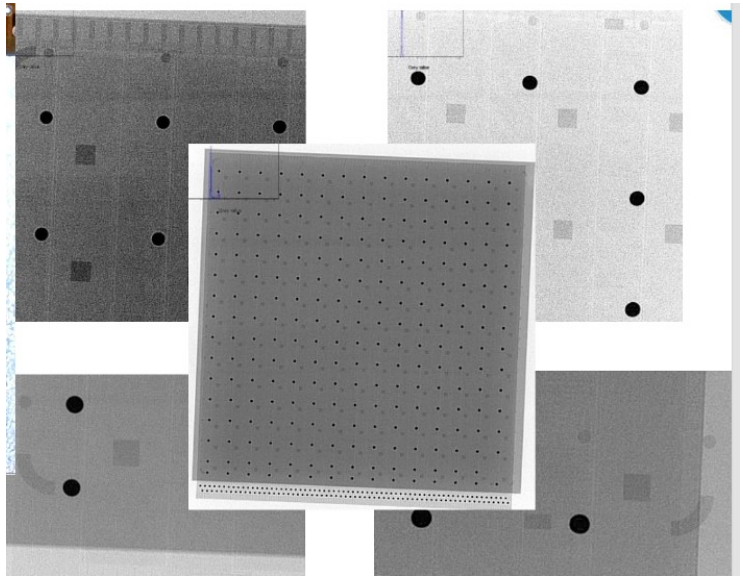


- China (IHEP) and Europe (Spain, France) share 50% of hybrids production
  - Challenge: ATLAS ITK pixel had hybrid bump delamination issue, delaying HL-LHC
  - IHEP led the hybrid R&D, solved the bump delamination issue in old HGTD hybrids

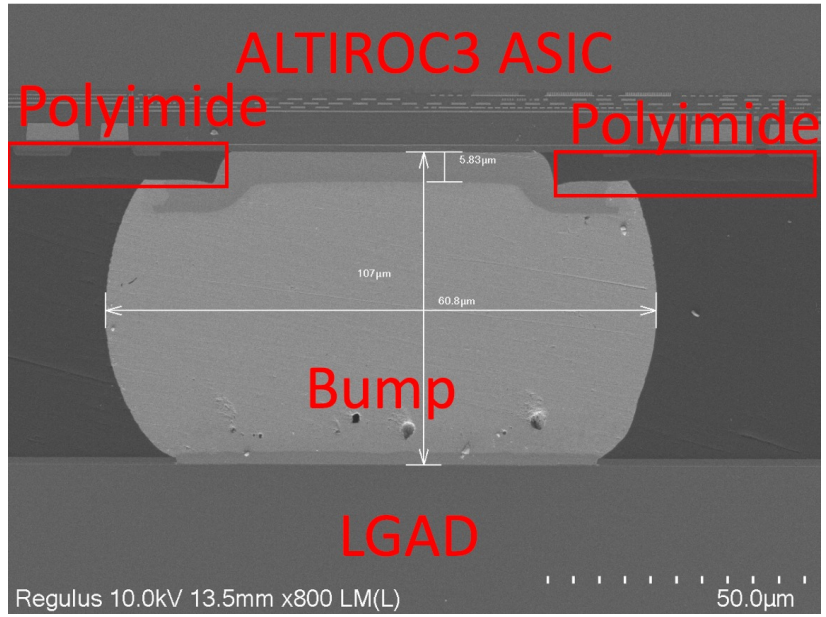
Sensor + ASIC hybrid



Hybrid X-ray photo



SEM photo of hybrid cross section



System-level large-scale engineering prototypes

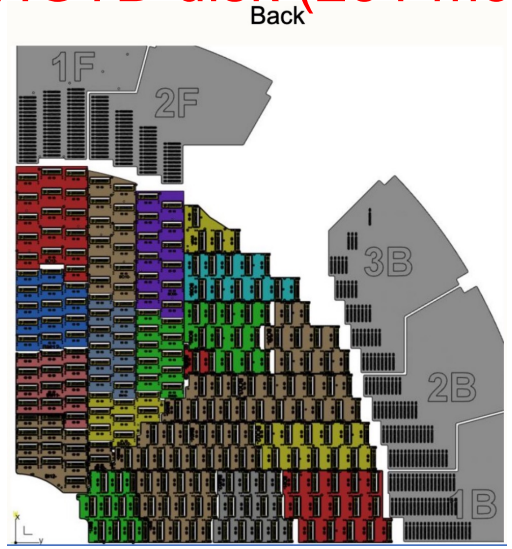
- China (IHEP/USTC/NJU) plan to contributed to system-level tests at CERN

Large-scale prototypes	Number of module	Time scale
Module-0 prototype system	251 (a quart of HGTD disk)	2026
Demonstrator v2	39	Early 2026
Demonstrator v1	54	2024

Demonstrator v1 with PEB1F (54 modules)

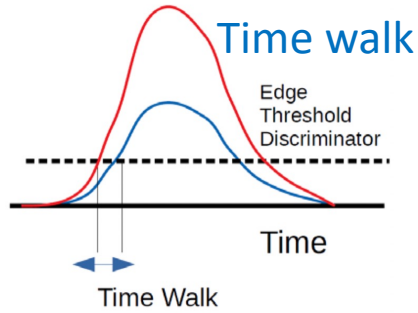
Demonstrators v1 and v2

Module-0: A full quarter of HGTD disk (251 modules)

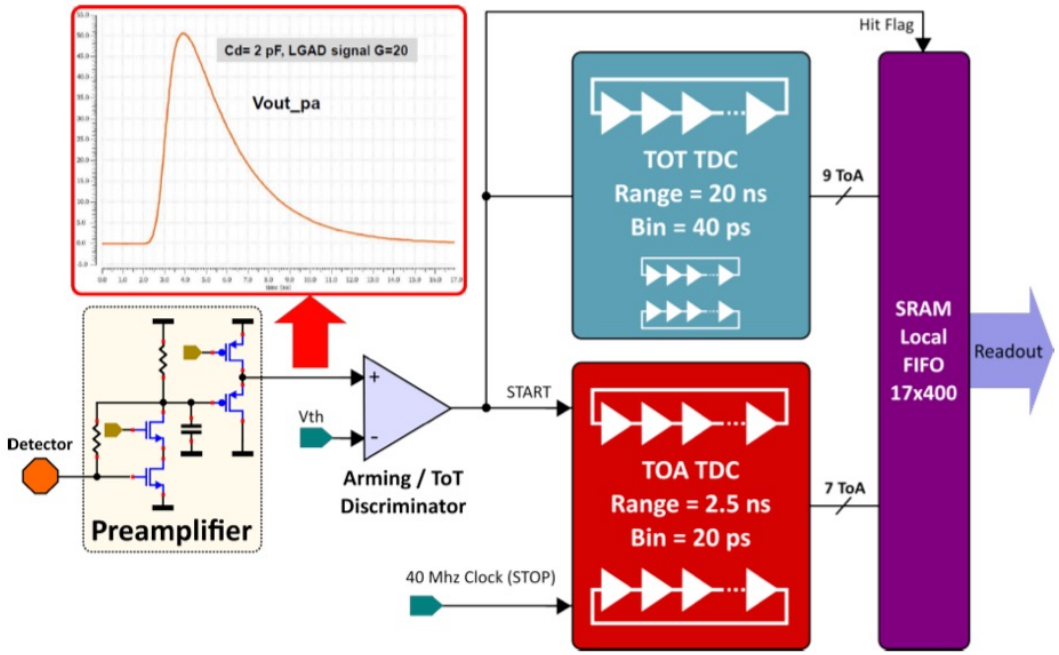


ALTIROC : Fast Timing ASIC

- 225 front-end channels in ALTIROC, each channel has
  - A preamplifier followed by a discriminator:
  - Two TDC (Time to Digital Converter) to provide digital **Hit data**
    - Time of Arrival (TOA) : Range of 2.5 ns and a bin of 20 ps (7 bits)
    - Time Over Threshold (TOT) : range of 20 ns and a bin of 40 ps (9 bits)
  - Local memory: to store the 17 bits of the time measurement until L0/L1 trigger (~ 1 MHz)



ALTIROC timing ASIC in nutshell



Time walk correction with TOT