CEPC Detector Working Plan

MDI Tasks in next Phase

BIB Study

- Validate the tools and codes we used
- Understand the missing issues in detector simulation using BESIII/BEPCII(IDRC)
- Finish the study flow to test the feasibility using CEPC Higgs mode
- Other modes and optimization of the IR design
- MDI Study(with accelerator and mechanical, mechanical requests also submitted to mechanical group)
 - Feasibility study of the mechanical issues, including the technique studies on manufacture and mockup
 - Optimization of the IR Geometry with detail(Together with accelerator colleagues, Later, IDRC)
- Luminosity Measurement Study
 - Study on diamond sensors used for Luminosity and Beam monitor(Nanking University: Ming Qi, Lei Zhang, etc; IDRC)
 - Study on Silicon Carbic sensors used for Beam monitor(IHEP: Xin Shi, Xiyuan Zhang, etc)
 - Study on silicon and LYSO modues in BEPCII/BESIII(IHEP&Nanking University)
 - Study on using IR BPM data to measure the Z-position of IP(Suen Hou, Weiming Song, Jun He, etc)

2025/12/18

BIB Study Plan

- 1. Validate the tools and codes we used(2026, more students needed)
 - a. Generator for Pair Production with cross-check and calculation(Boping Chen, Chenguang Zhang, Haoyu Shi, needs more)
 - b. Generator/Tracking tools for SR/Single Beam Loss BG with other tools and experiments in BEPCII(Haoyu Shi, Chenguang Zhang, Bin Wang, Shiyuan Wang, Yanbang Tang, Sha Bai, etc).
- 2. Understand the missing issues in detector simulation using BESIII/BEPCII(2026, Cong Li, Shiyuan Wang, Linghui Wu, Aiqiang Guo, Bin Wang, Haoyu Shi, etc, will needs more students since 2026.6)
 - a. Starting from the data taken in 2021, the 2022-2024
 - b. Dedicated experiments after the improvement if needed.
- 3. Finish the study flow to test the feasibility using CEPC Higgs mode(Hopefully 2026)
 - a. Study the impact of the misalignment of the IR beam pipe(Yanbang Tang)
- 4. Other modes and optimization of the IR design(Later, manpower needed)
- 5. More details can be found <u>here</u>

Vertex Detector Working plan

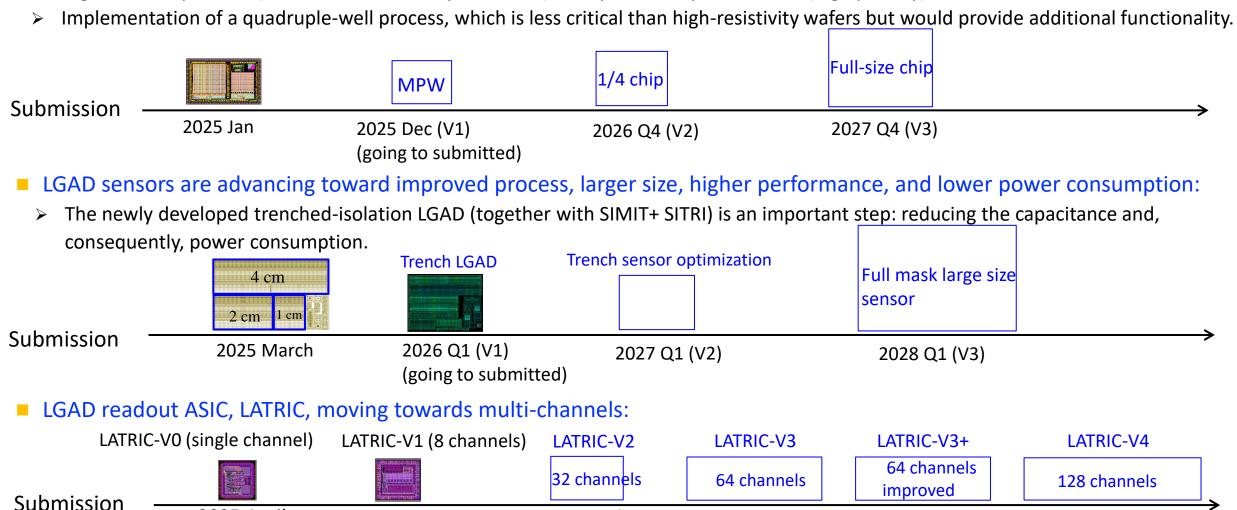
- Development of wafer-scale stitching MAPSs with 180nm technology (2026)
- Construction of a small-scale VTX prototype (2027)
 - Three inner layer prototype, Based on 180nm stitched MAPS
 - to address challenges in integration, mechanical, cooling performance, laser alignment
- Longer term: Explore CIS stitching MAPSs with 65nm/55nm technology (2028)
 - Baseline: TPSCo's 65 nm technology
 - Alternative: domestic CIS stitching foundry, eg: HLMC's 55 nm technology.

Silicon Tracker Sensor and ASIC Tape-out Plan

- HV-CMOS sensor R&D will be transferred to a new foundry (Chongqing), mainly to address process-related issues:
 - \triangleright High-resistivity wafers (~1000 Ω ·cm, currently ~10 Ω ·cm) to improve S/N performance (high priority).

2025 April

2025 Oct



2026 July

2027 April

2028 Jan

2028 Oct

Gaseous Detector Plan

Item	execution time
1. Test and validation of readout modules (double mesh Micromegas + high granularity pads)	2026
2. Readout ASIC optimization (including spark-protection measures)	2026-2028
3. Prototype ion backflow suppression techniques, independently of the selected solution (e.g., double mesh or graphene filter), to verify feasibility and performance	double mesh : 2026-2027 Graphene: 2026-2028
4. Pad size optimization in combination with the optimized gas mixture	2026-2029
5. Further studies of beam-induced background (together with Haoyu)	2026-2030
6. More detailed investigations of space-charge distortions. Calibration and correction strategy studies	2026-2030
7. Evaluate CO ₂ cooling as a potential alternative to water, preliminary design and FEA	2026-2027

- Reassess the choice of $500 \times 500 \ \mu\text{m}^2$ pad size in combination with the T2K gas mixture, as this configuration appears suboptimal for dE/dx-based particle identification.
- Extend the beam-induced background studies, incorporating recent improvements in simulation and mitigation methods to refine background estimates and design margins.
- Conduct more detailed investigations of space-charge distortions, ensuring that correction strategies are validated for all expected running conditions.
- Prototype ion backflow suppression techniques, independently of the selected solution (e.g., double mesh or graphene filter), to verify feasibility and performance.
- Demonstrate experimentally the effectiveness of spark-protection measures for the readout electronics.
- Evaluate CO₂ cooling as a potential alternative to water, taking advantage of its dielectric properties and ability to maintain constant-temperature heat removal without electrical risk.

Answer:

- The first four items have been included in Section 6.6 "summary and future plan". These studies are either in progress or about to begin.
- Spark-protection measures will be included in the next version of the readout ASIC and will be tested and verified later.
- Descriptions of CO₂ cooling as a potential alternative to water was added in Section 6.2.5. The detailed design will be guided by thermodynamic FEA.

R&D plans of the Cherenkov detector

Towards CDR in 1-2 years

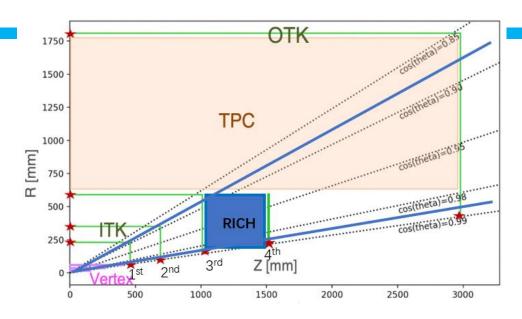
- -a baseline detector option for radiator and photosensor
- a preliminary simulation for determining the detector position
- the key technology development (SiPM/MCP-PMT and related readout electronics, aerogel)
 - a demonstrator of the baseline detector option

Towards TDR in 3-5 years

- a specific design of all components of the detector
- a prototype of the baseline detector and beam test
- a relatively mature simulation/reconstruction software

Current R&Ds needed

- a low noise, high spatial resolution, high radiation tolerance SiPM
- a fast, multiple anode, low material budget MCP-PMT
- a simulation framework in CEPCSW



A preliminary specification of SiPM

Items	Design values
Wavelength	200 nm – 600 nm
Photon detection efficiency	50% at 420nm
Size of single SiPM	1 mm x 1 mm or 3 mm x 3 mm
Time resolution	100 – 200 ps
Dark noise rate	<100 kHz /mm² @20°C
Spatial resolution	200 – 300 μm
Radiation tolerance	>10 ¹³ N _{eq} /cm ²

ECAL planning regarding to IDRC final report

- Development of QA/QC specifications for large-scale crystal and SiPM production
 - Close collaborations with institutions and industry partners on crystals and SiPMs
- Construction and testing of full-scale prototypes with final design choices
 - This will not be pursed at this stage, as this is not urgent for the CEPC project timeline
- Refinement of the calibration procedures
 - Continue simulation studies; joint efforts along with beam-induced backgrounds
- Exploration of the additional potential of the selected technology, such as timing
 - Potentials of fast timing will be explored: technological, physics performance
- Capabilities and advanced software developments
 - Further improvements of CyberPFA: combining ECAL and HCAL as a coherent system

ECAL R&D: planning of new items

- Note: these following R&D items are beyond the IDRC outlook scope, but we think they are "innovative and highly rewarding" for the CEPC calorimetry
- Explore new designs of ECAL
 - Based on new scintillator materials: BSO crystals, scintillating glass
 - R&D targets: performance potentials, technical readiness and possible bottlenecks
- Explore a new design of a calorimetry system
 - A homogeneous calorimeter with scintillating glass for EM and hadronic sections
 - Topics for R&D: requirements for scintillating glass, mechanics and cooling, glass granularity optimisation, readout electronics (boards, cabling)
- SiPM common R&D
 - Coherent developments with coordination of all sub-detectors using SiPM readout
 - Common needs and also diverse specifications on different SiPMs for ECAL, HCAL, muon and Cherenkov detectors

HCAL Recommendations

- Address intra-tile response variations, particularly given the design choice of using a single SiPM per tile, as these variations could significantly affect detector uniformity and calibration stability.
- Establish a robust and efficient QA/QC chain, building on the experience and methodologies developed for the PS-HCAL QA/QC programme.
- Answer to the recommendations:

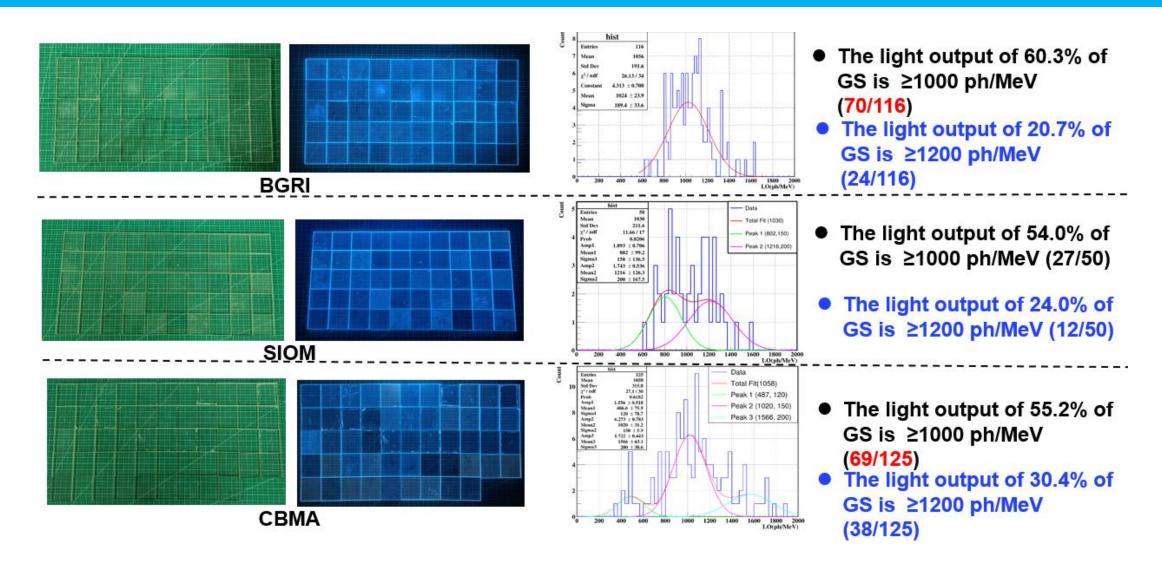
We have updated the Ref-TDR to address both recommendations:

- 1. Intra-tile Variations & Calibration: (figures next slide)
 Addressed in enhanced sections 8.4.2.4 (Quality Control) and 8.4.6 (Calibration). Our strategy uses MIP intercalibration and LED monitoring to ensure uniform response.
- QA/QC Chain:

Established in the new 8.4.2.4 (Quality Control), detailing procedures and presenting initial results. Recent data from ~290 GS tiles shows >55% with light yield >1000 ph/MeV, confirming good batch quality and providing a production baseline.

These updates document our committed approach, which will be refined in future project phases.

HCAL Recommendations



HCAL Future R&D Plan (2025–2030):

We will advance GS-HCAL technology through systematic prototyping, material optimization, and simulation validation, ensuring readiness for construction in the next 5 years.

Key Focus Areas:

- Glass Scintillator Enhancement Increase light yield and attenuation length;
 integrate accurate GS properties into Geant4 for reliable simulation.
- Photon Detector & Electronics Develop domestic SiPMs (NDL/Huawei) to reduce cost; design custom front-end ASIC for mass production.
- Prototype Validation Conduct beam tests with two small prototypes (2025),
 then build and test full 0.6 m³ prototype to validate performance and integration.

Concerns

- Technology is ready for a module prototype.
- We need systematic studies with long-term CR tests.
- Optimization of the geometry for better coverage.

- In 2-3 years
- Improve the software and simulation of the muon detector.
- Study with physics simulation → Potential for new physics.
- Radiation hardness. ——— Since the third year.

Table 9.3: Average hit rate in the PSUs of the endcaps due to backgrounds at the Z pole.

Layer#	Maximum hit density $(\times 10^{-7} / \text{ cm}^2/BX)$	Maximum hit rate (Hz/cm ²)	Average hit rate (Hz/cm ²)	Occupancy (×10 ⁻⁴)
1	7.86	10.24	0.80	7.6
2	7.86	10.24	0.96	7.6
3	10.48	13.66	1.22	10.0
4	9.16	11.96	1.16	8.8
5	6.58	8.60	0.88	6.2
6	5.24	6.82	0.28	5.0

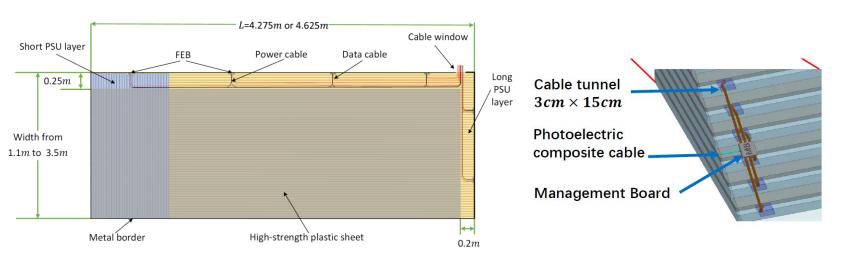
JINR is performing some R&D.

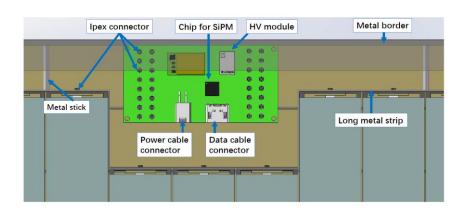
Module prototype

- The barrel module structure, with a length up to 5m! Not endcap yet.
- Key advantage: FEB inside module.

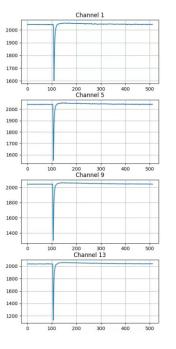
Barrel Module

- Need to design a preliminary FEB.
- We can revise our current DAQ with 250MSPS, which should yield a time resolution better 1 ns.
- We can build several layers at Fudan or IHEP, and perform CR test.



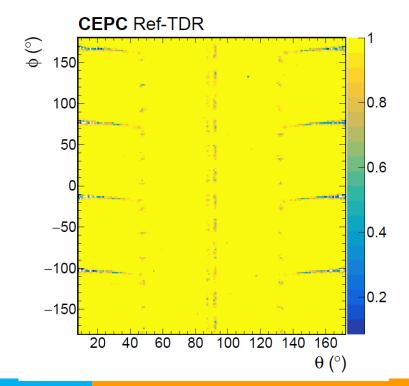


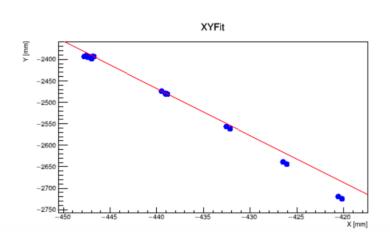




Software and simulation

- Optimization of geometry coverage.
- Study of standalone tracking for displayed vertex.
- Physics simulation for physics impact and new physics.





Magnet - Costs on different R&D stages

LTS R&D Time		Time	Costs (million RMB)	Contents
Box type	conductor	2025	0.69	Get the support from Henan
100 m B	ox type conductor	2026	1	Long cable development, optimize the cable performance;
Conduct	or test	2026	1.5	Critical current test; mechanical test; RRR value test; Bonding face; Cable joint
	1.5km conductor processing	2026	3.5	Scaled model coil, 300 m per layer, total 4 layers
	Coil	2027	1	Coil support, winding, vacuum epoxy impregnation
	Current leads	2027	1	20 kA current leads
Madal	Cryostat	2027	0.6	Thermal shield, vacuum cryostat, suspend system
Model coil	Valve box and temperature sensors	2028	0.7	Valve box, temperature sensors and monitoring, liquid helium monitoring
	Test experiments	2028	0.5	Based on the existing liquid helium recovery testing platform
	Power source and quench protection	2028	0.3	Borrow 20 kA power source and quench protection system.
	Total	2026-2028	7.6	

HTS R&D	Time	Costs (million RMB)	Contents
ASTC conductor	2025-2026	0.7	Get the support from Henan
REBCO tape	2026	0.8	Long cable development
ASTC	2027-2028	0.7	Cable processing
Conductor test	2026-2028	0.6	Critical current test; mechanical test; Cable joint
Quench protection study	2027-2028	1.5	0.9 million equipment, glass fiber, cryostat, sensors

2024.12			I I	2026	2027	2028
2024.11	2025.1	2025.4	2026.06	2026.12	2027.12	2028.12
GaN Selection	DC-DC Controller schematic design	1 st tapeout	PAL 2 nd tapeout	PCB-based Module prototype	Rad enhancement & Inductor design	Rad-tol & Mag proof PAL prototype
2024.10	2025.1		2026.04	2026.12	2027.12	2028.12
Protocol define	Scheme define		FEDI 1 st tapeout	FEDI prototype test	FEDI & OAT on detector test	Rad-tol FEDI DataLink prototype
2024.12	2025.1		1 	2026.12		2028.12
Preliminary scheme	Taichu-stitching-180 development		-	New process explorer		New candidate CIS process validate
ior streaming				Mod-design on single chip		
		2025.6			2027.12	2028.12
		Prototype beamtest	 		TEPIX modified design Pixel-TPC chip scheme	TEPIX finalization Pixel-TPC chip prototype
2024.12	2025.4	2025.12	2026.6	2026.12	2027.12	2028.12
FPMROC chip test (for FASTPMT) Preliminary scheme 1st tapeout optimization		(for FASTPMT)	LATRIC2	Next LATRIC improvement	LATRIC improvement	Chip Finalization & detector co-test
		inorough test	scheme	tapeout & test	detector to-test	
	2025.1	2025.4 2025.1	2 2026.06	2026.12	2027.12	2028.12
	Spec finalization & device selection	1 tapcout	Thomasah +a.	SIPAC-E SIPAC-H Improvement scheme	SIPAC-E SIPAC-H Improvement Tapeout & test	Chip Finalization
=	GaN Selection 2024.10 Protocol define 2024.12 Preliminary scheme for Stitching 2024.12 PMROC chip test (for FASTPMT)	GaN Selection DC-DC Controller schematic design 2024.10 Protocol define 2024.12 Preliminary scheme for Stitching 2024.12 2025.1 Taichu-stitching-180 development development 2024.12 PMROC chip test (for FASTPMT) Preliminary scheme 2025.1 Spec finalization &	GaN Selection DC-DC Controller schematic design 2024.10 2025.1 Protocol define 2024.12 Preliminary scheme for Stitching Preliminary scheme for Stitching 2025.4 PMROC chip test (for FASTPMT) Preliminary scheme 2025.1 Preliminary scheme 2025.1 Preliminary scheme 2025.1 Spec finalization & development 1st tapeout 1st tapeout	GaN Selection DC-DC Controller schematic design 2024.10 Protocol define Scheme define 2025.1 Taichu-stitching-180 development for Stitching 2025.4 2025.6 Prototype beamtest 2024.12 2025.4 PMROC chip test (for FASTPMT) Preliminary scheme 1st tapeout 2025.1 PMROC prototype test (for FASTPMT) Preliminary scheme 2025.1 Preliminary scheme Spec finalization & 1st tapeout 1st tapeout PAL 2nd tapeout FEDI 1st tapeout 1st tapeout PAL 2nd tapeout PAL 2nd tapeout PAL 2nd tapeout PAL 2nd tapeout FEDI 1st tapeout 1st tapeout PAL 2nd tapeout St tapeout PAL 2nd tapeout PAL 2	GaN Selection DC-DC Controller schematic design Scheme define Scheme define DC-DC Controller schematic design Scheme define DC-DC Controller schematic design Scheme define DC-DC Controller schematic design TEDI FEDI FEDI FEDI New process explorer T1180 Mod-design on single chi DC FORTOUT pe beamtest DC DC FORTOUT pe test (for FASTPMT) OTK detector optimization DC SIPAC-E SIPAC-H Improvement	Gan Selection DC-DC Controller schematic design 1st tapeout 2nd tapeout 2nd tapeout 2nd tapeout 2nd tapeout 2024.10 2024.10 2025.1 Protocol define Scheme define Scheme define 2025.1 2024.12 2025.1 Taichu-stitching-180 development 6evelopment for Stitching 2024.12 Preliminary scheme for Stitching 2025.1 2025.6 Prototype beamtest 71180 Mod-design on single chip 2024.12 2024.12 2025.1 2025.1 2025.1 2025.1 2025.1 2027.12 TEPIX modified design pixel-TPC chip scheme 2024.12 PMROC chip test (for FASTPMT) OTK detector optimization 2025.12 2025.1 2025.1 2026.6 Prototype beamtest Semme 2026.12 PFMROC prototype test (for FASTPMT) OTK detector optimization 2025.12 2025.1 2025.1 2025.1 2026.6 2026.12 2027.12 TEPIX modified design pixel-TPC chip scheme 2026.12 EATRIC2 Improvement scheme 2026.12 2027.12 Thorough test SiPAC-E SIPAC-E SIPAC-E SIPAC-H Improvement Impr

TDAQ R&D Working Plan

- Simulation and Study of Trigger Algorithms
 - Conduct in-depth simulations of detector-specific trigger algorithms,
 - Assess system throughput and real-time processing performance,
 - Further ML and Al algorithms.
- High-Speed Data Transmission Technology for Trigger Electronics
 - Develop high-speed data transmission interfaces operating at line rate 16-25 Gbps,
 - Deliver parallel computing resources optimized for trigger processing,
 - FPGA-based RDMA readout protocol.
- Distributed High-Bandwidth Parallel Computing Solutions
 - Distributed computing frameworks with terabit-per-second data transmission capabilities,
 - Heterogeneous parallel processing architectures.

Mechanics and integration

Further design: yoke, sub-detectors, connection structure

- structure design & FEA (IHEP engineers), process (keep communication with manufacturers and institutions)
- Cooling design: water(HCAL, ECAL, beam pipe), air (VTX), water or
 CO2 (ITK, OTK, TPC)

Installation related

- Scheme optimization (keep communication with manufacturers and institutions)
- Design of the tooling and fixtures
- Layout of the underground EH and auxiliary hall
- Surface Assembly building
- Survey, alignment, monitoring

Service

- Cabling and piping
- Cooling system : water, CO2
- Air condition system
- Electrical & gas system
- Facilities: crane, forks....

Mockup and cooling valuation

- Beam pipe
- VTX (air): From IDRC
- ITK,OTK
- TPC: cooling plate

Study on the supercritical CO₂ cooling system

Simulation

- From IDRC
- Mockup and validation

Process study (with sub-system)

- Production
- Assembly
- Key material comparing and test: Carbon fiber

Installation

 Digital installation study: methodology framework, key enabling technology, prototype, test

Service study: from IDRC

Routing prototype test

Software Recommendations SOFTWARE AND COMPUTING

- Establish well-defined reference performance benchmarks and corresponding validation plots to qualify simulation and reconstruction quality, as well as detector performance. Integrate these benchmarks into the new monitoring system.
 - > Task 1 and 2 in the 2026 Plan
- Define sub-detector—specific performance plots while maintaining a common set of global physics performance benchmarks to ensure consistent validation of software improvements.
 - > Task 1 and 2 in the 2026 Plan
- Once consolidated, establish clear reference detector performance baselines within the Ref-TDR so that future detector and physics studies use consistent software versions, calibration constants, and conditions (e.g., ensuring that jet resolution and b-tagging results are derived under identical configurations).
 - > Task 1 and 2 in the 2026 Plan
- Provide more quantitative details in the resource estimate, including the ratio of Monte Carlo to data events used, expected number of events, and average file sizes per event.
 - > This recommendation has already been implemented.

Software Work plan 2026

#	Task	Duration
1	Develop a validation system that integrates reconstruction and analysis algorithms to produce comparative efficiency and resolution plots	Q1
2	Implement automation pipelines with Kafka and database integration to streamline validation workflows	Q2
3	Optimize CyberPFA algorithms and validate their performance against baseline results	Q2
4	Deploy new Gaussino simulation framework	Q2
5	Enhance Phoenix event display with point cloud visualization and CEPCSW integration	Q3
6	Integrate DAQ system with CEPCSW workflows	Q3
7	Upgrade core software stack: migrate to the latest version of EDM4hep integration and provide Gaudi multithreading support	Q4
8	Apply ML to calorimeter simulation	Q4

Detector & Physics Performance

- Iterate closely with detector design and optimization, update relevant object/benchmark performance
- Work closely with software group, MDI group for studies with more realistic conditions: beam-induced background, mis-alignment, noise, non-uniform magnetic field, etc. (IDRC recommendation)
 - Some tools to be further developed and integrated into CEPCSW, e.g. ACTS
 - Computing speed to be improved for beam background simulation
 - Independent cross checks for certain major issues, e.g. alternative beam background generator
- Further develop existing physics benchmarks and add new benchmarks
 - E.g. H->ss, Z->ss (IDRC recommendation)
- Explore further AI/ML/QC to improve sensitivities
- Investigate LEP dada, to validate some CEPC performance

Backup Slides

TPC R&D Plan in next 3-5 years

- Reassess the choice of 500 imes 500 μ m² pad size in combination with the T2K gas mixture, as this configuration appears suboptimal for dE/dx-based particle identification.
 - Concerning to NO funding for the TEPIX chip v2 (from Henan sources), the v1 test studies have identified parameters that need optimization.
 - Recently, launch studies that require only modest funding and can be tested with existing hardware: use the available Topmetal-L chip (40 μ m \times 40 μ m) and its test setup to implement different pixel sizes (by combining pixels: 2 \times 2, 3 \times 3, 5 \times 5, 7 \times 7, etc.) and experimentally determine the key parameters of each pixel configuration.
 - The drawback is that the Topmetal-L chip performs readout via capacitive integral charge processing. the approach still allows for studies of readout granularity.
- Extend the beam-induced background studies, incorporating recent improvements in simulation and mitigation methods to refine background estimates and design margins.
 - Studies on beam-induced backgrounds have already been discussed with the ILD collaboration. Ties (DESY) and Daniel (KEK) recommended integrating them into the FCC-ee background programme, and this work is now proceeding within the ILD framework.
- Conduct more detailed investigations of space-charge distortions, ensuring that correction strategies are validated for all expected running conditions.
 - Research on small modules is already underway.
 - A full-scale model measuring 2.9 meters in length is also under construction.

TPC R&D Plan in next 3-5 years

- Prototype ion backflow suppression techniques, independently of the selected solution (e.g., double mesh or graphene filter), to verify feasibility and performance.
 - Research on double- and multi-layer micromegas has been initiated between IHEP and USTC, and ongoing collaboration is being pursued.
 - Research on graphene is proceeding through the well-established collaboration between IHEP and Shandong University (Imad and Chengguang Zhu).
- Demonstrate experimentally the effectiveness of spark-protection measures for the readout electronics.
 - With adequate funding, this protection feature could be integrated directly into the TEPIX v2 chip as agreed between Deng Zhi and Paul.
- Evaluate CO₂ cooling as a potential alternative to water, taking advantage of its dielectric properties and ability to maintain constant-temperature heat removal without electrical risk.
 - As discussed, the relevant requirements will be passed to the mechanical engineering group.

ECAL R&D items: outlook from IDRC

- The outlook for future activities is coherent and appropriate for the current project stage. Planned efforts include:
 - Development of QA/QC specifications for large-scale crystal and SiPM production
 - Construction and testing of full-scale prototypes with final design choices
 - Refinement of the calibration procedures
 - Exploration of the additional potential of the selected technology, such as timing
 - Capabilities and advanced software developments
- Although no showstoppers have been identified in relation to the current design, the scope and importance of the remaining work call for robust planning and sustained focus.

ECAL R&D items: outlook from IDRC

- In summary, the ECAL design has reached an advanced Technological Readiness Level (TRL). The overall detector concept and its subcomponents are well defined and well understood. The underlying technologies are mature and validated through prototypes, and the assembly process closely follows that of other large homogeneous calorimeters.
- Mass production could begin soon after completion of the remaining prototyping steps and definition of assembly engineering, QA/QC procedures, and logistics in line with the project schedule.