CEPC Inner Silicon Tracker
COFFEE Preliminary Results

CMOS SENSOR IN
FIFTY-FIVE NM PROCESS

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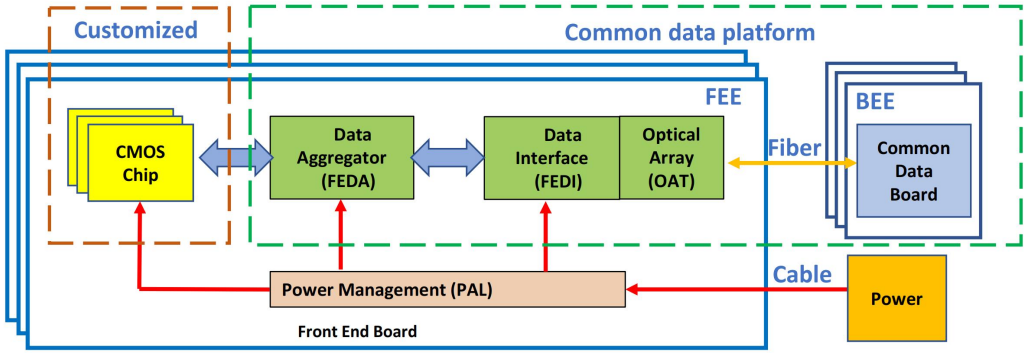
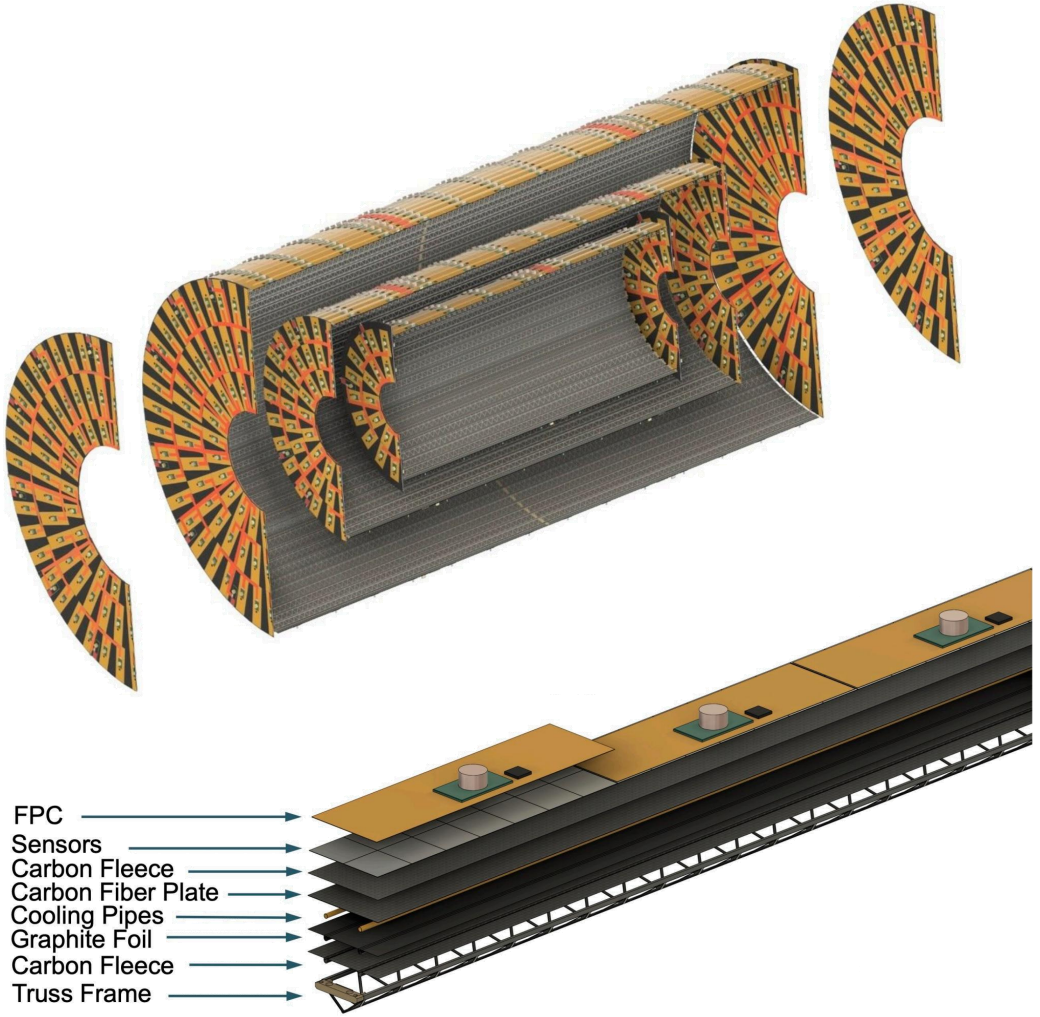
on behalf of COFFEE team

CEPC Phy and Det, 24-Dec-2025

CEPC Inner Silicon Tracker with HV-CMOS

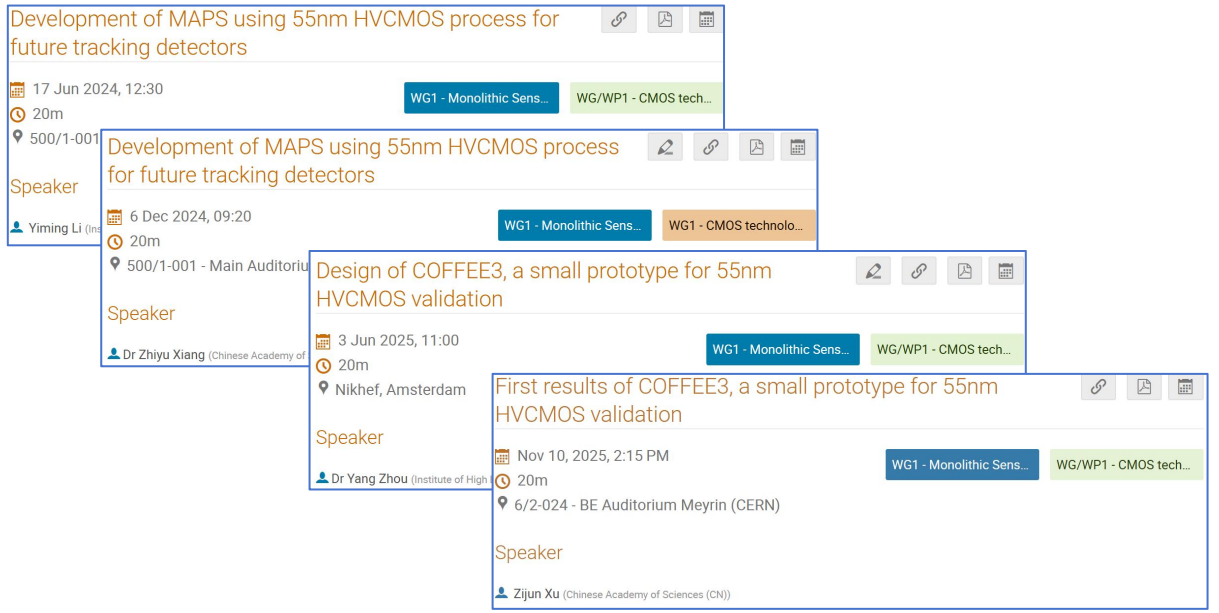
- monolithic High Voltage Complementary Metal Oxide-Semiconductor (HV-CMOS) pixel sensor technology has been selected for the ITK
- spatial resolution of ~ 8 μm in the bending direction and a timing resolution of 3~5 ns
- covering area of ~ 20 m^2

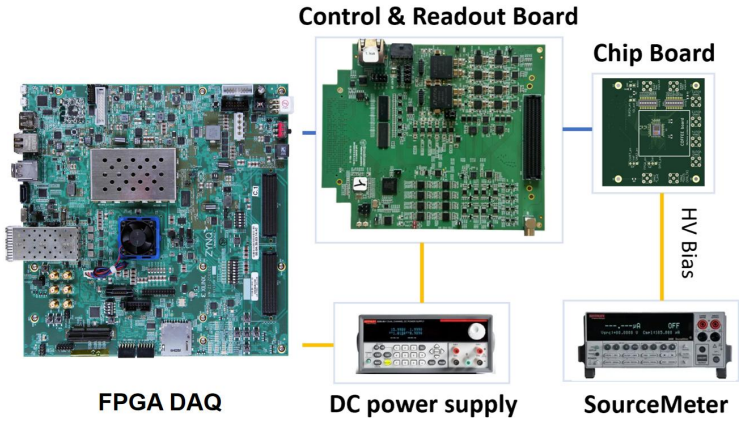




HV-CMOS R&D at IHEP

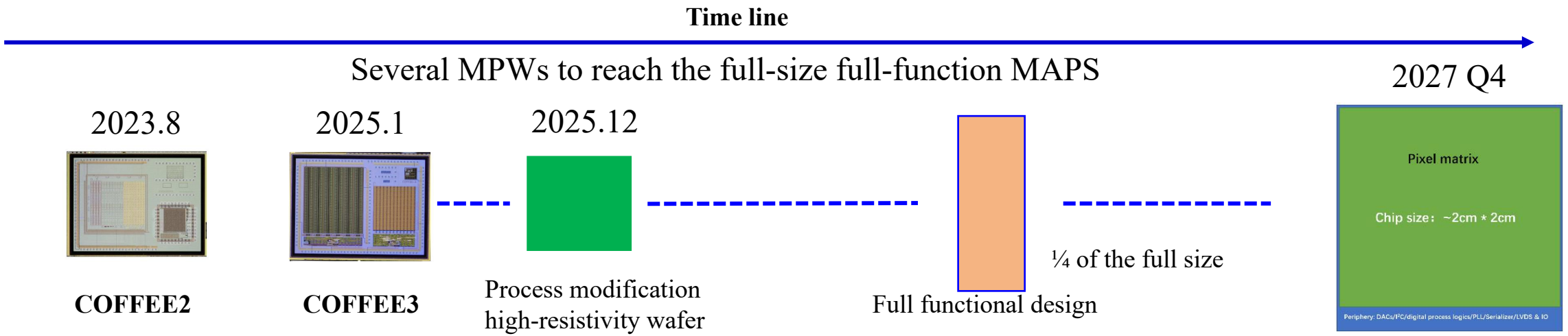
- IHEP/HV-CMOS team actively involved in DRD3 WG1/WP1
  - Monolithic silicon technologies
  - COFFEE progress presented every DRD3 week
  - test-beam and irradiation facilities sharing
  - joint serial powering R&D with US/UK/Italy
  - joint aluminum flex R&D with Italy/UK
- Caribou DAQ for MAPS readout
  - Open source hardware, firmware and software
  - FE chip specific carrier board, firmware and software IP blocks developed by ourself
  - as a user, keep reporting bugs and solutions
  - *an economic DAQ replacement in developping with CCNU





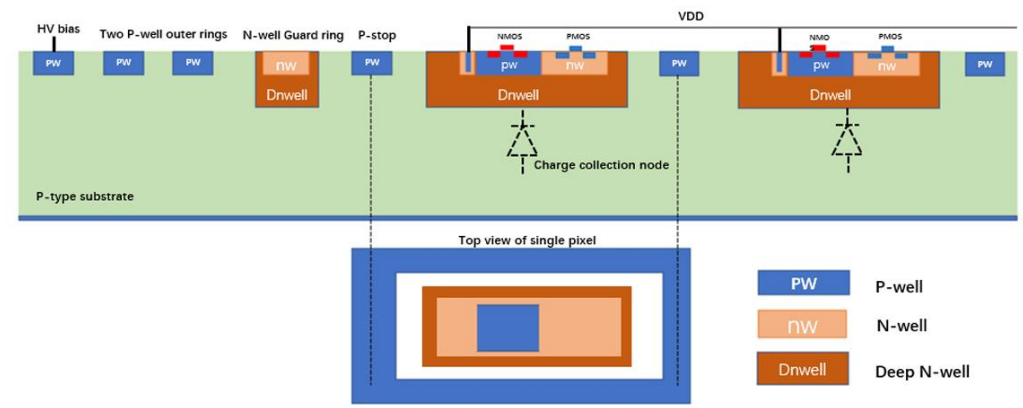
CMOS sensOr in Fifty-FivE nm procEss (COFFEE)

- HVCMOS pixel MAPS for CEPC silicon tracker, LHCb UT upgrade, etc.
- As of now, two tape-outs in a commercial 55nm HV-CMOS process
  - COFFEE2: exploring and verifying the process characteristics
  - COFFEE3: verifying readout circuit structures and core performances
  - next: **process modification and high-resistivity wafter** for better performance



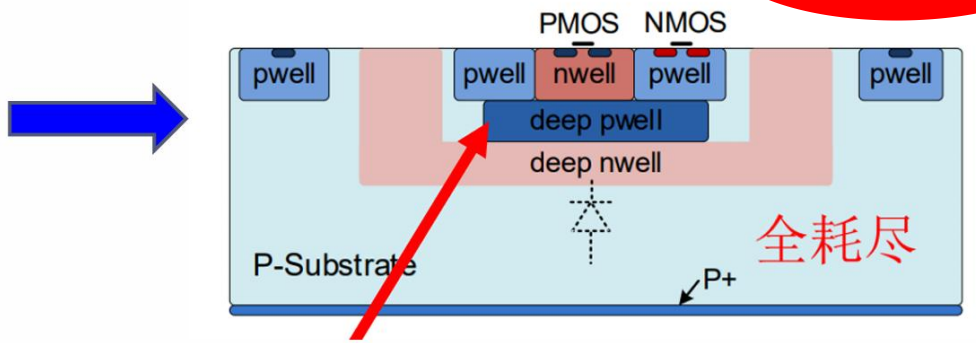
COFFEE Design: Now and Next

Current condition of the used 55nm commercial process:



Process modifications:

2025-Dec



- **Triple-well:** transistors are enfolded by Dnwell
- **Wafer resistivity:** **10 Ω·cm;**
- **Metal layers: 9 (1 top metal); benefit for routing**
- The charge sensing diode formed by DNW & PSUB could be biased > **70V** before breakdown;

  Depletion depth about 10 — 20 μm;

  (corresponding to 1k – 2k e^- total signal charges)

Several modifications are desired:

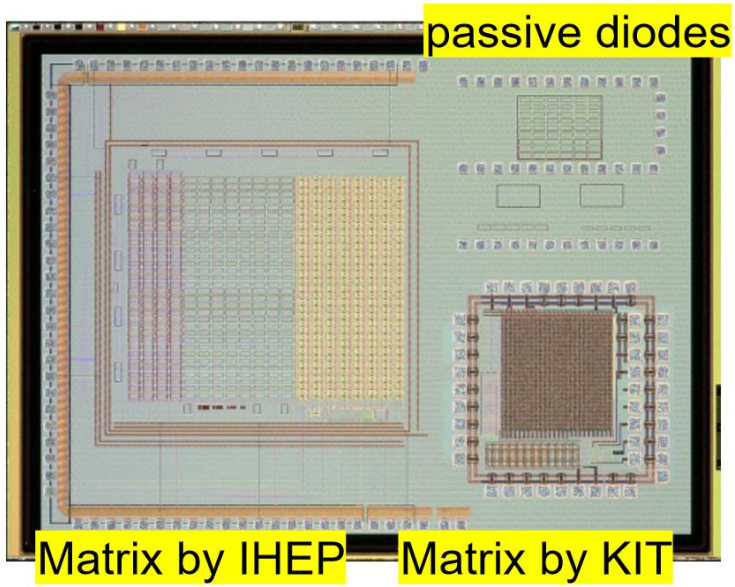
1. **Replace the wafer for a higher resistivity substrate:** significantly increase the depletion depth, enhancing the total signal charge (2k – 20k e^-) and reducing the front-end equivalent capacitance -> resulting in a higher SNR (signal-to-noise ratio);
2. **Fine-tuning the well structure:** Adding an isolation layer between the Nwell and DNW allows for the integration of complex digital circuits within the pixel -> greatly increasing design flexibility and improving overall performance.

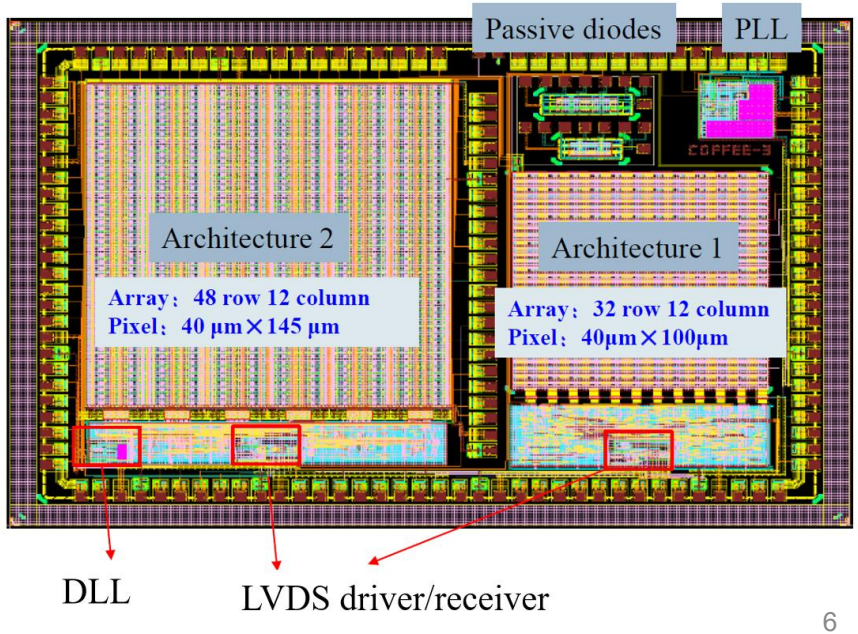
……. Efforts are still on going

COFFEE Layout

- COFFEE2
  - Passive diode for sensor charactizing
  - the big pixel matrix design leaded by IHEP team
  - R&D for pixel electrode structure, in-pixel Amplifier and comparator

- COFFEE3
  - PLL, DLL, LVDS IP accumulation
  - Two pixel matrix & readout architectures:
    1. NMOS design in-pixel: for current triple-well process; Less X-talk between analog and digital circuits
    2. CMOS design in-pixel, for future quadruple-well process. Advanced readout design, more suitable for high hit density environment

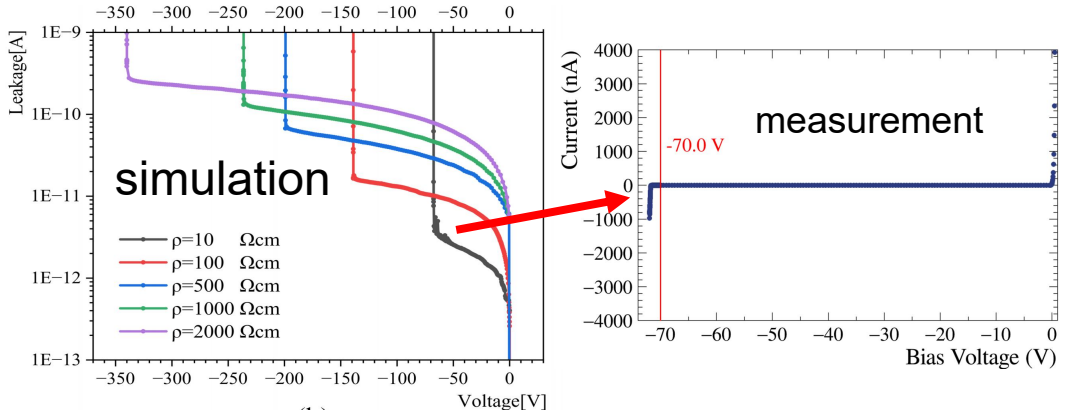


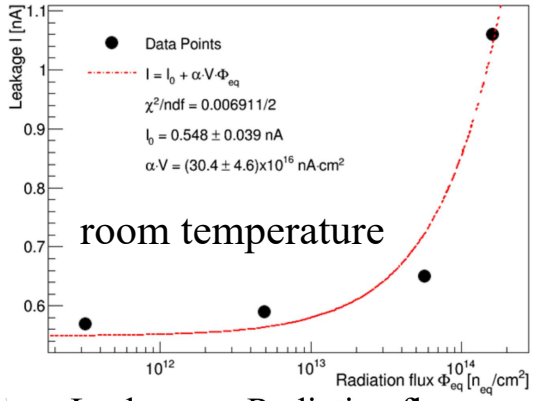


MPW chip size ~ 3×4 mm^2

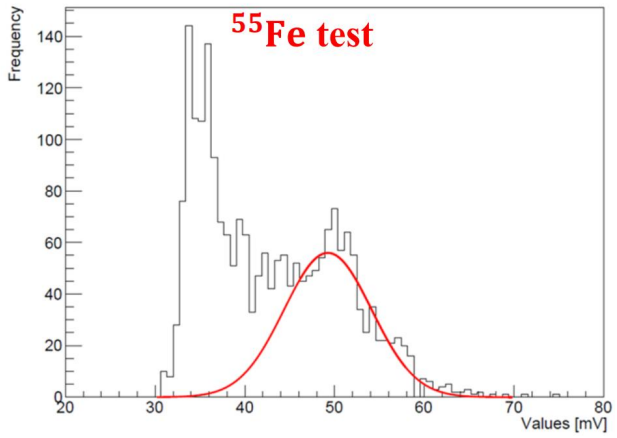
Sensor (charge sensing diode)

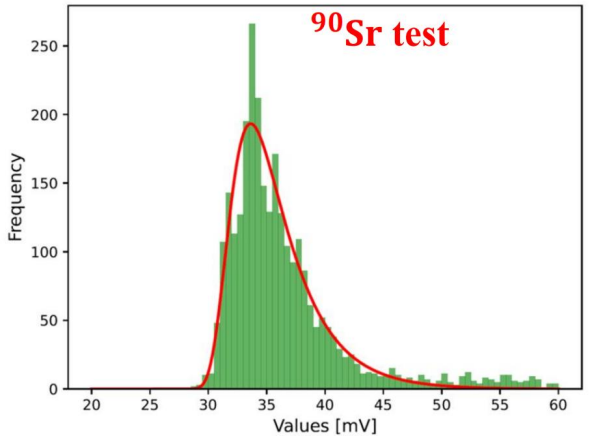
- COFFEE2/3 got consistent sensor IV/CV performance
  - consistent with TCAD simulation
  - V(Breakdown) ~ 70V for 10 Ω·cm resistivity wafer
  - irradiation @CSNS, 80MeV proton
- sensor depletion depth only ~10 μm from simulation, and inferred from radiation source (^{55}Fe vs ^{90}Sr) study of COFFEE2
  - high resistivity wafer will improve S/N

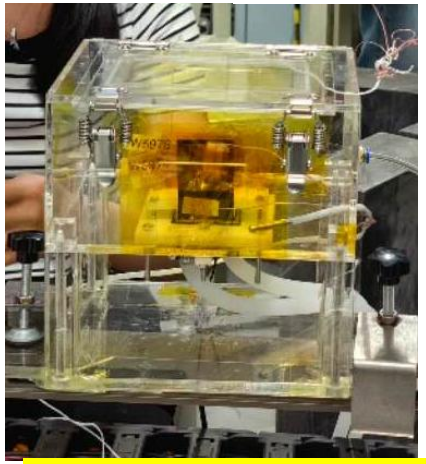


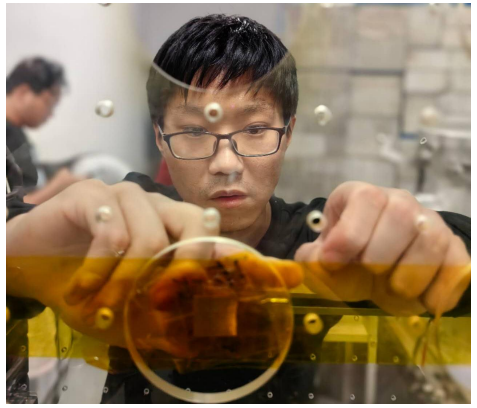


Leakage vs Radiation flux





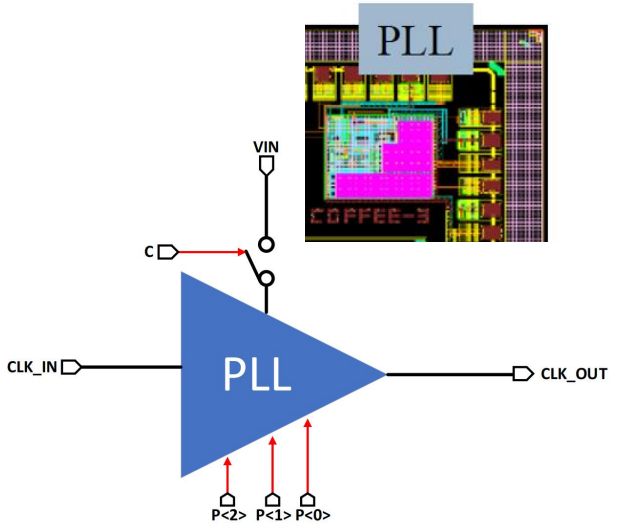


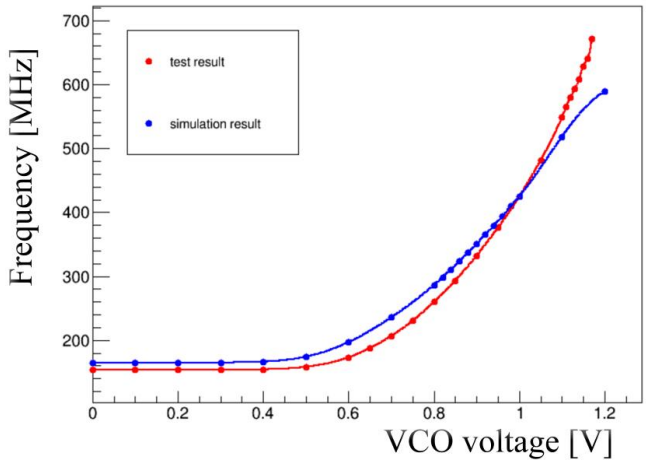


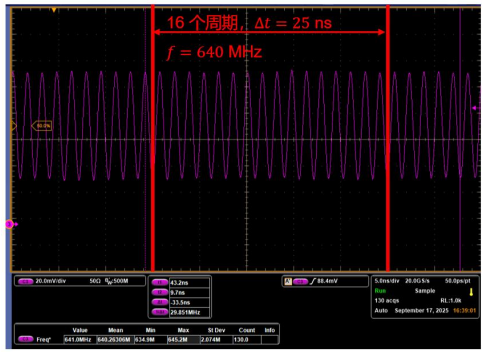
Zhiyu Xiang etc @ CSNS, IHEP

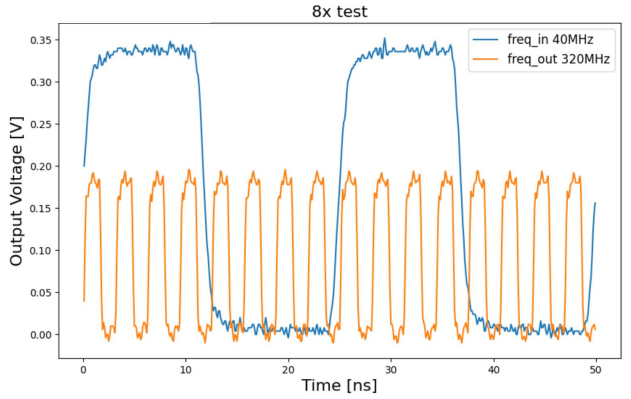
COFFEE3 PLL IP

- synchronizing the clock between FE chips and back-end DAQ
- converting input low-speed CLK to internal high-speed clock to support TDC and data transmission
- VCO control and frequency multiplication (x4, 8, 16) function works up to ~660 MHz
  - jitter noticed at highest speed, will improve in the next version
- working from room temp. to -50C



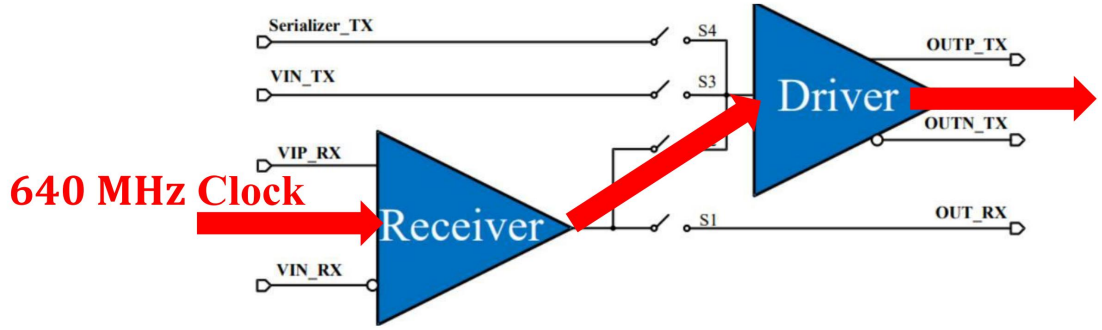


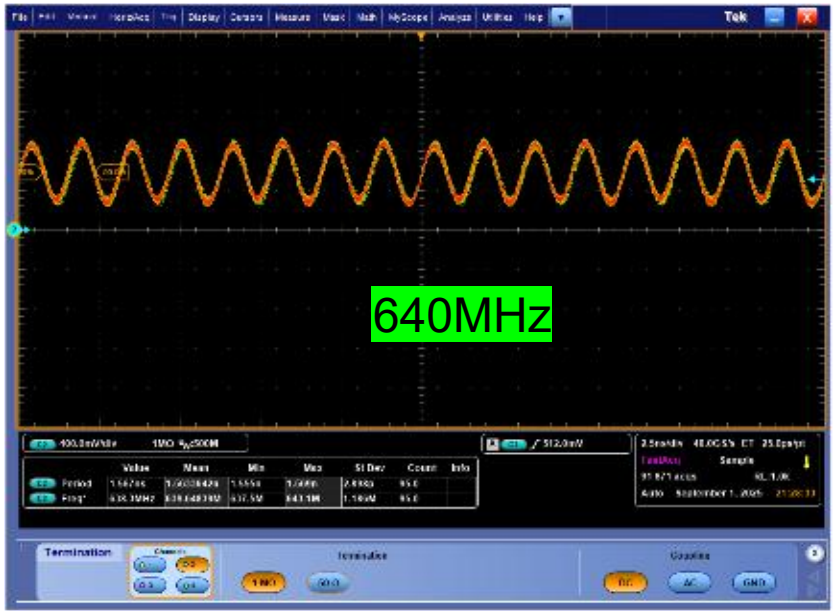




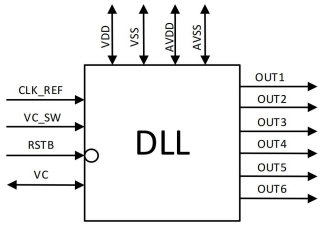
COFFEE3 LVDS and DLL IP

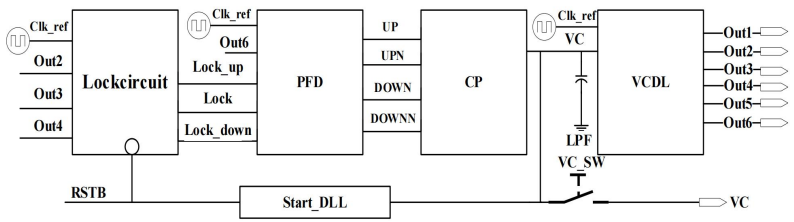
- LVDS transceiver Tx/Rx works up to 640 MHz CLK
  - high speed data transmission test in preparing (1.28 Gbps PRBS for example)





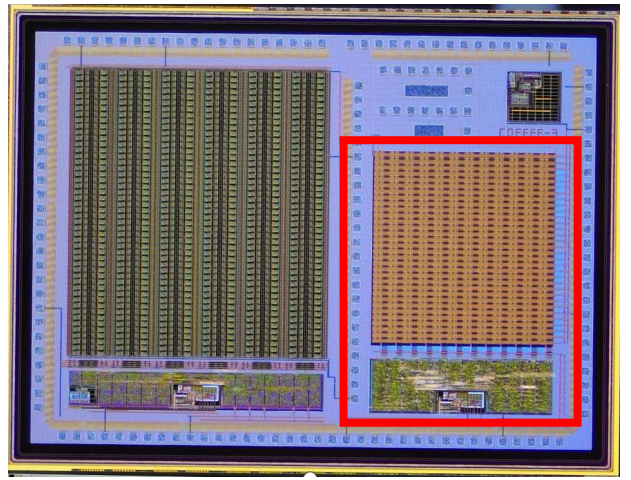
- Delay Locked Loop (DLL) delivers clock phase shifted as expected, for finer LSB of in-pixel TDC

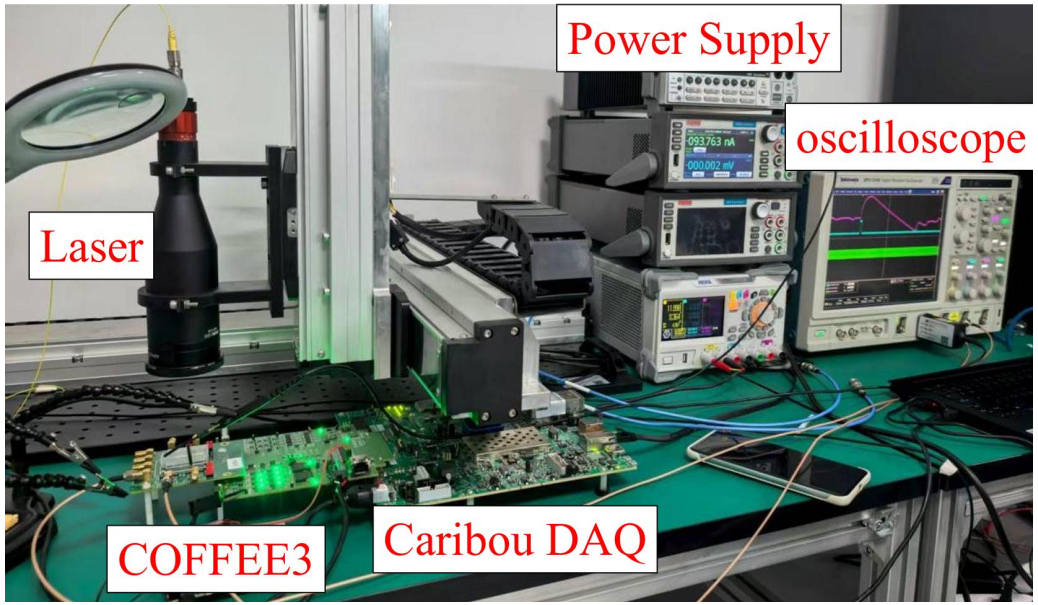




COFFEE3 Pixel-matrix-1

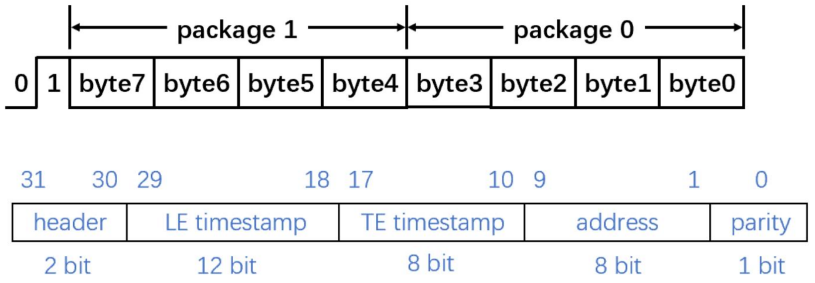
- in-pixel circuit + digital peripheral responsing to global charge injection and laser injection
  - digital readout schemes logics check are on going
  - time resolution measurement are on going
  - radiation source study in preparing

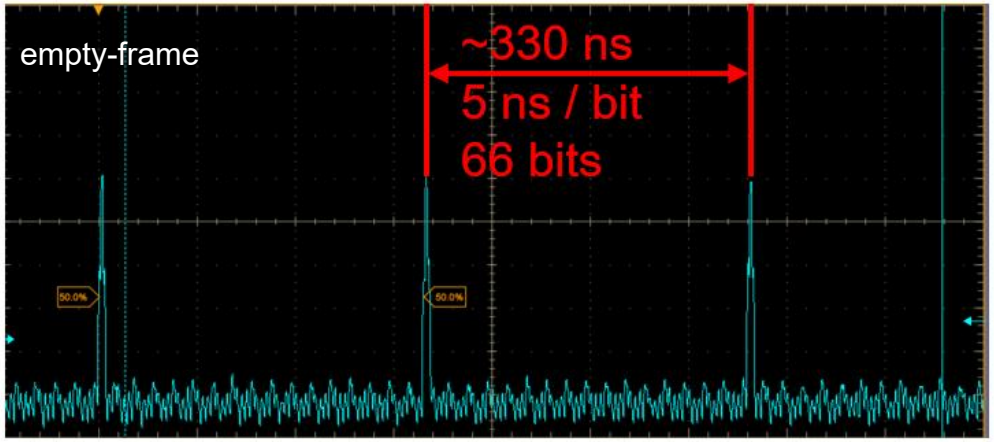


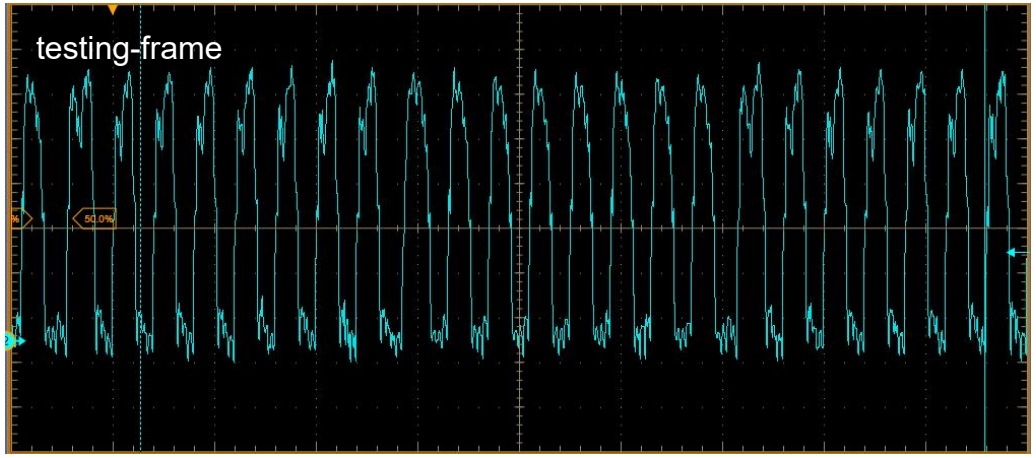


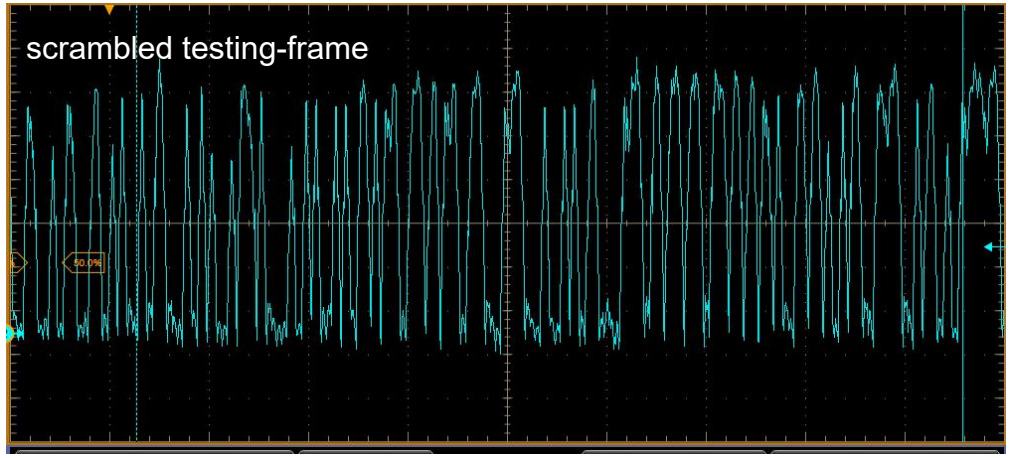
COFFEE3 Pixel-matrix-1: digital peripheral

- 64/66 encoder, scramble, testing/empty frame functions verified



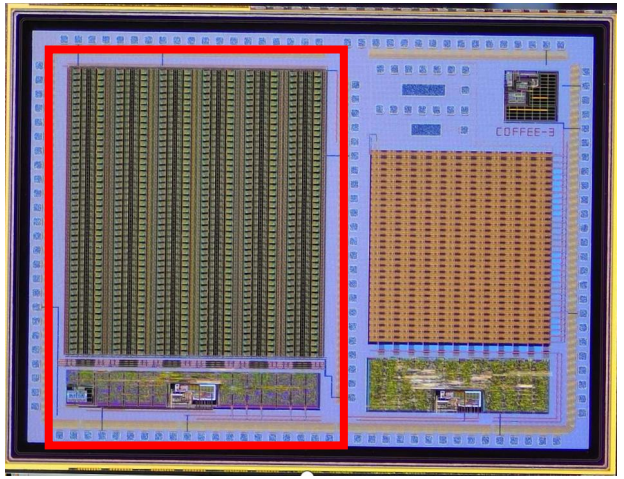


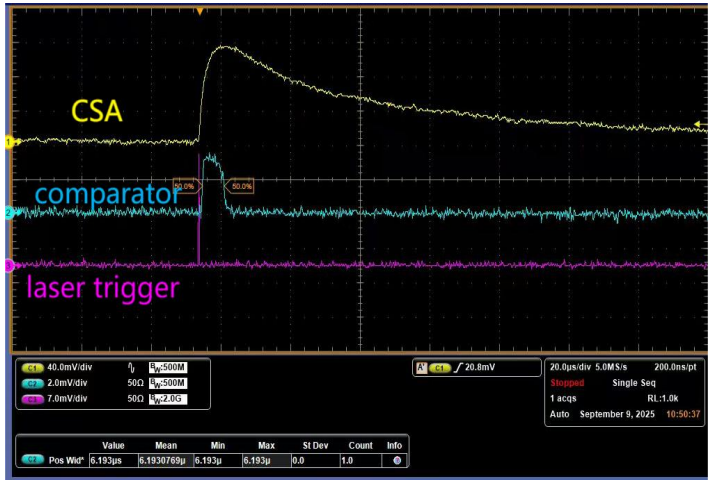


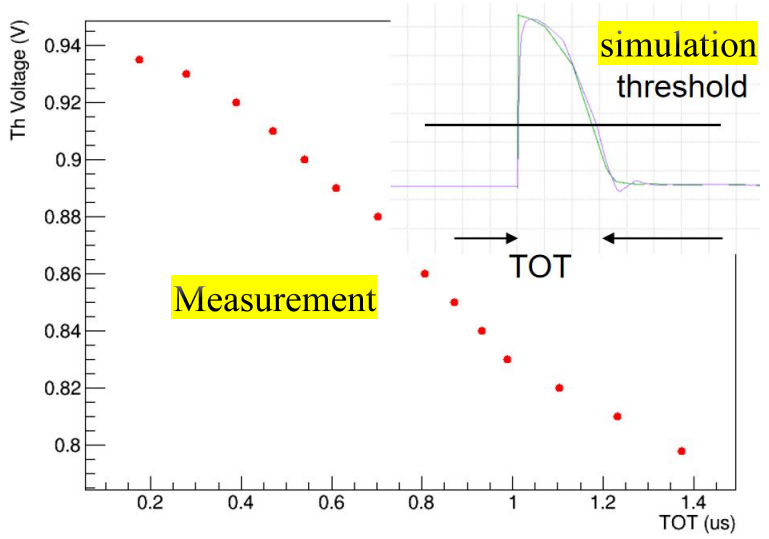


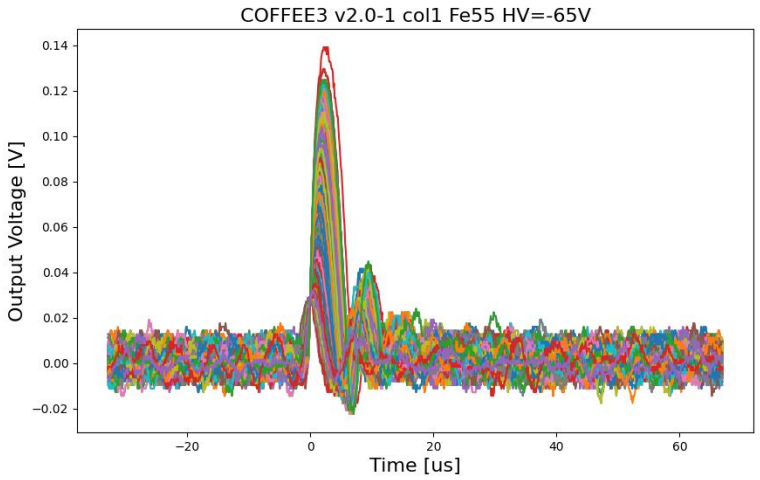
COFFEE3 Pixel-matrix-2

- In-pixel CSA and comparator output for laser signal
  - time-over-threshold (TOT) ~ 1 us, agree with chip simulation
- CSA responsing to ^{55}Fe source (6 keV X-ray)
  - carefully tuning reference-Voltages for in-pixel circuits will improve S/N



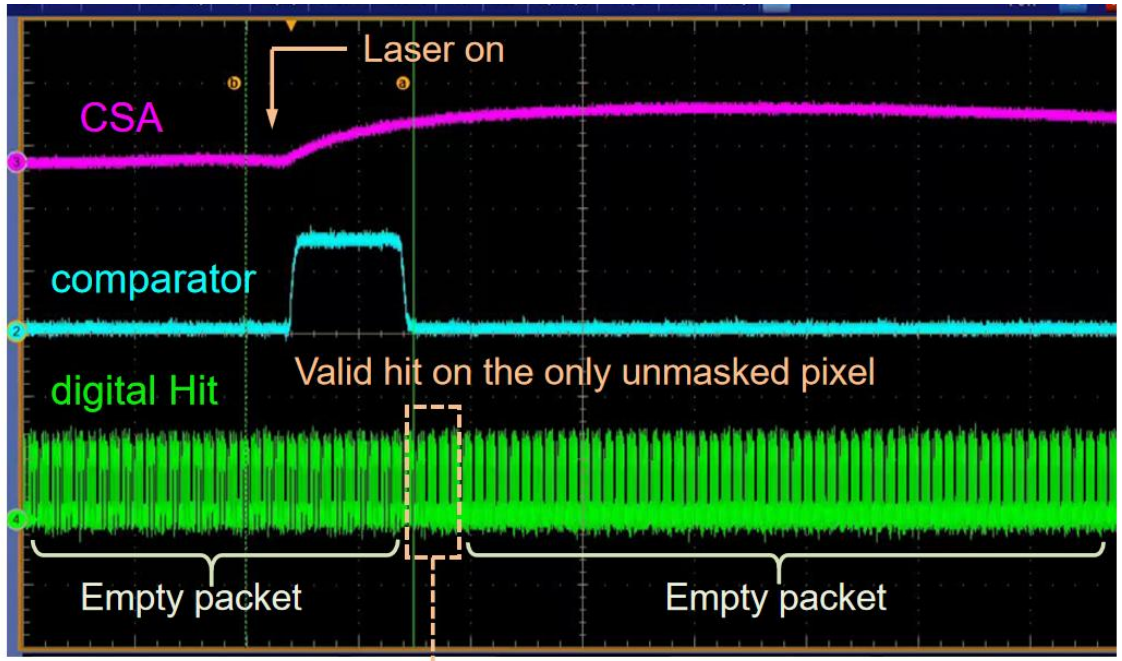






COFFEE3 Pixel-matrix-2

- Full-readout-chain with laser injection
- charge sensing diode → in-pixel (CSA\comparator\TDC) → digital peripheral serializer



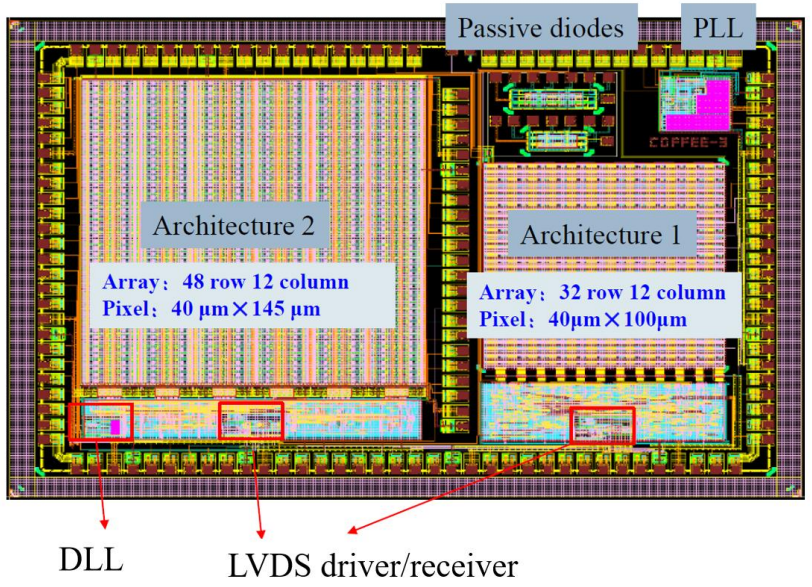
4 bit	4 bit	8 bit	8 bit	6 bit	2 bit	7 bit	3 bit
header	CHIP_TS	LE_coarse	TE_coarse	LE_fine	TE_fine	Addr_Row	Add_Col
0 1 1 0	0 1 0 1	0 0 0 1 0 1 1 0	0 1 1 0 1 0 1 1	1 1 0 0 0 0	0 0	0 0 0 0 0 0 1	0 0 0

A valid transmission packet corresponding to a hit

Correct row & column address

Summary and Next

- Encouraging results from COFFEE2/3:
  - V(Breakdown)~70V so far. High-Resistivity wafer will significantly improve
  - most analog/digital, in-pixel/EOC circuits verified
  - TDC/TOT timing performance on going
  - radiation source, cosmic ray, testbeam on going
- irradiation by DRD3 collaboration: 2026-Jan
- test-beam by DRD3 collaboration: next year
- **process modification + high-R wafer** for 55nm HV-CMOS will submit soon



COFFEE3 goals

- **In-pixel analog: CSA, comparator** ☑
- In-pixel digital: TDC, memory
- **Data-driven readout** ☑
- **DLL** ☑
- **LVDS transceiver** ☑
- **Function configuration; serializer** ☑
- End of Column; **data scrambler**

COFFEE Teams

- **Chip design:**
  - **COFFEE2**：Weiguo LU, Mei ZHAO, Kunyu Xie, Leyi Li, Ruoshi DONG, Yang CHEN, Xuekang LI，Xinyang GUO, Zhuojun CHEN, Yang ZHOU;

  & **Independent KIT design**: Hui ZHANG, Ruoshi DONG, Ivan PERIC；
  - **COFFEE3:** Leyi Li, Xiaoxu ZHANG, XiaoMin WEI, Weiguo LU, Pengxu LI, Mei ZHAO, Yang CHEN，Yujie WANG, Huimin Wu, Zexuan ZHAO, Yu ZHAO, Zheng Wei, Jianpeng DENG, Zhan SHI，Yang ZHOU;
- **Chip test and validation:**
  - Zhiyu Xiang, Zijun Xu, Zeng CHENG，Menke Cai, Boxing Wang, Yuman Cai, Weiguo LU, Mingjie FENG, Hui ZHANG, Jianpeng DENG, Pengxu LI , Hongbo ZHU, Yiming Li …….

More collaboration and experts are desired for the chip development……

Backup

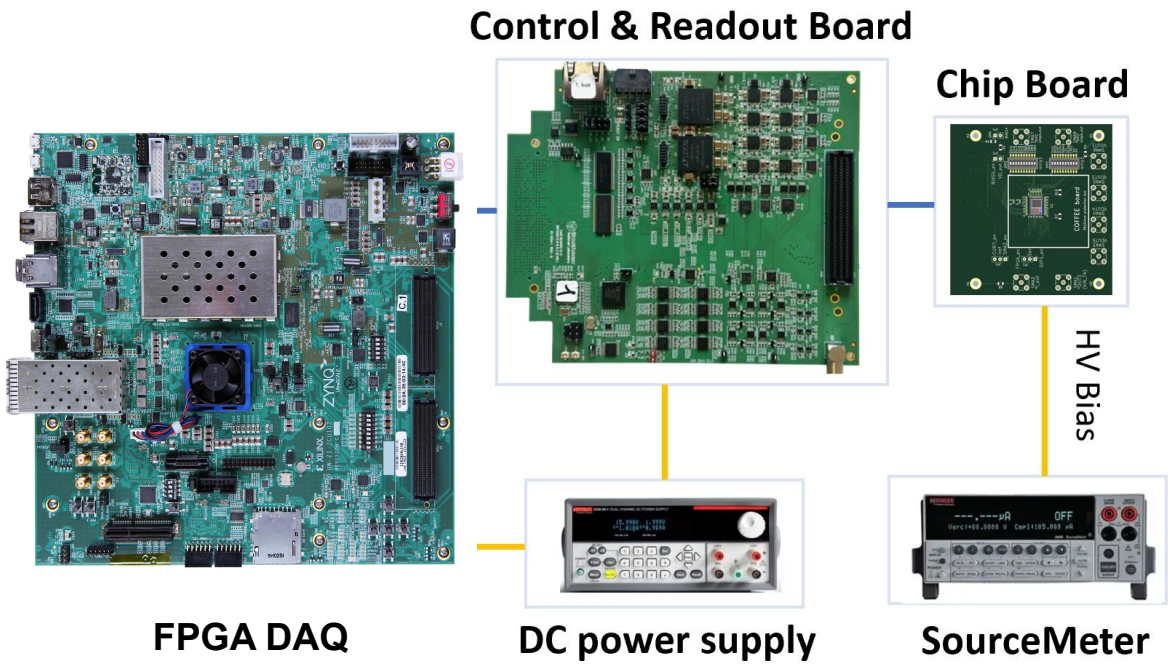
Bench-top DAQ Setup

- Caribou DAQ from DRD3: power, clk, DAC, slow-ctrl, fast readout, …
- FE chip specific carrier board, firmware IP, and software by ourself

Control and Readout (CaR) board

Feature	Description
Adjustable Power Supplies	8 units, 0.8 – 3.6 V, 3 A
Adjustable Voltage References	32 units, 0 – 4 V
Adjustable Current References	8 units, 0 – 1 mA
Voltage Inputs to Slow ADC	8 channels, 50 kSPS, 12-bit, 0 – 4 V
Analog Inputs to Fast ADC	16 channels, 65 MSPS, 14-bit, 0 – 1 V
Programmable Injection Pulsers	4 units
Full-Duplex High-Speed GTx Links	8 links, <12 Gbps
LVDS Links	17 bidirectional links
Input/Output Links	10 output links, 14 input links, 0.8 – 3.6 V
Programmable Clock Generator	Included
External TLU Clock Reference	Included
External High-Voltage (HV) Input	Included
FEAST Module Compatibility	Supported
FMC Interface to FPGA	Included
SEARAY Interface to Detector Chip	320-pin connector

Resources for various target applications



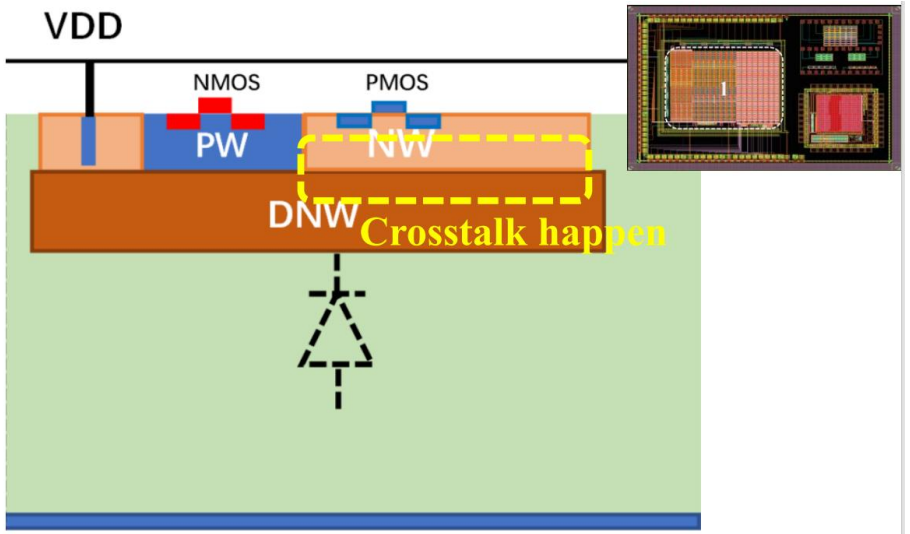
HV-CMOS

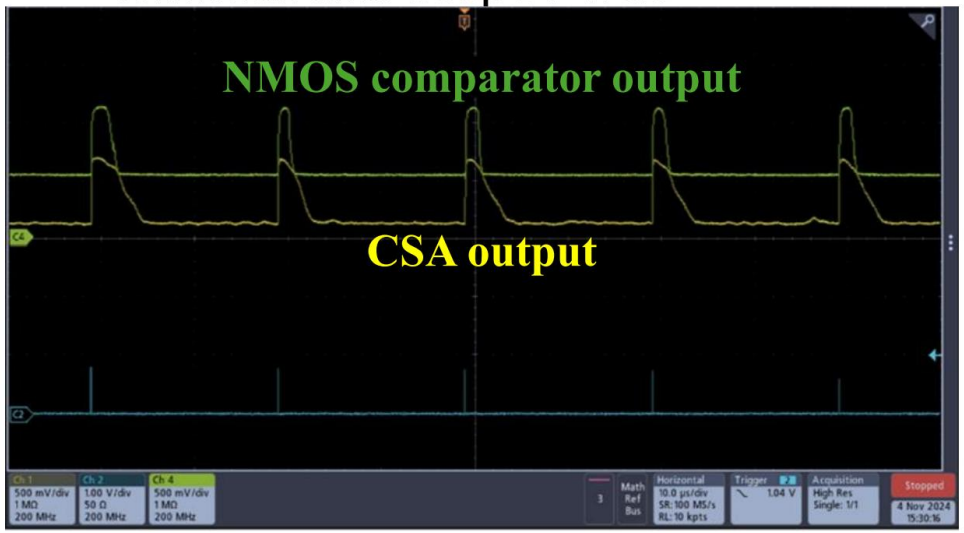
Table 5.3: The HV-CMOS sensor key parameters

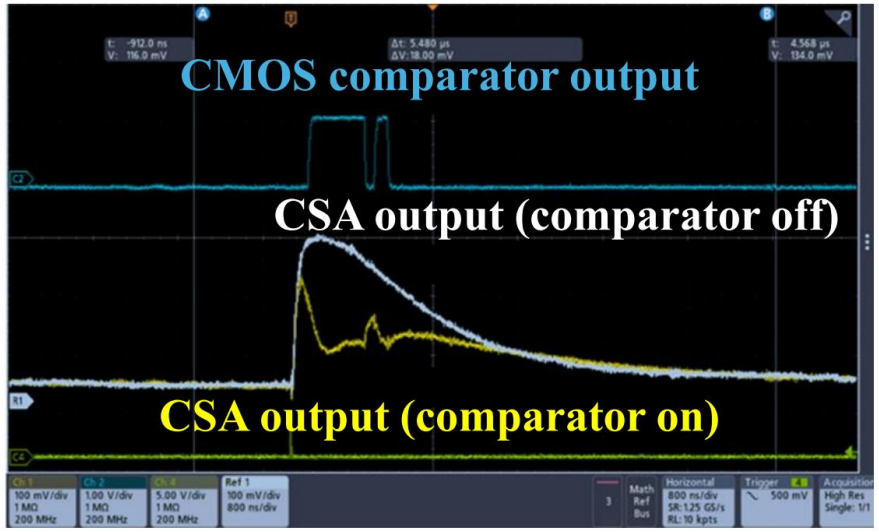
Parameter	Value
Sensor size	2 cm × 2 cm (active area: 1.74 cm × 1.92 cm)
Sensor thickness	150 μm
Array size	512 × 128
Pixel size	34 μm × 150 μm
Spatial resolution	8 μm × 40 μm
Time resolution	3–5 ns
Power consumption	200 mW/cm^2
Technology node	55 nm

COFFEE2: in-pixel Ana/Digi-circuit X-talk

- Laser test : JINST 20 (2025) C10011
  - NMOS comparator work well
  - Crosstalk issue seen among CMOS comparator and CSA.
  - Potential flip in digital circuitry cause the disturbance between N-well of PMOS bulk terminal and deep N-well







HV-CMOS

	2023				2024				2025				2026				2027				2028			
	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4
Key funtions				COFFEE3 design																				
									production															
										COFFEE3 test														
Process modification											MPW design													
													production											
													test											
Quarter-size chip												quarter-chip design												
																production								
																	quarter-chip test							
Full-size chip															full-size chip design									
																			production					
																				full-size chip test				