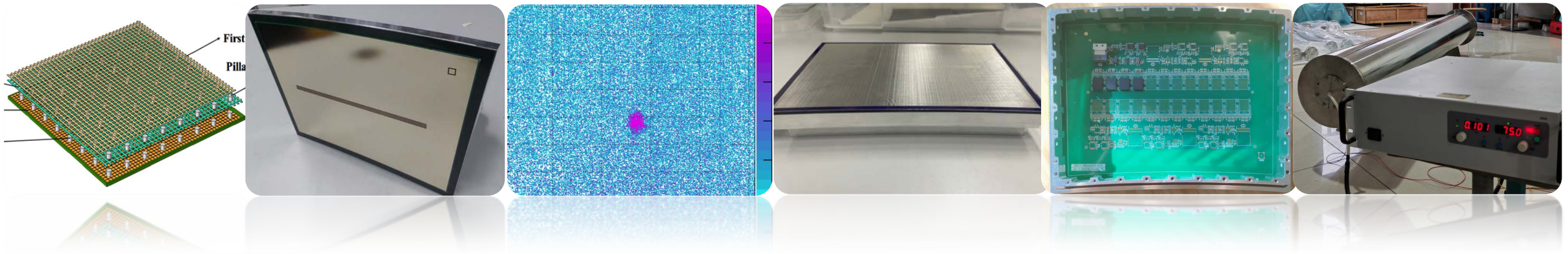


Progress of TPC module and prototype R&D

Huirong Qi

28 January 2026, IHEP

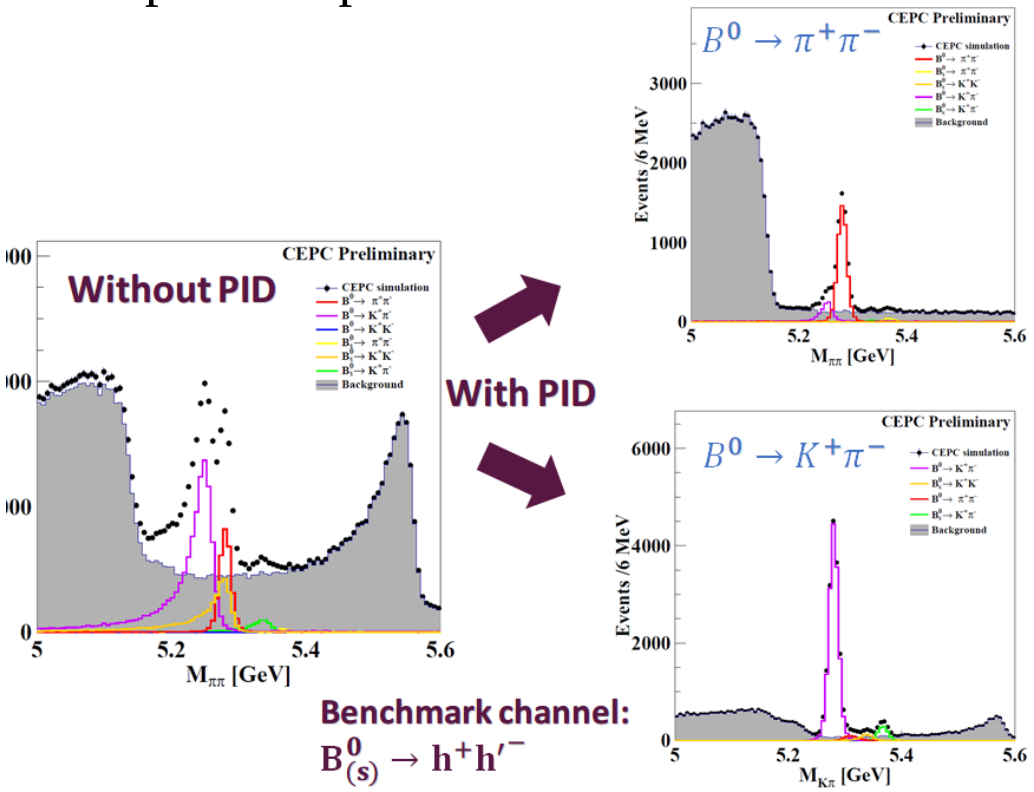
Content

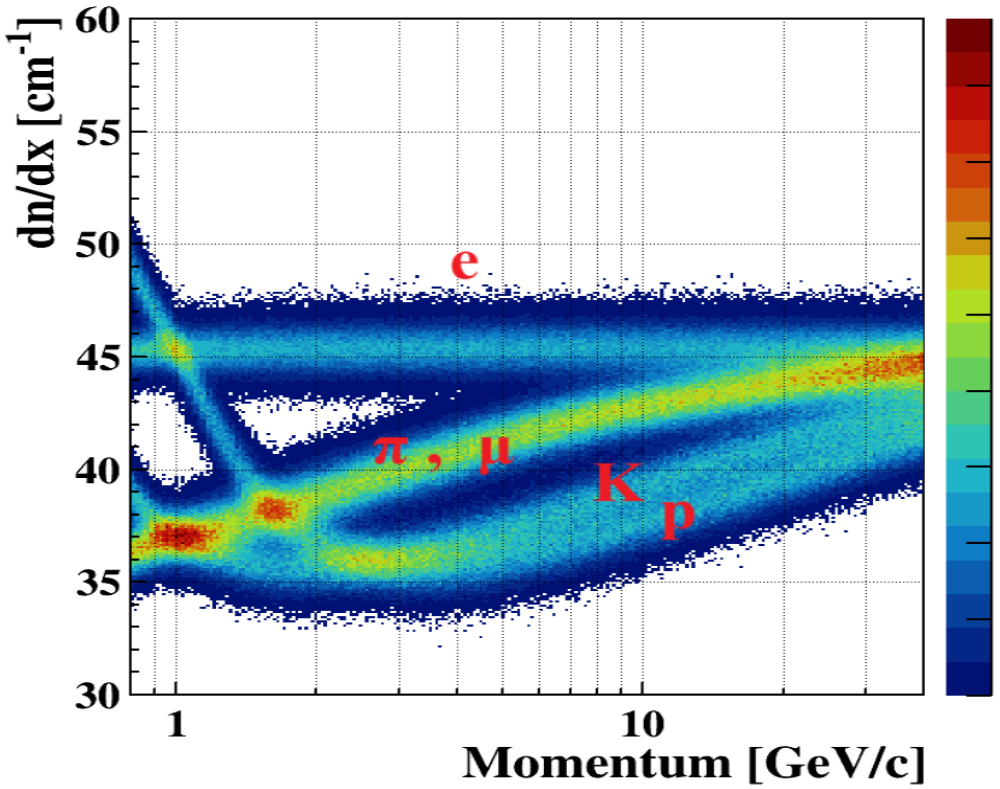
- **Motivation**
- **High granularity readout R&D**
- **Status of TPC module and prototype**
- **Work plan and summary**

Motivation: Physics requirements in CEPC

- Circular e+e- collider operation stages in TDR: **10-years Higgs @3T → 2-years Z pole → 1-year W**
- Gaseous tracker leading contribution to PID and the high resolution: jet & differential
  - High granularity readout readout and better than 2σ separation power between π and k for P using dn/dx

Calibration: Low luminosity Z at 3T
Approximately $10^{35}cm^{-2}s^{-1}$
20% of high luminosity Z





TPC technology in CEPC ref-TDR

TPC technology detector for e+e- collider

Pad readout TPC
- To meet Higgs physics
- 1mm×6mm of Pad
- < 100mW/cm^2
- dE/dx
- Triple, double GEMs
- Micromegas

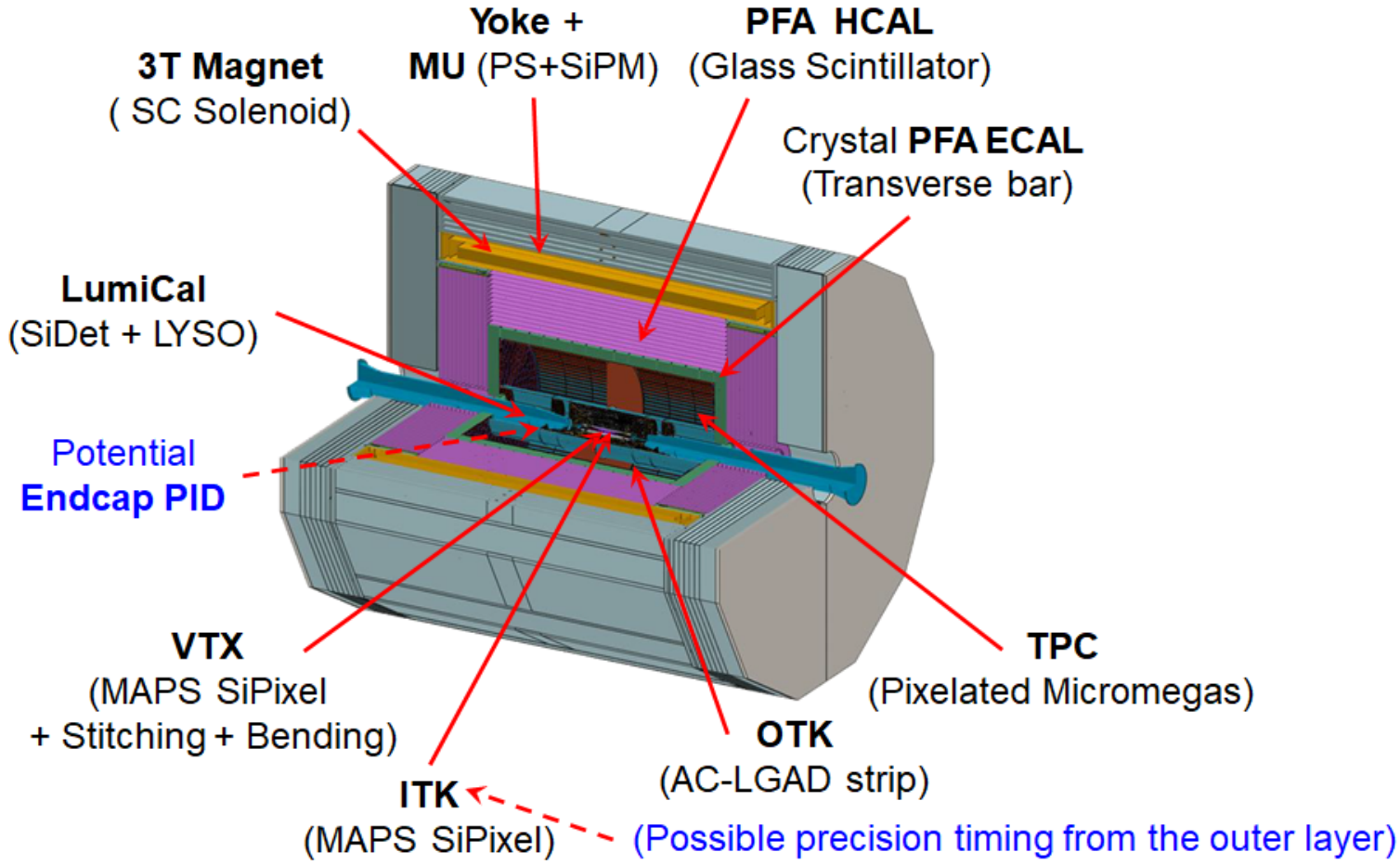
Pixelated readout TPC
- To meet Low-lumi Z physics
- TPX3 and TPX4
- ~1W/cm^2
- dN/dx+dE/dx
- GirdPix
- Interposer
- Direct mode

- CEPC community initiated the technical comparison and selection, balancing factors including **R&D efforts, detector performance, cost, power consumption and construction risks**.

Baseline Detector Design in TDR

- Will explore the possibilities of
  - A forward PID detector inside TPC
  - The outer layer ITK also provides precision timing

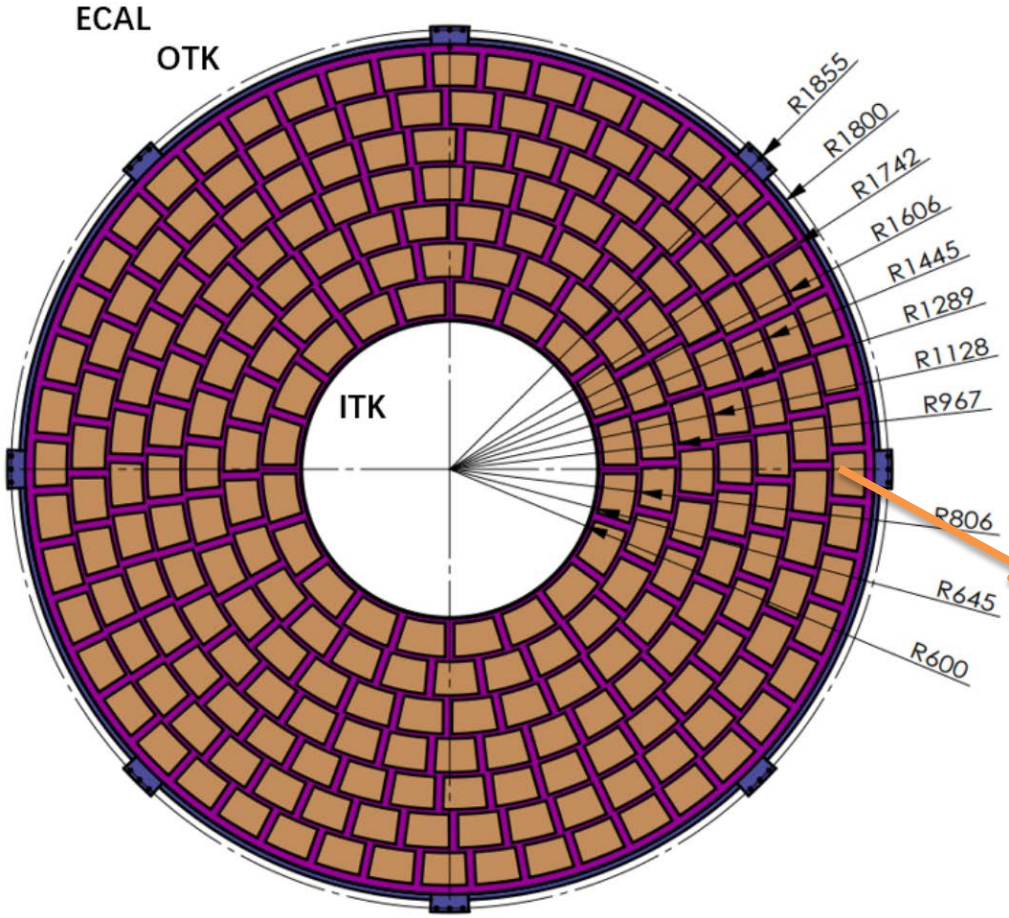
- After 10-year operation, the majority will remain, a few may be upgraded, including
  - VTX: for a better performance and radiation tolerance
  - TPC: to deal with higher luminosity

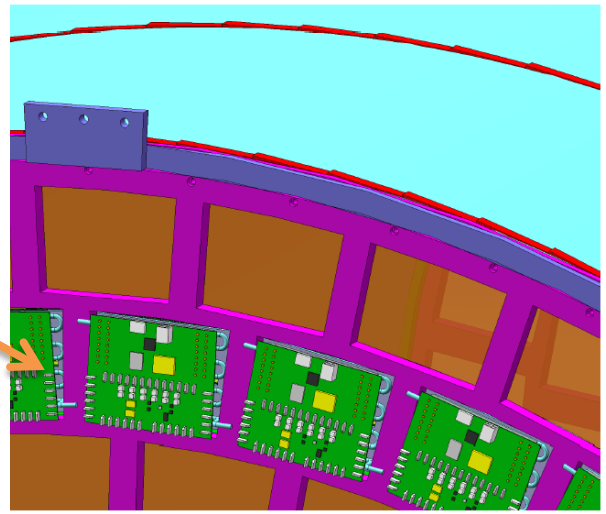


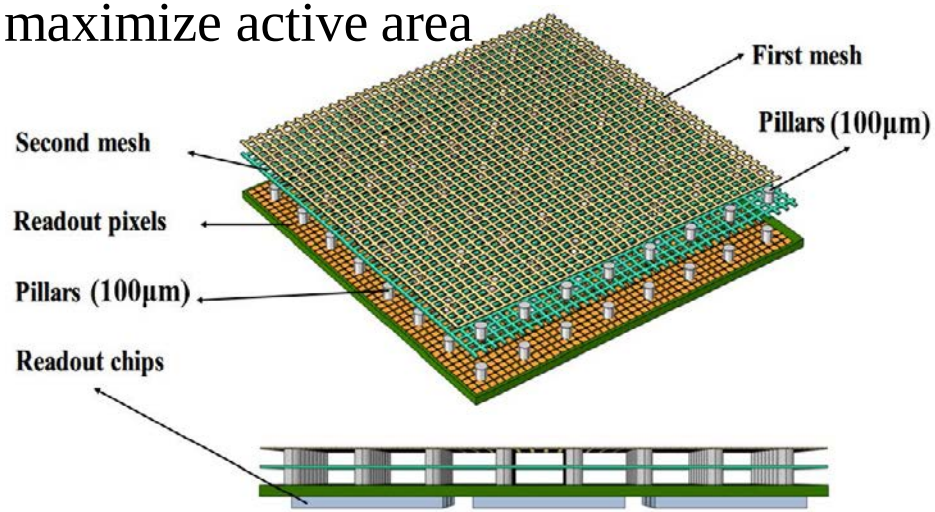
https://arxiv.org/abs/2510.05260

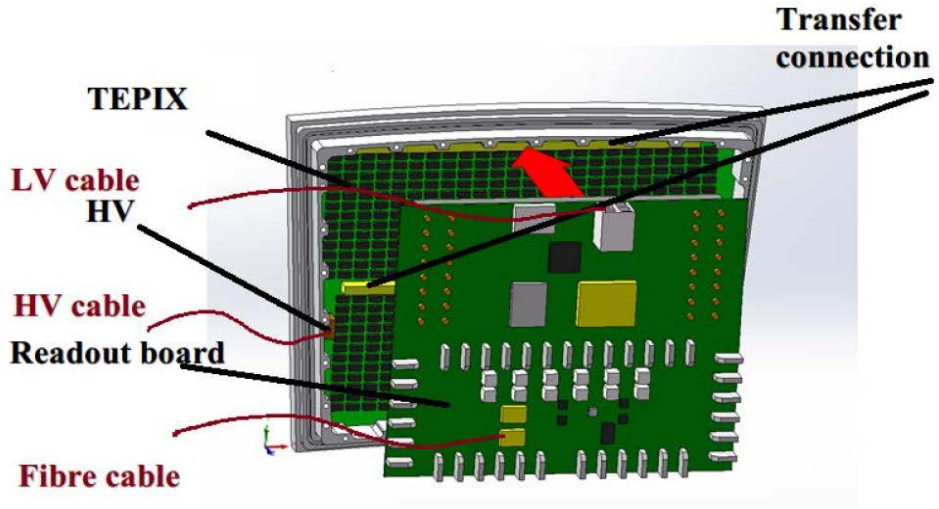
Readout module design

- Readout modules on the endplate
  - 25mm thick aluminum endplate: 7 layers of windows along the radial direction
  - Readout modules with support frame installed in windows to maximize active area



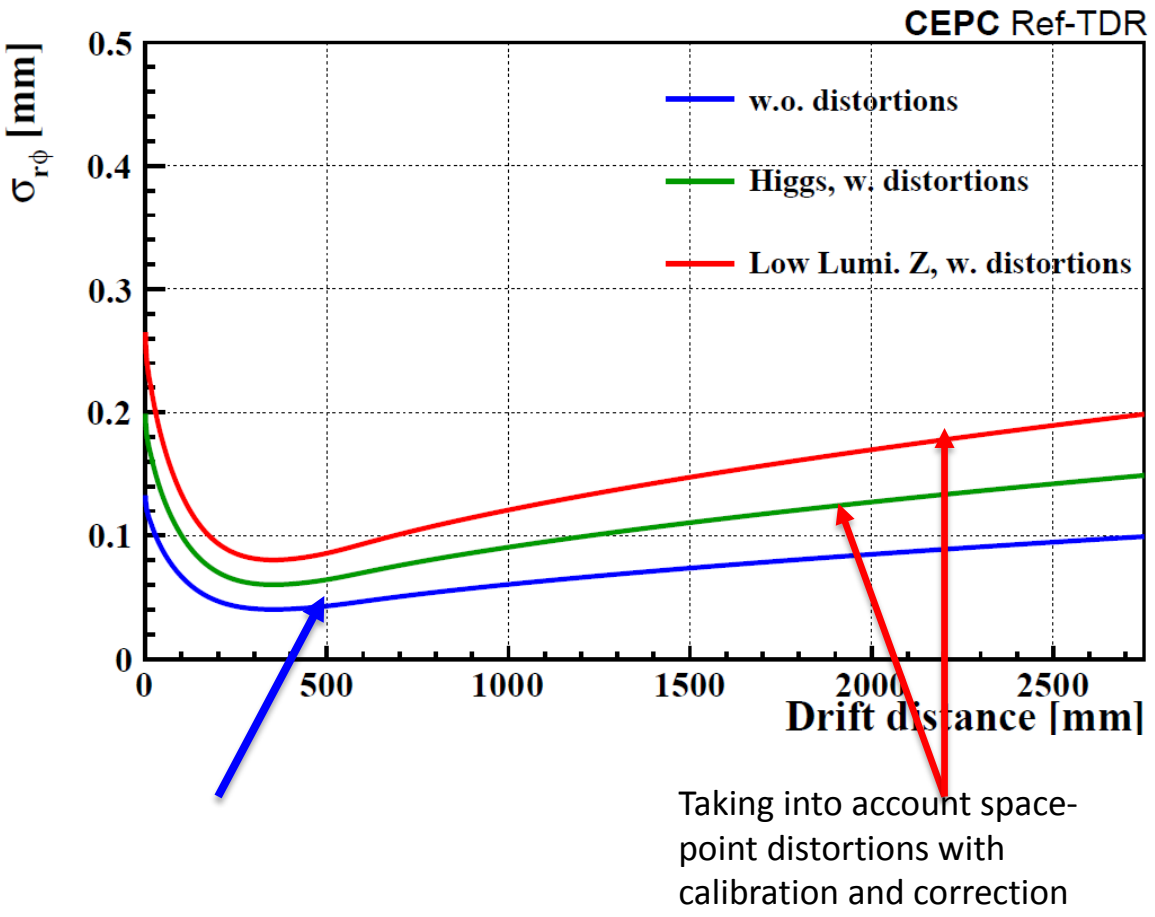






Full Simulation of High granularity readout TPC – Spatial resolution

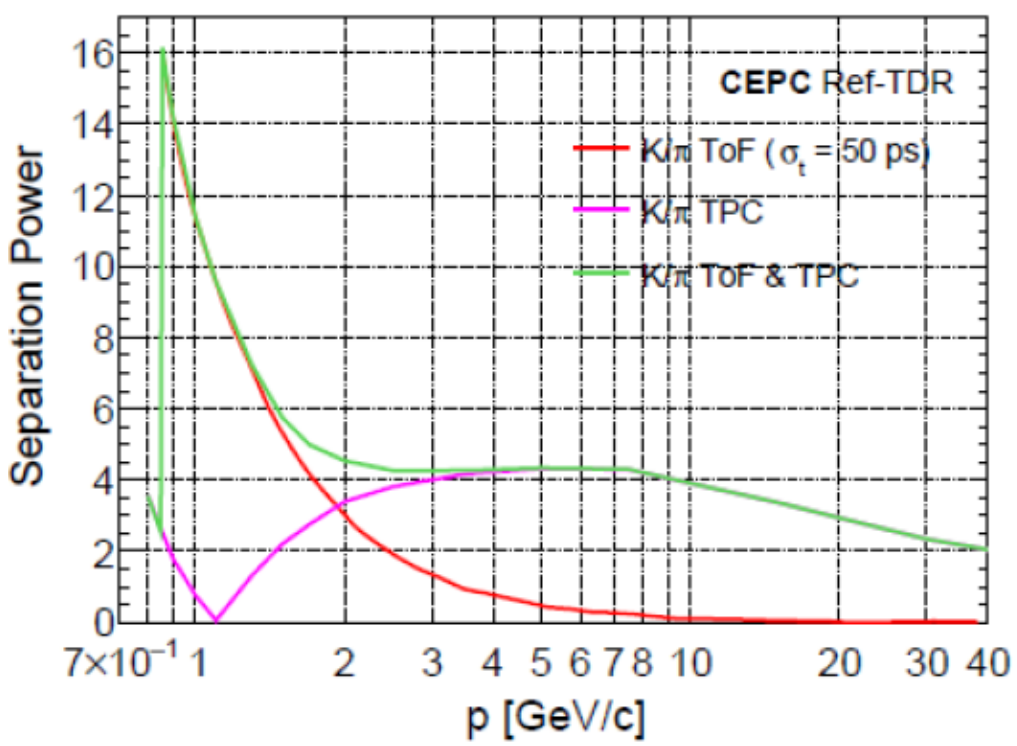
- Impact of space-point distortions on spatial resolution
  - Space-point distortions can be corrected by the data-driven track-based calibration
  - Error contributions to the calibrated spatial resolution :
    - Space-charge distortion: < 80μm in Higgs, <160μm in low-lumi. Z, dependent on L_{drift}
    - NUMF effects on the drift process (after correction with B field map): <65 μm
- Conservatively estimated, the calibrated spatial resolution degrades by ~50% and 100% at the point with the longest drift distance in Higgs and low-luminosity Z modes respectively.



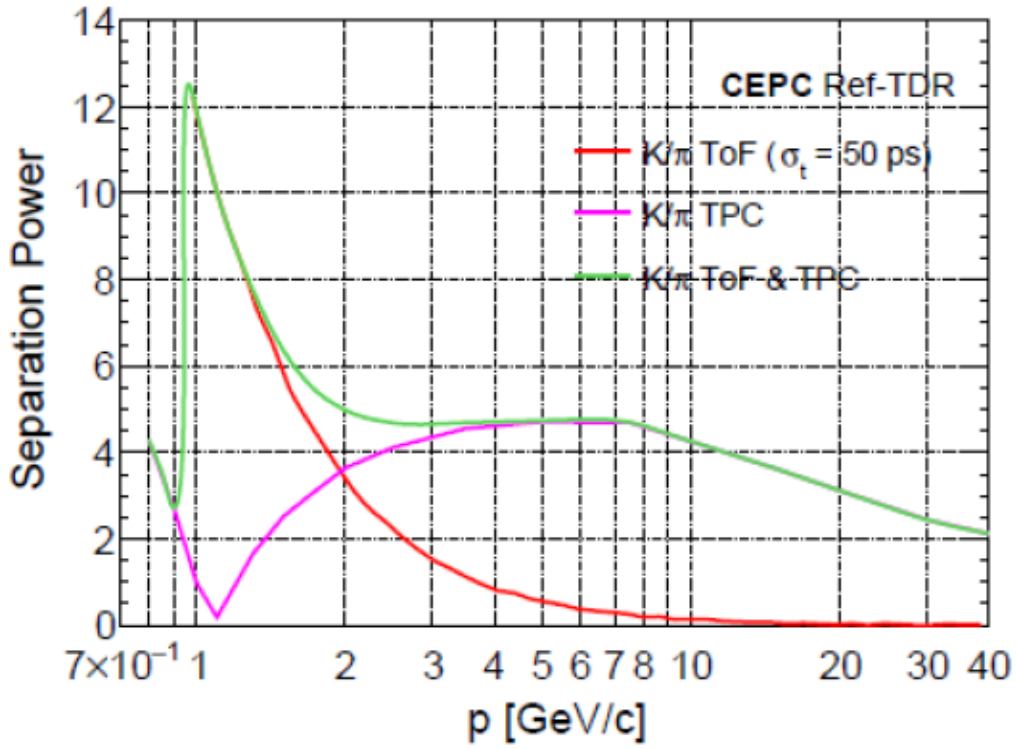
Full Simulation of High granularity readout TPC – PID performance

- K/π separation power using the combined information of ToF and TPC
  - ToF information compensates for momentum range of around 1GeV/c
  - Larger than 3σ separation between k/π with momentum up to 20 GeV/c

$$\eta_{A,B} = \frac{|\mu_A - \mu_B|}{\sqrt{(\sigma_A^2 + \sigma_B^2)/2}}$$



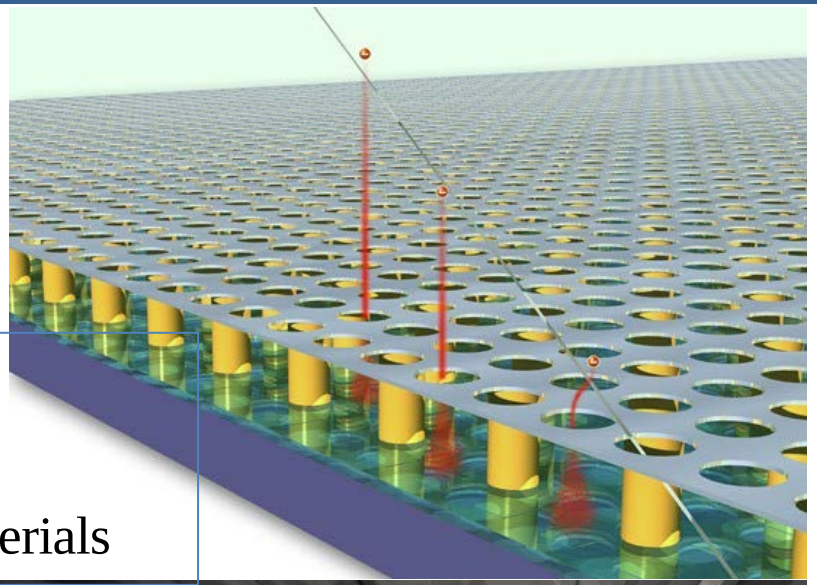
(a) $\theta = 85°$

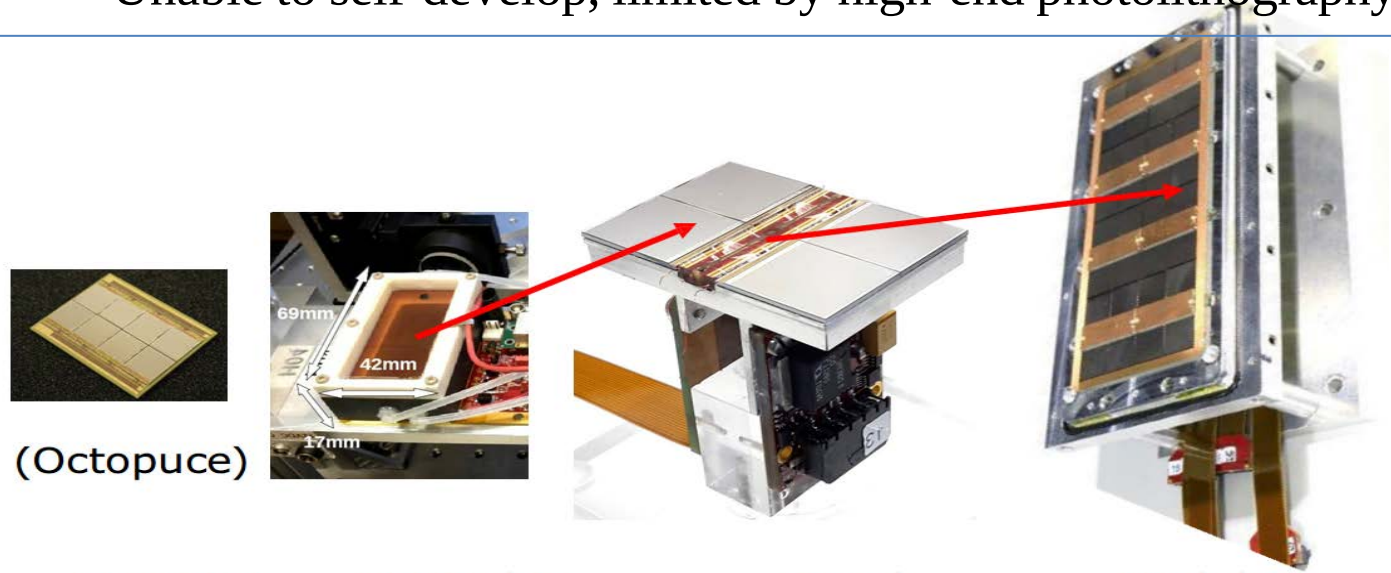


(b) $\theta = 60°$

High granularity readout: Micromegas - GridPix

- GridPix from Timepix3 to Timepix4 ASICs. Tests with quad devices have been successfully done under B=1.0T at DESY.
- Very high detection efficiency results in excellent tracking and dE/dx performance. All results showed that a pixel TPC is realistic. (~10^6 events)
- **Key issues to address**
  - High power consumption (2W/cm^2)
  - Unable to self-develop, limited by high-end photolithography mask materials

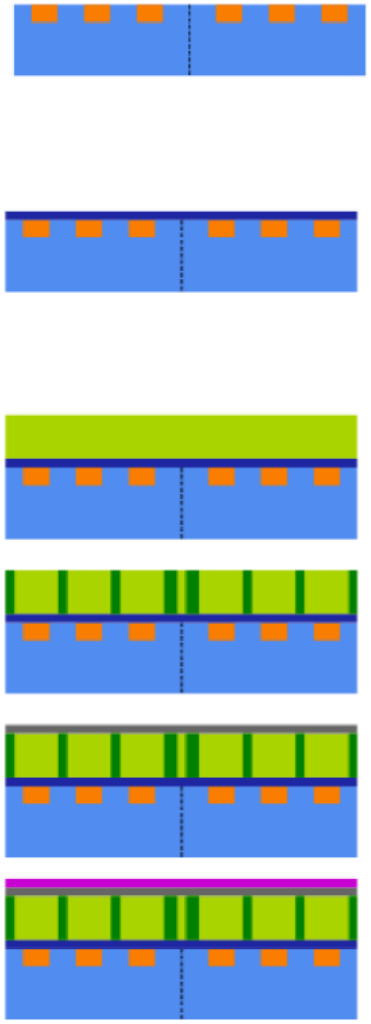




NÌM A535 (2004) 506-510
NIM A845 (2017) 233-235

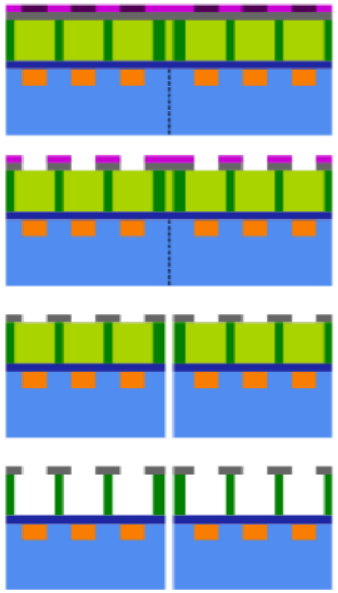
Production: Micromegas - GridPix

- The Timepix3's pixel pitch of 55 µm × 55 µm is matched by a grid with 35 µm diameter circular holes.
- The 1 µm thick aluminum grid is supported by 50 µm high SU8 pillars.



1. The wafer is prepared: the chips are probed to find electronic failures and the surface is cleaned
2. A high-resistive 4 µm thick SiRN protection layer is deposited on the chip in order to protect the chip from discharges. A protection layer on the bonding pads would hinder electrical connections, and is avoided by temporarily covering them with polyamide.
3. The wafer is covered with a 50 µm thick layer of SU-8 photoresist.
4. Using a special mask, part of the SU-8 is exposed to UV light, solidifying it to create the pillar structure.
5. A 1 µm thick aluminium layer is deposited.
6. Another 1 µm thick layer of photoresist is applied.

NIKHEF and Fraunhofer Institute

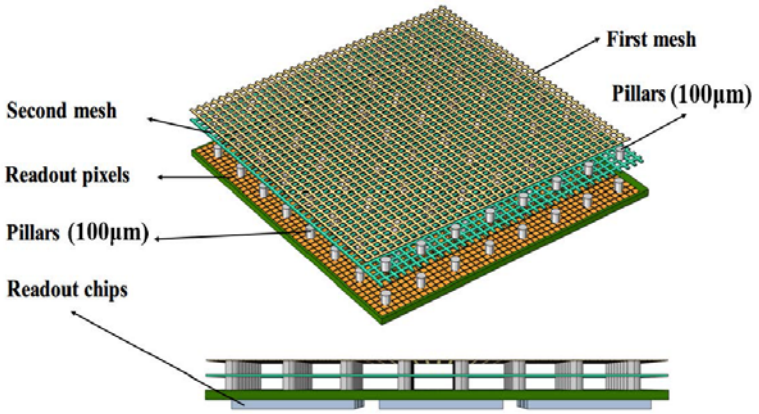


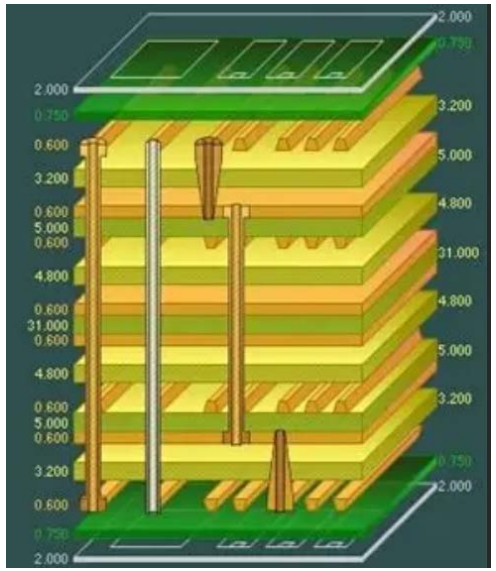
7. With UV light and another mask, a hole pattern is created.
8. The grid holes are chemically etched.
9. The wafer is diced into individual chips using a saw.
10. The unexposed SU-8 photoresist is resolved and the chips are ready.

S. Tsigaridas, *New Generation GridPix: Development and characterization of pixelated gaseous detectors based on the Timepix3 chip*. PhD thesis, Amsterdam U., 2017. http://www.nikhef.nl/pub/services/biblio/theses_pdf/thesis_S_Tsigaridas.pdf.

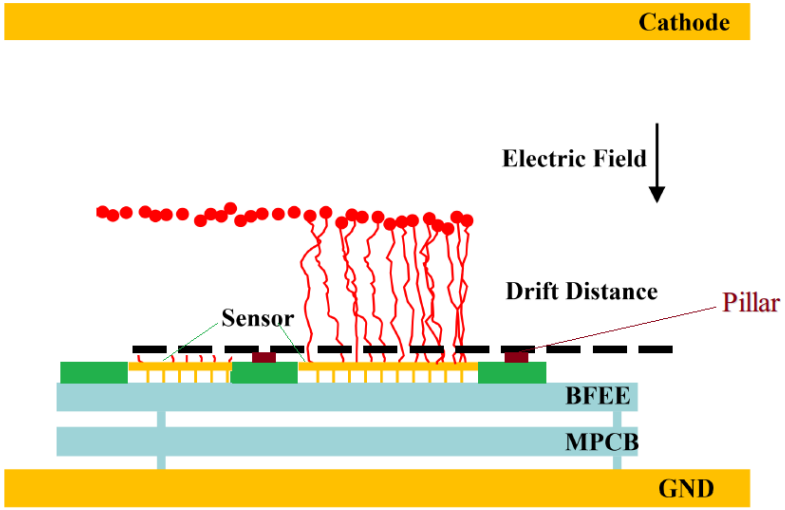
High granularity readout: Micromegas – Interposer and direct mode

- #1: Interposer mode
  - Readout pads on top layer, readout chips on bottom layer, requiring multi-layer routing—high difficulty and high cost
  - 1.2mm PCB board with 12 layers routing
  - Potential for increased signal noise





- #2: Direct readout mode
  - Similar to GridPix but without photolithography masking
  - Readout sensor chips are used directly for readout, with Micromegas as the amplification layer above.

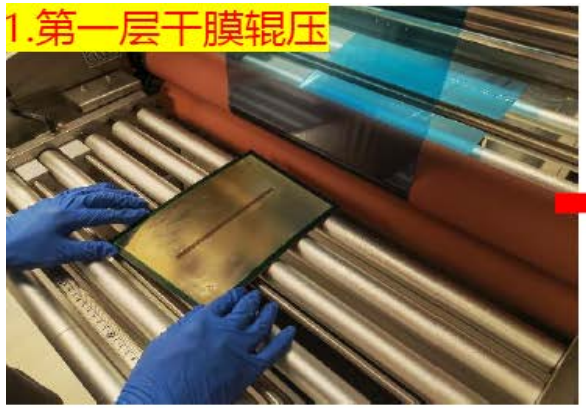


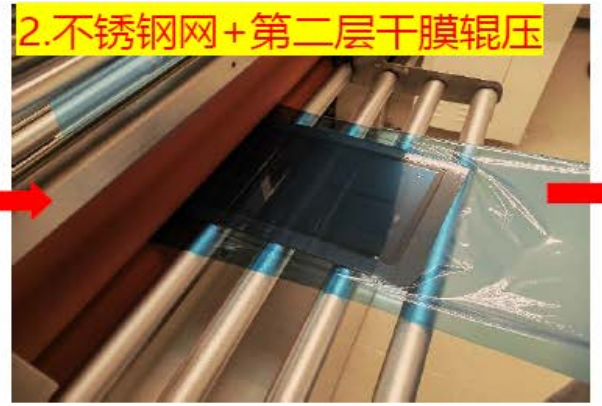
- **Key issues to address**
  - Requires low power consumption readout chips and further R&D.

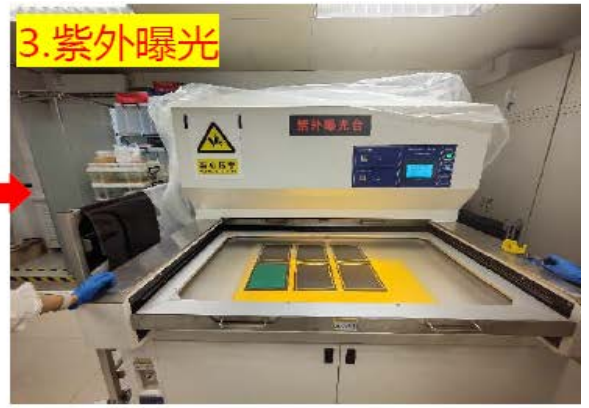
- **Status of TPC module R&D**

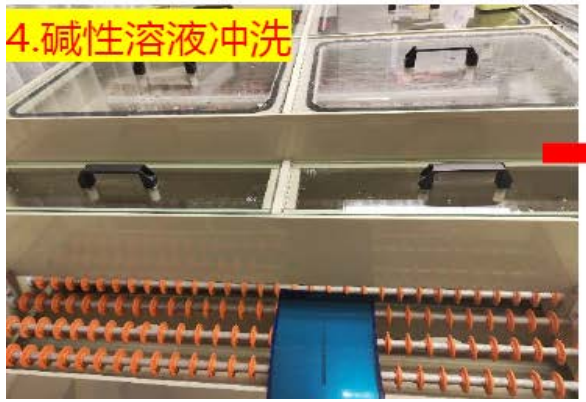
Production of TPC module: double-mesh Micromegas

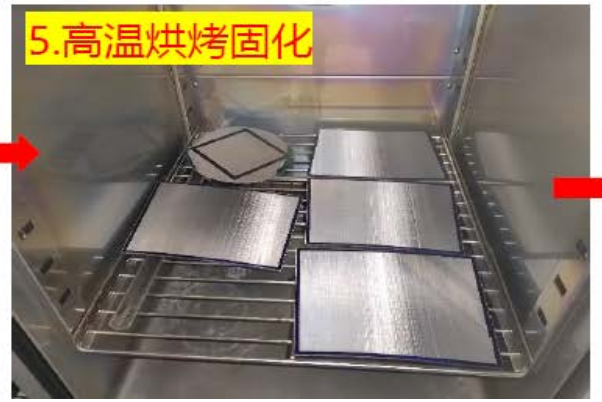
- Achievements:
  - R&D on high granularity readout PCB board
    - 12-layer PCB inner routing, surface gold-plated flat finish
    - Top layer with Micromegas, bottom layer with the pixel readout chips

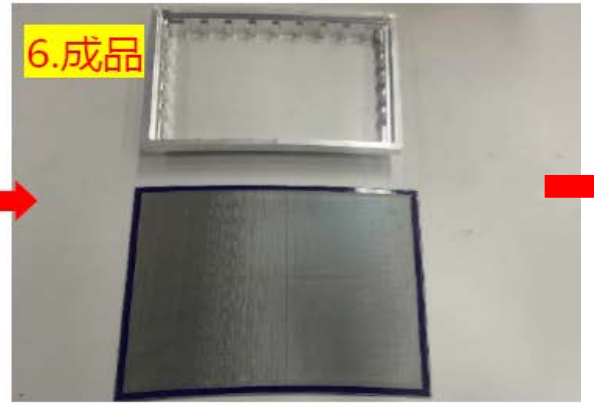


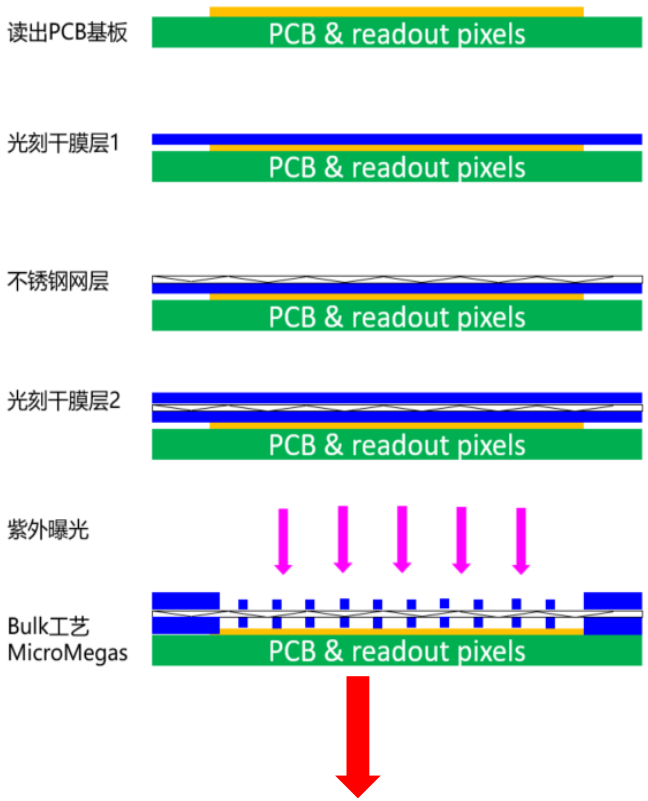


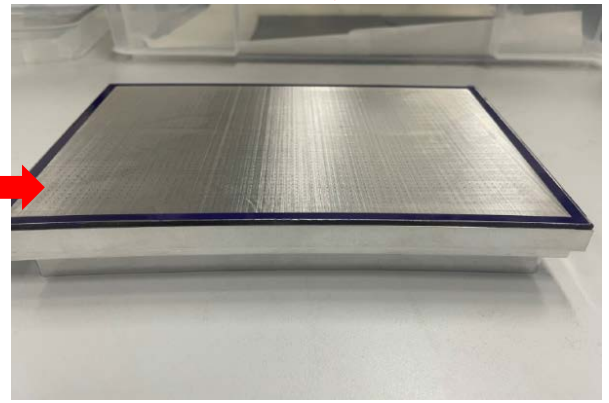








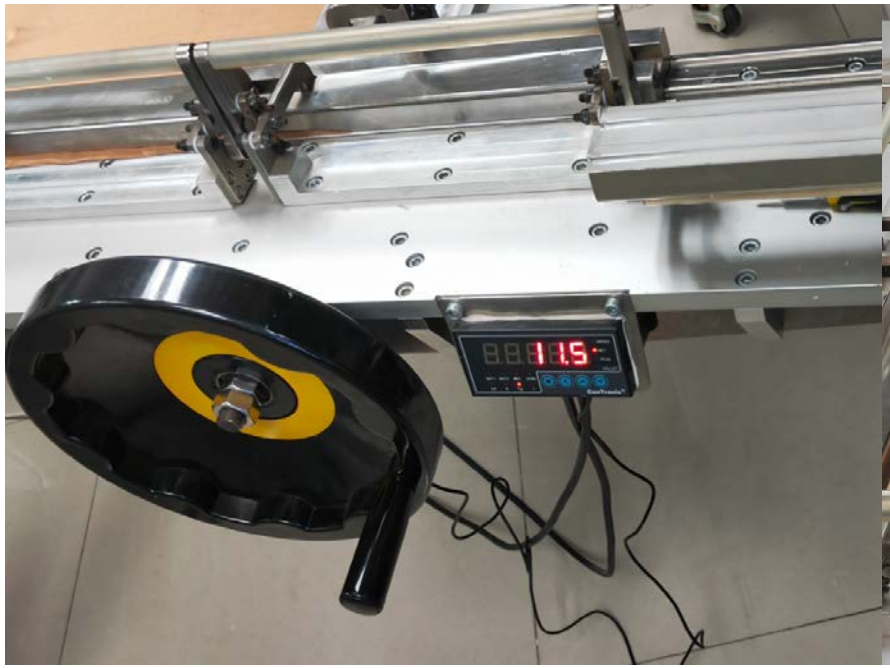
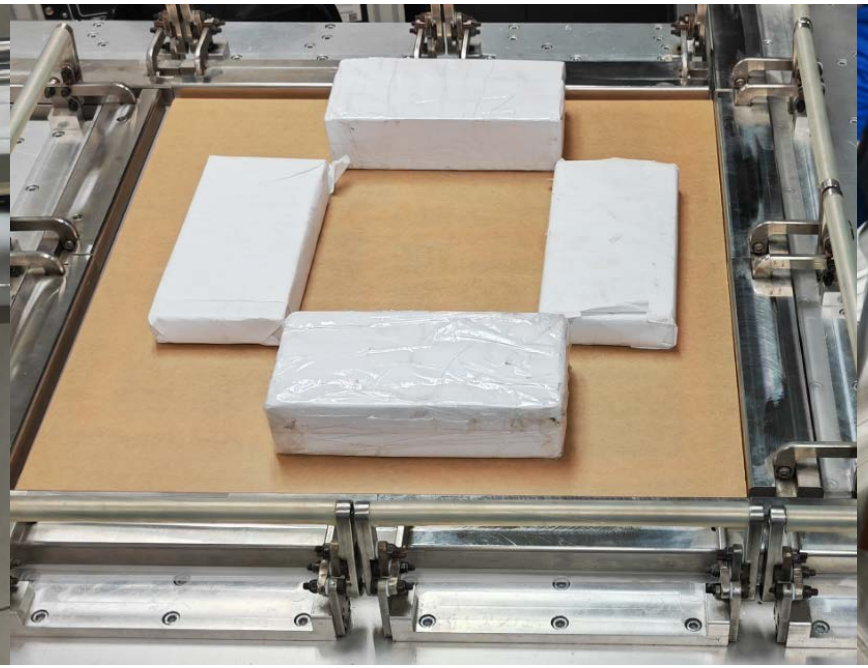
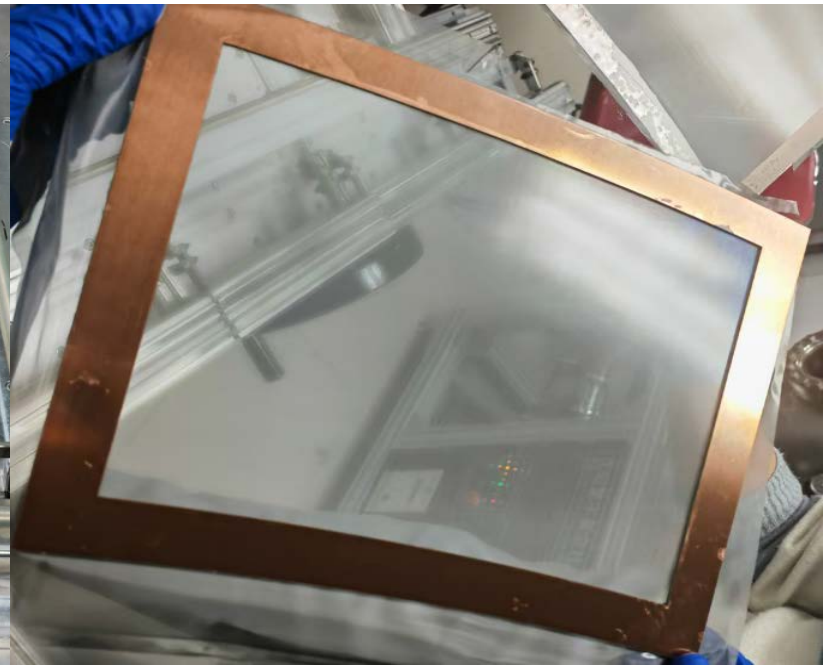




Production of TPC module

- Key Issues to Address
  - Multilayer screen tension control (>10 kg)
  - Flat roller pressing of mesh, mesh node control
  - Uniform 100°C baking control in the oven
  - Mutil-crimping of double-layer micromesh

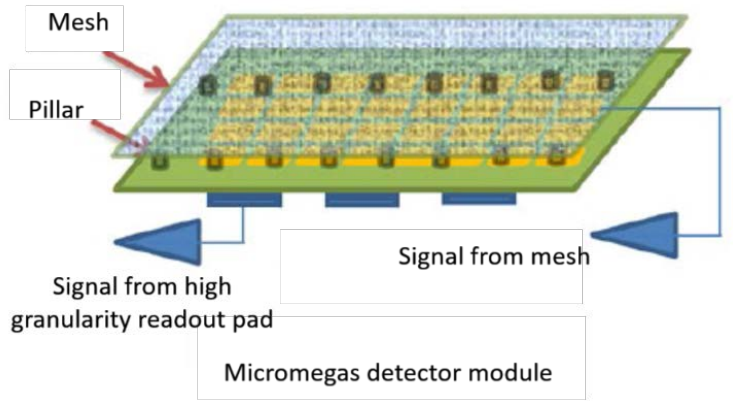
→ Improved detector gain, resolution and overall performance.

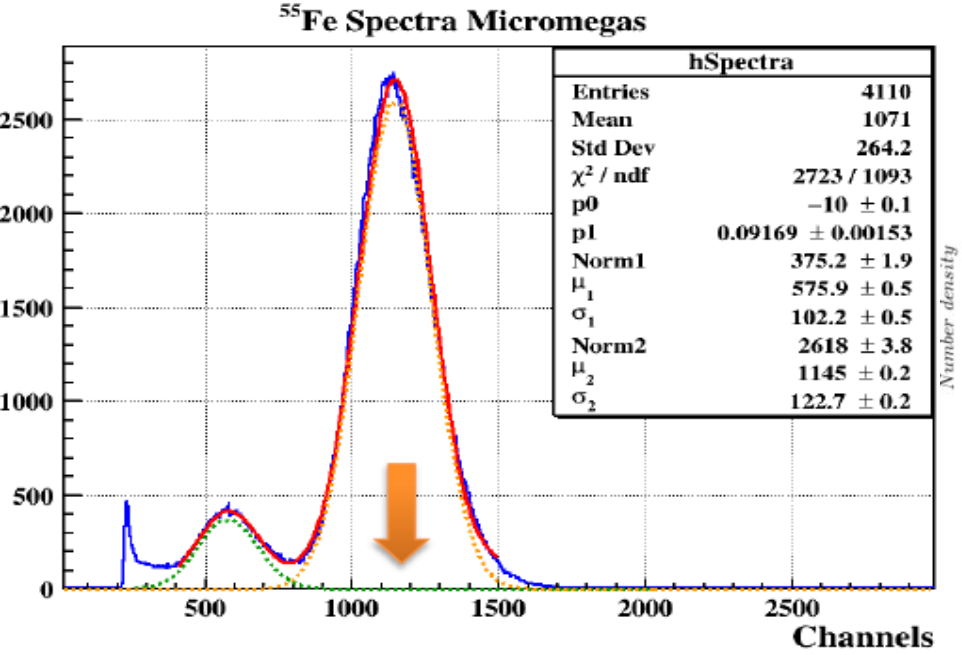




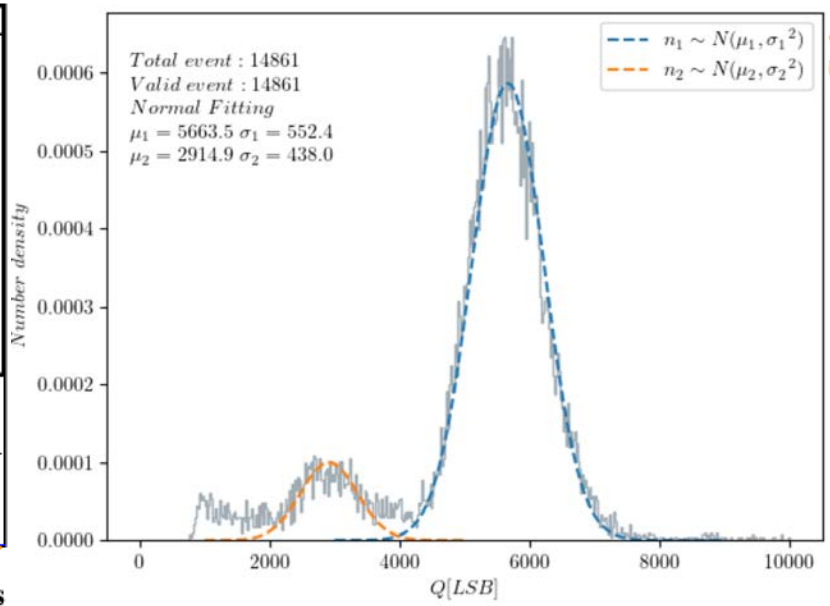
Fe-55 spectrum of TPC module

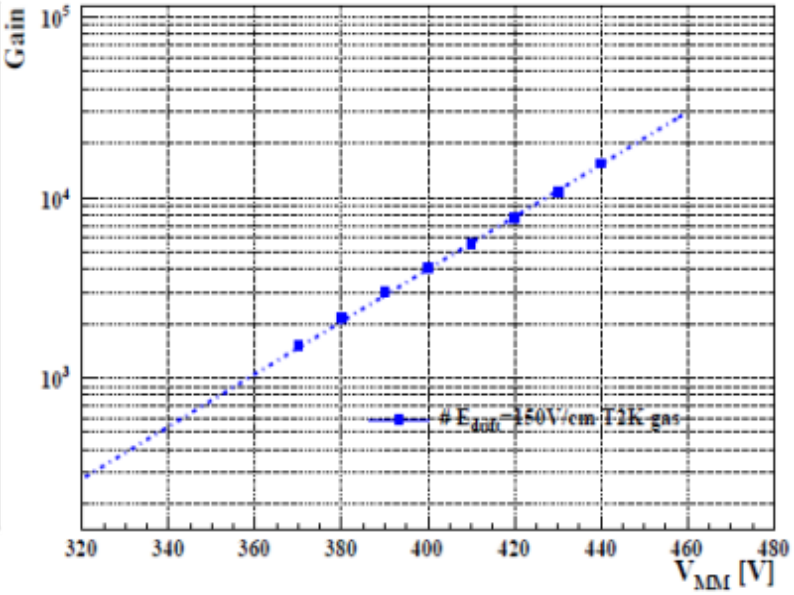
Achievement of TPC module:

- Used Fe-55 source to acquire energy spectrum on mesh; energy spectra obtained through the small pixel readout and the **two results are consistent.**
- Micromegas detector gain measured in T2K gas — good gain linearity achieved





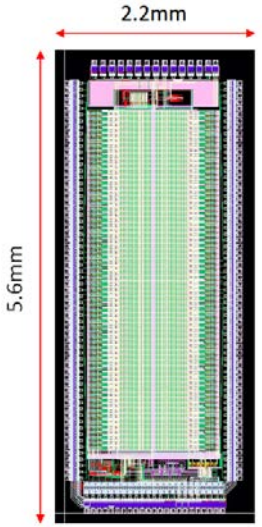




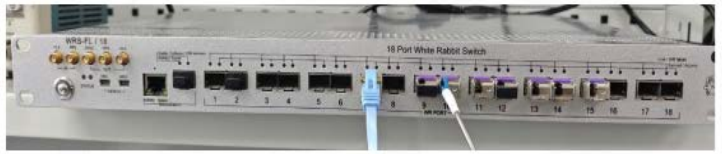
Prototype of the interposer mode readout ASIC: TEPIX v1

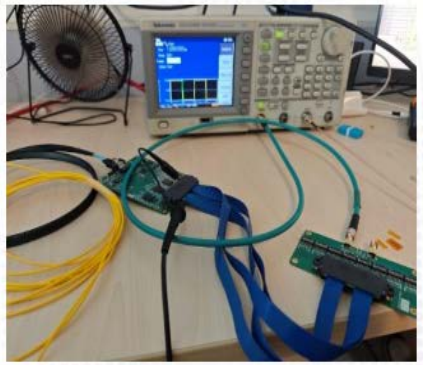
- High granularity readout Electronics: TEPIX v1
  - Charge-sensitive preamplifier
  - Correlated double sampling shaper
  - 4-channel sample/hold circuits and 10 bit ADC
  - 128 channels using 180 nm process
  - Chip size: 2.2 mm × 5.6 mm
- Only 40 chip-in-package devices were tested in two batches; full-readout Micromegas readout has not yet been completed.

In collaboration with Tsinghua University



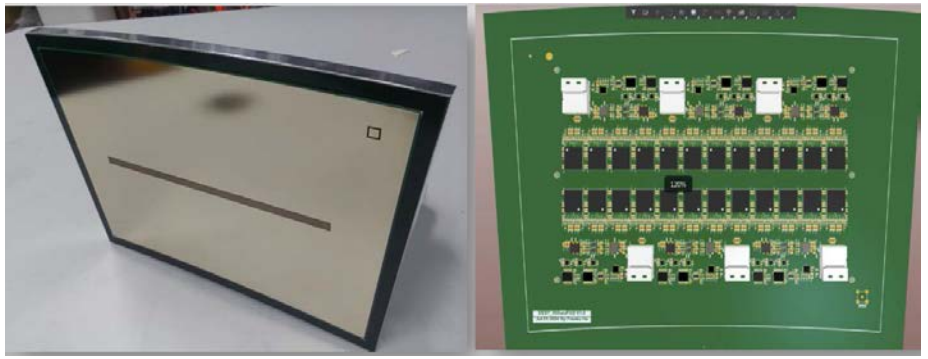
Total number of channels	30 Million per endplate
Pixel size	500 μm × 500 μm
Equivalent Noise Charge (ENC)	100 e^-
Dynamic range	20 fC
Charge buffer dynamic range	8-10 bit
Event rate	12 kHz/cm^2 max. in low-lumi. Z mode
Event size	64 bit
Readout bandwidth	<10 Gbps per module with compression
Power consumption	<100 mW/cm^2

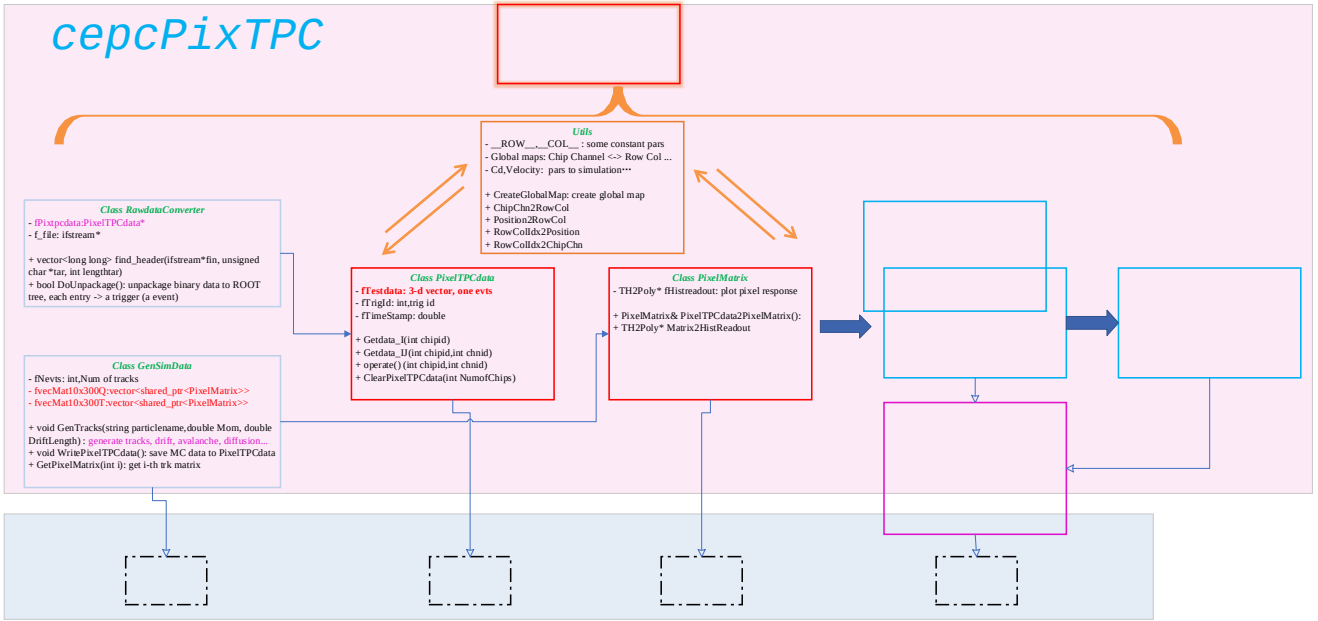


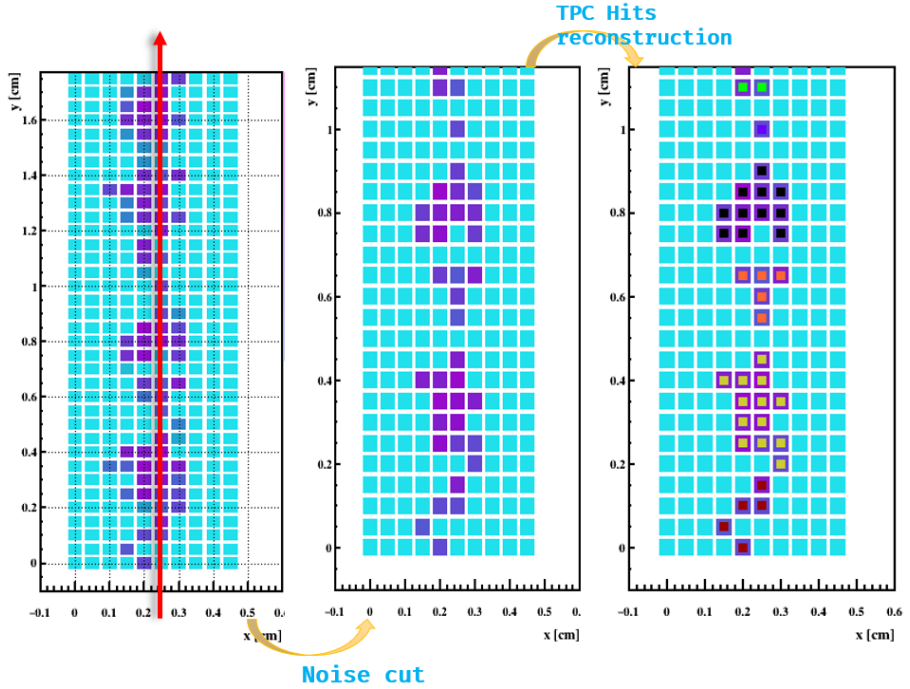


Progress of the simulation integrate TEPIX mode

- Based on Garfield++, KalTest and a pixel-type TPC simulation framework
  - Offline data-processing code developed
  - Time-stamp misalignment across multiple channels
  - Channels time-stamp alignment, raw data to root conversion processing
  - From hits funding, clusters funding to track-reconstruction algorithms completed







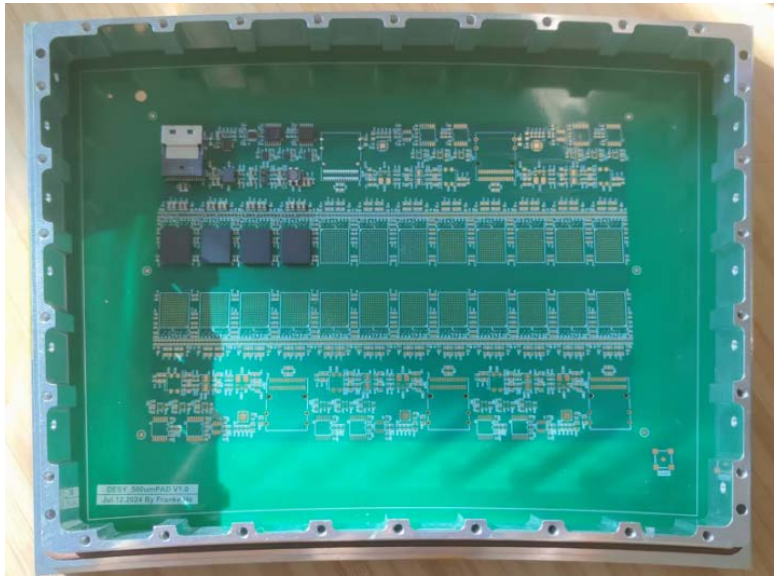
Hit reconstruction process integrated with the high granularity readout

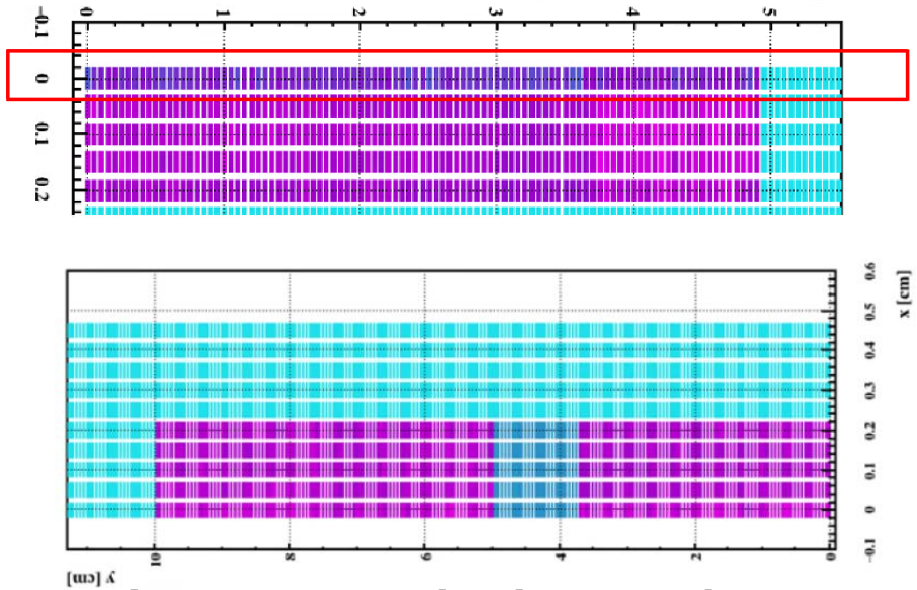
Validation and commissioning of TPC prototype

- R&D on High granularity readout TPC readout using 4 chips integration.
  - ASIC chip developed and has been tested at IHEP.
- Energy/Time value of the channels according to the charged injected
  - Chip-to-chip threshold consistency varies greatly; some channels of the chip operate at excessively low thresholds.
- A TPC readout module has developed with 10×300 readout channels (24 TEPIX v1 chips)

- **Key issues to address and resolve**

  Micromegas detector requires further optimization, and the chip threshold inconsistency issue needs to be resolved, still needs more debugging and time.



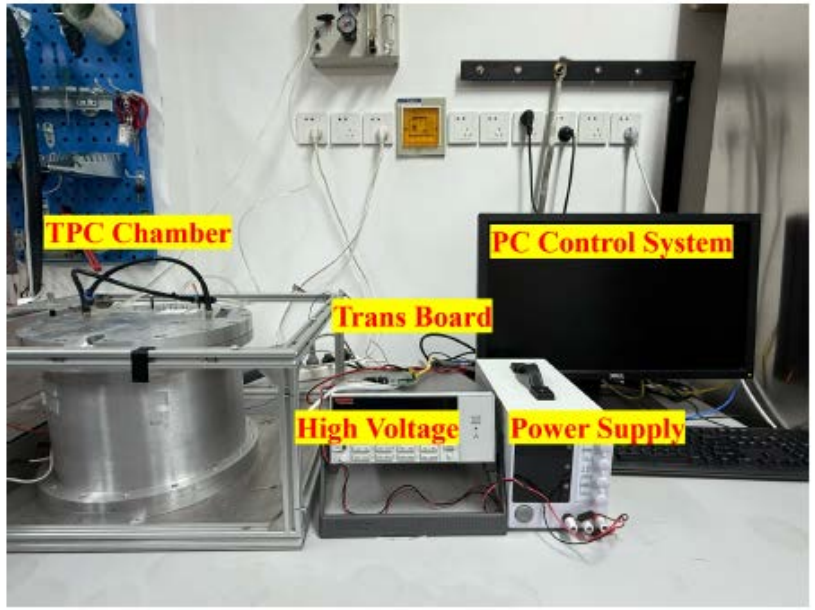


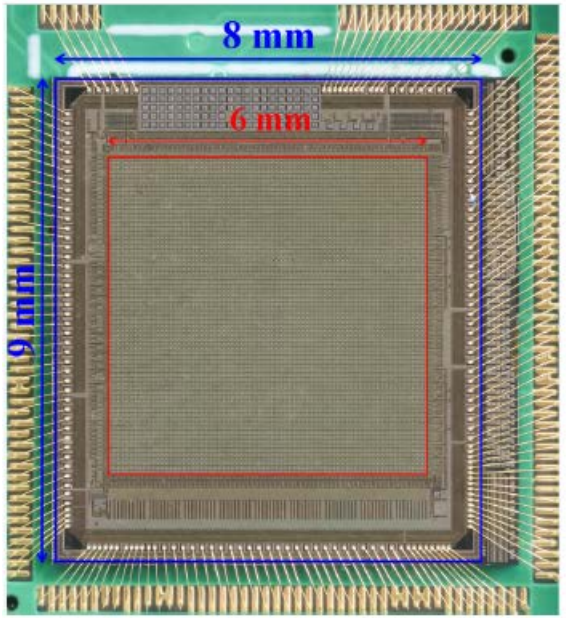
Some test result of Micromegas detector integrated with TEPIX chip

Prototype of the direct readout mode readout ASIC: Topmetal II chips

In collaboration with Central China Normal University

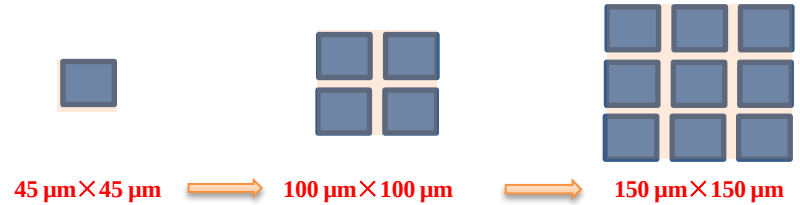
- High granularity readout Electronics: Topmetal L
  - Switched-capacitor readout: 72 × 72 array (high granularity readout size: **45 μm × 45 μm**)
  - The analog output of the Topmetal L sensor is read out through a row/column time-multiplexed switching network to a single on-chip output buffer.
  - Time per pixel is 128 ns which corresponds to a full-frame readout time of 0.6 ms

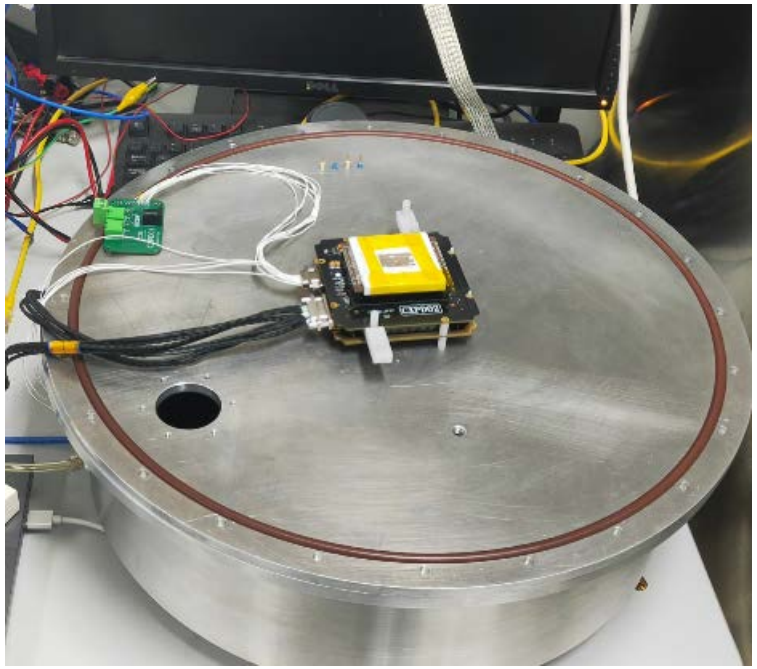


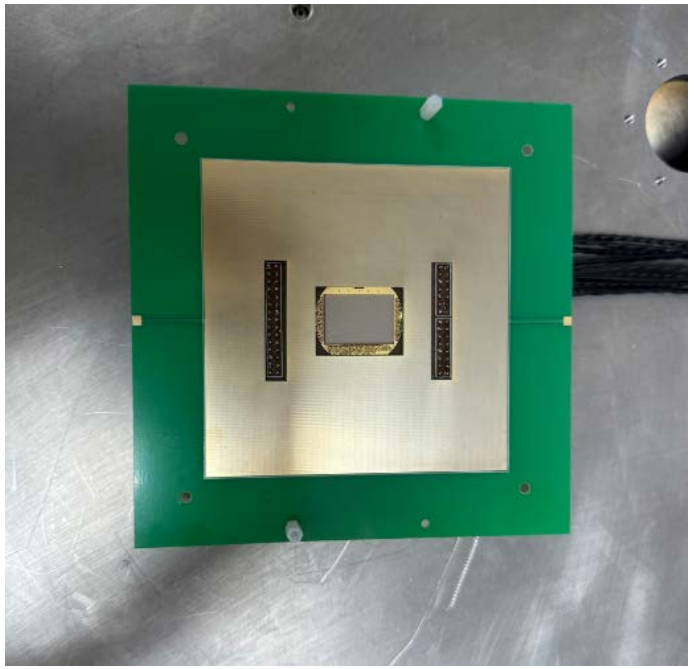


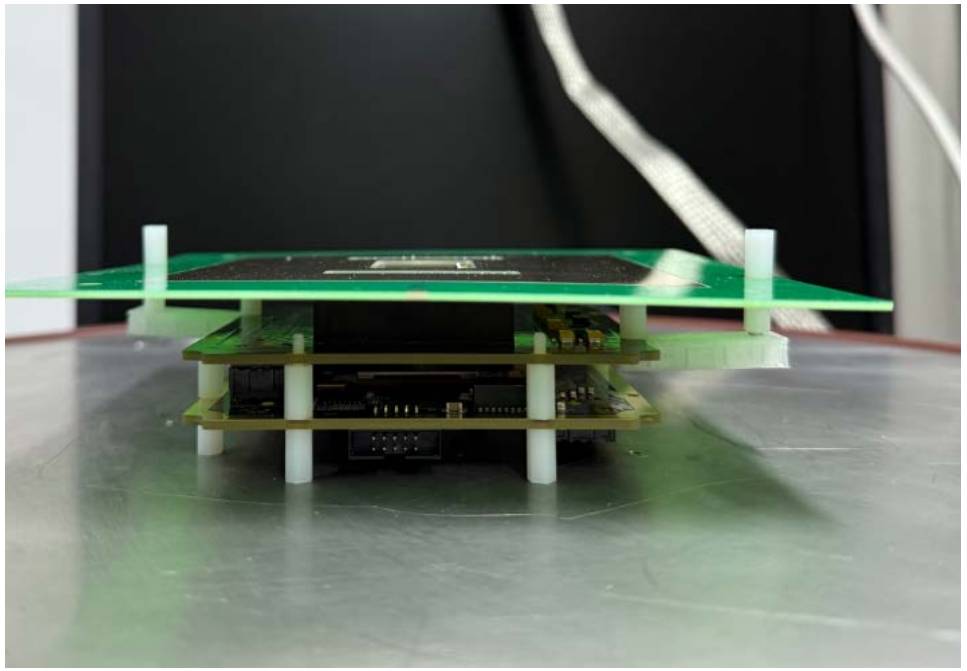
Prototype of the direct readout mode readout ASIC: Topmetal II chips

- High granularity readout Electronics: Topmetal L
  - Switched-capacitor readout module: 356×512 (**45 μm × 45 μm**)
  - Using read-out data to simulate and optimize single-pixel, 2×2, 3×3, 4×4, … pixels — mimic study of different pixel sizes.
  - **First step**: GEMs as the amplification device



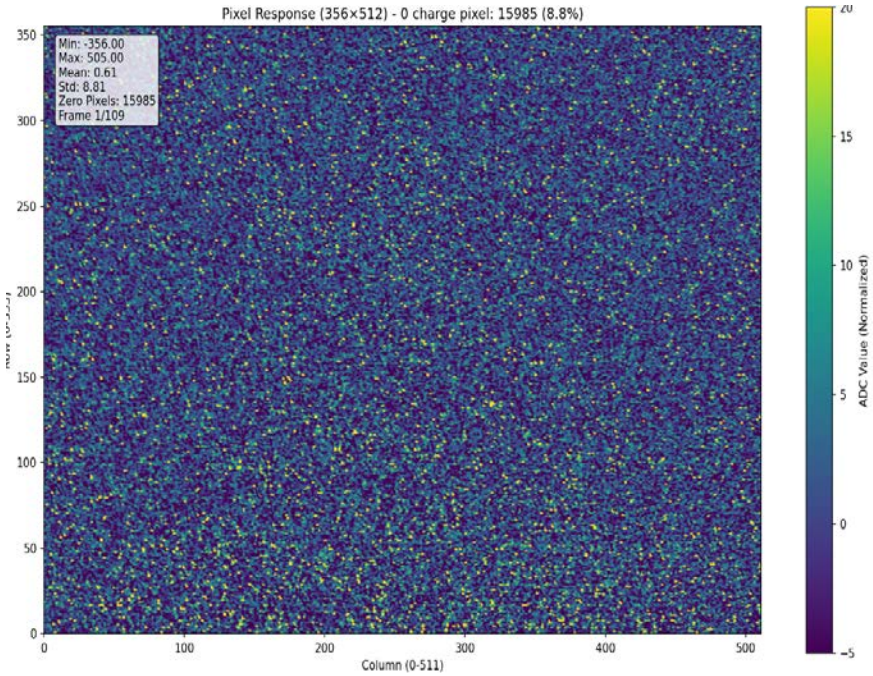


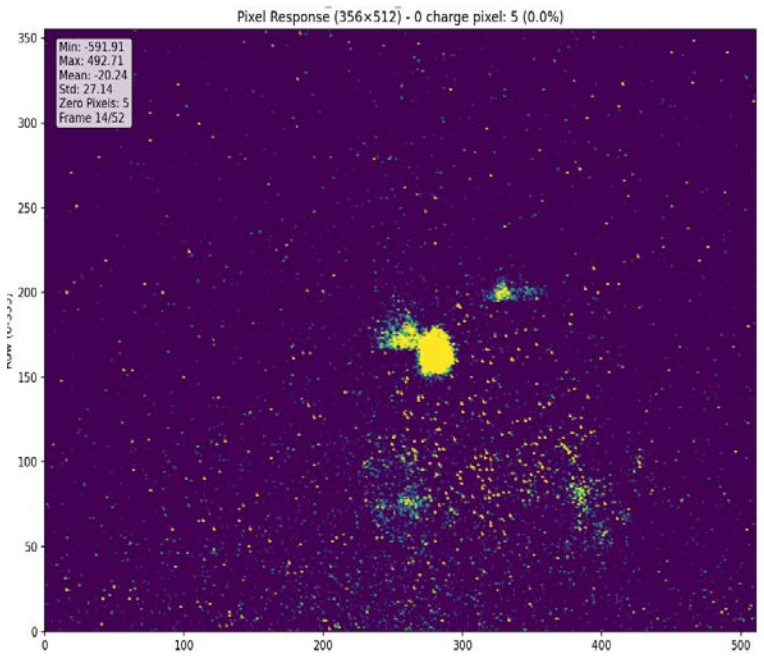


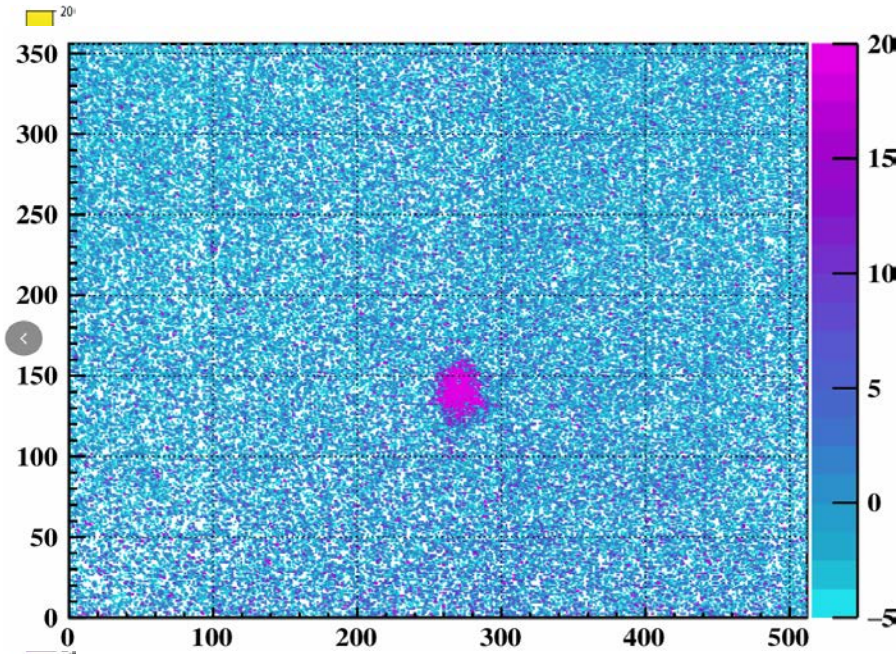


Prototype of the direct readout mode readout ASIC: Topmetal II chips

- High granularity readout Electronics: Topmetal L
  - 2 mm aluminium collimator
  - 1 mCi Fe-55 source
  - GEM detector for amplification were used
  - **Next steps**, a Micromegas detector is being fabricated and will be tested with Bi-207 tracks.







- **TPC prototype R&D**

Plans of TPC R&D

- Prototyping R&D and validation with the test beam
  - mechanics, manufacturing, beam test, full drift length prototype
- Development of the full drift length prototype
  - Drift velocity. Attachment coefficient, T/L Diffusion, etc.
- R&D of Ion Backflow using Grapheme
  - **In collaboration with Shandong University** (580LPI mesh)
- Development of TPC prototype and beam test
  - Collaboration with LCTPC and DRD1 group
  - First half-year: TEPIX v1 chip validation completed; beam-test application submitted for second half-year upon success.

Milestones achieved	Short term	Long term
Ion backflow suppression	IBF×Gain<1 (Gain=2000)	Graphene technology
High granularity readout readout prototype	Validation with beam test	Prototype with Multi-modules
Power consumption ASIC	~100mW/cm^2 (60nm ASIC)	Optimization readout size
PID resolution	3% (dN/dx)	<3% (dN/dx)
Material budget (barrel)	Carbon Fiber	Full size prototype

Summary

- High granularity readout TPC is choose as the baseline detector as main track in CEPC TDR. The simulation framework has been developed using Garfied++ and Geant4.
- The TEPIX chip v1 based on the Interposer readout has been developed. Some chips have undergone joint debugging with the Micromegas detector, though consistency in noise and threshold still requires further resolution.
- Experiments using the Topmetal L chip with pixel-by-pixel readout have been conducted. The chip has undergone joint calibration with the GEM detector, yielding well-calibrated information from the Fe-55 radiation source.
- Further commission and optimization are required to validate the technical application of high-granularity readout for future circular colliders. **Funding and recourse are also urgently needed.**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Many thanks!