

面向LHCb升级和未来希格斯工厂的 CMOS径迹探测器研发

中国科学院高能物理研究所
李一鸣

中国物理学会高能物理分会学术年会
2026年7月15日，广州

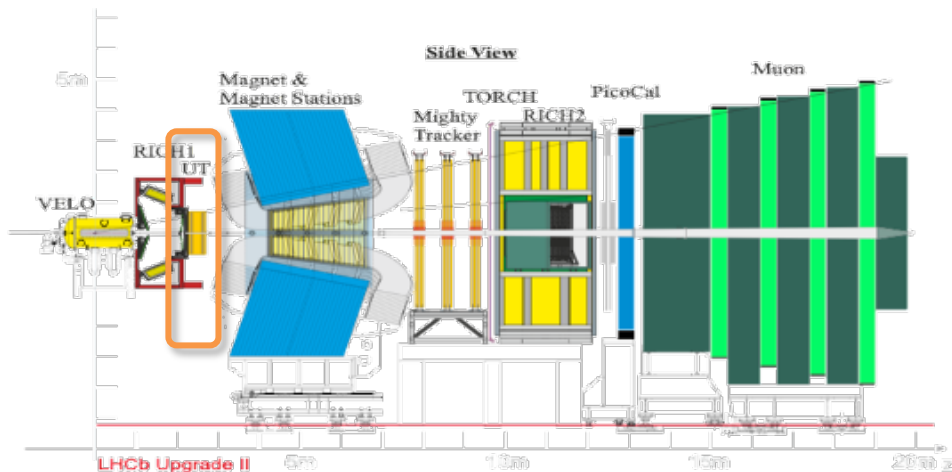
内容提要

- 未来径迹探测器需求
 - 以 LHCb 和 CEPC 为例
 - 硅像素探测器技术选择
- 基于HV-CMOS的研发：COFFEE系列
 - COFFEE3设计和测试结果
 - 工艺局限和改进计划
- 基于COFFEE芯片的径迹探测器系统
 - LHCb UP进展
 - CEPC 内径迹探测器
 - 轻质化集成探索：串行供电
- 总结

未来对撞机实验需要怎样的径迹探测器？

▪ 强子对撞机：LHCb升级

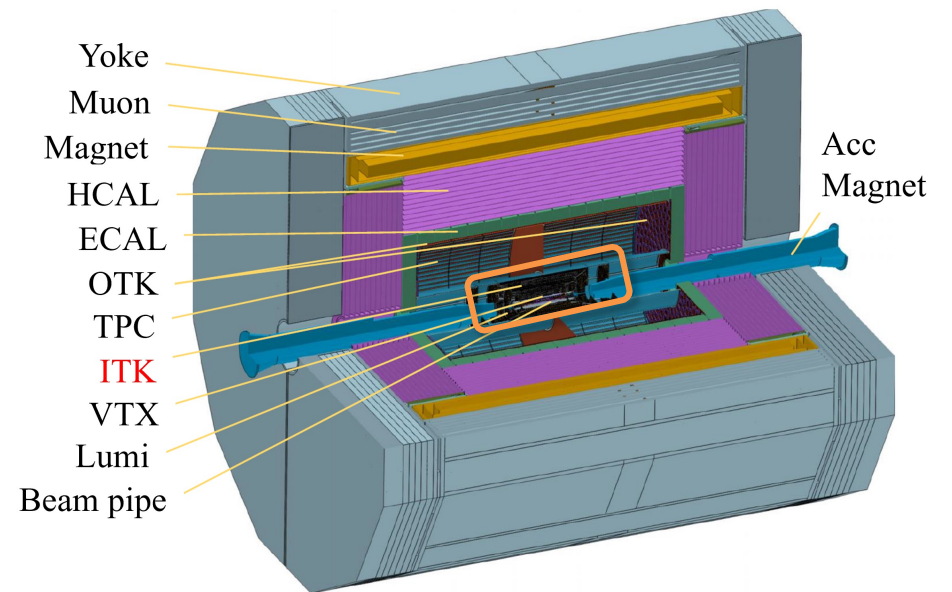
- 高位置分辨率 → 像素 < 100 μm
- 高时间分辨率 → 可区分 25 ns 束团
- 良好抗辐照 → $3 \times 10^{15} \text{ n}_{\text{eq}}/\text{cm}^2$
- 高事例率 → $\sim 100 \text{ MHz}/\text{cm}^2$
- 大面积 → $\sim 7 \text{ m}^2$



LHCb Upgrade II @ $1.0 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$
Installation expected 2034-2035

▪ 正负电子对撞机：

- 高位置分辨率 < 10 μm
- 高时间分辨率 → 可区分 23 ns 束团
- 低质量、低功耗
- 大面积 → $\sim 20 \text{ m}^2$

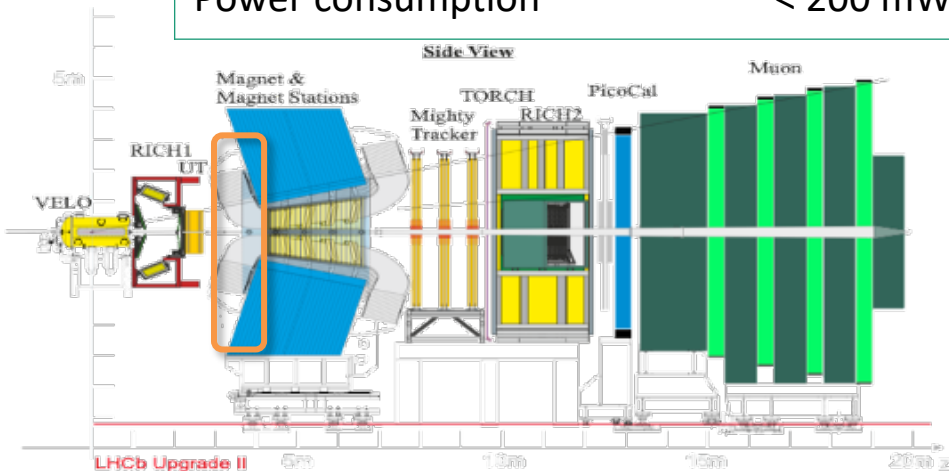


AGORA Detector concept for CEPC / FCCee

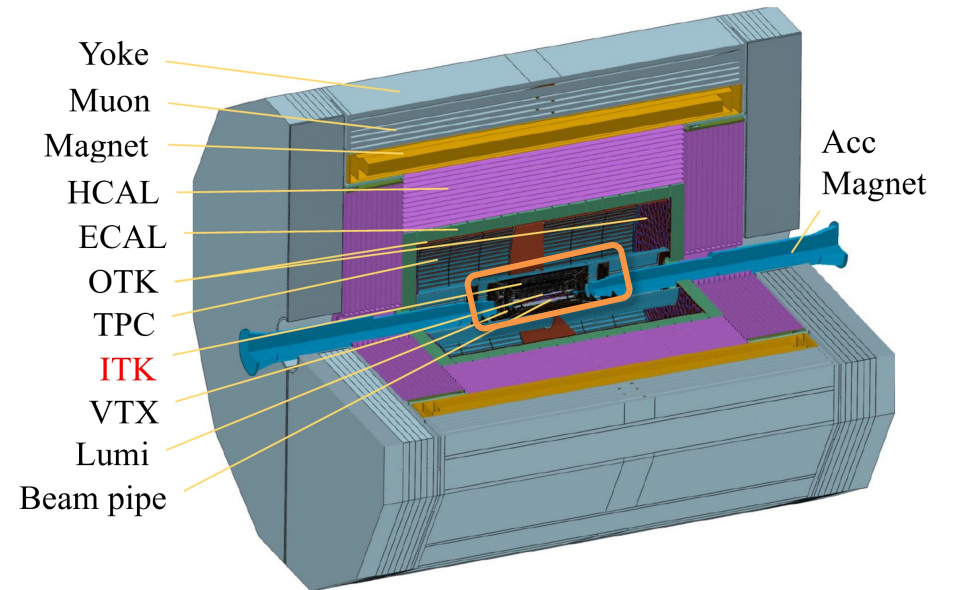
未来对撞机实验需要怎样的径迹探测器？

Key parameter	Requirement
Sensor size	2 cm x 2 cm
Spatial resolution	< 10 μm
Time resolution	3~5 ns
NIEL	$3 \times 10^{15} \text{ n}_{\text{eq}}/\text{cm}^2$
Max hit rate	100 MHz/cm ²
Power consumption	< 200 mW/cm ²

硅像素探测器有望满足要求



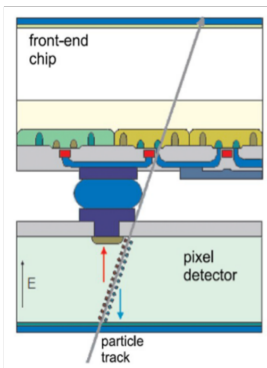
LHCb Upgrade II @ $1.0 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$



AGORA Detector concept for CEPC / FCCee

半导体径迹探测器技术路线

复合型 (Hybrid)

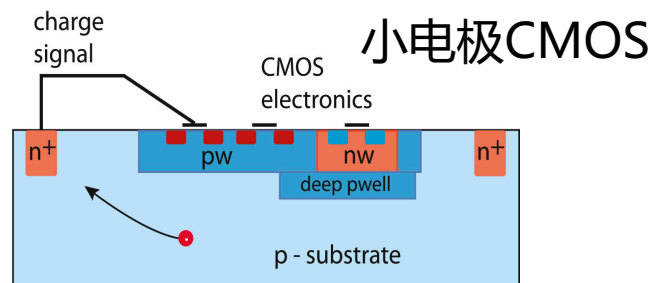


- 传感器与ASIC分别设计制造，需倒装焊连接
- 像素到几十微米后难再降低
- 可集成复杂功能，功耗高

已应用于： DELPHI Silicon Tracker
LHCb VELO,

计划应用： ATLAS ITK Pixel,
CMS Inner Tracker

单片型 (Monolithic / MAPS)

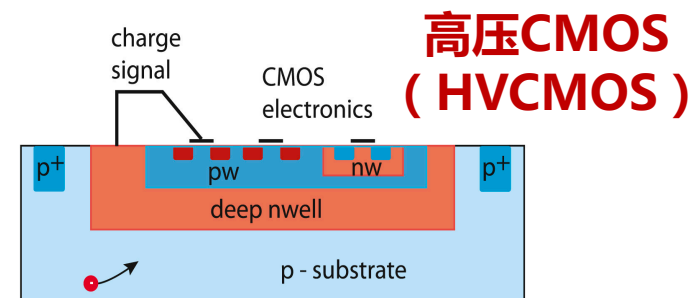


- 像素小、空间分辨好
- 噪声低
- 耗尽区小，电荷收集较慢
- 抗辐照性能需通过工艺修改提高

STAR, ALICE ITS + MFT
ALICE ITS3
CEPC AGORA VTX*

*CEPC Ref-Det TDR, arXiv:2510.05260

基于CMOS技术，集成传感器和前端读出



- 空间分辨好
- 易实现全耗尽，电荷收集快
- 天然具有良好抗辐照性能
- 基于商业半导体加工过程

LHCb Upstream Pixel Tracker
LHCb Mighty Tracker Pixel
CEPC/FCC AGORA ITK*
CEPC/FCC IDEA Silicon Wrapper

COFFEE Timeline

基于国产 55 nm HVCMOS 先进制程



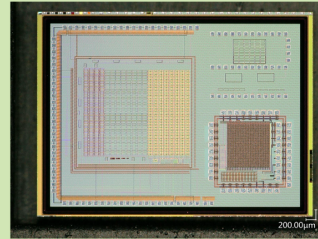
CMOS SENSOR IN
FIFTY-FIVE NM PROCESS

NIM A1069 (2024) 169905
JINST 20 (2025) C10011

COFFEE 2

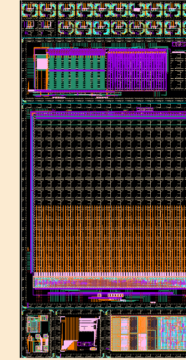
First HVCMOS 55nm
prototype chip

- Breakdown at -70V
- Responsive to laser, X-/beta-ray sources

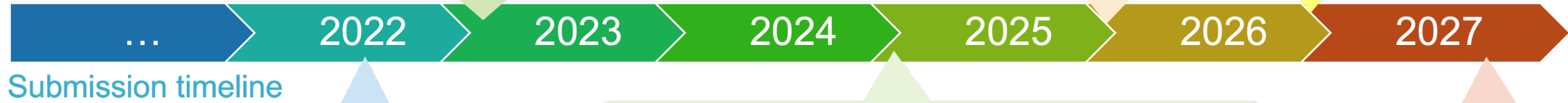


CHiR (COFFEE-HiRes)

- Validation of process modification
- Key design feature

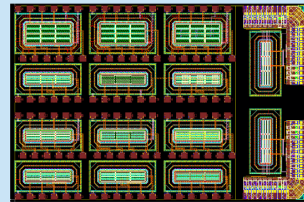


Quarter-size
chip submission



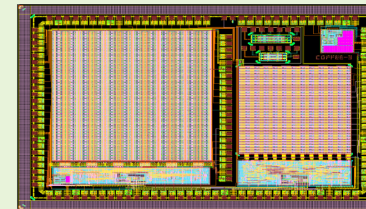
COFFEE1

- Prototype in LL process
- Validation of deep N-well structure

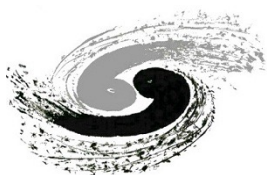


COFFEE3

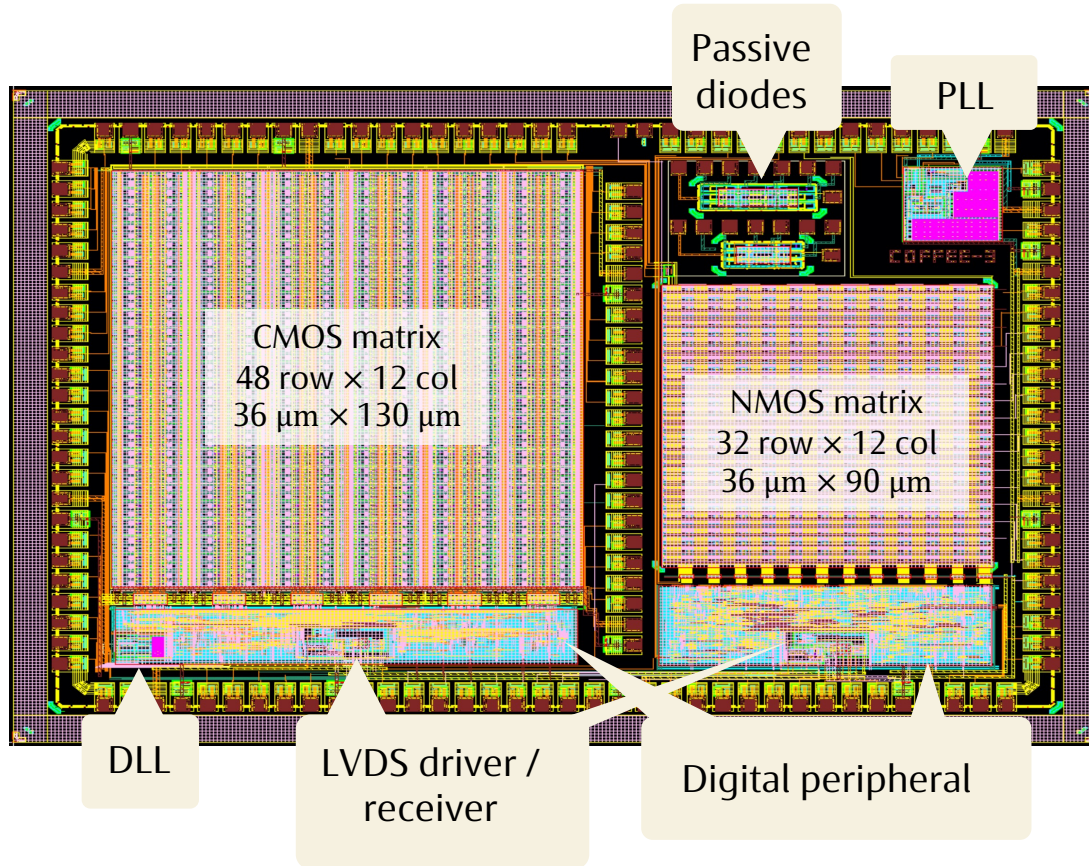
- Two pixel arrays with data-driven readout
- Designed for good timing resolution and moderate power consumption



Large
prototype
planned
~end 2027

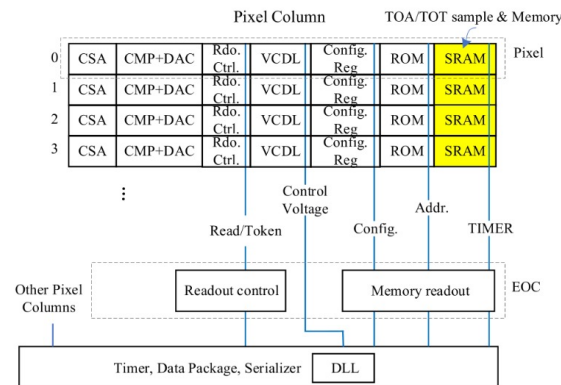


COFFEE3

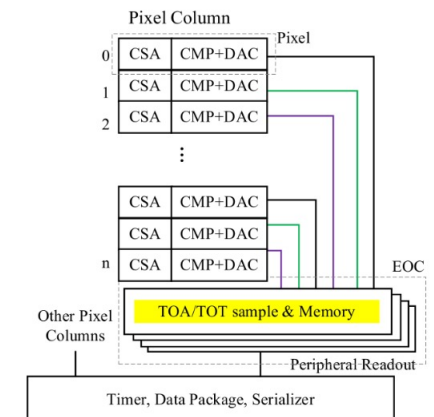


JINST 21 (2026) C04075

- Prototype in 55nm HVCMOS process with two readout architectures for fast timing
 - 4 mm x 3 mm
 - 'CMOS matrix' : digital TDC in pixel
 - 'NMOS matrix' : limited design flexibility yet no crosstalk using 3-well process
 - Passive diodes for sensor study
 - IP validations: PLL, DLL, LVDS driver/receivers ...

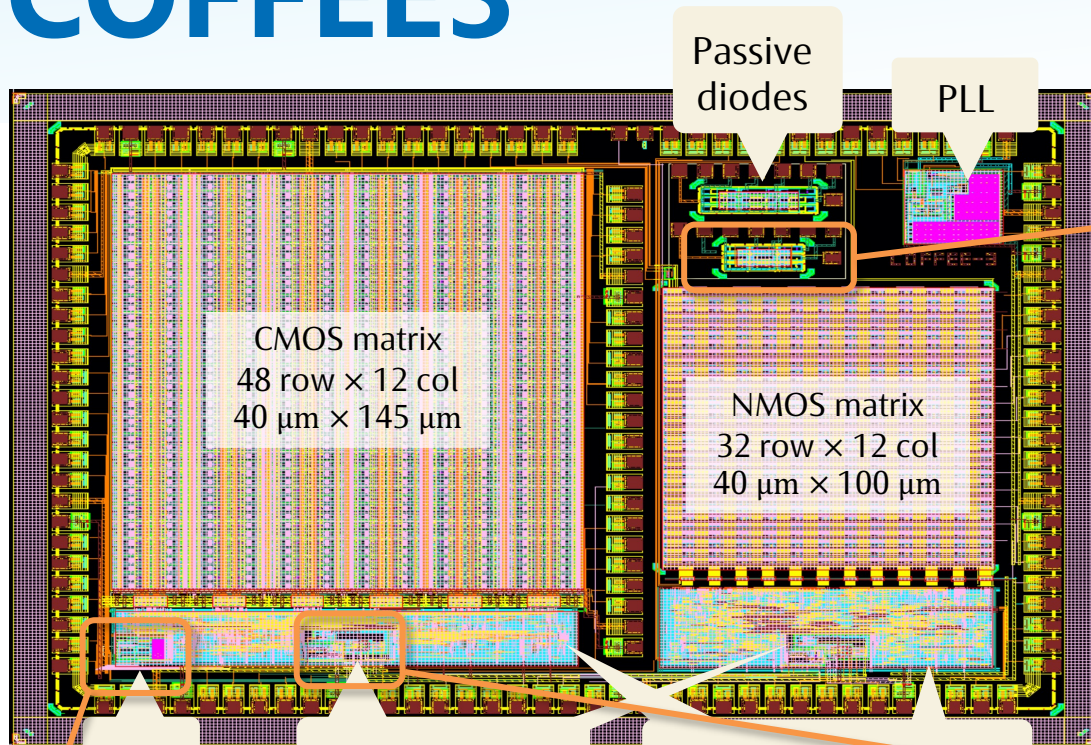


CMOS in-pixel circuitry

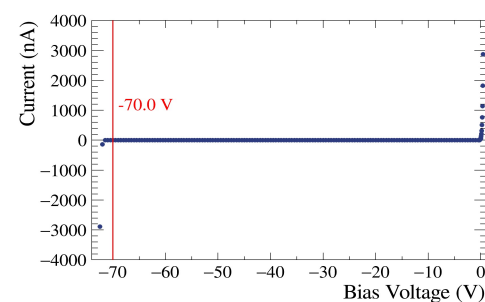


NMOS-only in-pixel circuitry

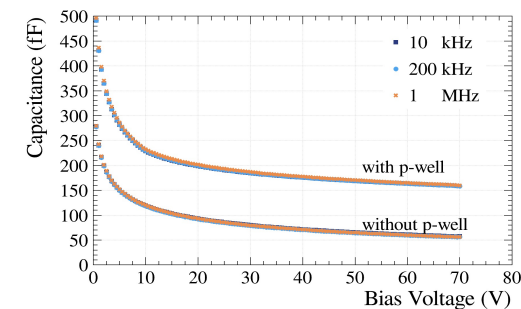
COFFEE3



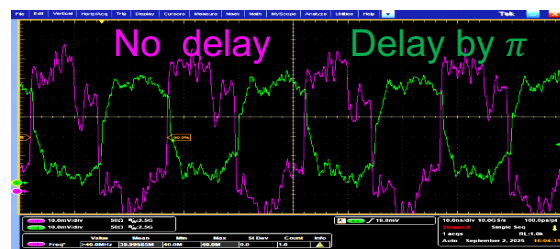
Passive diodes



IV:
breakdown at -70V, expected for low-res (10 $\Omega\cdot\text{cm}$) wafer

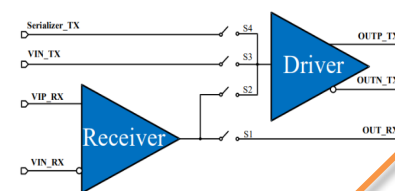


CV:
- Single pixel C $\sim$ 50fF at -70V
- Higher with circuits (+ p-well)



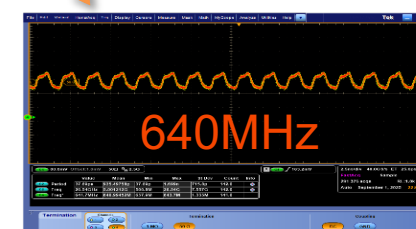
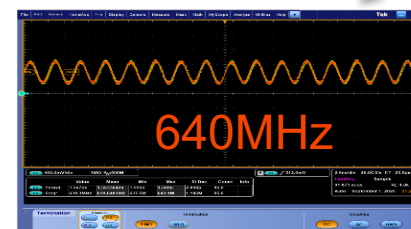
DLL

Input clock (320 MHz) successfully delayed by 6 phases to achieve finer timing



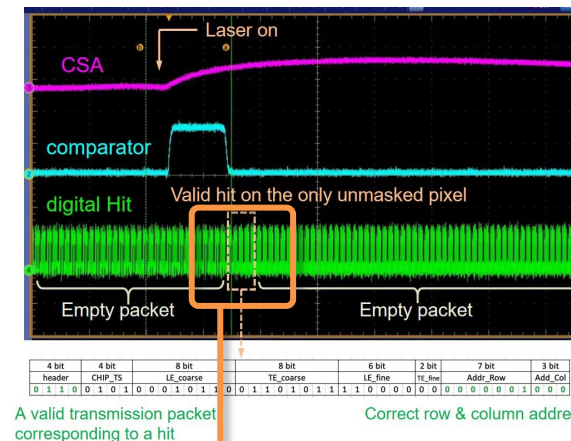
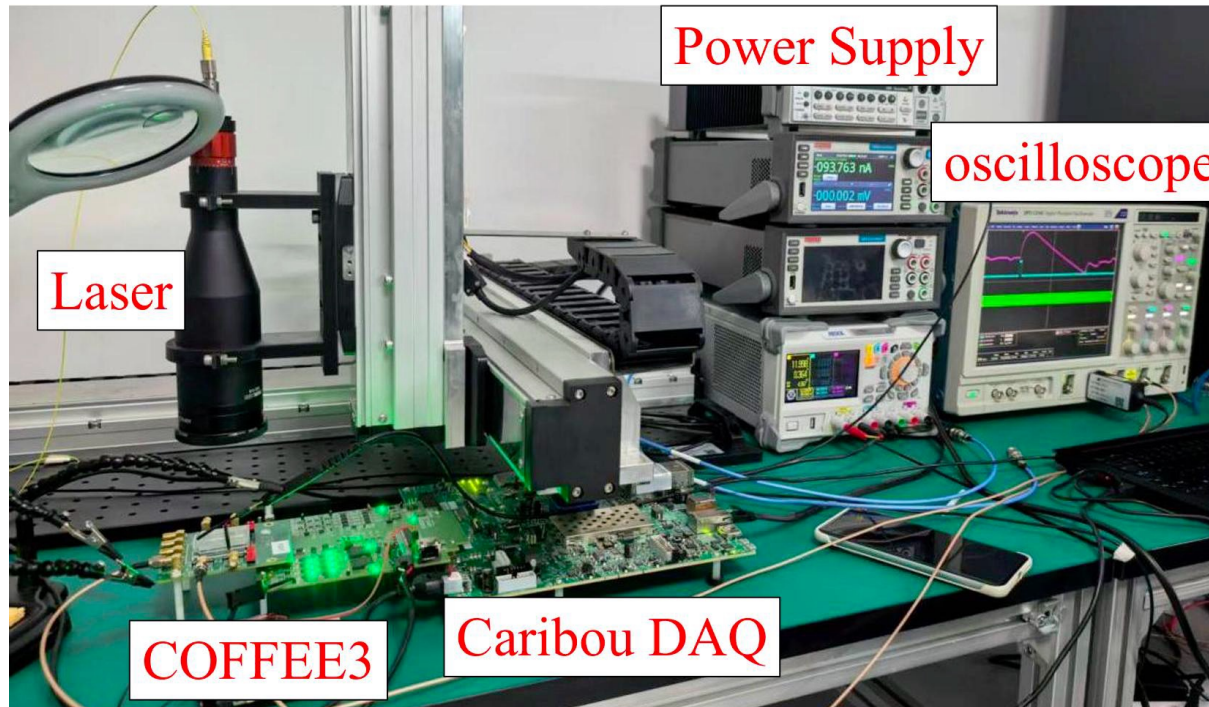
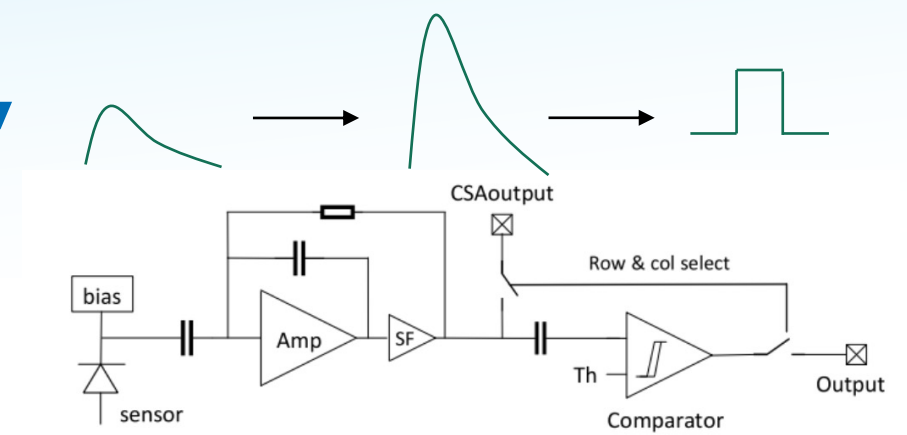
LVDS

Both driver & receivers function well with 640 MHz clock



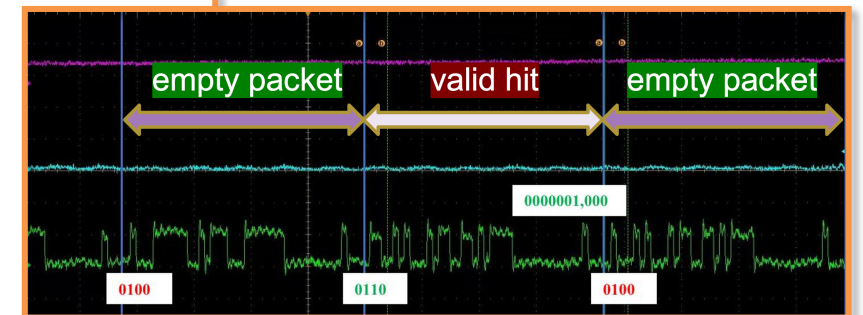
COFFEE3 'CMOS array'

- Readout chain of a single pixel successfully demonstrated using laser



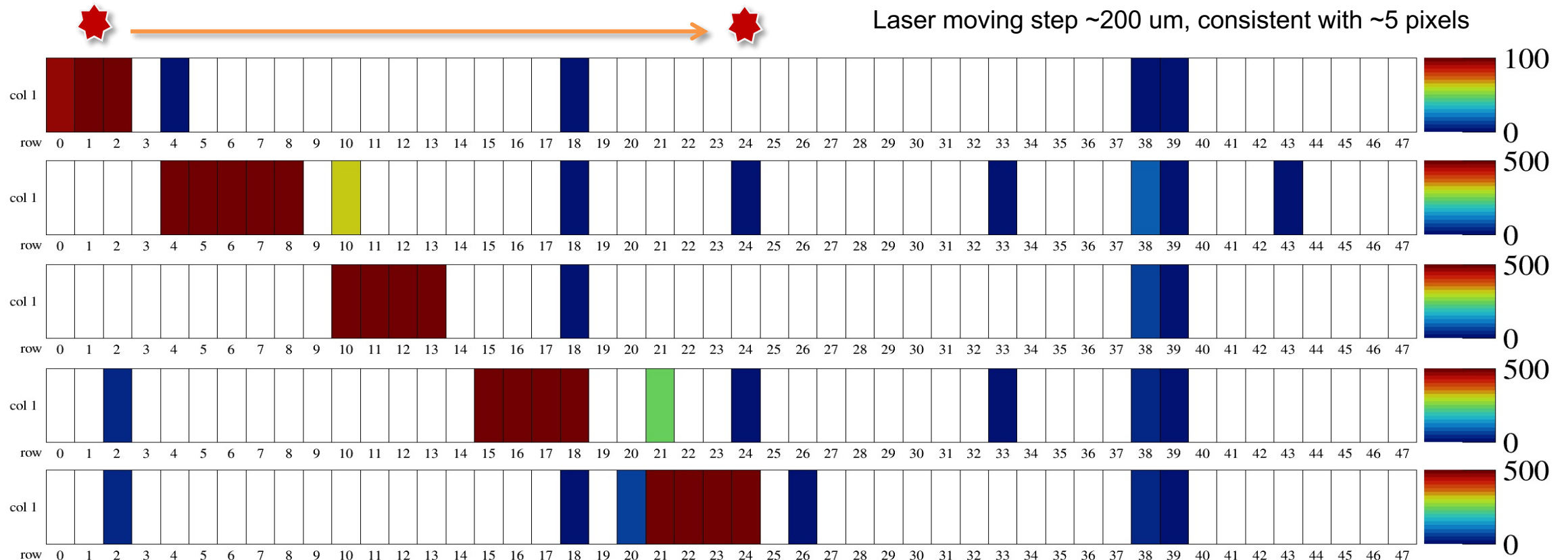
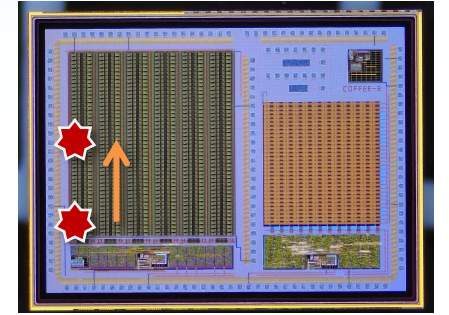
Amplifier & comparator output of a test pixel available

42-bit data packets for all hits



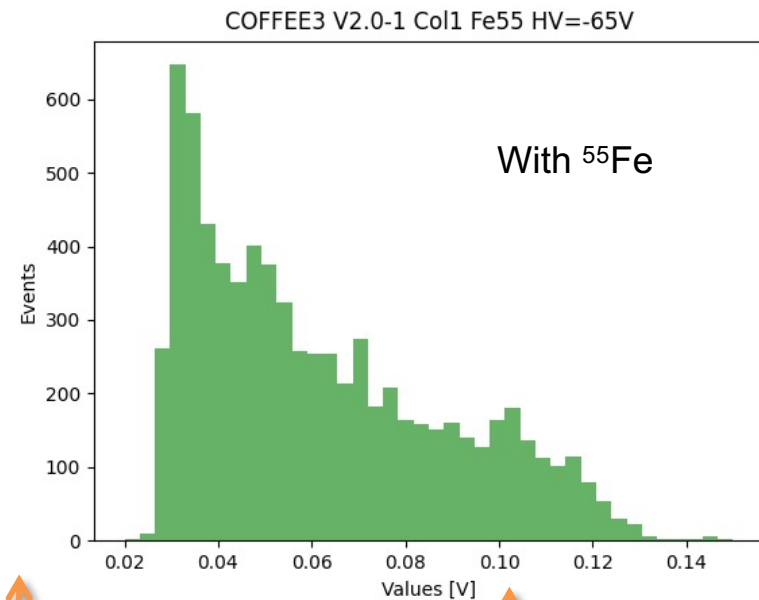
COFFEE3 'CMOS array'

- Readout of a **full column** successful
- Clear response to a laser spot moving along the column



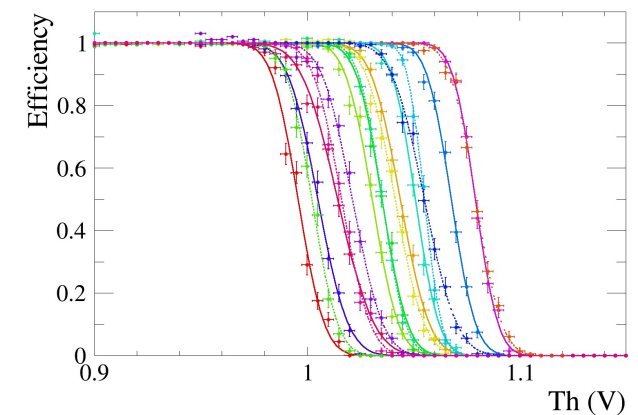
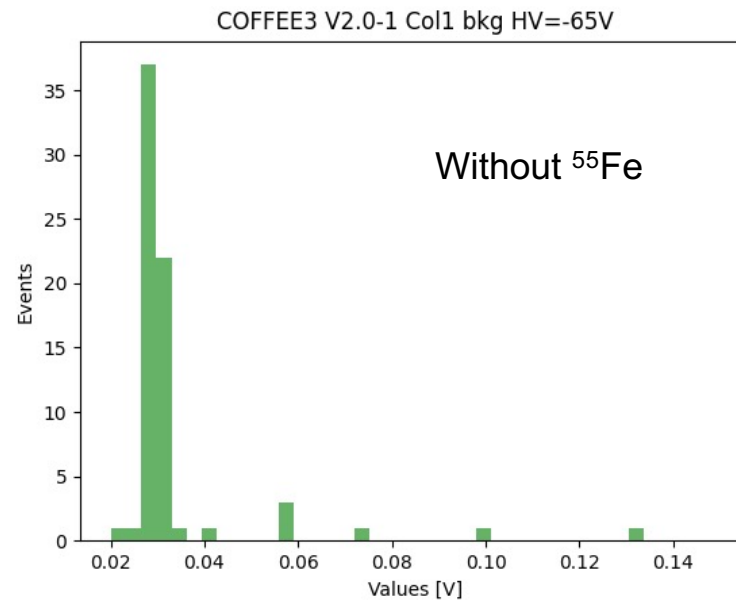
^{55}Fe test

- Single pixel response to ^{55}Fe sources observed
 - Pedestal position determined by Oscilloscope trigger; could improve with full DAQ
- Noise is large
 - Combined with S-curve with laser: noise $\sim 200e^-$
 - Consistent with low-resistivity wafer (and shallow depletion)



Expected pedestal

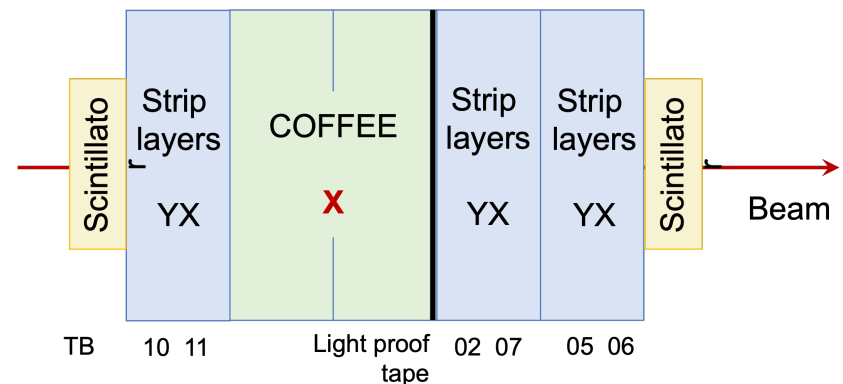
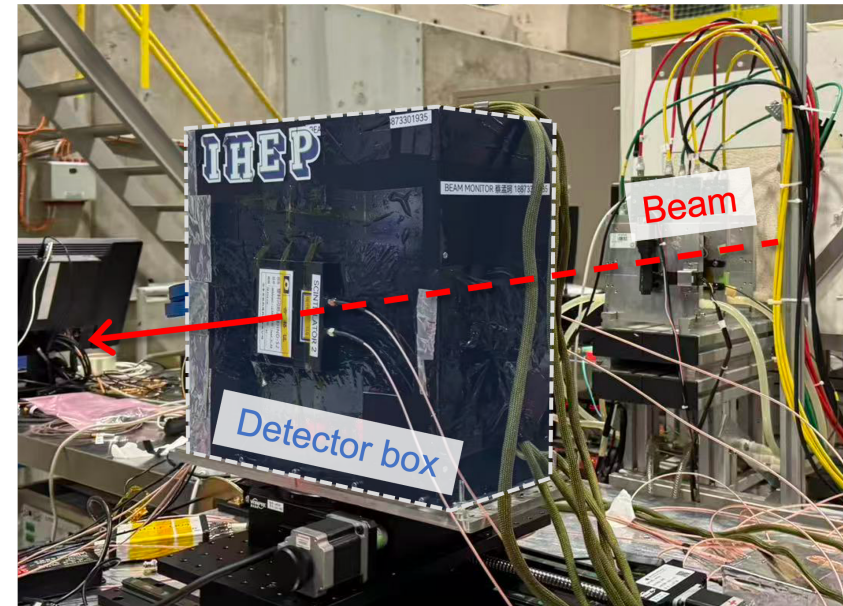
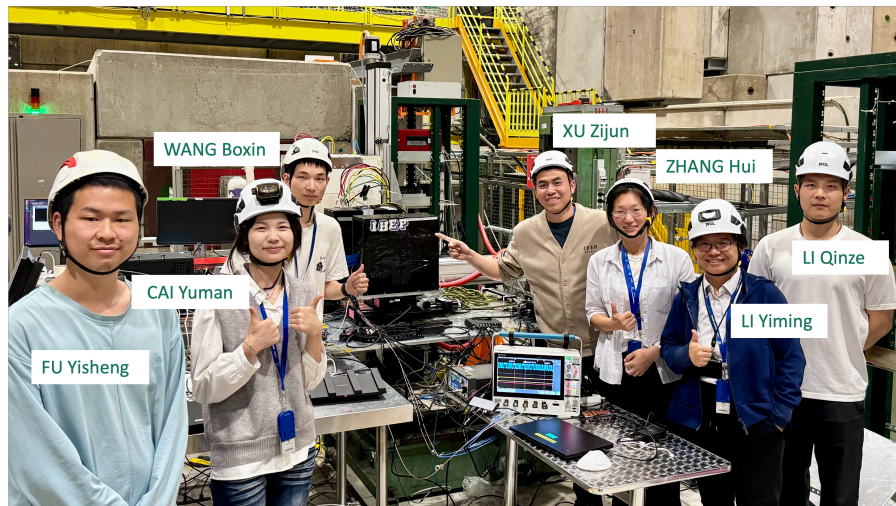
K alpha



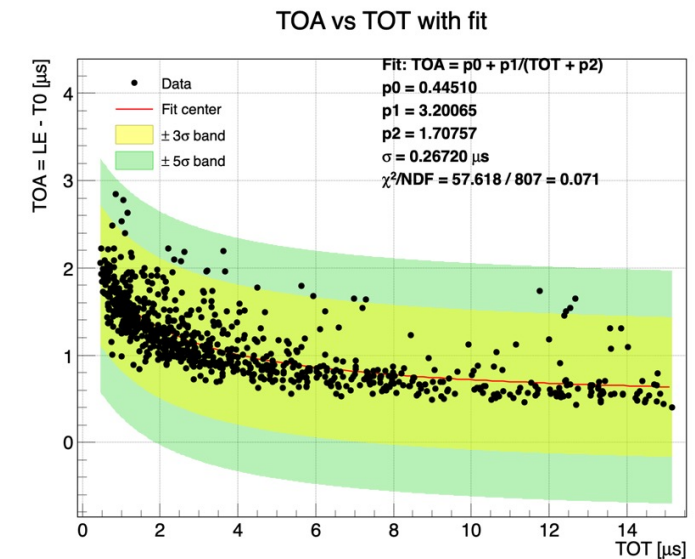
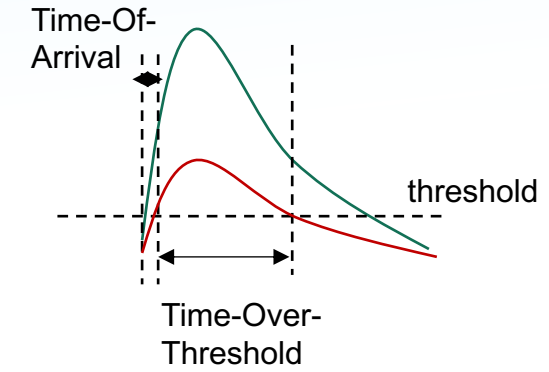
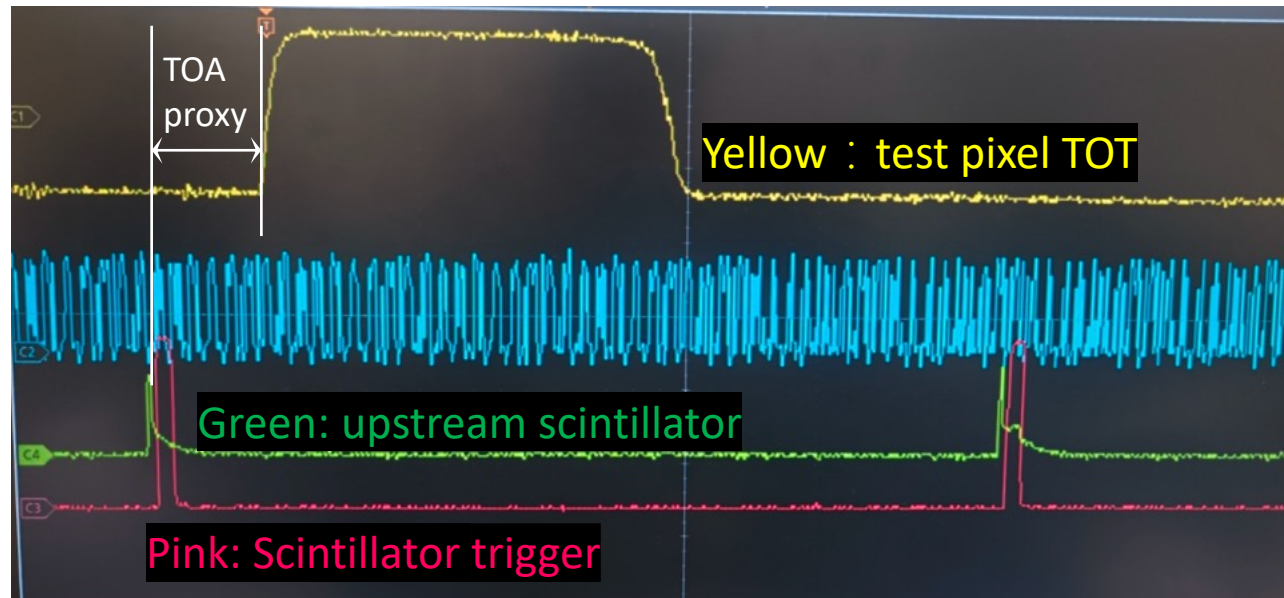
S-curve with laser for one design variation: $\sigma \sim 10\text{mV}$

COFFEE testbeams – first results

- Two beamtest campaigns @ CERN SPS using hadron beams ~120GeV
 - May 2026 with DRD3
 - Jul 2026 with LHCb (finishing today!)
- Setup:
 - COFFEE3 chip with scintillator up-/downstream
 - In May a tracking telescope with silicon strips available

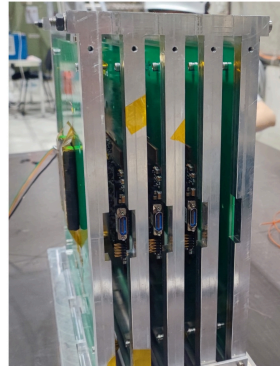
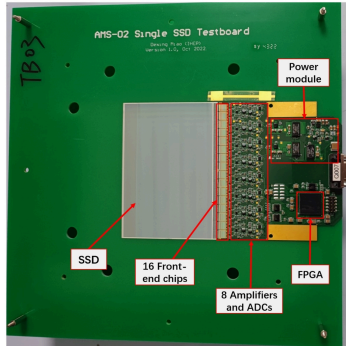


COFFEE sees hits!

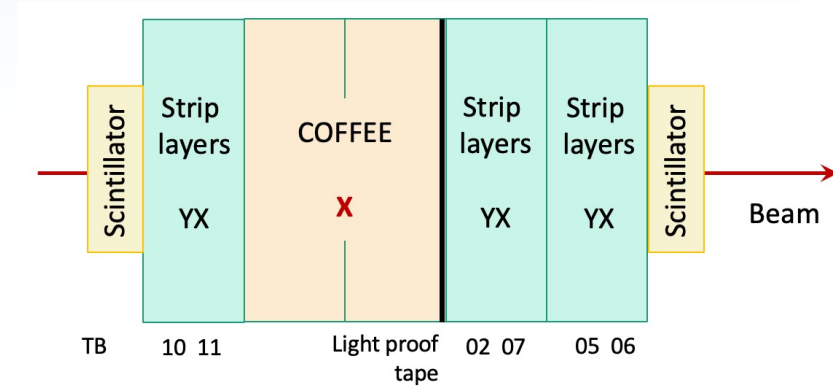


Timewalk effect clearly visible

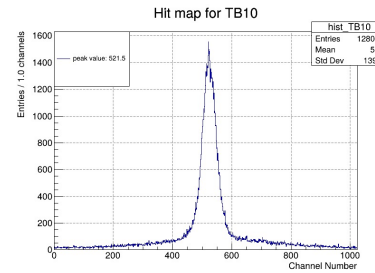
COFFEE sees tracks



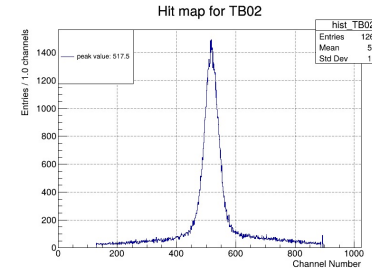
Silicon Strip
telescope
109um pitch



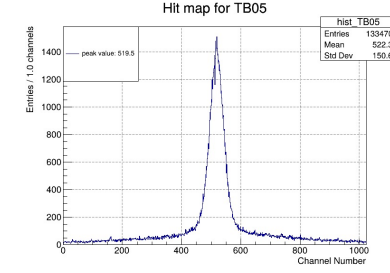
Beam profile:



peak 521.5

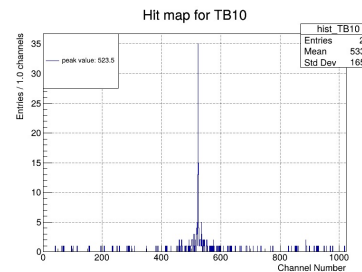


517.5

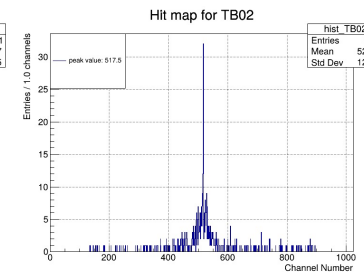


519.5

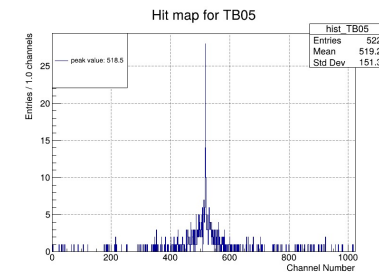
Tracks passing
COFFEE3:



peak 523.5



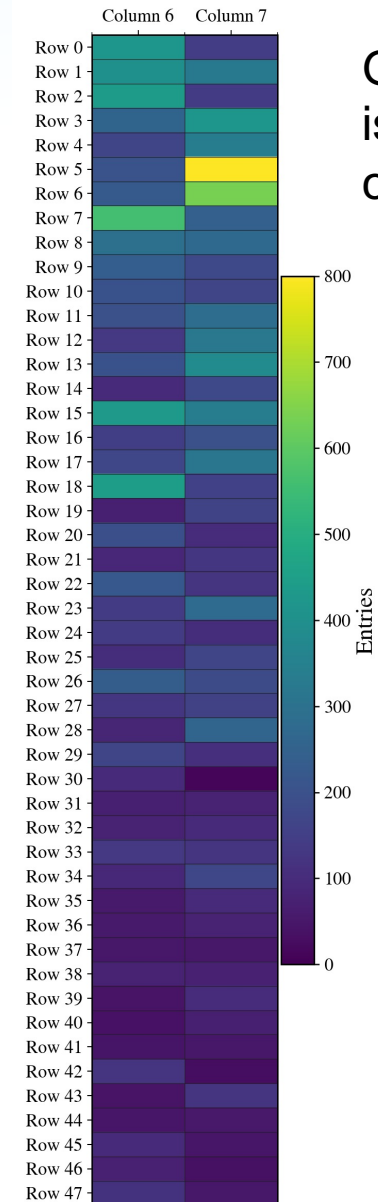
517.5



518.5

COFFEE readout working

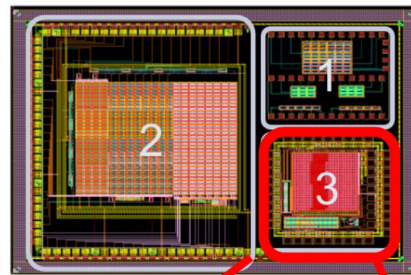
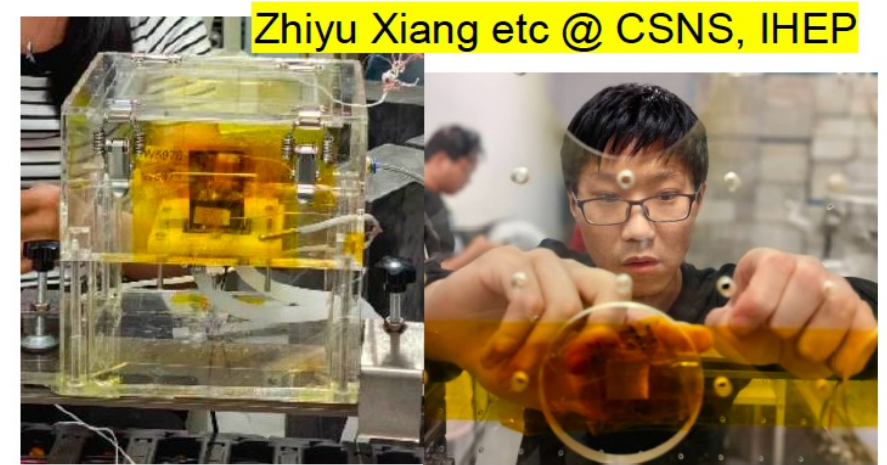
- All pixels in CMOS-matrix turned on and responsive to the beam
 - The pixel map can be equalized by adjusting 4-bit TDAC – work in progress
- Results shown here are fresh and just to give a flavour – more analysis to follow



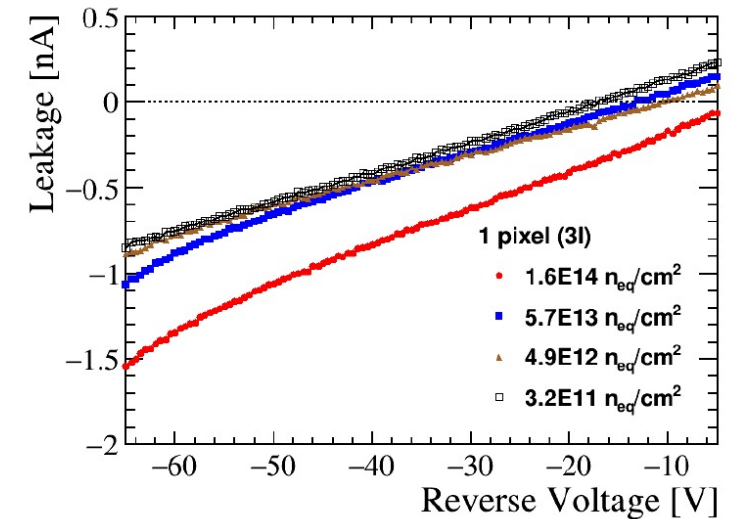
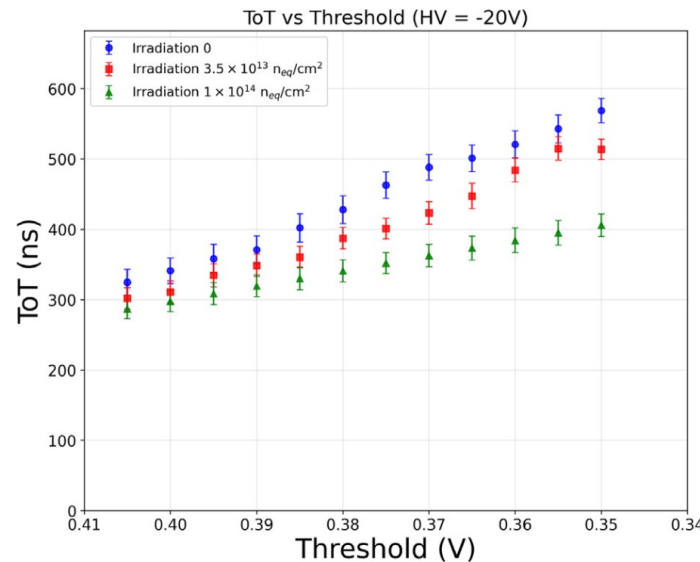
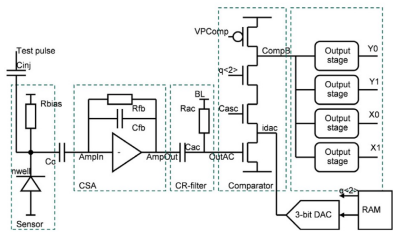
Guess where
is the beam
centre 😊

First study on radiation hardness

- COFFEE2 samples were irradiated at CSNS up to $1.6 \times 10^{14} \text{ n}_{\text{eq}}/\text{cm}^2$
- Leakage current increase as expected
- Pixel array designed by KIT team working after $10^{14} \text{ n}_{\text{eq}}/\text{cm}^2$ fluence
- More COFFEE sensors irradiated by DRD3



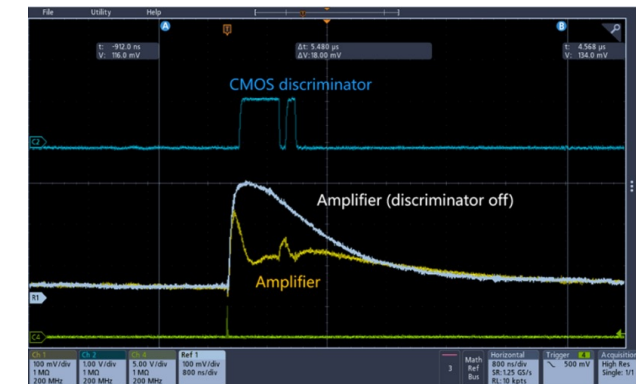
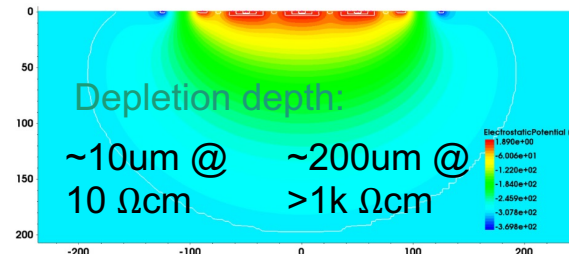
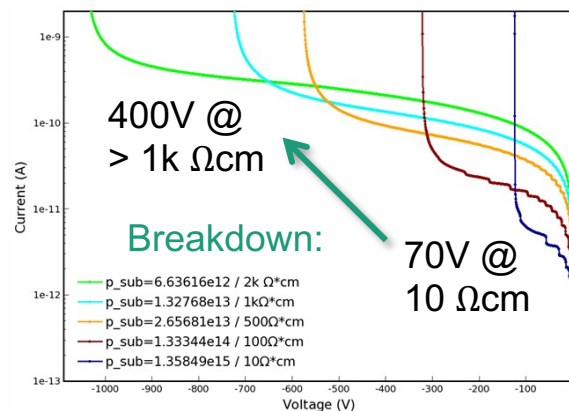
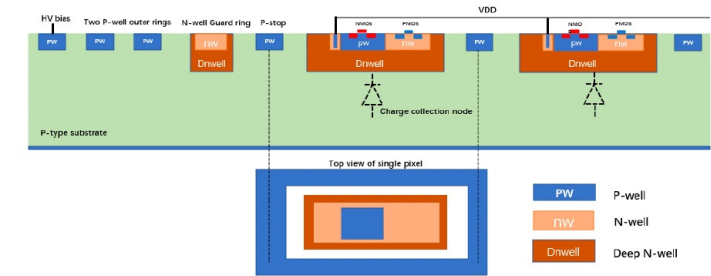
KIT Array



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Limitation of current process

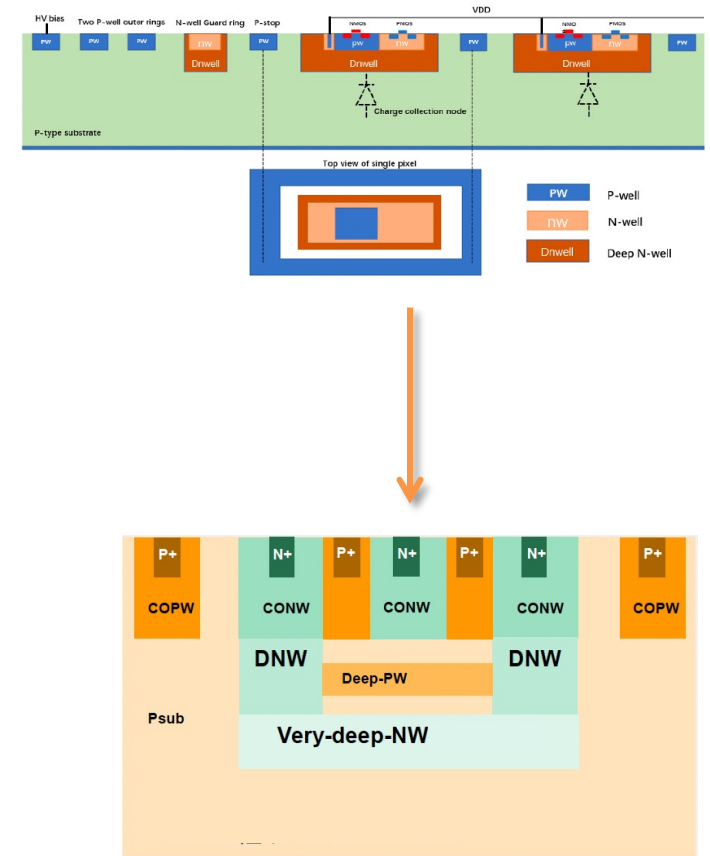
- No access of high-resistivity wafers
 - Small depletion, large capacitance, low S/N ratio
- Triple-well process
 - → cross-talk between sensor (deep-n) and PMOS circuit (hence the NMOS-only matrix!)



Crosstalk betw sensor & digital circuit @ COFFEE2

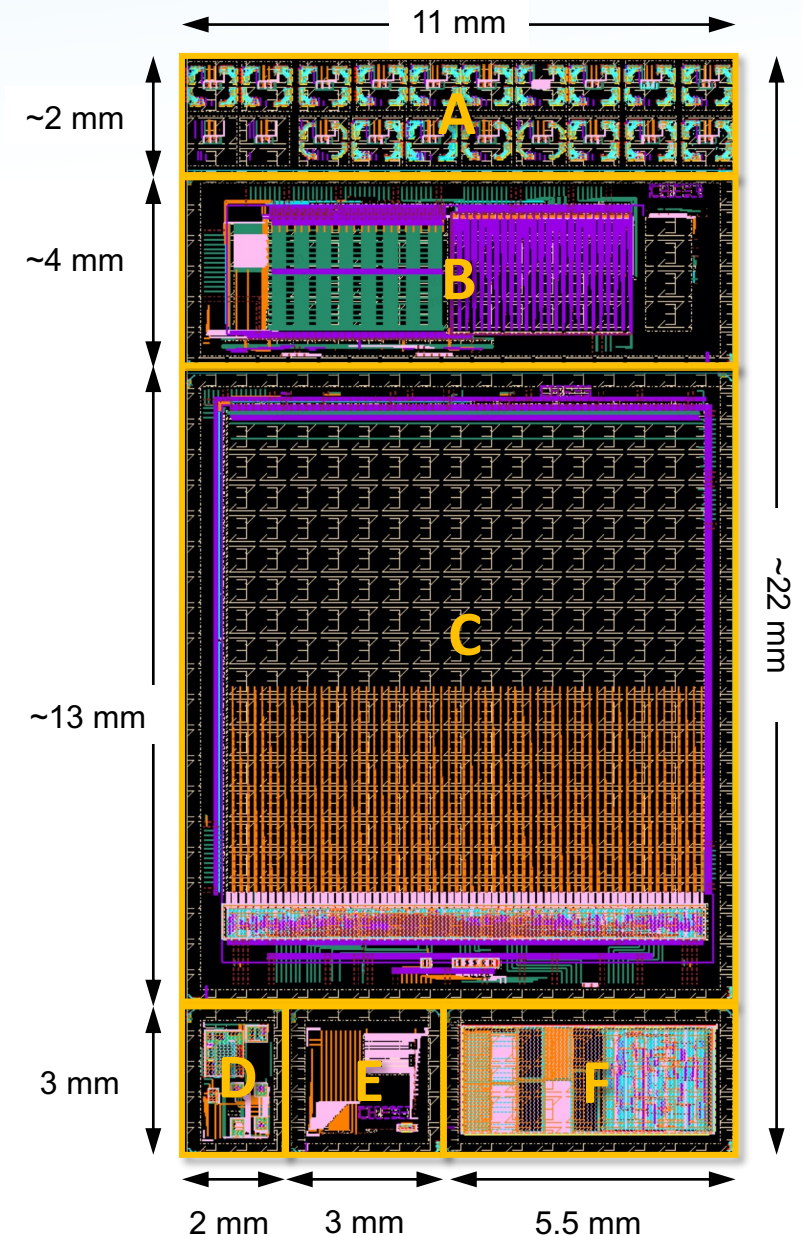
Process improvement: CHiR

- Agreement with foundry by process modification
- **CHiR** (**C**OFFEE-**H**i**R**es) design goal
 - Priority: to validate the process with high-res wafers
 - 1k/2k/4k Ohm cm wafers available from two manufactures
 - Radiation effects of simple components (eg. MOS) with or w/o radiation hardening
 - Implementation of “Five-well process” : to validate basic IP not affected by process modification



CHiR1 chip(s)

- Can be diced into a number of chips serving various goals
- Passive sensor validation:
 - (A) 20 arrays of 3x4 passive pixels with diff guard ring designs, each can be diced into individual 1x1 mm² chip
 - Pixel size: 38 um x 175 um
- Pixel array design
 - (B) 9 variations of in-pixel frontend designs
 - (C) main pixel array of 256 x 64 pixels; similar as COFFEE3 with readout data format compatible with 32-bit UP spec
- IP validations
 - (D) necessary analog Ips: PLL, DLL, LVDS transceivers ...
 - (E) alternative small pixel arrays
 - (F) digital modules and transistors for TID and SEE studies
- Submitted in Jan 2026
 - First batch with 2kOhm cm wafer expected back in July
 - Iteration within fab in ~2 months for the rest
- Future MPW planned in early 2027 if tests positive



内容提要

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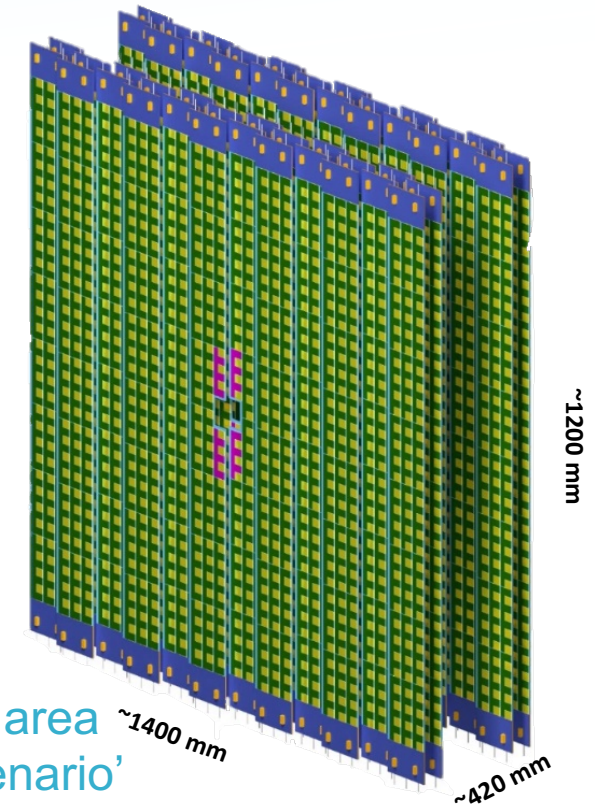
LHCb Upstream Pixel Tracker (UP)

- Collaborations from China, France, Mongolia and US
 - Chinese groups playing leading role
- Aiming to deliver Tracker TDR by Nov 2026

Project Leader: Jianchun Wang / IHEP

Deputy: Tomasz Skwarnicki / Syracuse, Benjamin Audurier / IRFU

WPs	Work Packages and Sub-WPs	Leaders
WP.0	TDR preparation	Marina Artuso / Syracuse
WP.1	Simulation, reconstruction and performance	Xuhao Yuan / IHEP, Steve Blusk / Syracuse
1.1	Detector description and simulation software	Xiaokang Zhou / CCNU
1.2	Reconstruction and performance study	Peilian Li / UCAS
WP.2	Pixel sensor chip development	Yiming Li / IHEP, Fabrice Guilloux / IRFU
2.1	Sensor chip design	Xiaomin Wei / INPU, Yang Zhou / IHEP
2.2	Sensor chip evaluation	Elisabeth Niel / LLR, Hui Zhang / IHEP
WP.3	Module and stave	Ray Mountain/Syracuse, Jiesheng Yu/HNU, Manuel Guittiere/Subatech
3.1	Design and prototyping	(Xuhao Yuan / IHEP), Theo Bigourdan / Subatech
3.2	Stave mechanical and thermal study	Yi Yang / HNU, (Arnaud Cadiou / Subatech)
3.3	Module evaluation	Charlotte Riccio / IRFU
WP.4	Overall mechanics, installation and cooling	Arnaud Cadiou / Subatech
4.1	Mechanical support	Meriadeg Guillamet / Subatech
4.2	Detector integration and installation	Meriadeg Guillamet / Subatech, Bassem Khanji / Syracuse
4.3	Cooling system	Hangyi Wu / Syracuse
WP.5	Data acquisition system	Kai Chen / CCNU, Zijun Xu / IHEP
5.1	Overall readout scheme	(Jianchun Wang / IHEP)
5.2	UP-specific firmware	(Kai Chen / CCNU)
5.3	Control and monitoring	(Zijun Xu / IHEP)
5.4	DAQ system for evaluation and production	(Marina Artuso/ Syracuse)
WP.6	Electronics	Kai Liu / LZU, Christophe Renard / Subatech
6.1	Design of FE electronics	Zhiqiang Fu / LZU
6.2	HV and LV systems	Kechen Li / HTU

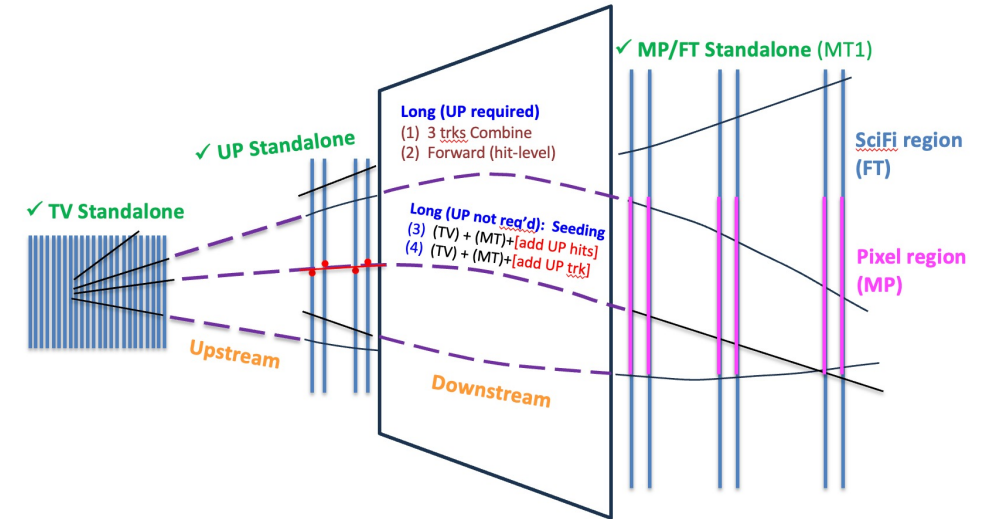


6.8 m² active area
in 'middle-scenario'

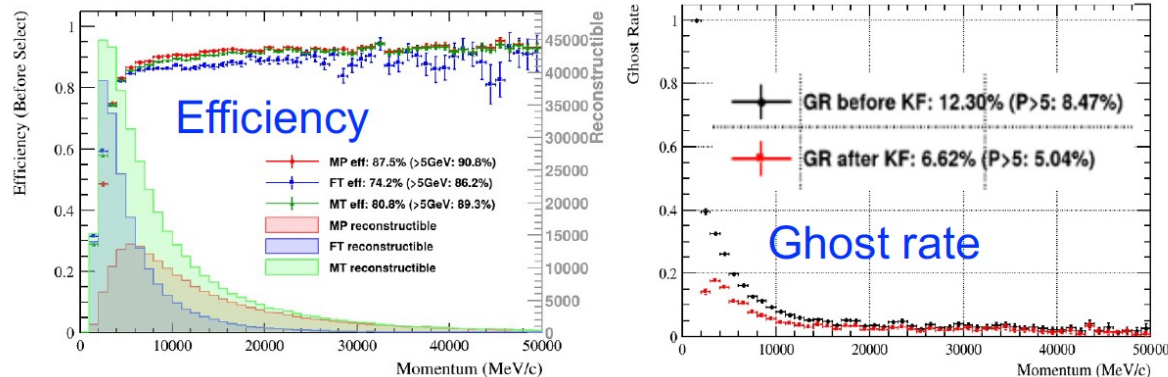


UP: simulation and performance

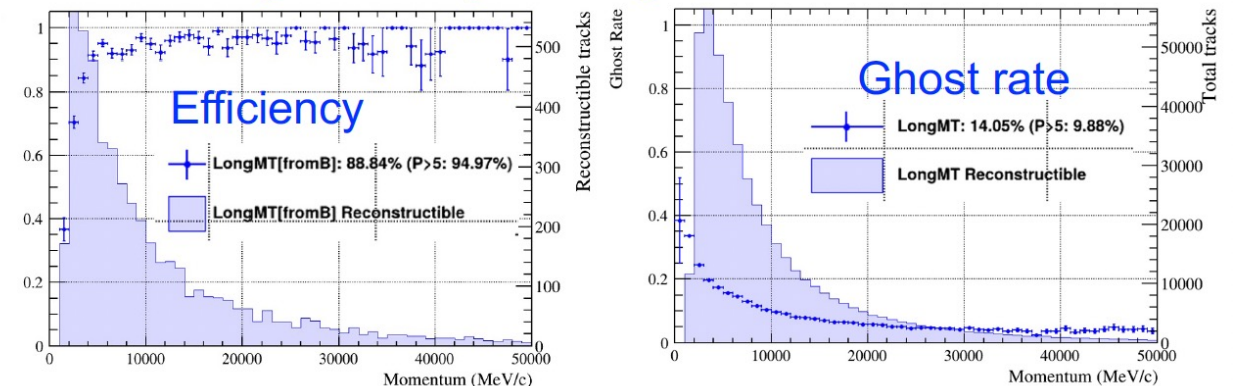
- Standalone UP tracking possible with pixel sensors
- More possibilities in tracking algorithms
 - Forward alg.: VELO $\rightarrow$ UP / MT
 - Match alg.: VELO + MT $\rightarrow$ + UP
 - Backward alg. (new!): combine all 3 standalone tracks
- Merging all algorithms give good performance (eff $\sim 95\%$, ghost rate $O(\%)$) as of now, under >8 times more tracks!



Long Tracks by "backward alg"

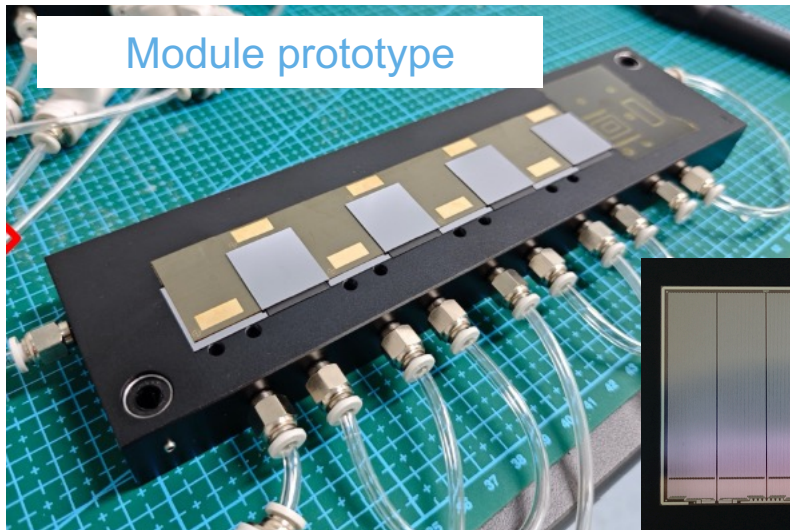
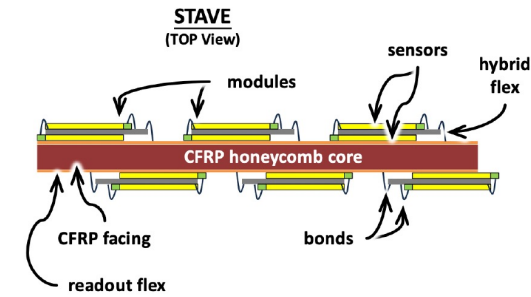
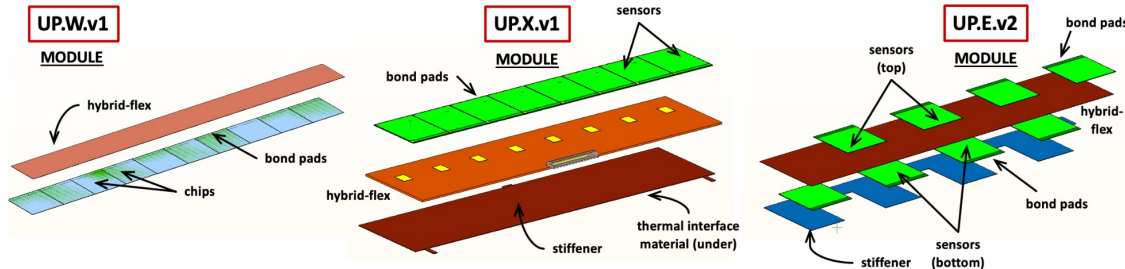


Long Tracks by all 3 algs. after clone killer

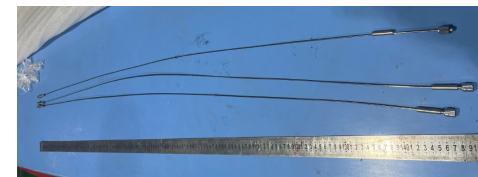
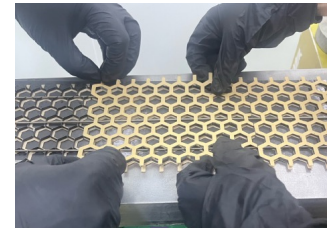
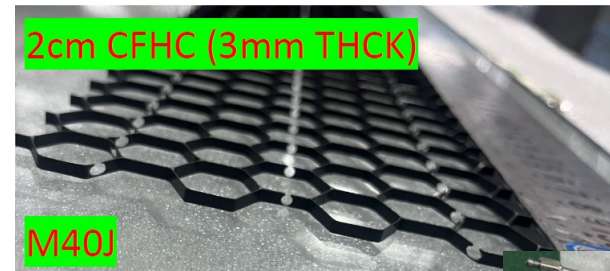
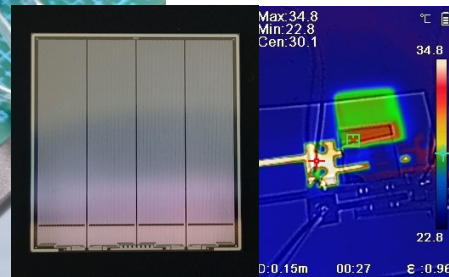


UP: design concept & prototyping

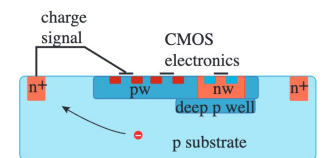
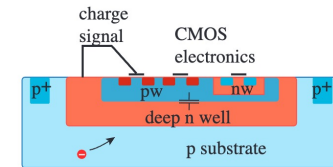
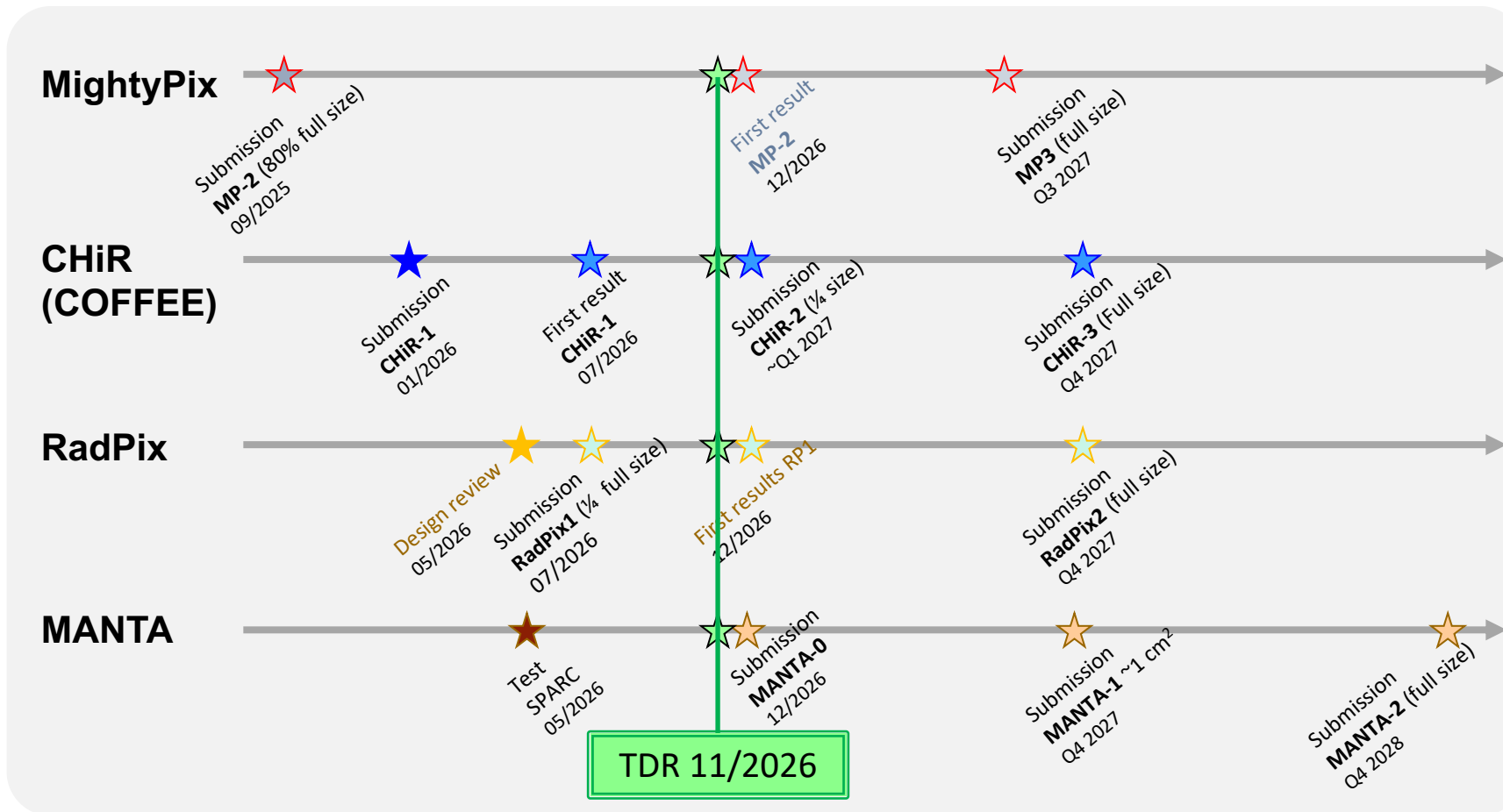
- Three module concept designs
 - Unique **gapless design** proposed by Chinese groups; prototypes with dummy chips
 - Mechanical prototypes of light-weight bare stave



Module prototype



UP: Sensor options

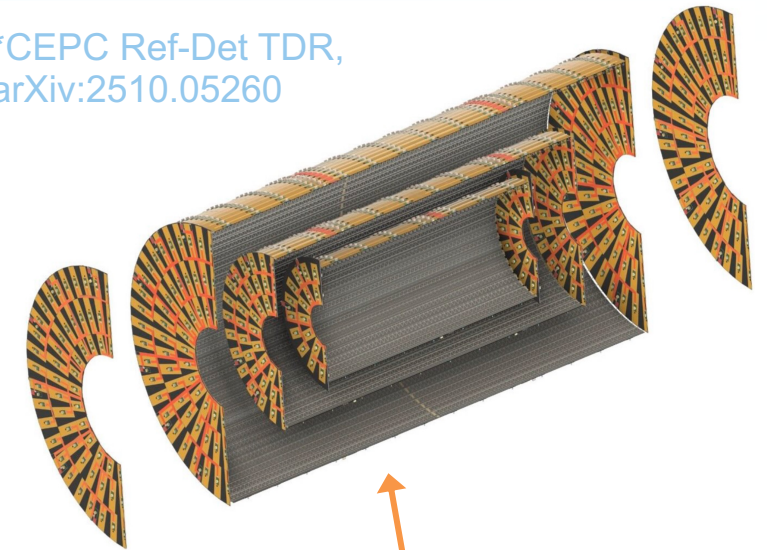


We start relatively late, but progressing fast - and using more advanced process!

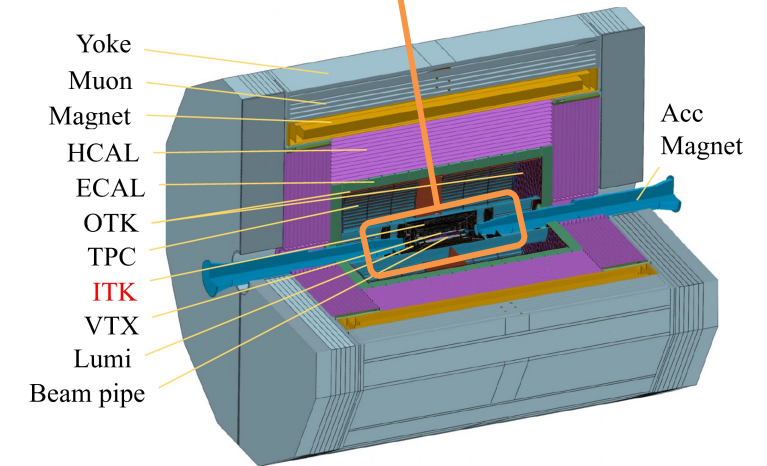
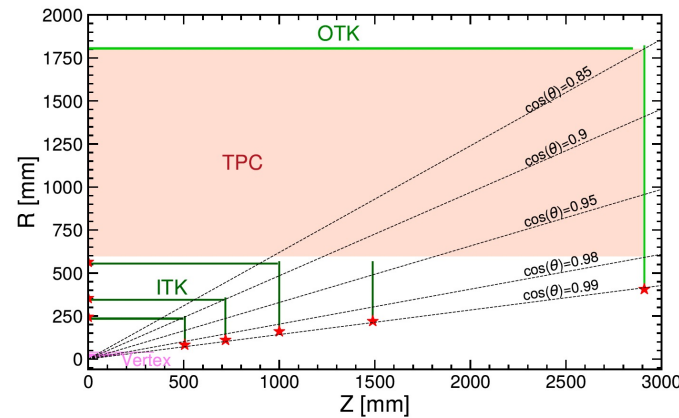
AGORA Inner Tracker for CEPC / FCCee

- Inner Tracker is a central part of CEPC Ref-Detector tracking system
 - Using HVCMOS pixel sensors covering an area of $\sim 20 \text{ m}^2$.
 - With spatial resolution of $\sim 8 \mu\text{m}$, ITK aims for good time resolution to allow tagging of 23.1ns bunch spacing at most demanding high-lumi Z operation
- 3 barrels layers + 4 pairs of endcap disks

*CEPC Ref-Det TDR,
arXiv:2510.05260

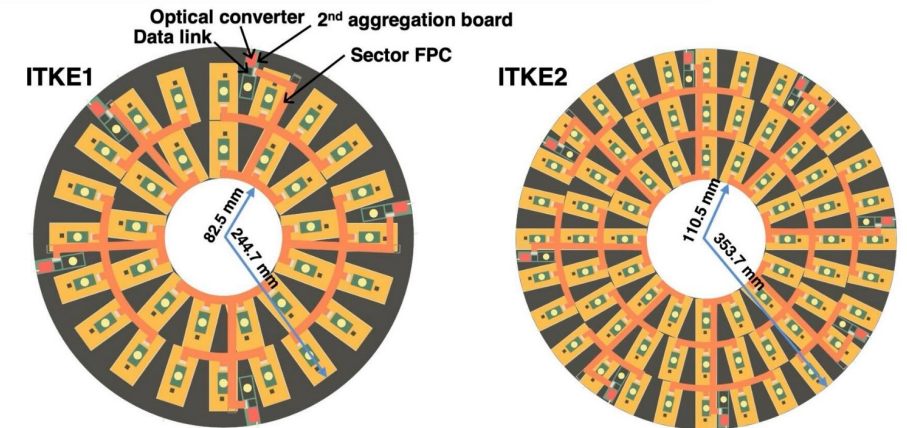
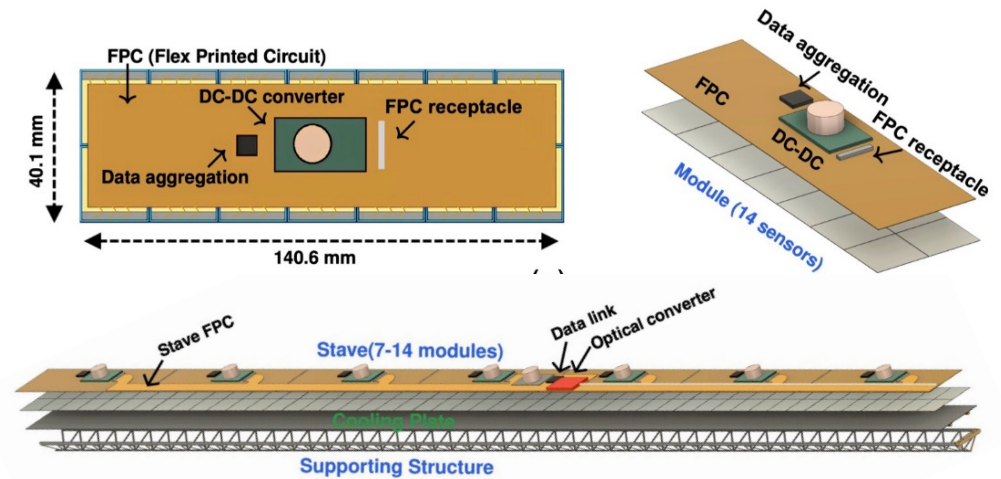
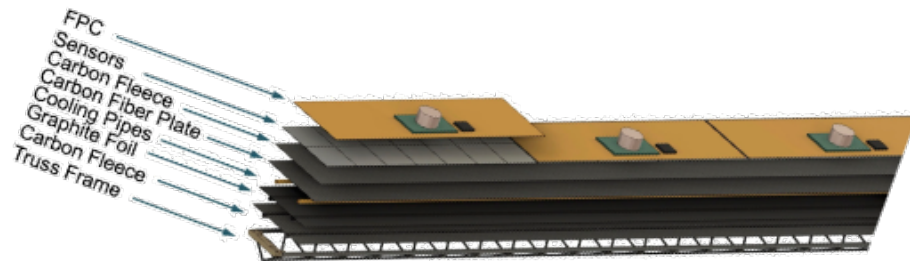
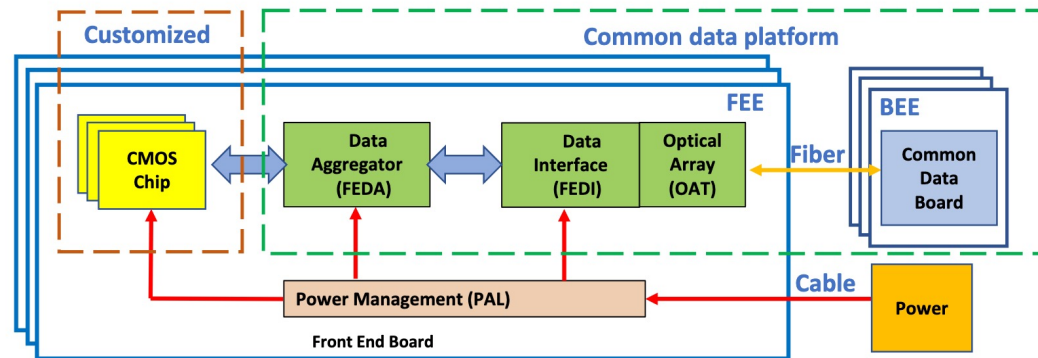


Parameter	Value
Sensor size	2 cm × 2 cm (active area: 1.74 cm × 1.92 cm)
Sensor thickness	150 μm
Array size	512 × 128
Pixel size	34 μm × 150 μm
Spatial resolution	8 μm × 40 μm
Time resolution	3-5 ns
Power consumption	200 mW/cm ²
Technology node	55 nm



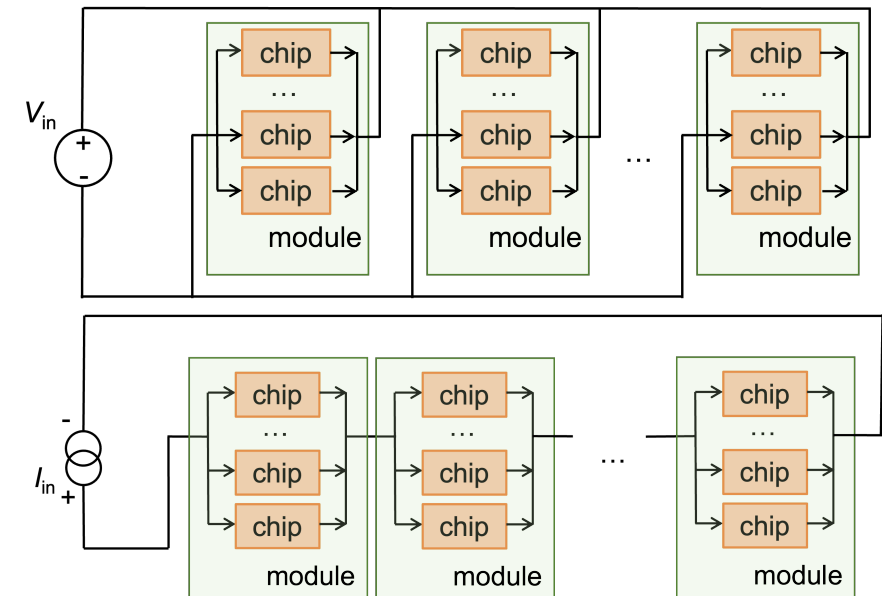
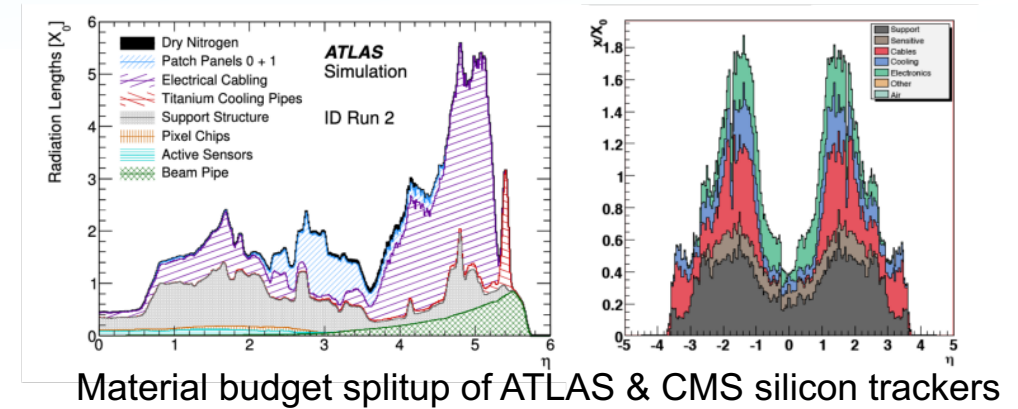
AGORA Inner Tracker for CEPC / FCCee

- Both barrel and endcap shares a common module design
 - With 3 variations of pixel numbers
- Readout and power supply in line with common electronics
- Low-material budget for reduction of multiple scattering
 - Aiming for $< \sim 0.7\% X_0$ / layer in barrel



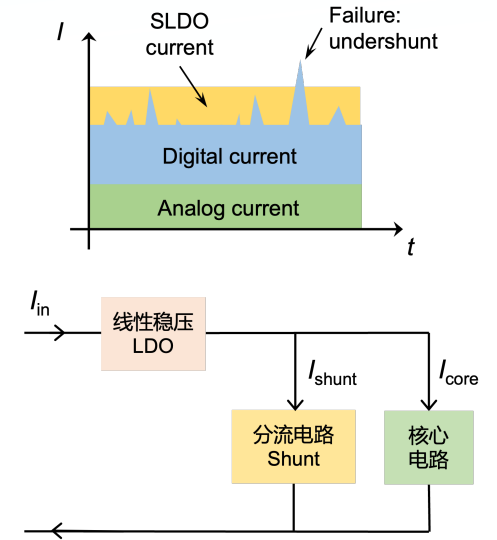
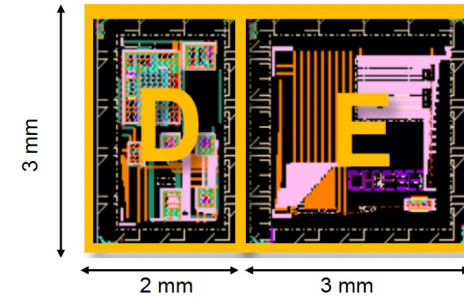
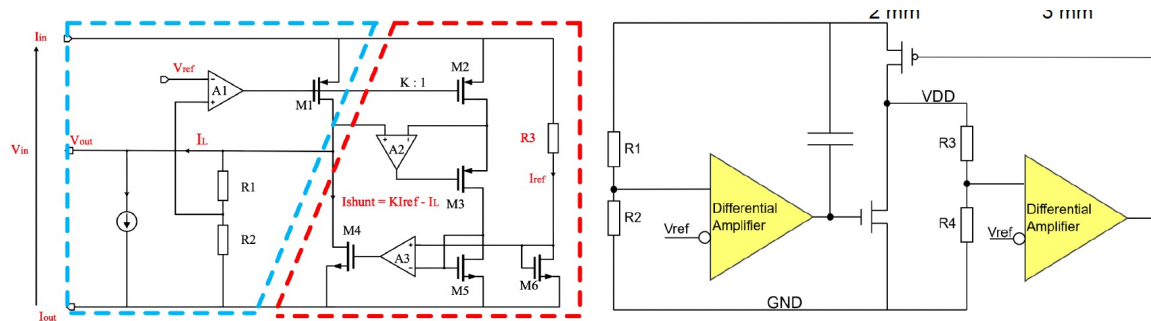
New prototyping initiative

- Cables /services become challenge for large tracking detector system
 - Material budget! → deteriorating momentum resolution
 - Space, installation complexity
 - Power consumption
- An approach towards less cables: **Serial powering**
 - As pixels increases by N
 - Parallel power (or +DCDC) by N^2
 - Serial power by N
- Adopted by ATLAS/CMS Phase II trackers



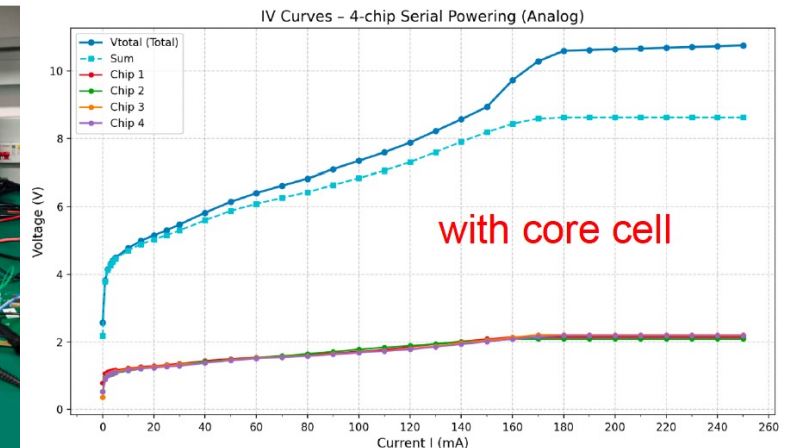
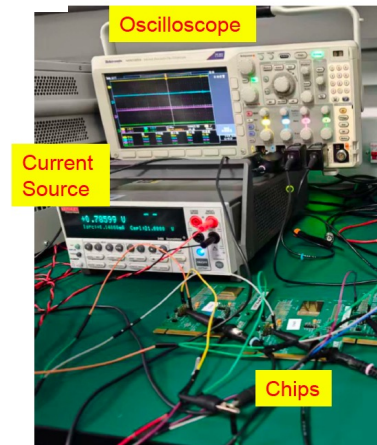
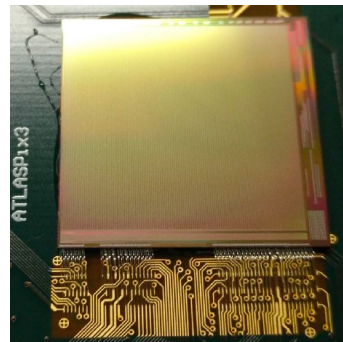
Serial powering development

- Design of SLDO for 55nm process aiming IP for integration into final chip
 - CHiR1.0 already implemented two different designs of Shunt LDOs



- Demonstrator of multi-module tests
 - experience using ATLASPix3 chips

ZHANG Hui's talk @ 5th DRD3 week



Summary

- COFFEE series chips are developed for the LHCb UP and CEPC ITK requirements, using advanced 55nm CMOS process in China
 - COFFEE3 tests show readout architecture functioning for the fast readout
 - First testbeams successfully taking MIP data
 - Process limitation understood and modified – CHiR designed & back soon
 - Aiming for a full size chip in 2028
- Detector system progress based on the COFFEE sensors
 - UP to deliver TDR this year
 - CEPC Ref-TDR published
 - New development such as serial powering ongoing

Thank you for your time & collaboration welcome!