Zero Degree Calorimeter (ZDC) at BESIII

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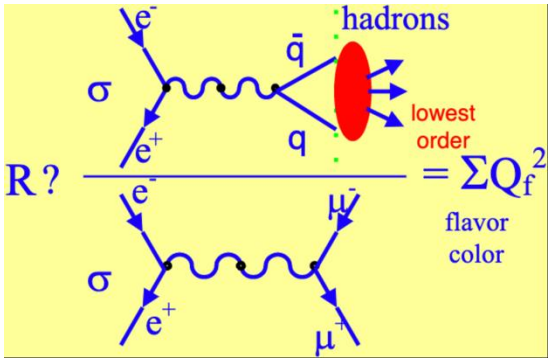
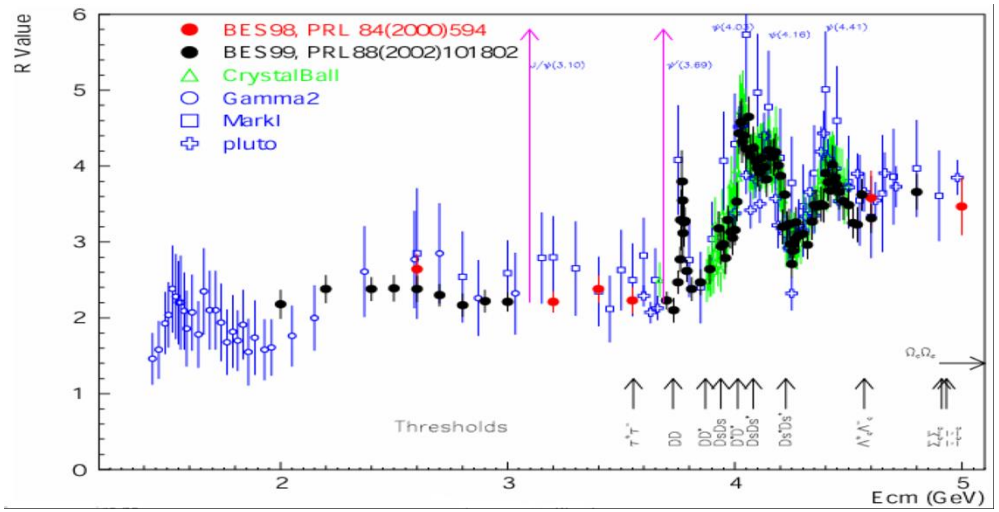
On behalf of the BESIII-ZDC team

Guangzhou, Jul 13 to 19, 2026

Physics in Energy Scan

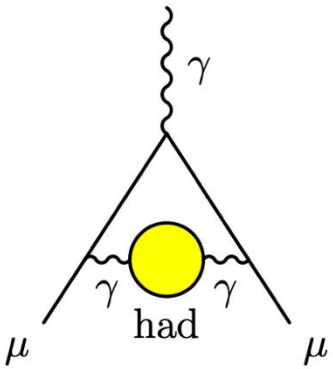
- R-value

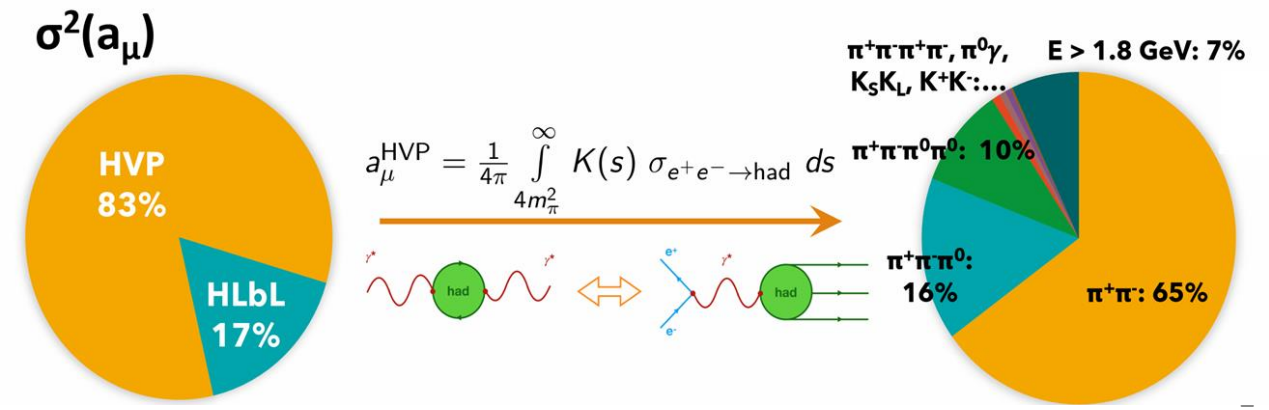




- Dominant uncertainty for muon g-2 (>80%)
  - hadronic vacuum polarization (HVP)
  - Extracted from ee→hadrons cross section

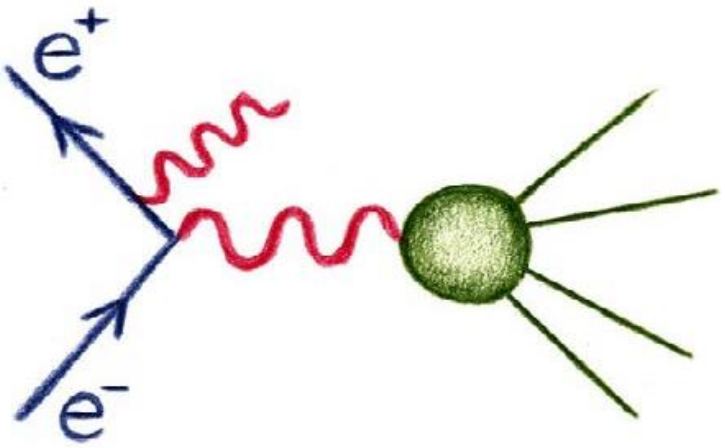
$$a_\mu^{SM} = a_\mu^{QED} + a_\mu^{Weak} + a_\mu^{Had.}$$

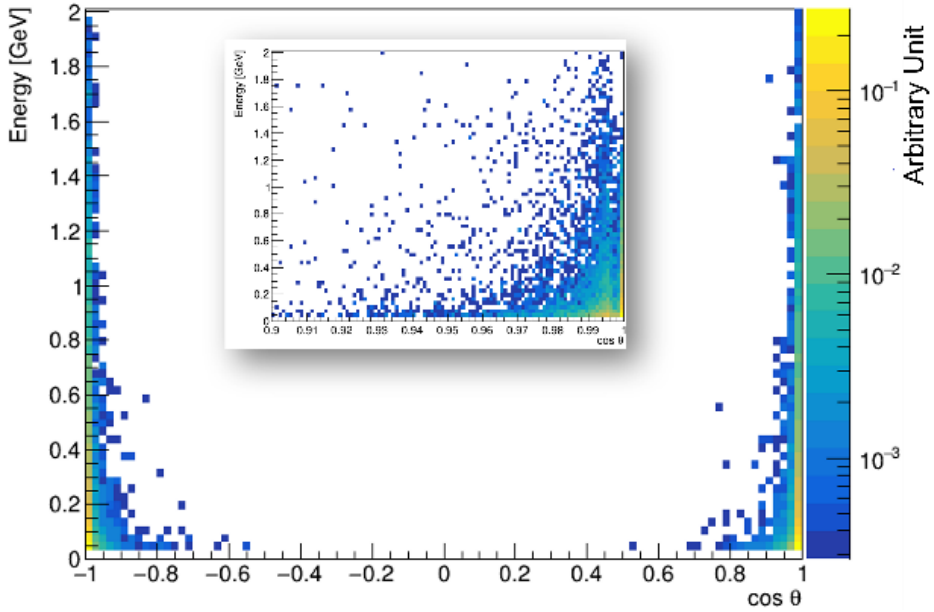




ISR return

- Initial State Radiation (ISR) return
  - $e^+e^- \to \gamma_{ISR} e^+e^- \to \gamma_{ISR}$ X lows e^+e^- collision energy, by radiating a photon
- ISR photon mostly in forward region (|cosθ|>0.99)
  - EMC (|cosθ| <0.93) only detect large angle ISR photon, very low efficiency

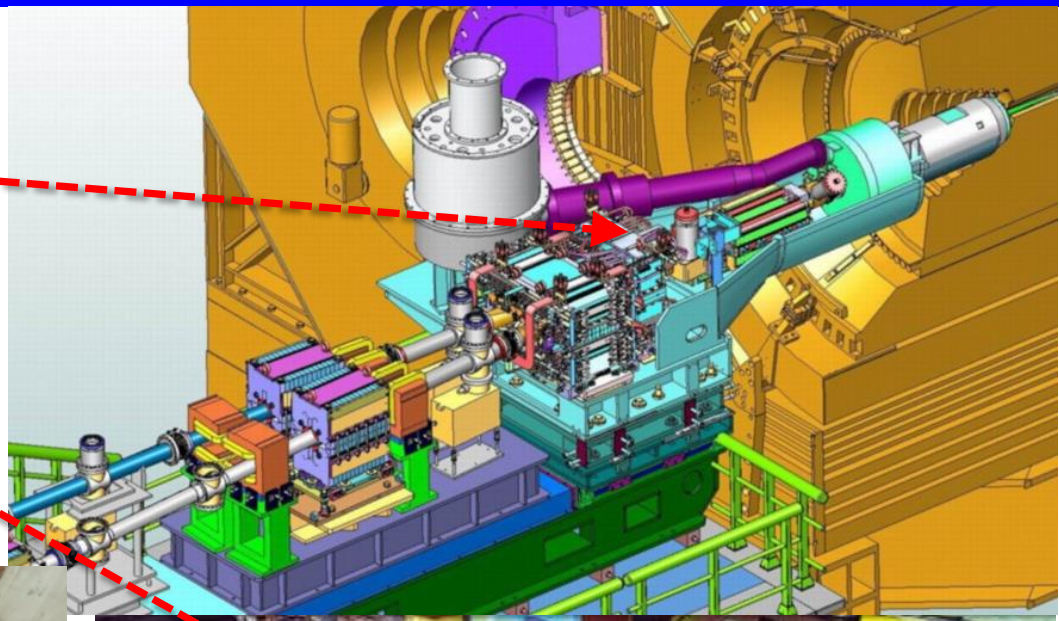




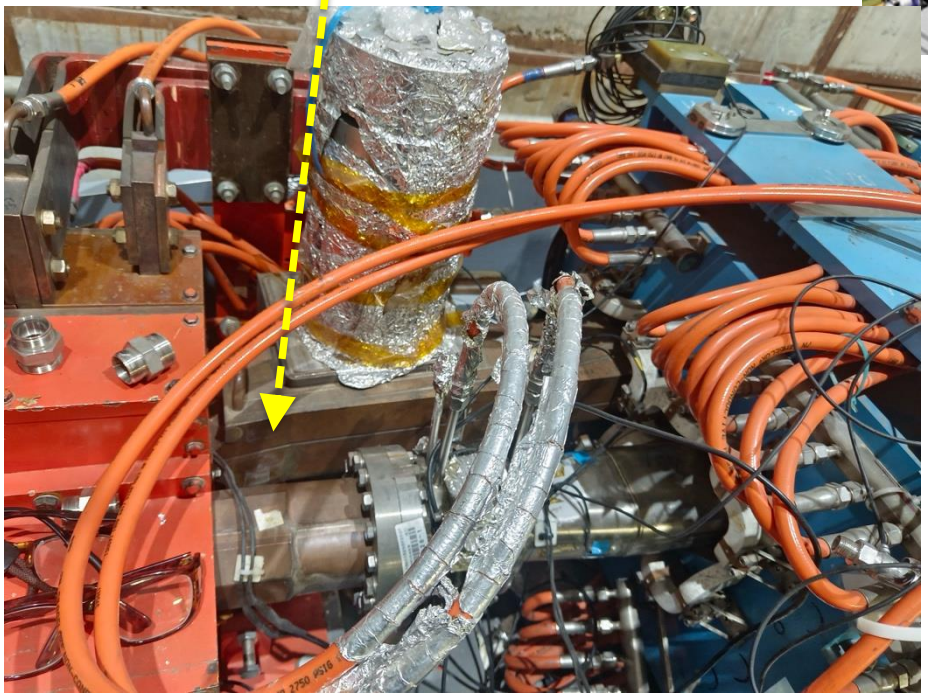
A forward detector will significantly boost ISR physics

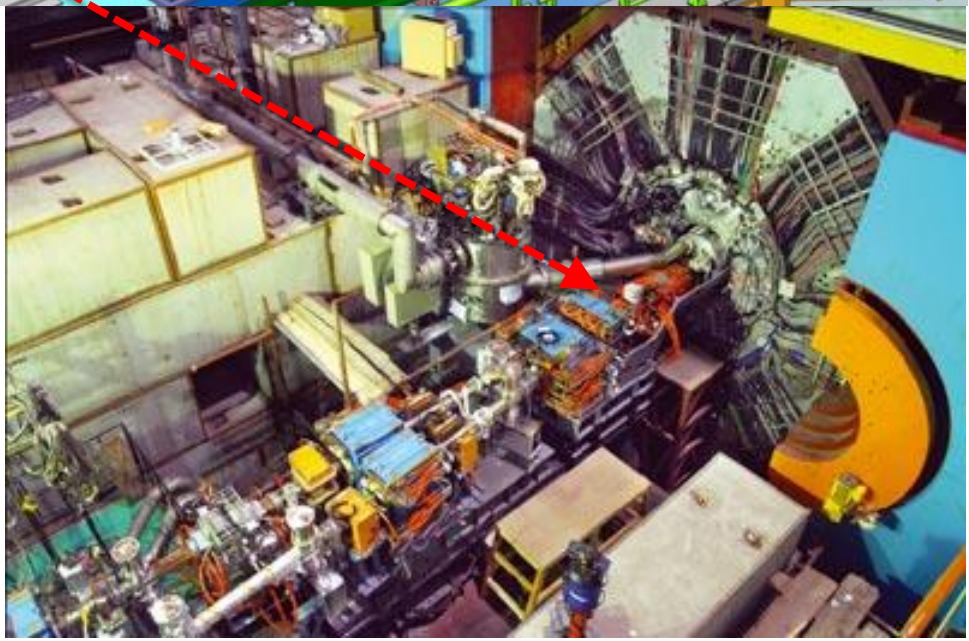
Location for Zero Degree Detector

- 3.3m <z<3.5 m,
  θ=0 in CMS frame



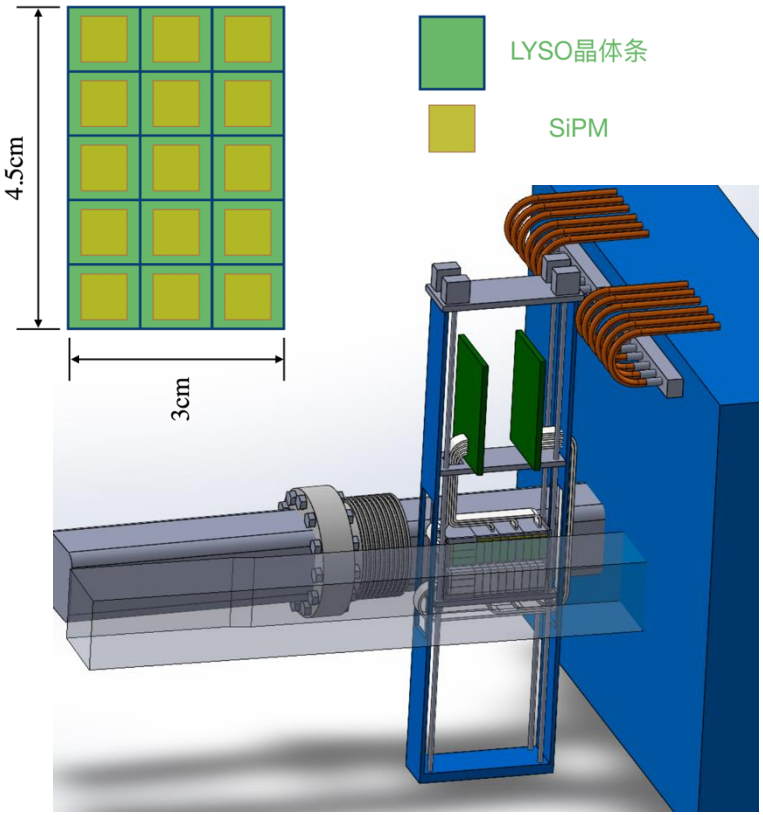
Copper window of out-going beampipe

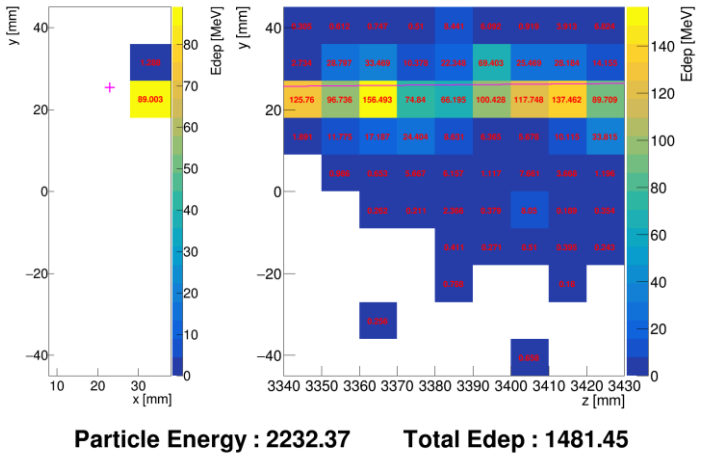


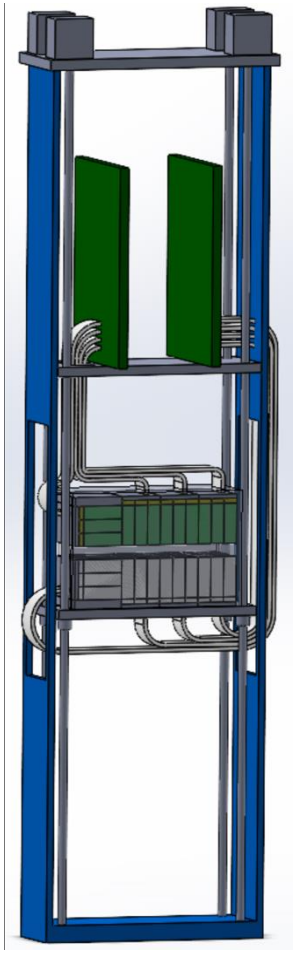


Crystal+SiPM array calorimeter

- Zero Degree Calorimeter (ZDC)
  - LYSO+SiPM array, 240 channels in total
  - Fully modalized design, optimal for energy and position

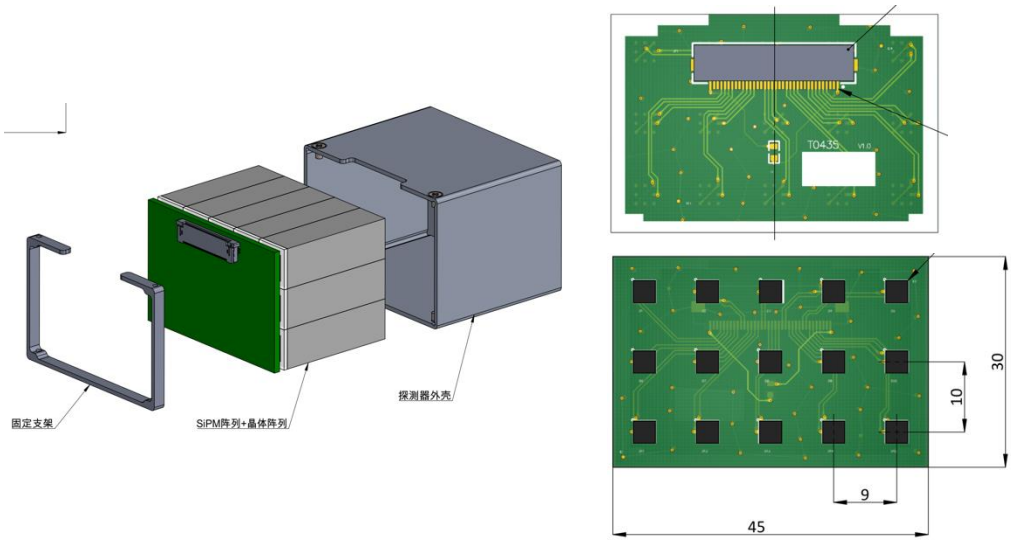




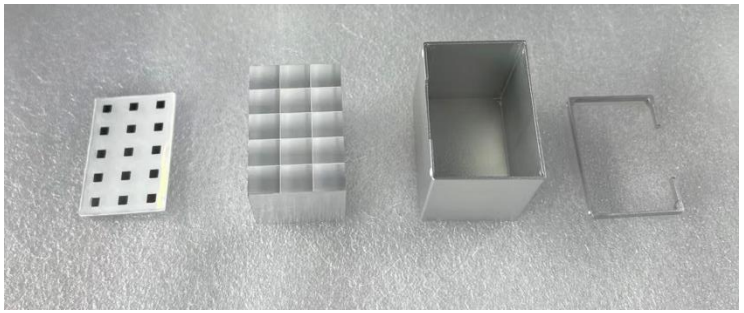


Module design

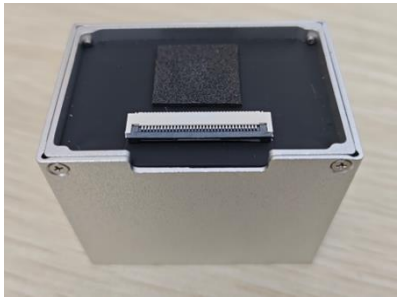
- Module design
  - 3x5 LYSO bar array (LYSO bar dimension: 9mm x 10mm x 30mm)
  - SiPM back board mounted with corresponding 3x5 SiPM array and a small-profile connector
  - Shielded with metal box



Module conceptual design

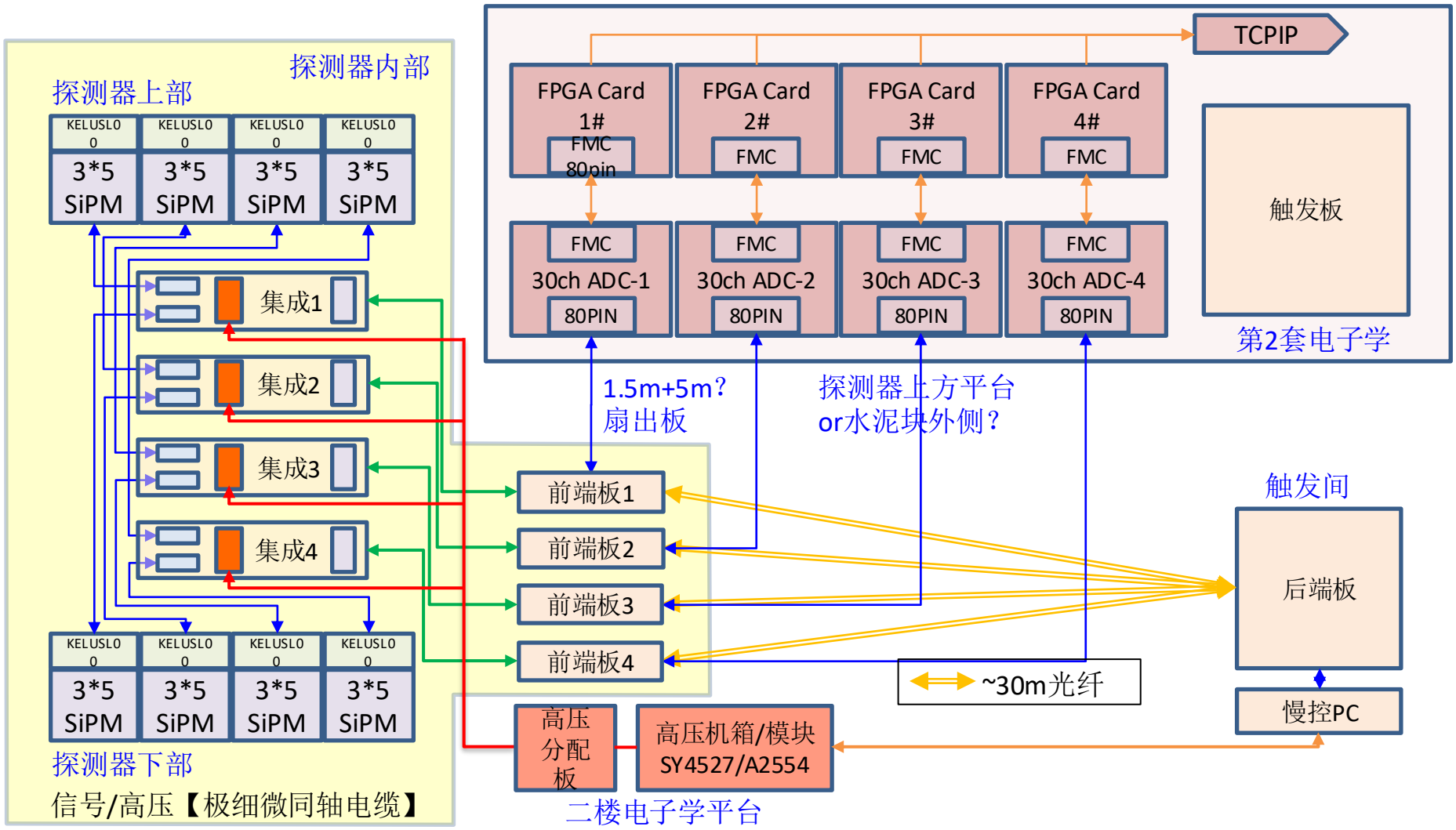


Components before assembly



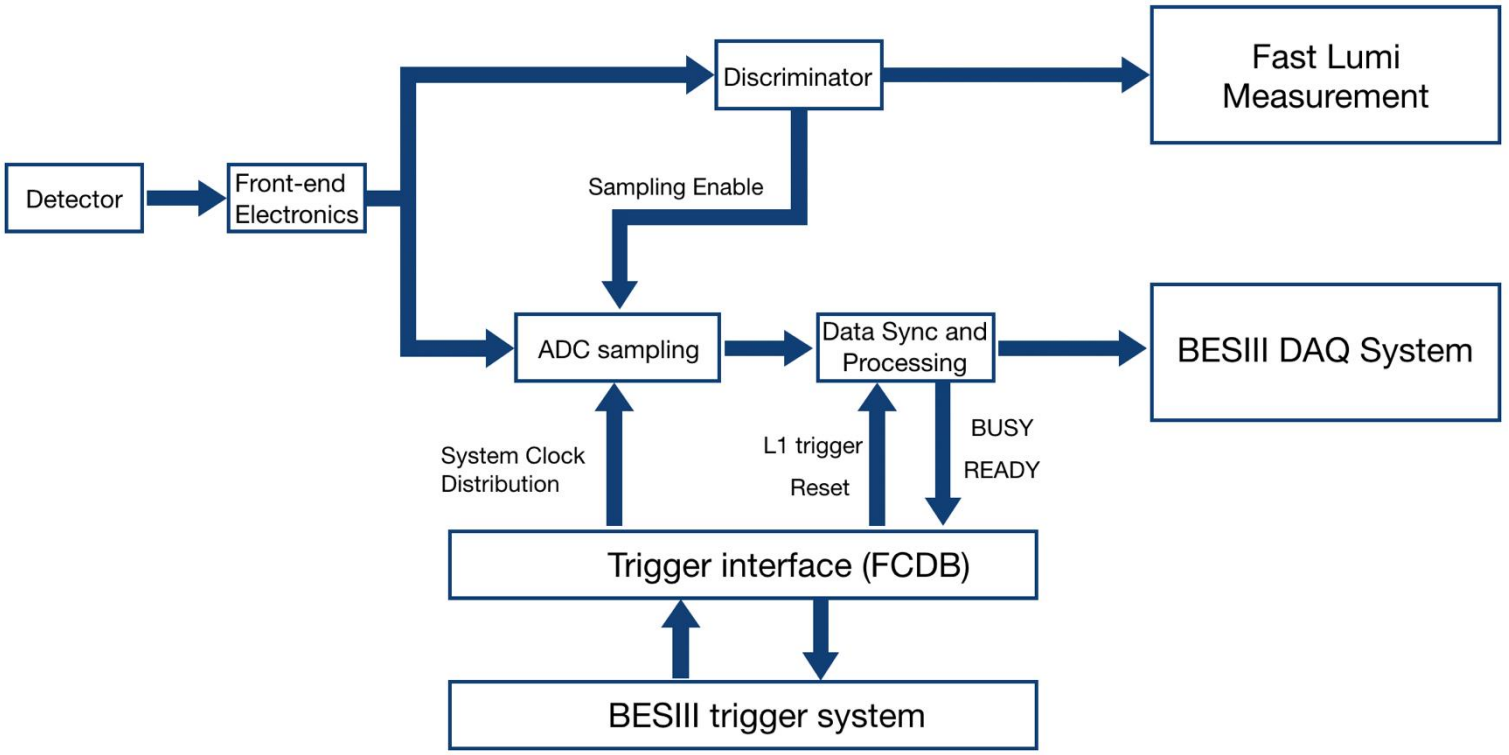
Picture of the module

Readout Electronics Architecture

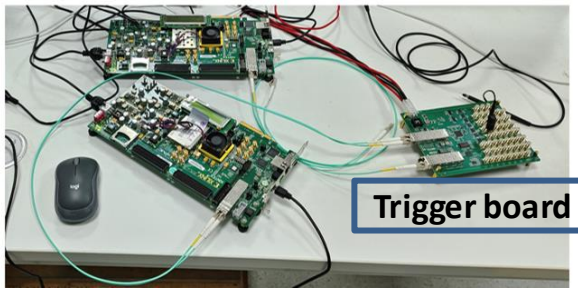


Readout Electronics Architecture

- Three blocks: Front-end, Fast Luminosity, Energy meas. & DAQ



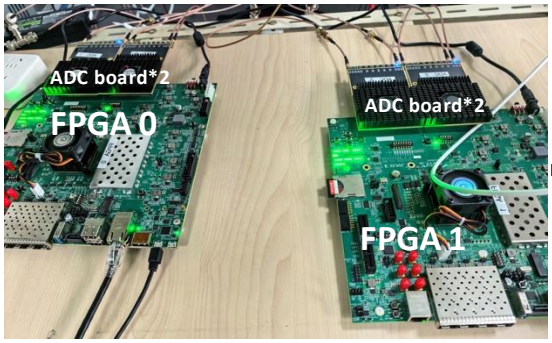
Full Data Flow Chain



Trigger board (fiber input)

KC705 emulate BESIII L1 signal
Later will be replaced by BESIII new trigger system

L1, CHK, CLK



ADC+FPGA
(32 CH inputs)

TCPIP

8*RJ45 to PCIe network card

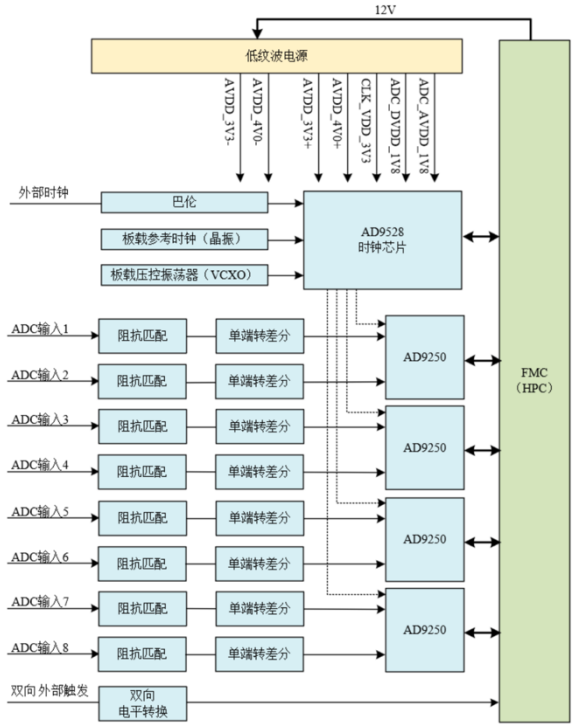
UART

TCPIP

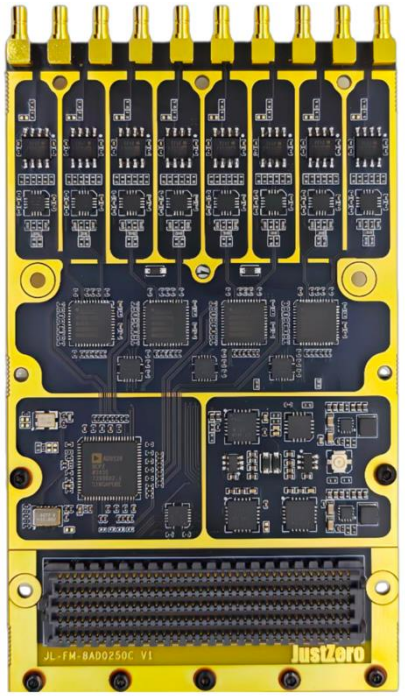
- Energy measurement & Trigger DAQ
  - ADC board: High speed sampling, connected to FPGA via FMC
  - FPGA board: clock and ADC config., data package, send to DAQ with L1
  - Trigger board: synchronize with BESIII Trigger system
  - Full waveforms readout and reconstructed offline via Ethernet cable to PCIe network card
  - Event build at PC with multiple FPGAs based on Trigger ID and CHK count

Hardware: ADC board

- 8-ch inputs with 14-bit resolution at 250MSPS sampling rate
- FMC connector to FPGA carrier board
- Dedicated connector reserved for L1 trigger and check signal



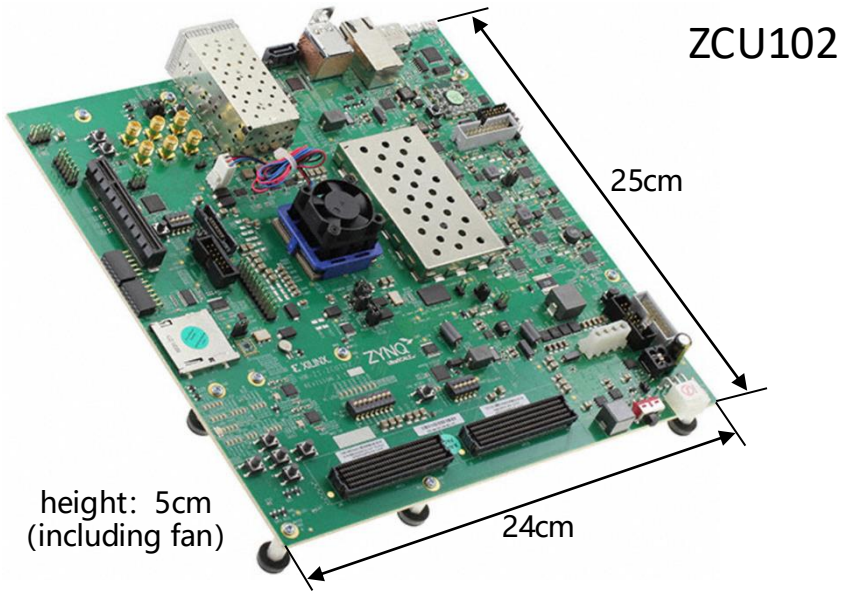
Block diagram of the ADC board



Top and bottom view of the ADC board

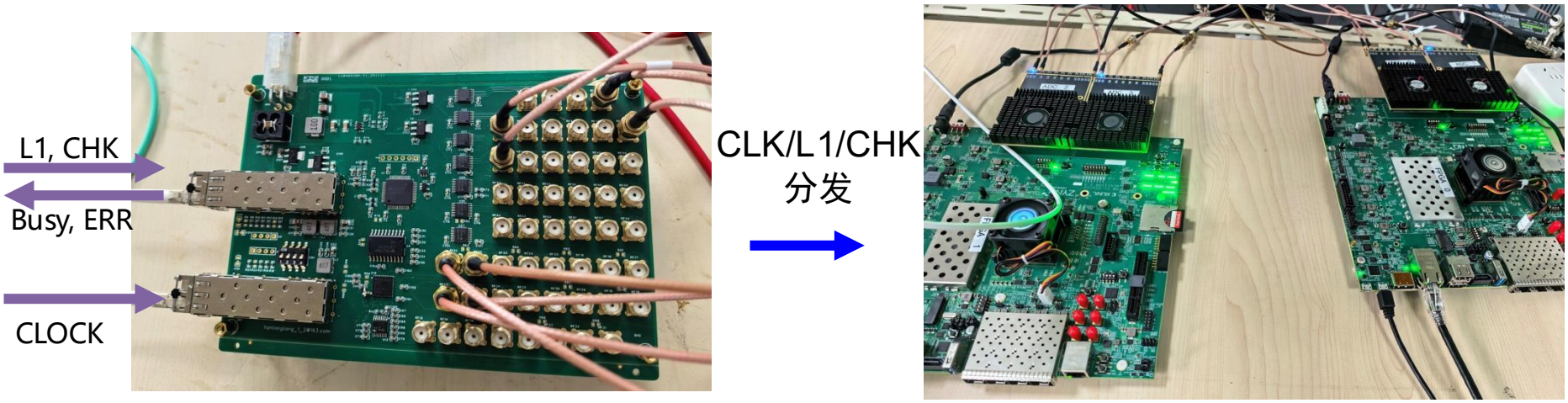
Hardware: FPGA board

- Two ADC boards connected via FMC to handle 16 ch in total
- SoC with FPGA Programmable Logic(PL) and Processing System (PS), which facilitates data processing
- Optional Ethernet cable or optical fiber to DAQ



Hardware: Trigger board

- Timing Synchronization:
  - Fan-out to distribute **CLK/L1/CHK** signals to different boards, enabling system-wide timing synchronization.
  - **CLK:** BESIII clock from trigger board used as the clock source
  - **L1/CHK:** Distribute the decoded L1/CHK signals to 4 FMC daughter cards
  - Fan in feed-back signals from ZDC electronics

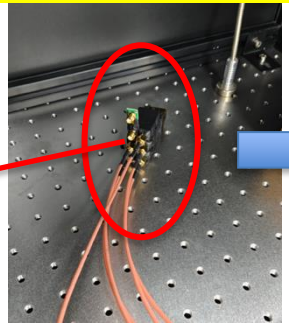


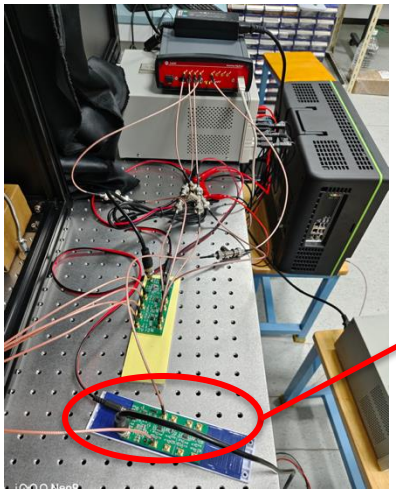
LYSO+SiPM detector R&D

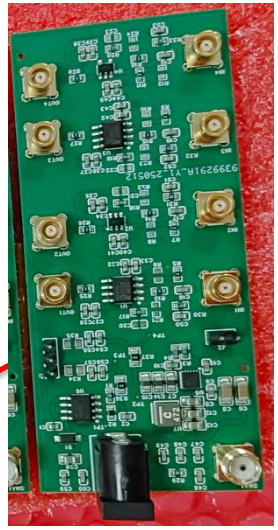
- Integration of LYSO+SiPM module and readout electronics
  - Front-end electronics (1st version)

SiPM readout board

LYSO+ SiPM module

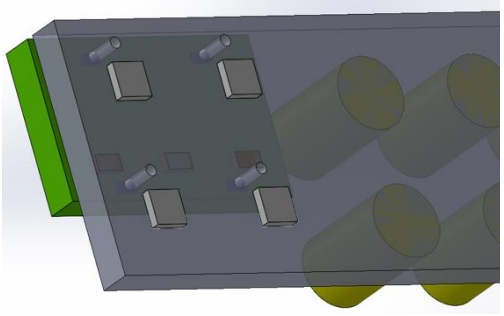


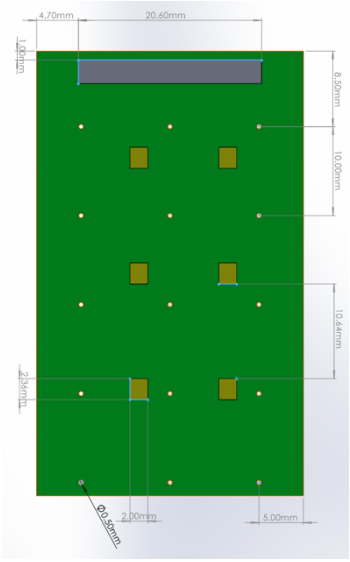


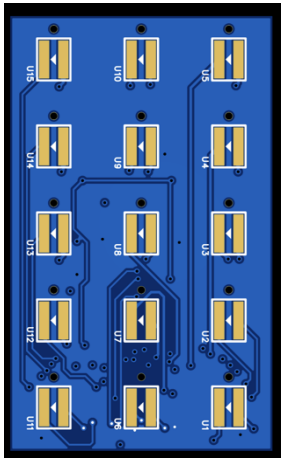


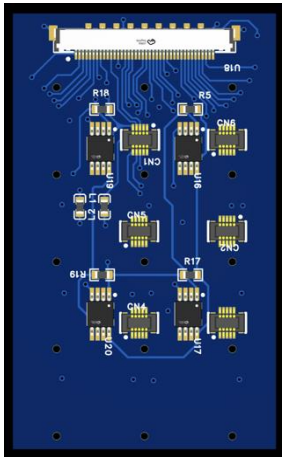
PreAmp board

- LED calibration system



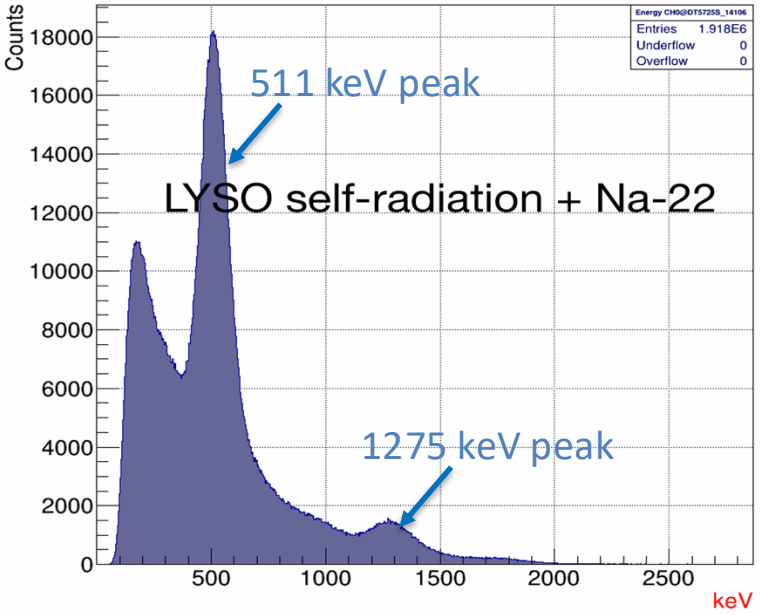


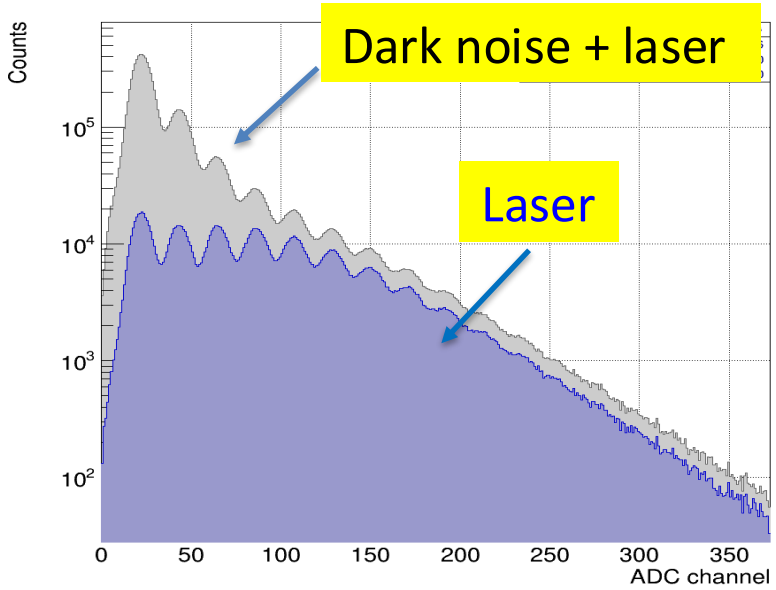




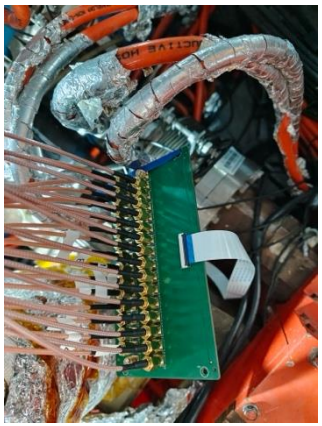
LYSO+SiPM: tests at Lab

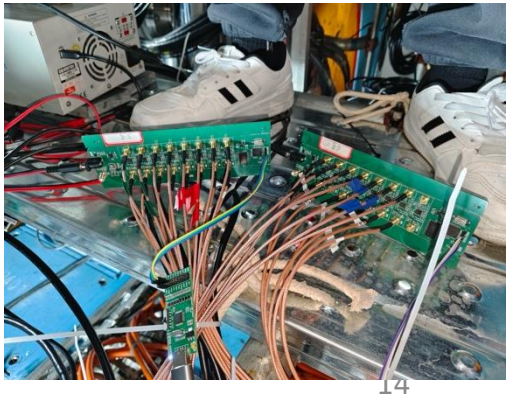
- Tests with radioactive sources and laser system



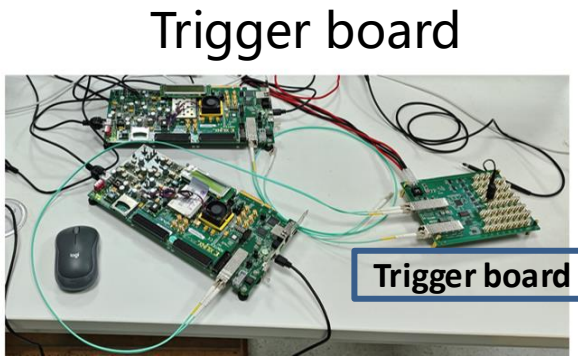


- Reliability test at BEPCII

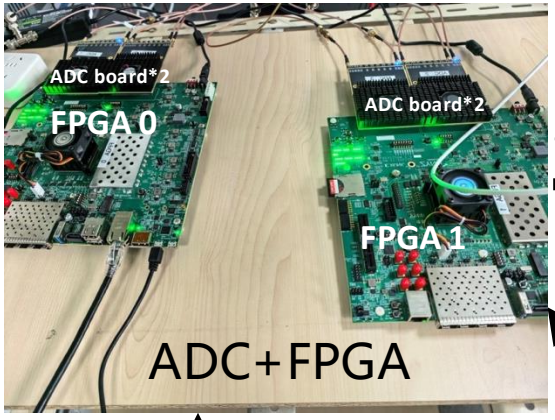




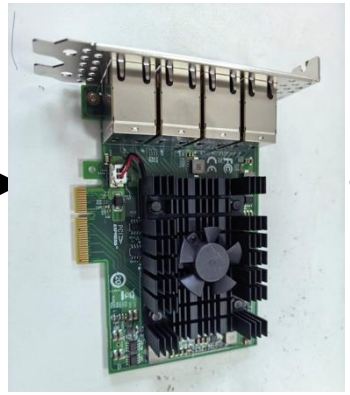
Joint test



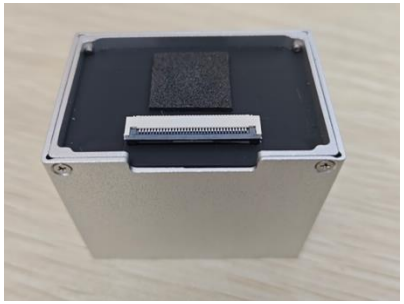
L1, CHK, CLK



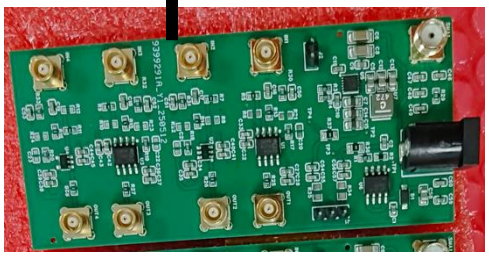
TCPIP



8*RJ45 to PCIe network card



15xSiPM signals



Amplified signals

Pre-amp board

UART

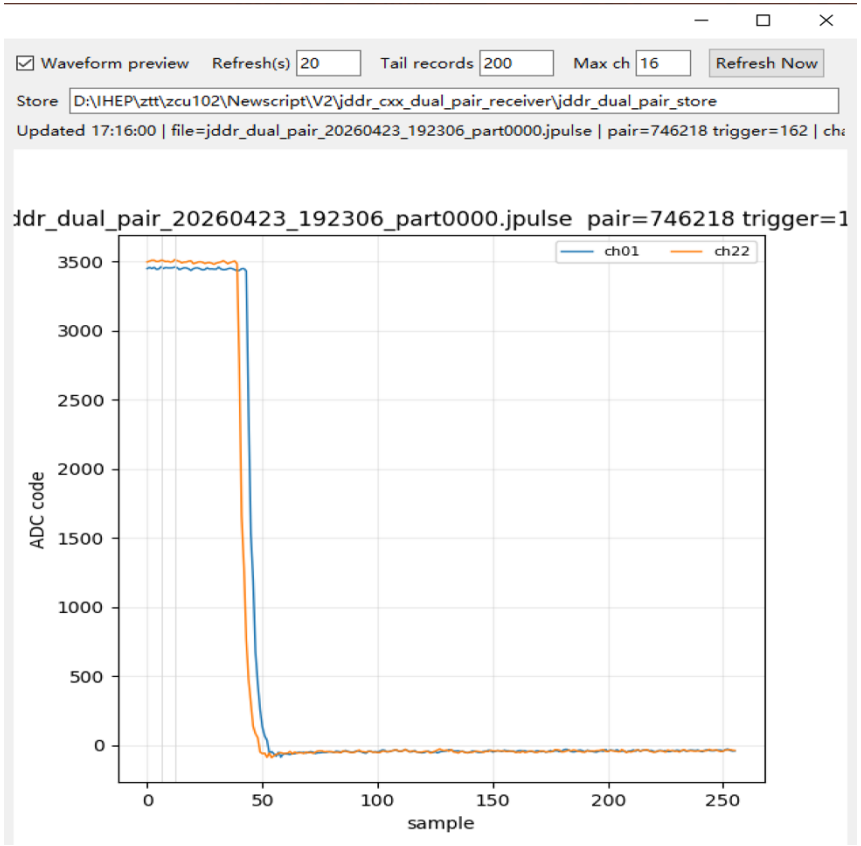
TCPIP

- 15 CH detector module as signal inputs
  - Amplified and routed to the ADC+FPGA system
  - 7 ch to FPGA-0 and another 8 ch to FPGA-1

Event Synchronization and Alignment:

- DAQ firmware and software framework developed
  - Package loss rate measured below 0.7×10^{-8}.

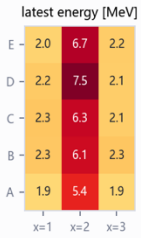
Online waveform monitoring interface showing the waveforms of the same event simultaneously acquired by two FPGAs.



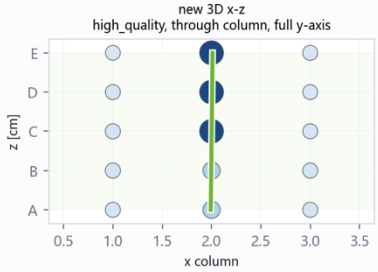
Measurements

- Typical reconstructed cosmic-ray muons events

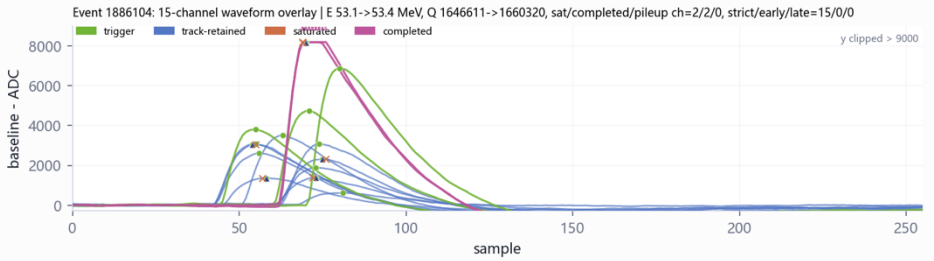
Energy deposition (MeV)

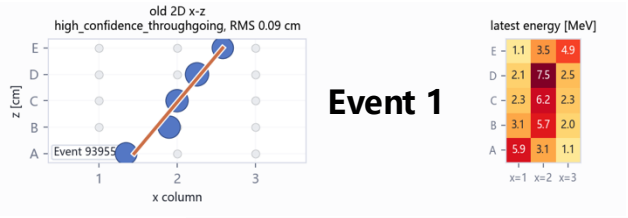


Track fit

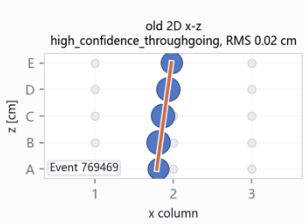


Waveforms

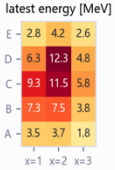


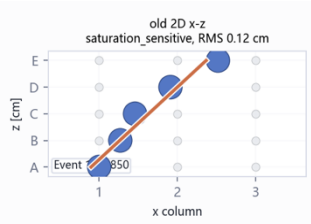


Event 1

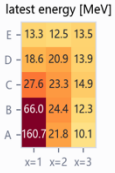


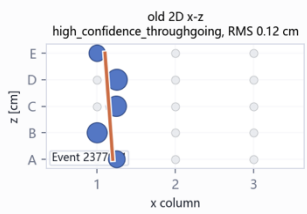
Event 2



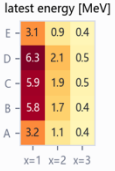


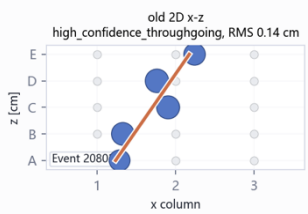
Event 3



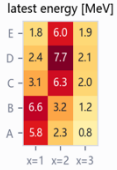


Event 4



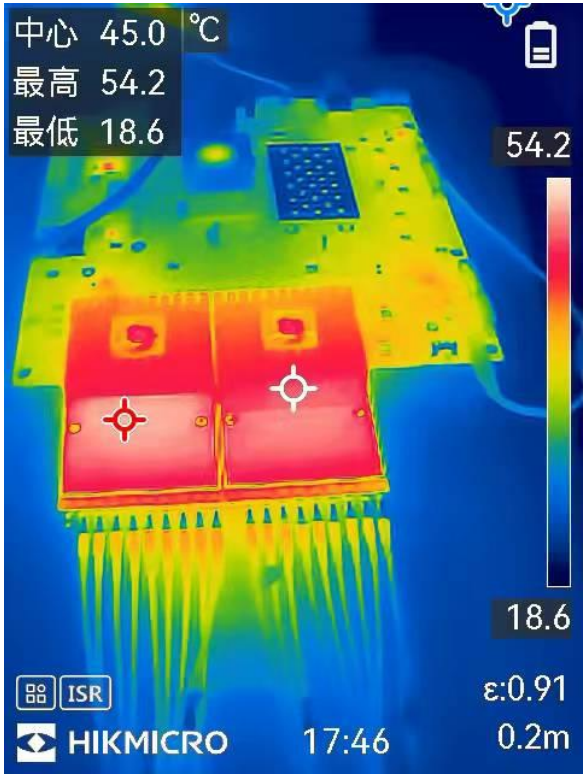


Event 5



Thermal performance

Hardware setup

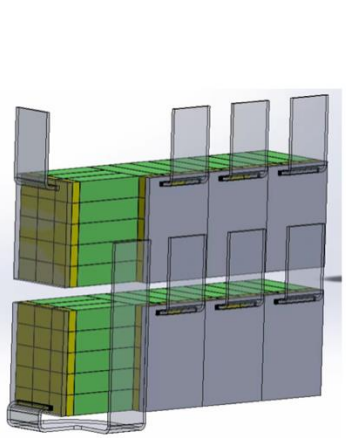


Temperature heat map

- ADC full load run for ~5 hours and temperature remains < 55 degree

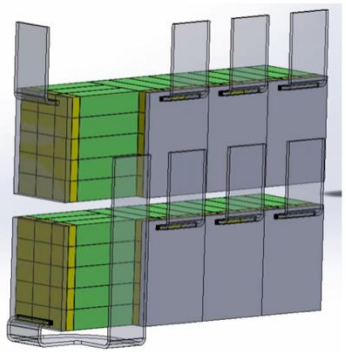
Towards 240 CH readout

- Extension from 32 CH → 120 CH (east) + 120 CH (west)



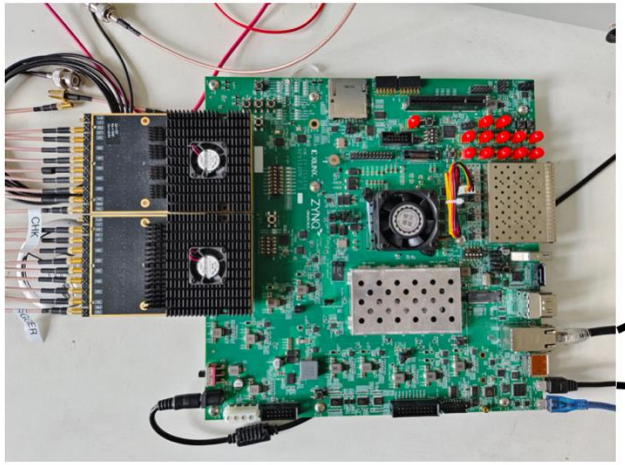
ZDC（east side）

fanout—>120 CH



ZDC（west side）

fanout—>120 CH



ADC board+ZCU102

X 16

Ethernet
X 16

USB-UART X 16

RJ45 to PCIe
network card
X 2

USB expansion dock X 2

Timeline and Outlook

- Timeline
  - 2026: detector engineering stage, installation, backend electronics R&D, commissioning, performance study,
  - 2027: physics study with ISR tagging; and future upgrade, e.g. more compact ASIC based readout

- Plenty of places for extra participants
  - Detector&TDAQ R&D, Sim&Rec software, performance study
  - Physics prospect with ZDC, e.g. ISR, two-photon, new physics…
- Further detector R&D, e.g. diamond, SiC, LGAD, etc
  - Once effect Trigger&DAQ with at BESIII developed, the forward region could be a great place for novel detector R&D, e.g. radiation hard diamond, silicon detector, etc.

The end

BESIII-ZDC team

- Nanjing University
  - Lei Zhang, Liangliang Han, Shenjian Chen, + 4-5 PhD students
  - Detector design, sim.&rec. software, detector unit R&D, Backend & Readout electronics, Energy measurement system, …
- IHEP
  - Xiao Cai, Fei Li, Jingzhou Zhao, Sheng Dong
  - Frontend electronics, Luminosity system, Trigger&DAQ global system
- Close collaborators
  - Tianjun Li (HNU), Xiaoshuai Qin (SDU), Xiaolin Kang (CUG), ……
- More collaboration are welcome!

In line with future projects in China

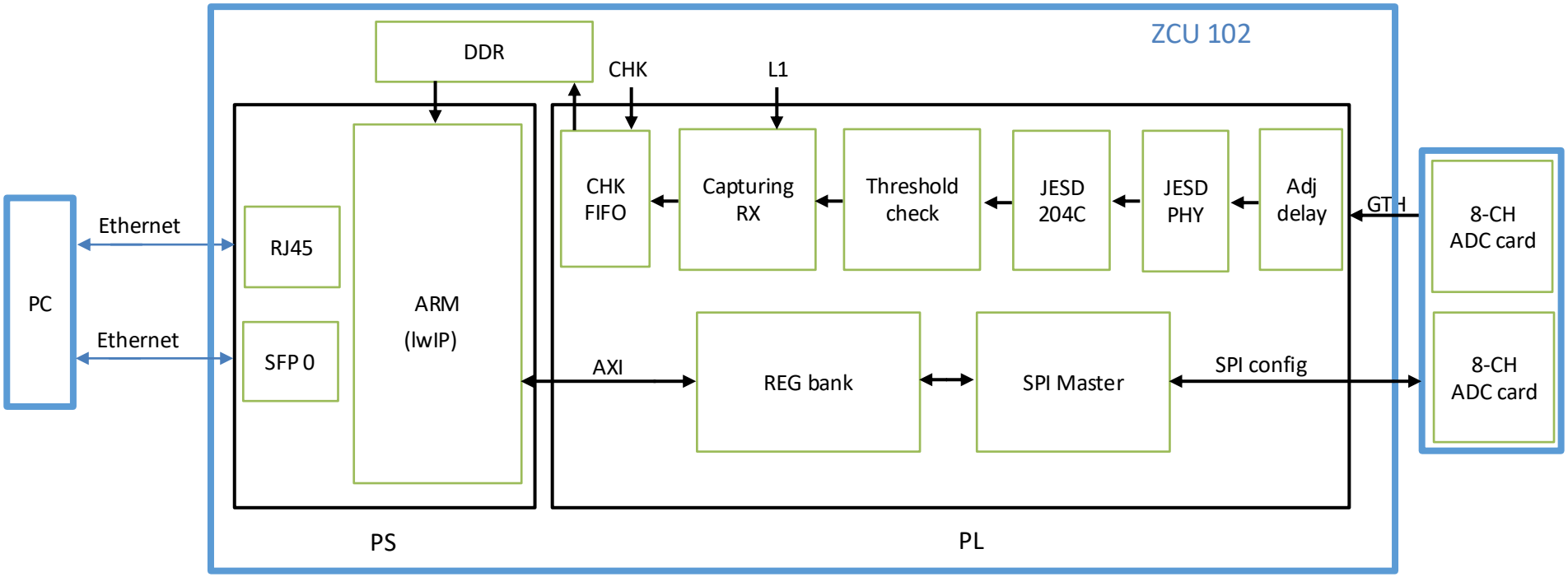
- CEPC
  - EM calorimeter: BGO+SiPM
  - Hadronic calorimeter: Glass+SiPM
  - LumiCal: LYSO+SiPM

- STCF
  - EM calorimeter: pCsI+APD
  - Muon: Scint.+WLS+SiPM (one of two options)

- LYSO crystal and SiPM
  - Quality & Yield improved significantly over recent years
- BESIII Zero Degree Calorimeter
  - A great platform for the future projects R&D

Firmware

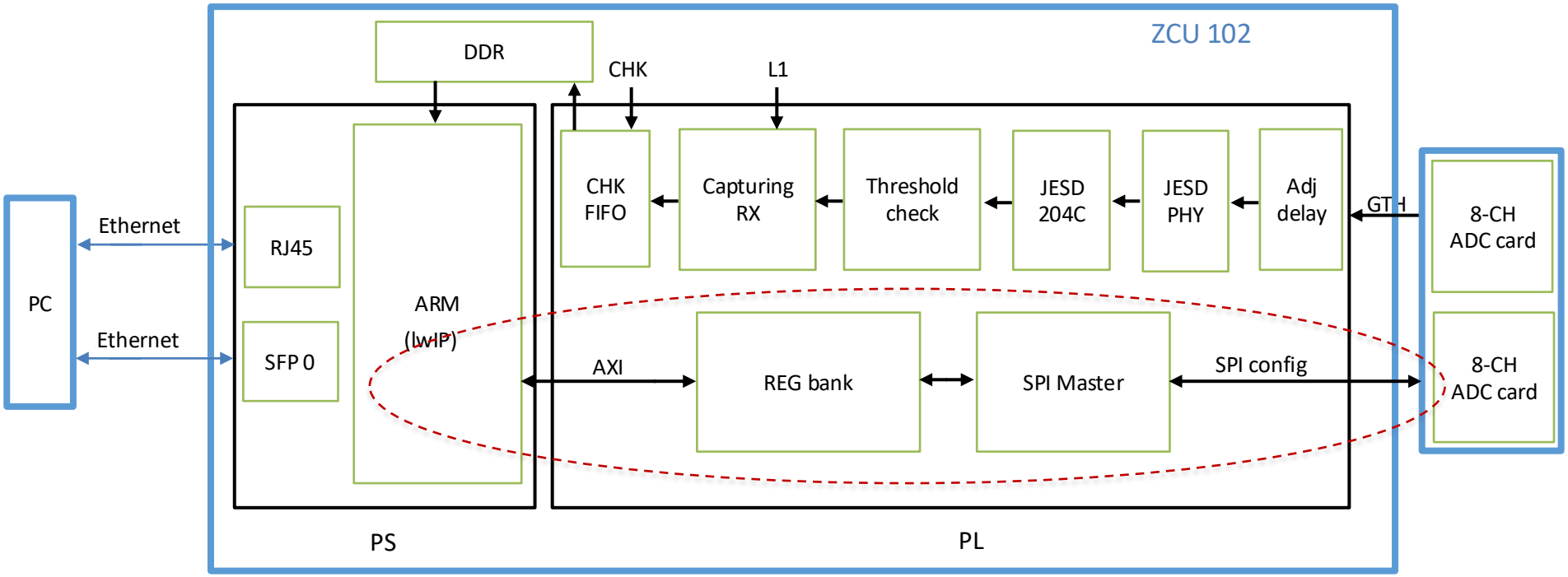
Overview



- The **data link** is used to transmit waveform data, which is finally transferred out through an Ethernet cables
- The **slow-control link** is used to configure the ADC chips via the SPI protocol.

Firmware

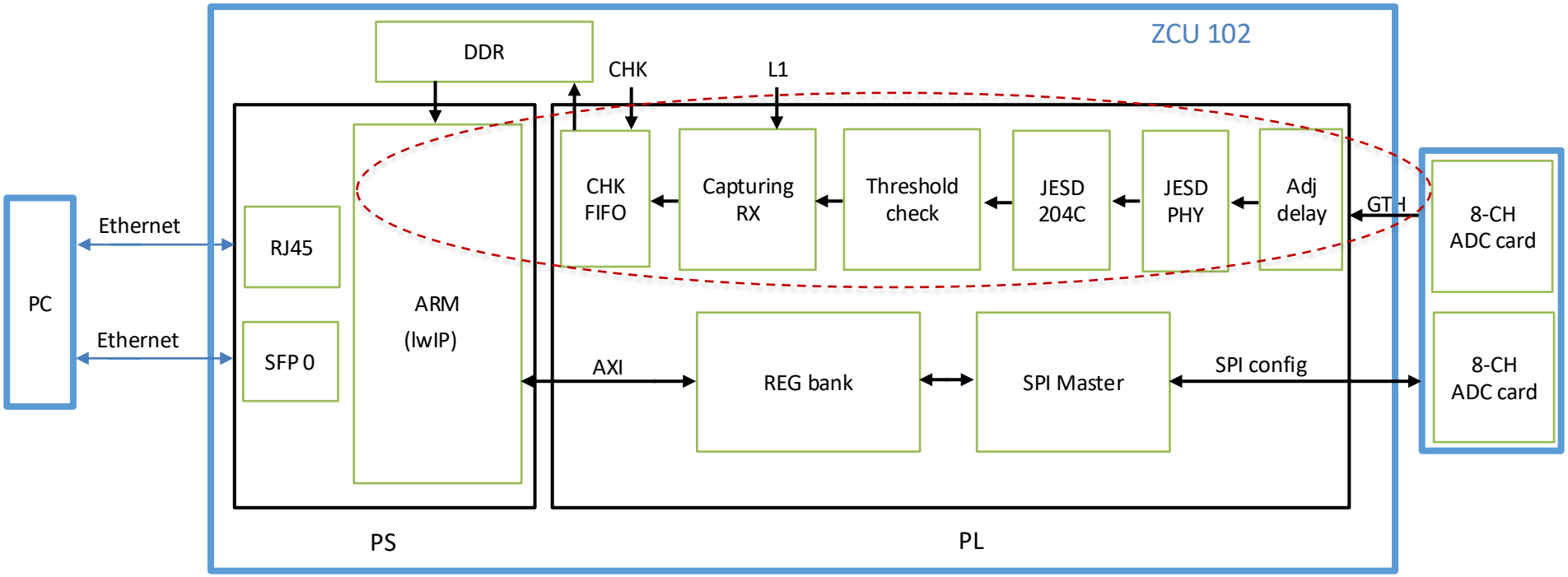
Slow-control link



- The ARM core controls the master SPI through the AXI bus, which further configures the ADC and clock chips
- The register layer supports readback functionality, enabling on-site verification of whether the configuration has been correctly applied.

Firmware

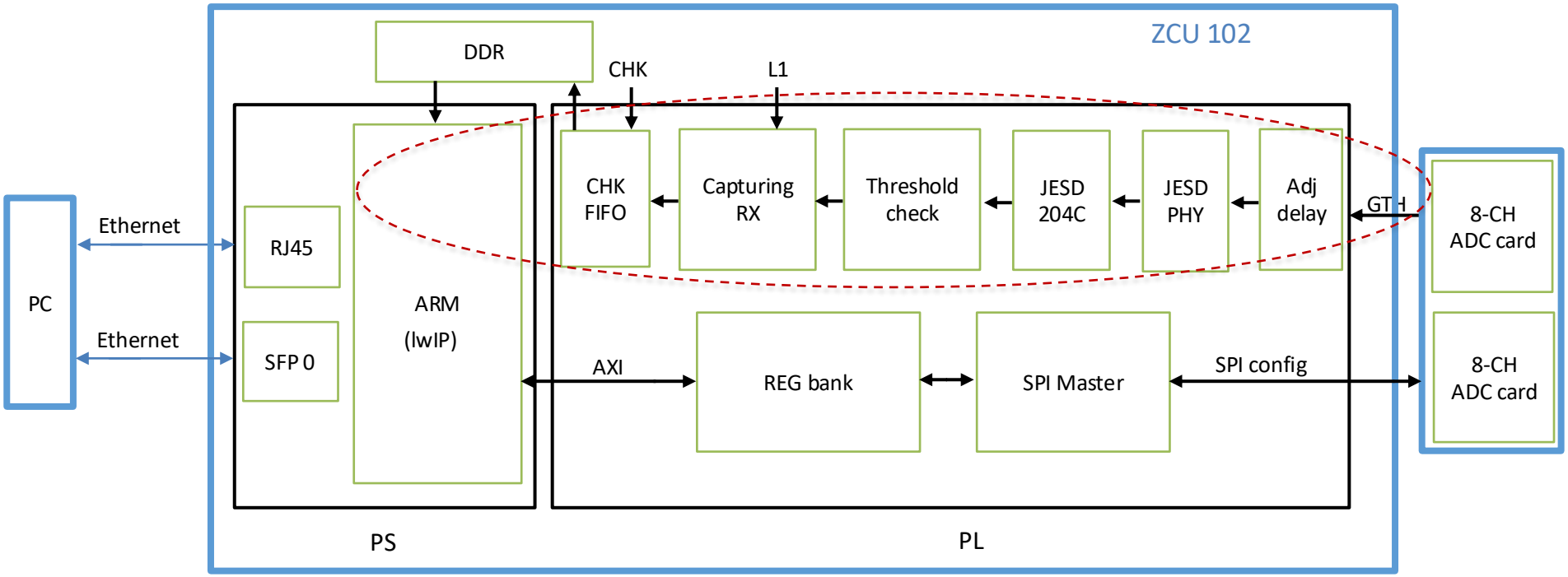
Data link



- The **PL side** performs JESD data reception, trigger alignment, event buffering, and DDR writing
- The **PS side** is responsible for slow control and network data transmission, with jumbo frames used to reduce network packet overhead.

Firmware

Data link

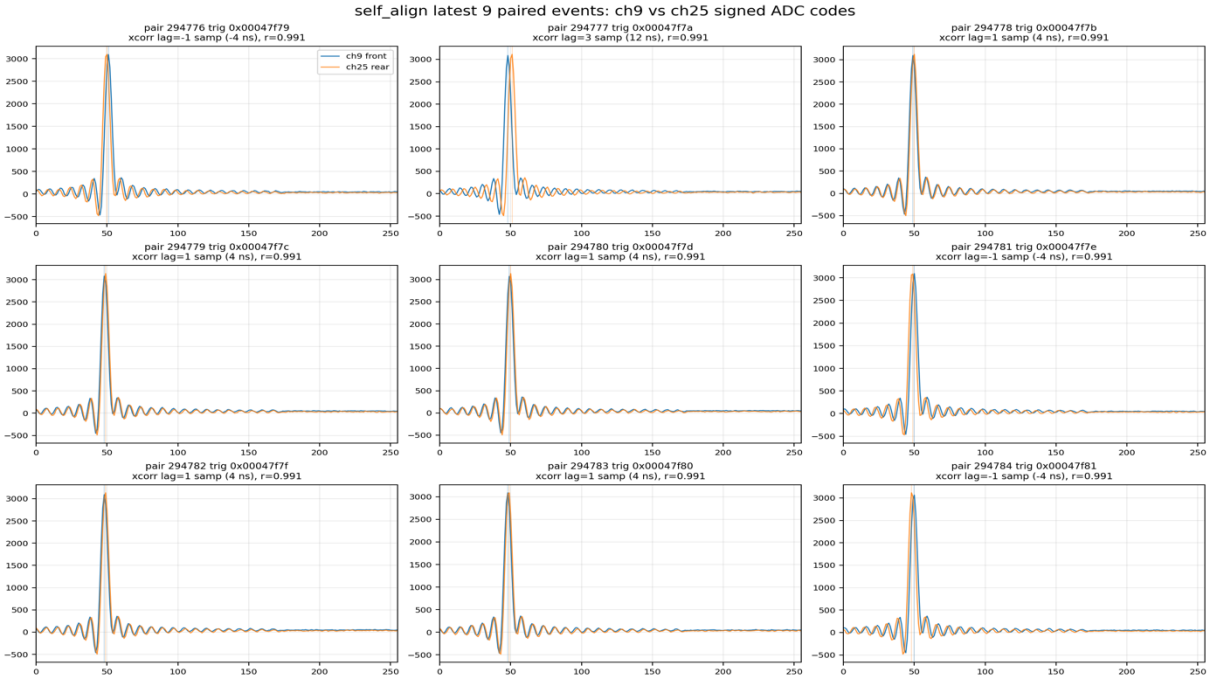


- **Data throughput:** At an L1 trigger rate of ~4 kHz, each triggered event contains 8192 bytes of waveform data, corresponding to a data rate of ~300 Mbps per Ethernet link.
- In addition, some non-triggered over-threshold waveforms can be transmitted through an additional Ethernet link. (i.e. self-triggering)

Firmware

Data link -- self-triggering function

- The threshold check logic determines whether the input signal exceeds the predefined threshold.
- Event alignment is performed using arrival time information.

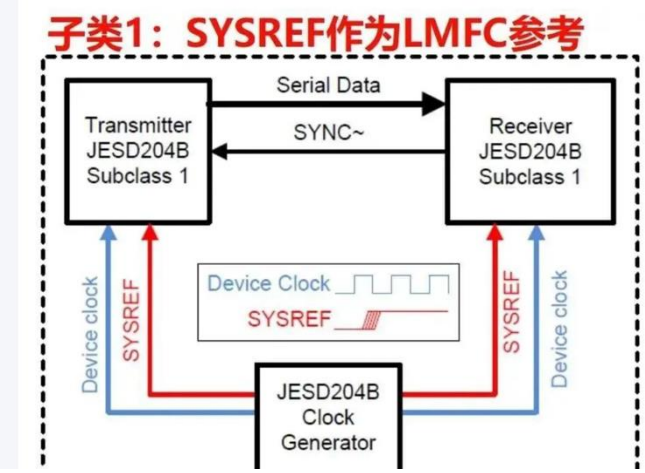


Waveforms from the same event acquired by two FPGAs remain consistently aligned through self-triggering sampling.

Firmware

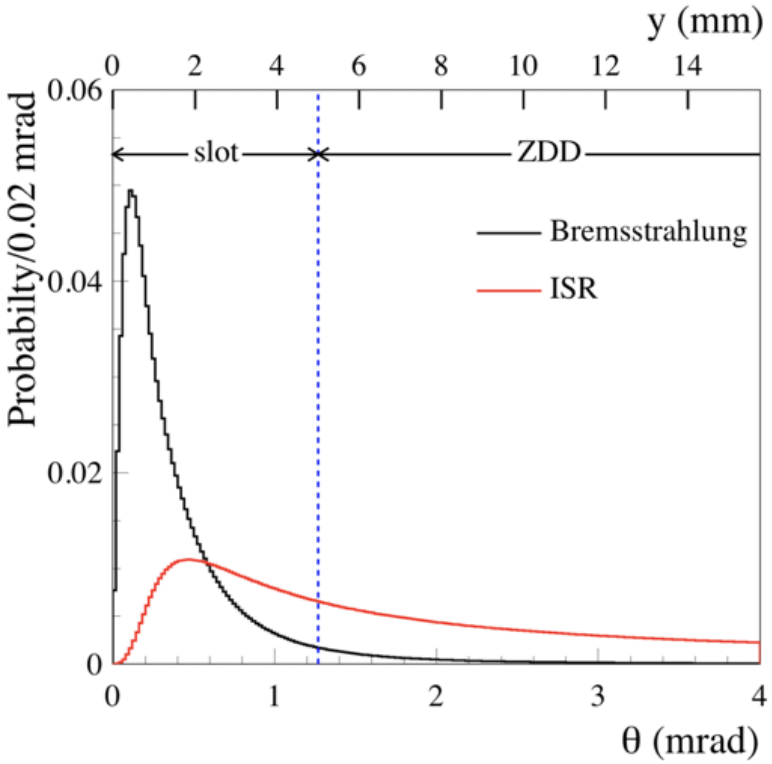
- Data link -- JESD204B interface:
  - JESD204B Subclass 1 is adopted to achieve deterministic multi-channel phase alignment, while maintaining compatibility with Subclass 0.
  - The JESD parameters of the ADC and FPGA are configured consistently. The SYSREF signal is operated in a hardware-requested N-shot mode to ensure stable operation during CGS, ILAS, and data transmission phases.
  - The status of each JESD link, including lane errors, PHY clock status, and SYNC status, can be read back by the PS side.

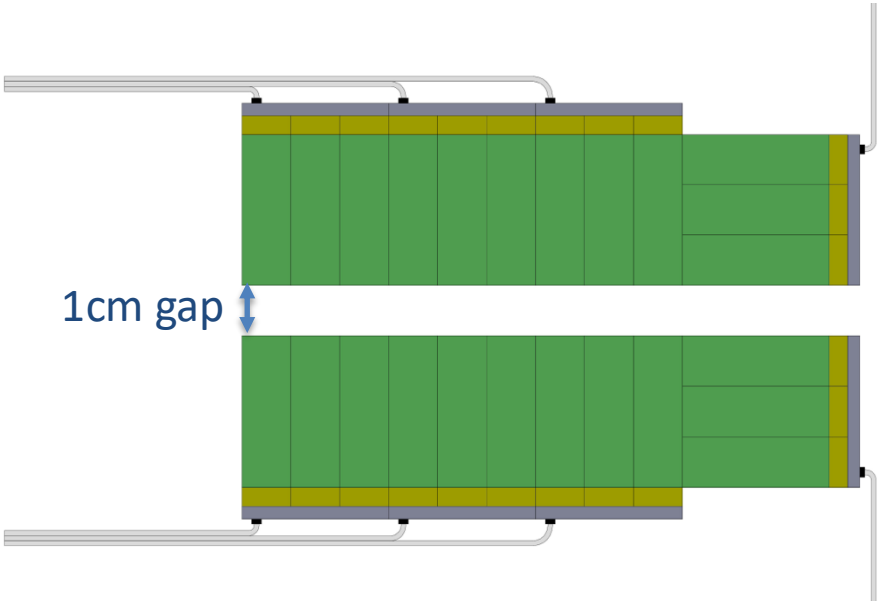
参数	当前配置
L / M / F / S	2 / 2 / 2 / 1
K / N'	32 / 16
Line rate	约 5 Gbps
Device clock	125 MHz
JESD REFCLK	250 MHz
AXI clock	100 MHz



Luminosity measurement physics process

- For ZDC, we count the number of ISR photons
  - Main background: scattered e- and e+ from Bhabha events, Bremsstrahlung photons from Bhabha events
  - Background can be significantly reduced by adjusting ZDC away from the photon-peaked position (~1cm gap)

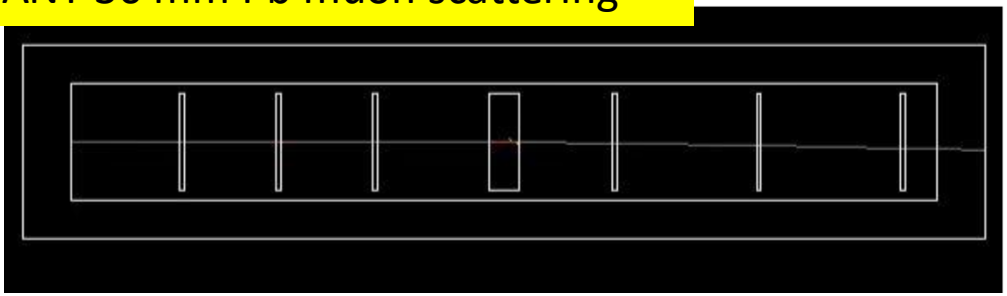


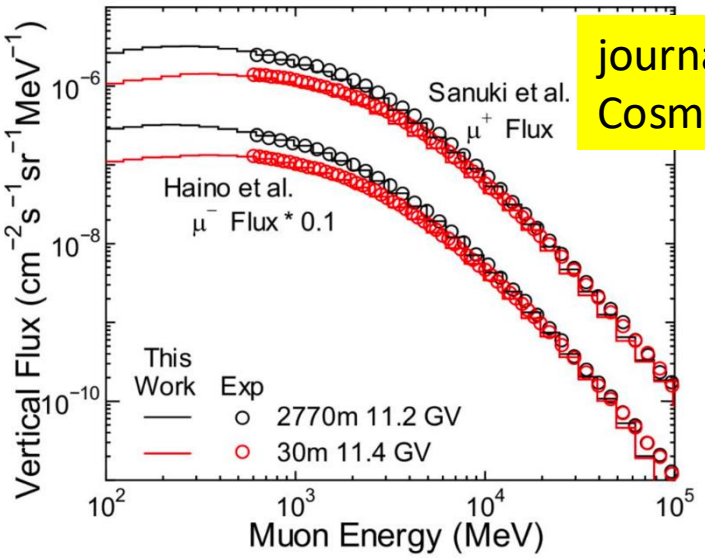


Multiple scattering test at NJU

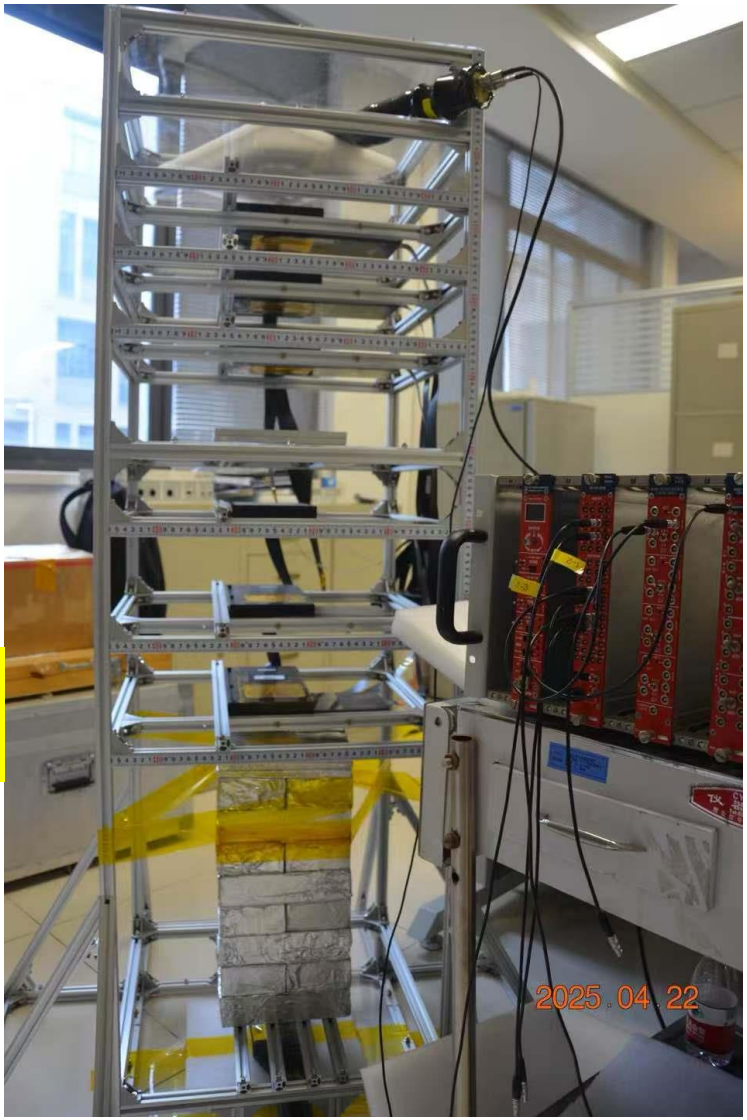
- 12 Si-strip tracker
  - Cosmic ray Muon, > 1 GeV filtered
  - 6 sets (x,y) 200 µm pitch

GEANT 30 mm Pb muon scattering





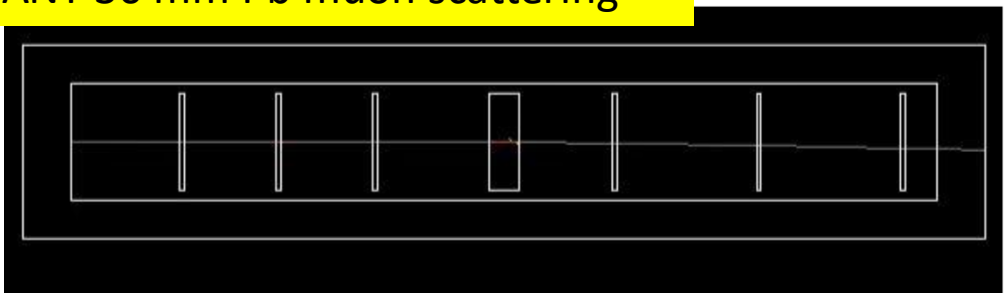
journal.pone.0144679
Cosmic Muon energy

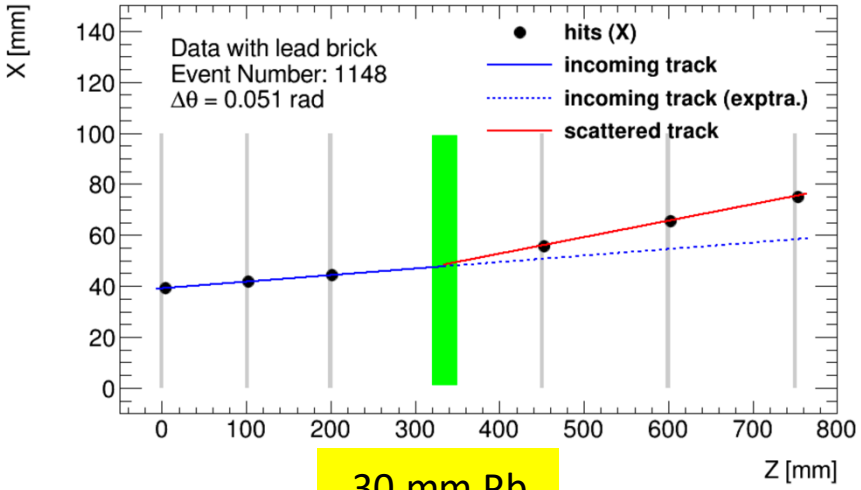


Multiple scattering test

- 12 Si-strip tracker
  - Cosmic ray Muon, > 1 GeV filtered
  - 6 sets (x,y) 200 μm pitch

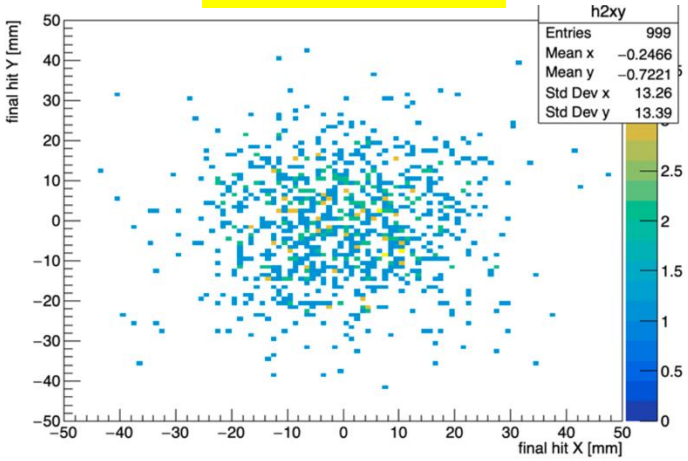
GEANT 30 mm Pb muon scattering



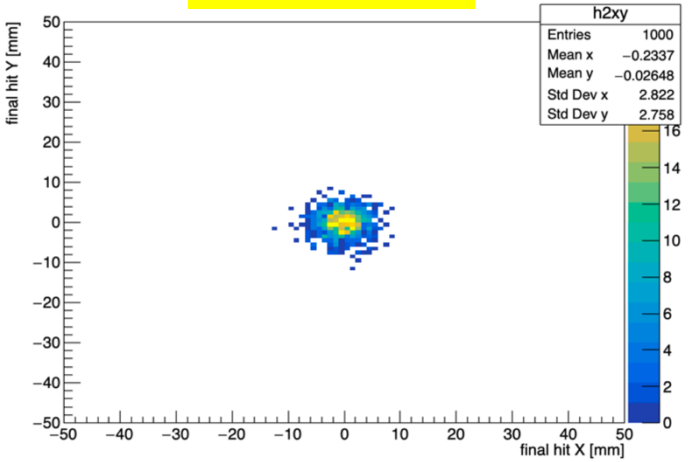


30 mm Pb

1 GeV muon

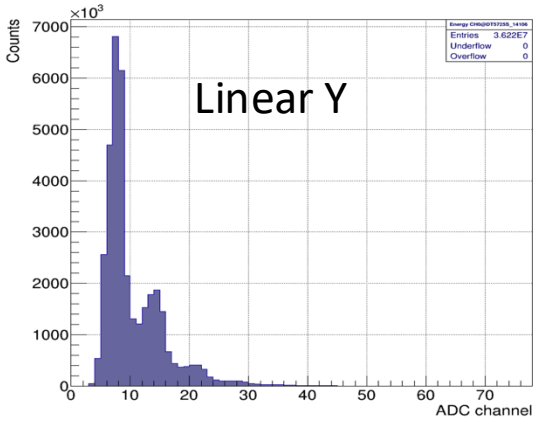


5 GeV muon

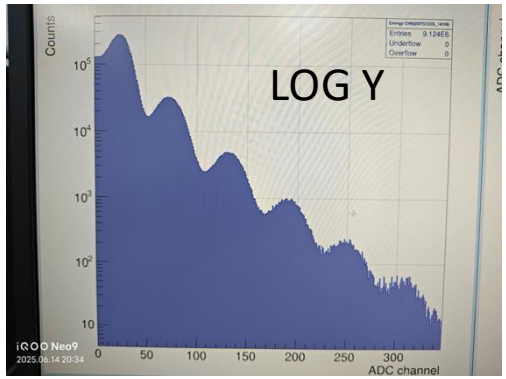


ZDC: detector unit R&D

- Dark noise, five-finger peaks



ADC spectrum

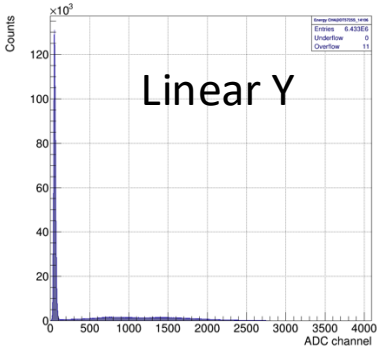


ADC spectrum

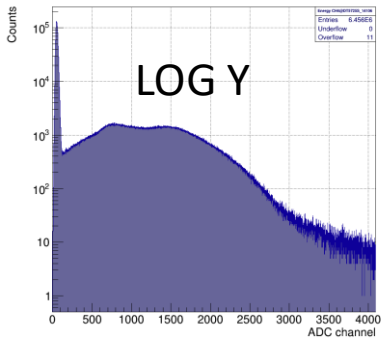
SiPM test in dark box:

- Clear Multiple pixels triggers (五指峰)
- Indicates low noise, high S/B

- LYSO self-radiation



ADC spectrum

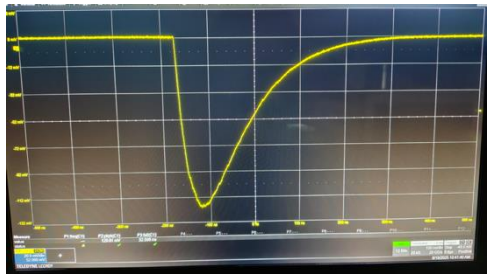


ADC spectrum

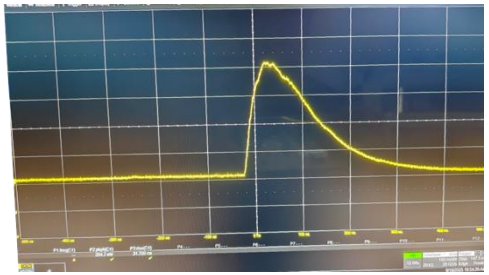
测LYSO+SiPM输出谱→LYSO自辐射谱

- Signal waveform of self-radiation

Onsemi SiPM: 30035, 3mmx3mm, 35um microcell



Directly from SiPM board



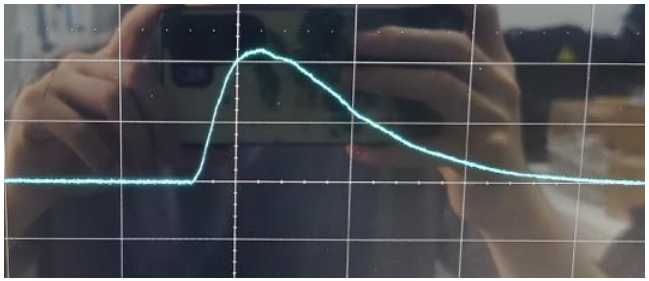
After PreAmp board

一个典型的LYSO自辐射信号波形，~100mV

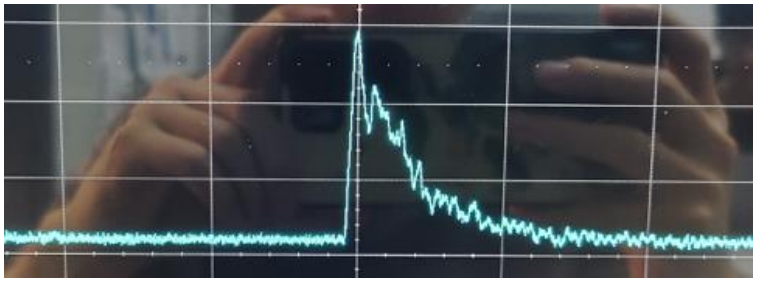
Trade-off between time and energy resolution

- The original SiPM signal can be high-pass filtered for better time performance
  - Pros: sharp edge leads to better time resolution
  - Cons: distorted signal shape makes energy resolution worse

- High-pass filter tuning
  - A capacitor in series with signal input + pre-amp feedback resistor
  - The shape becomes sharp but noisy

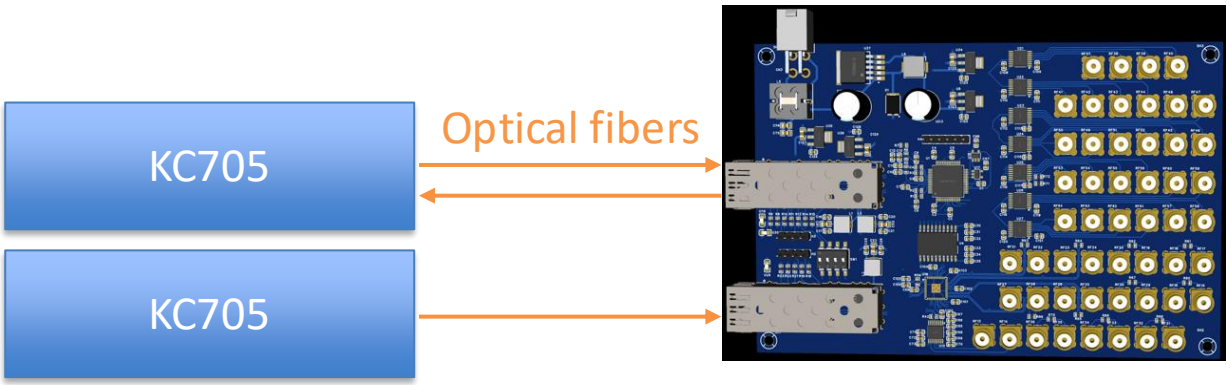


High-pass filtering

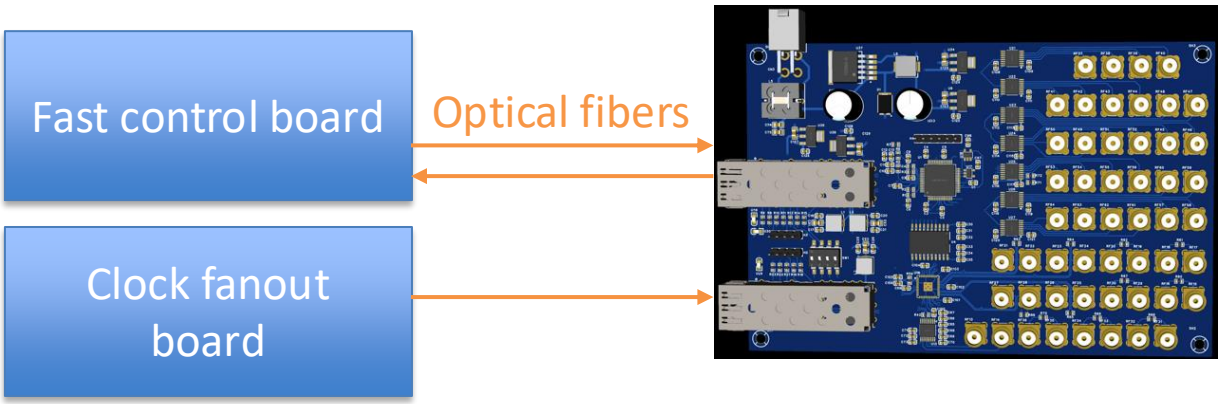


FCDB test plan

- Basic function test with KC705

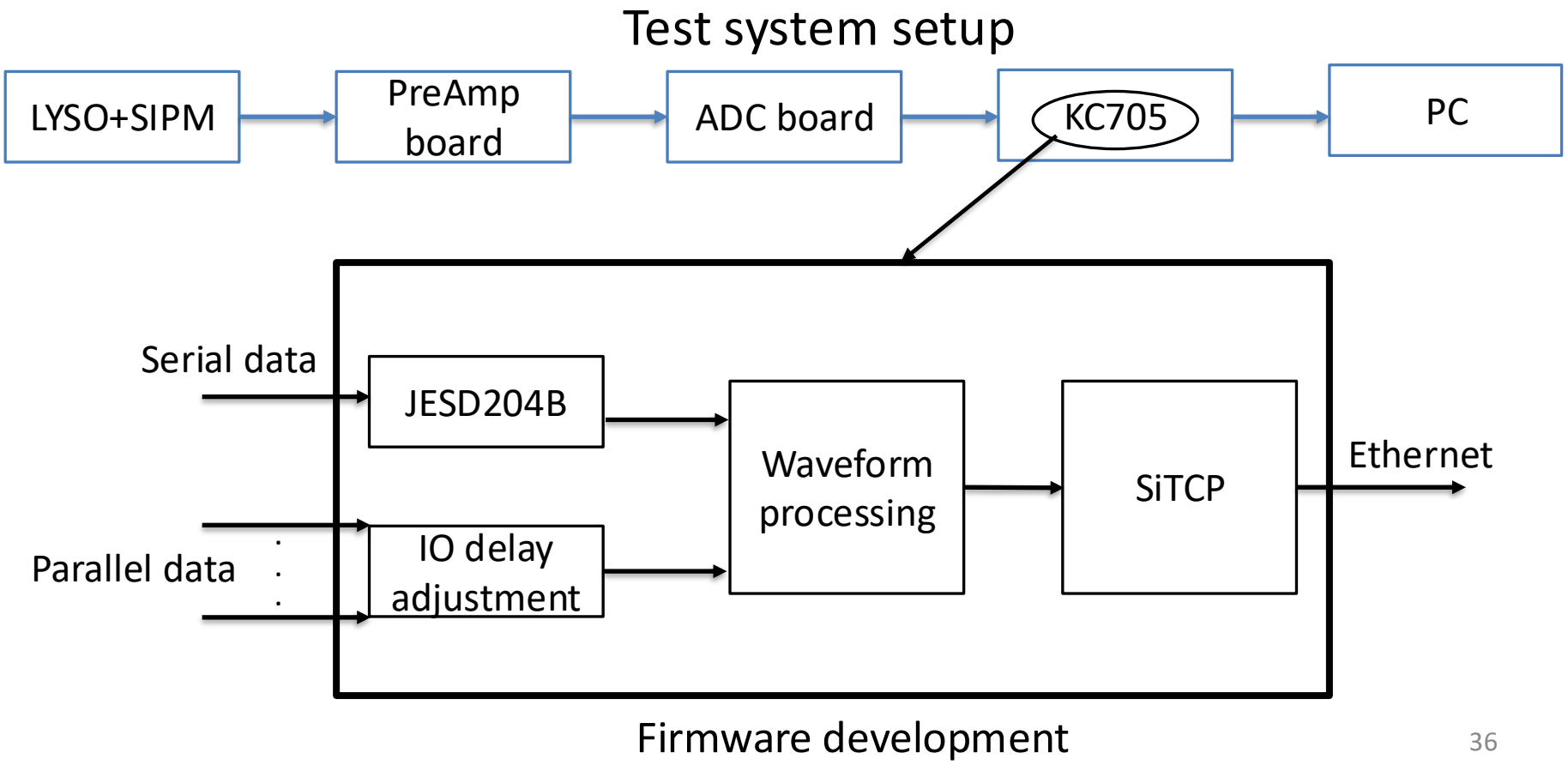


- Test with BESIII fast control board and clock fanout board



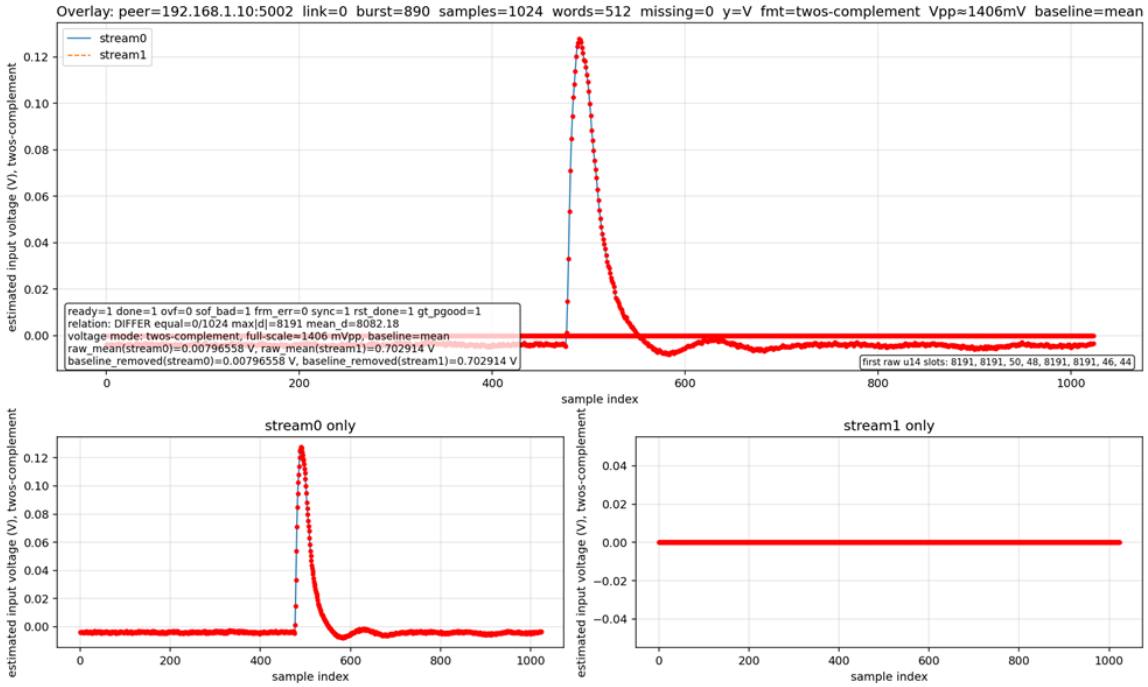
ADC board test plan

- Test with KC705
  - KC705 as the data processing board
  - A dedicated FPGA board will be designed to replace KC705

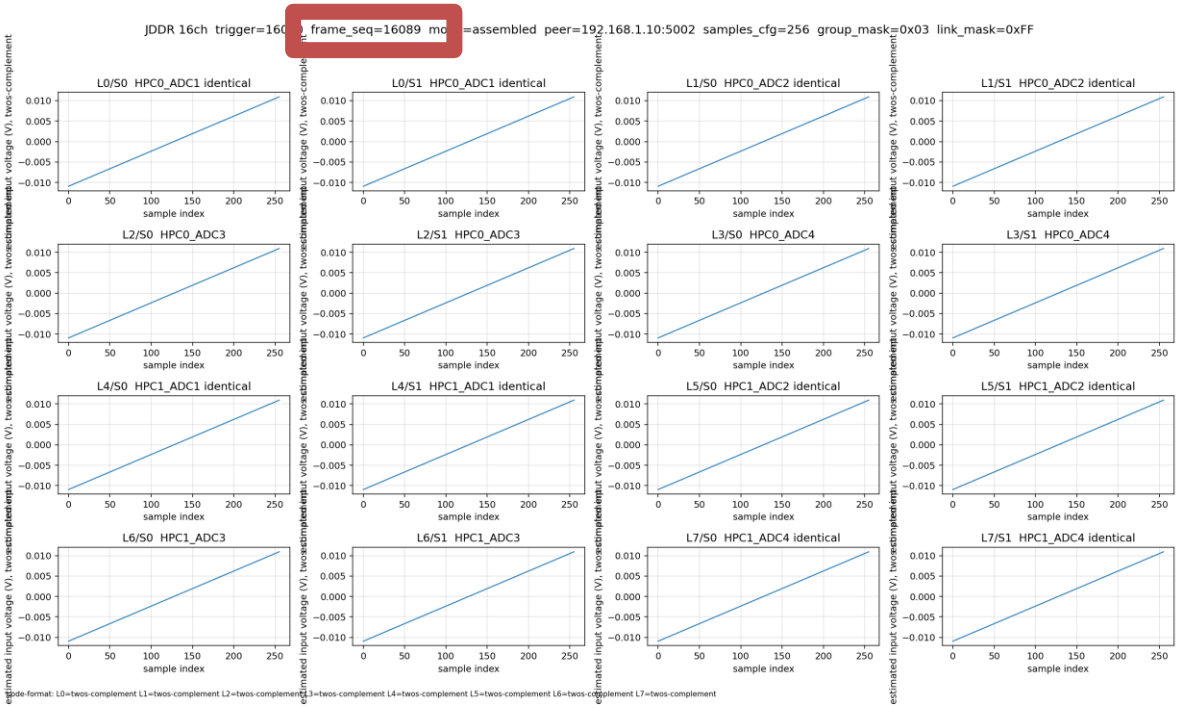


测试结果：探测器信号读出

- 读出单通道小探测器模块信号（SiPM特征波形）　能量积分，波形预处理



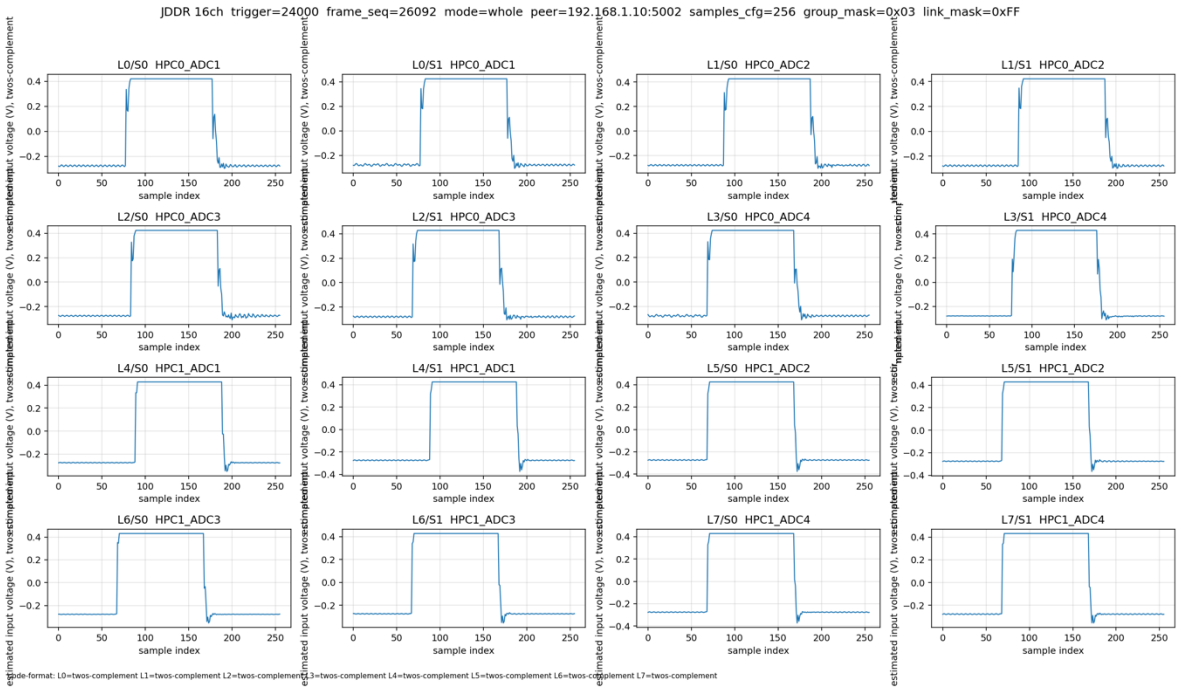
测试结果：16 通道波形读出



PC 端重建的 16 通道波形示例

- 16 通道波形均可在 PC 端重建显示
- 通道顺序、事件编号和采样窗口保持一致
- 结果用于确认 ADC → JESD → PL → PS → PC 全链路连通性
- 当前结果为后续外部触发和系统集成提供基准

测试结果：4 kHz 触发与 6400 ns 延迟



数据的压缩与预处理，降低数据量

- 外部 4 kHz 触发条件下，CHK和与trigger匹配的4KHz16 通道脉冲波形稳定输出
- trigger 相对 波形窗口延迟约 6400 ns，与固件延迟设计一致
- 每触发事件大小：256 samples × 2 bytes × 16 ch = 8192 bytes
- 使用 jumbo frame 后，PL→PS→PC 传输稳定在约 300 Mbps 量级

L1触发延迟

➔ **定义：从对撞发生到L1信号分发到各子探测器的时间**

- 该时间延迟是固定的，6.4us

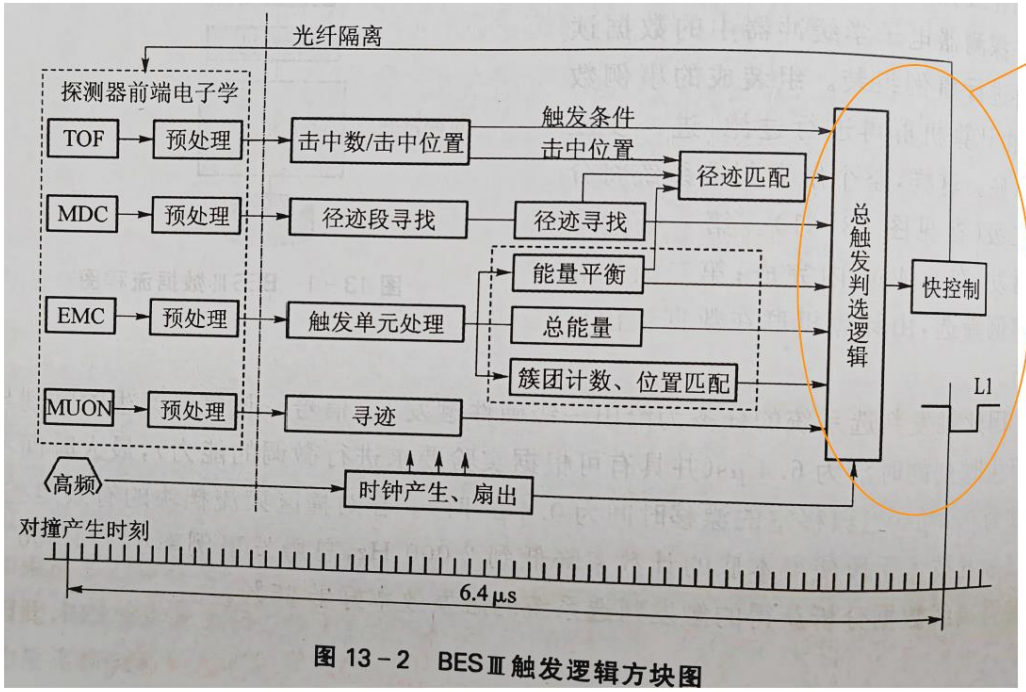


图 13－2　BESⅢ触发逻辑方块图

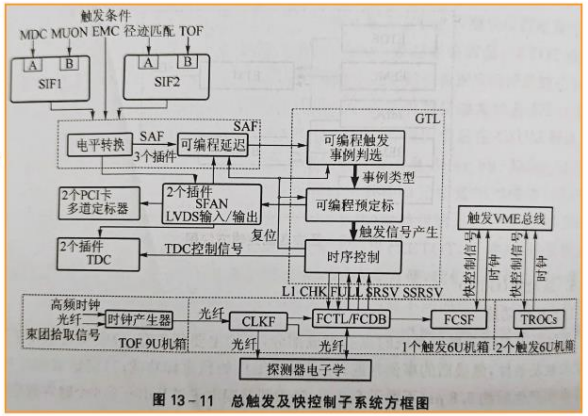


图 13－11　总触发及快控制子系统方框图

8. Level 1 trigger

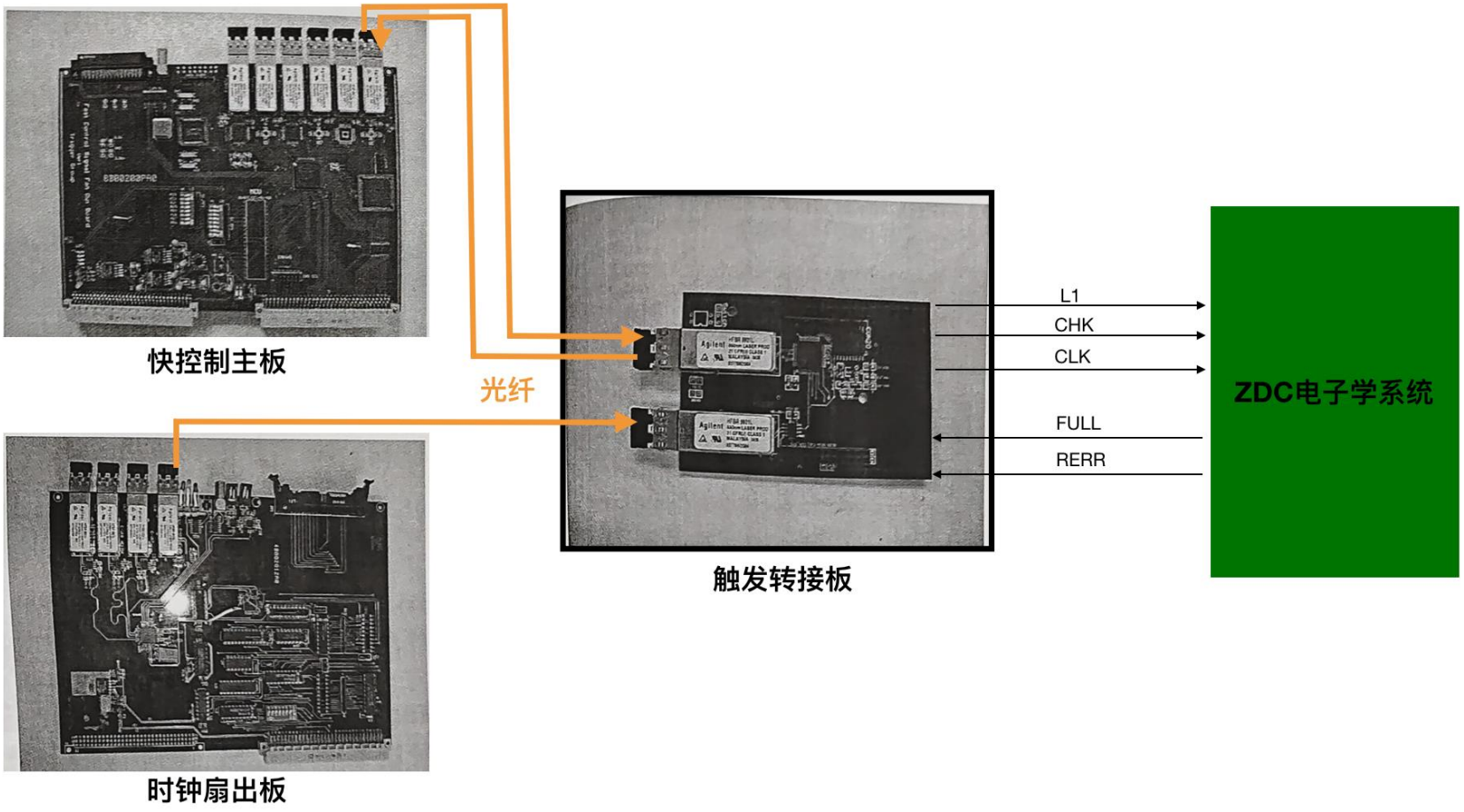
8.1. Overview

8.1.1. Data flow

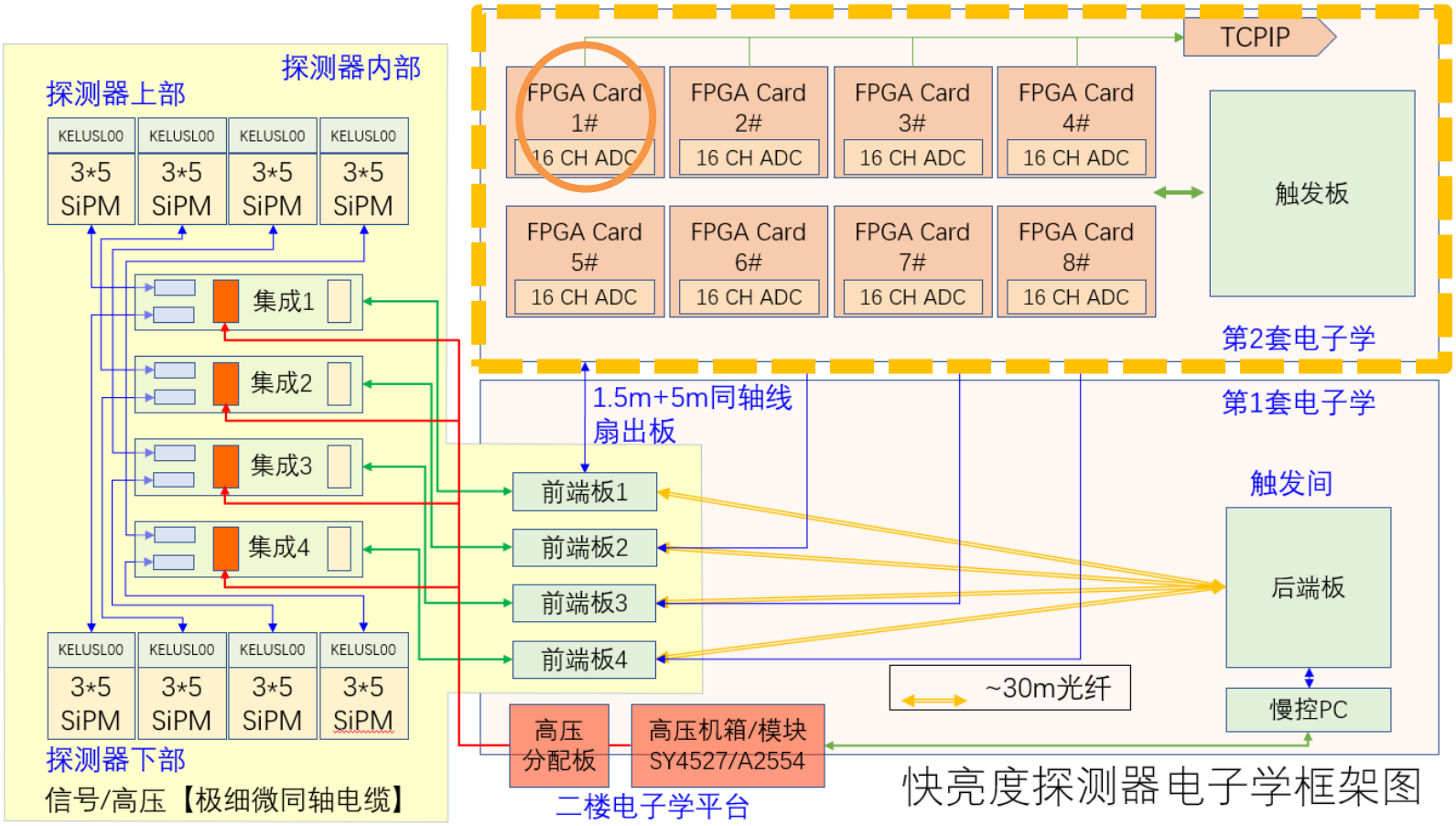
The BESIII trigger system [49] is a two level system consisting of the Level-1 hardware trigger and the Level-3 software trigger (event filter), performed in the online computer farm. The data flow diagram in the BESIII is shown in Fig. 64. The L1 trigger is designed to select good physics events with high efficiency and to reduce the cosmic ray and beam related backgrounds to a level smaller than the 2 kHz physics event rate expected at the J/ψ peak. The maximum L1 trigger rate is designed to be 4 kHz.

The BESIII frond-end electronics and DAQ system are completely pipelined. Data in the front-end buffers are read out once an L1 accept signal is received, 6.4 μs after the collision. Data are transmitted to an online computer farm where event building takes place. The event stream goes through an event filter based

BESIII 子探测器触发和时钟分发



第二套电子学在系统中的位置



Trigger 与 Signal 的时序关系：Matched 与 Miss

Trigger / signal timing: matched events and miss events

4000 trigger/s 与 4010 signal/s 的区别：多数信号有 trigger，少量过阈值信号没有外部 trigger

- 有 trigger 的信号：self_hit + delay 后，外部 trigger 落入 match window，作为 matched event 走 RJ45 主线。
- 无 trigger 的信号：ADC 仍然过阈值，但窗口内没有外部 trigger；该事件进入 miss 路径并通过 SFP0 输出波形。
- 该时序用于解释下一页 4000 trigger/s + 4010 signal/s：4000 个 matched，额外 10 个 miss。

总结

- 硬件：从单FPGA（16 CH）扩展到双FPGA（32 CH）同步读出
- 固件：增加了自触发逻辑、同时传出未经过触发的数据
- 联合测量：事例对齐测量、15通道探测器模块刻度、宇宙线缪子测量与重建、宇宙线缪子入射仿真与对比，证明了该电子学读出方案的可行性！

电子学机械架子：50cm * 60cm * 120cm

后续采购计划

ZCU102：16用2备

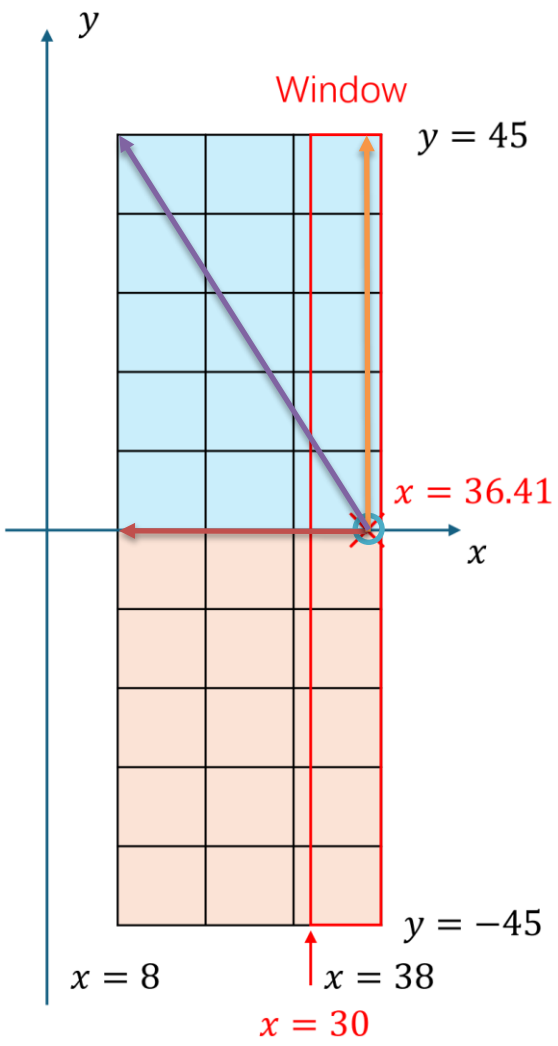
ADC板卡：32用4备

机械架子和面板定制

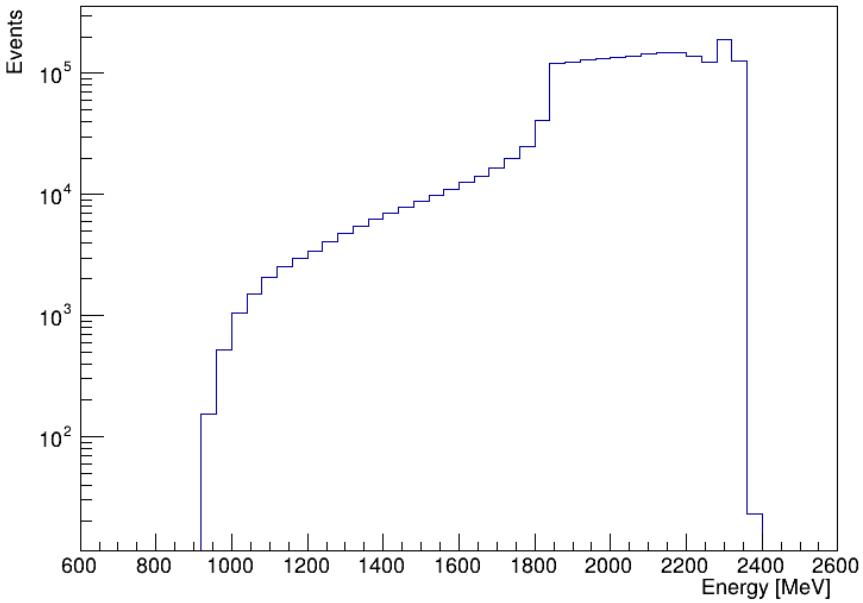
Simulation

- BOSS 8.0.0-pre6, Phokhara
- $e^+e^- \to \gamma_{ISR}\mu^+\mu^-$
  - $\mu^+\mu^-$ $22° < \theta < 158°$
- $\sqrt{s} = 4.68\ GeV$
- 2M events (μ efficiency ~94 % → ~ 1.9 M events)

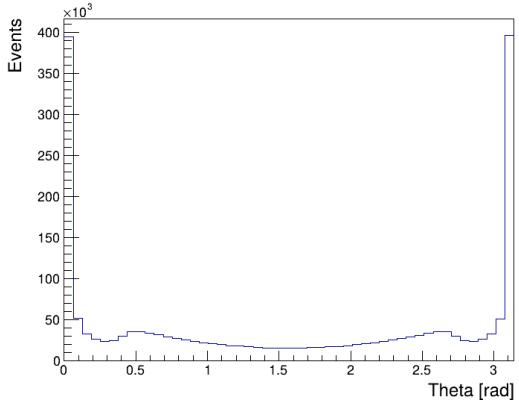
- Detector θ Range
  - $0 \to 0.48\ mrad\ (right)$
  - $0 \to 8.58\ mrad\ (left)$
  - $0 \to 13.6\ mrad\ (top\&bottom)$
  - $0 \to 17.5\ mrad\ (left\ corner)$

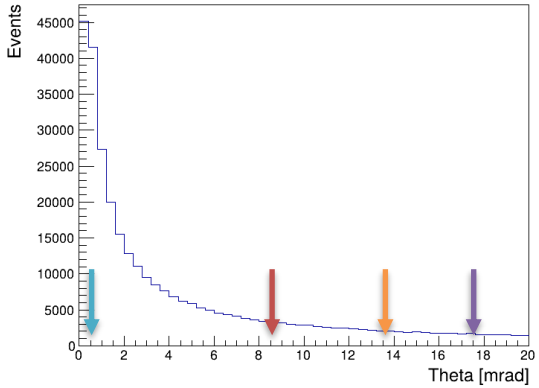


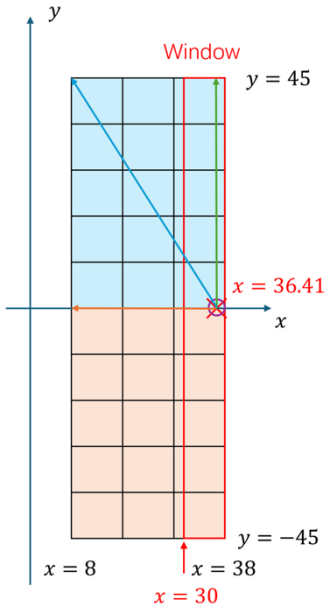
E_γ (truth)



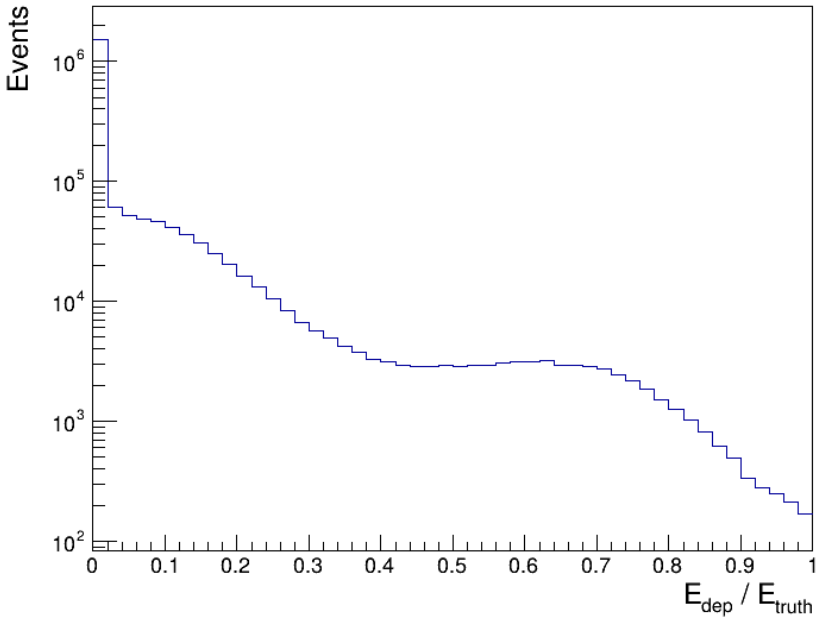
θ distribution (CM frame)



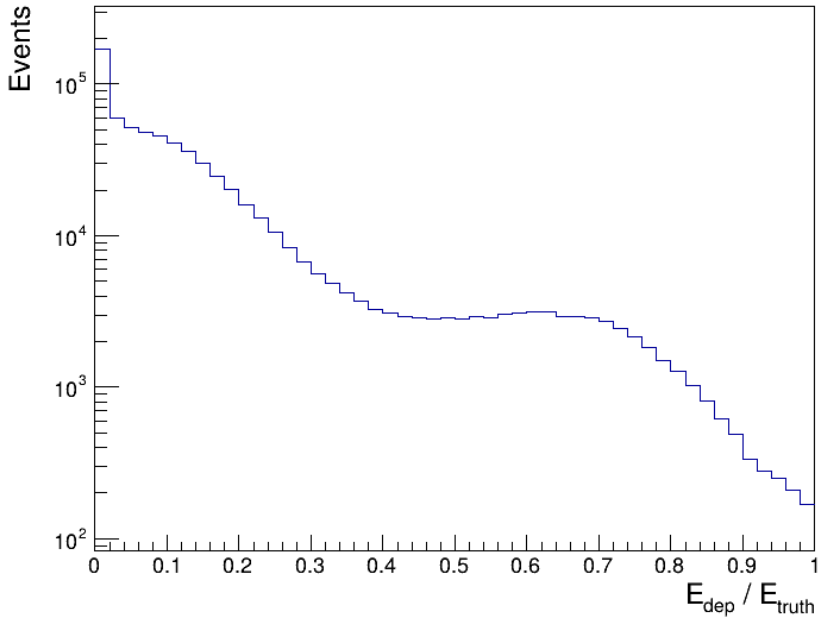




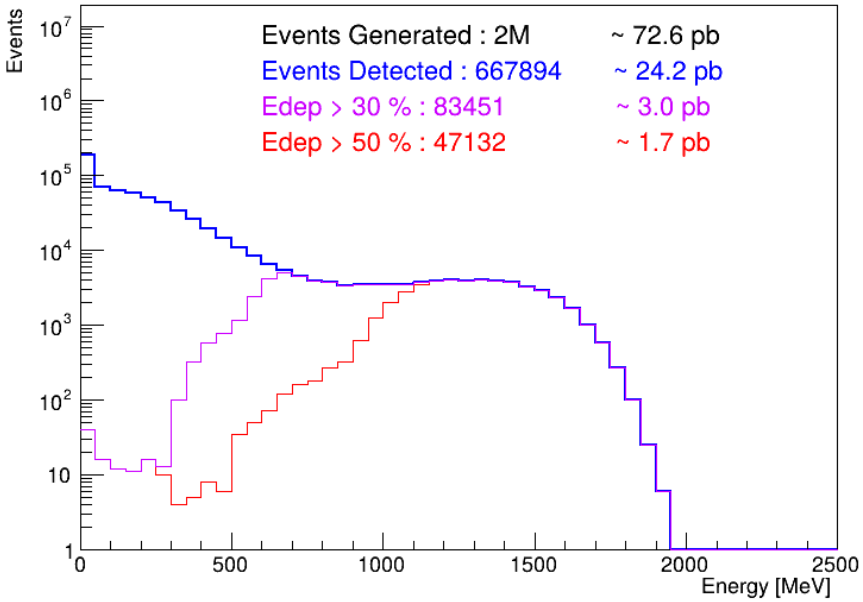
$\frac{E_{dep}}{E_{truth}}$



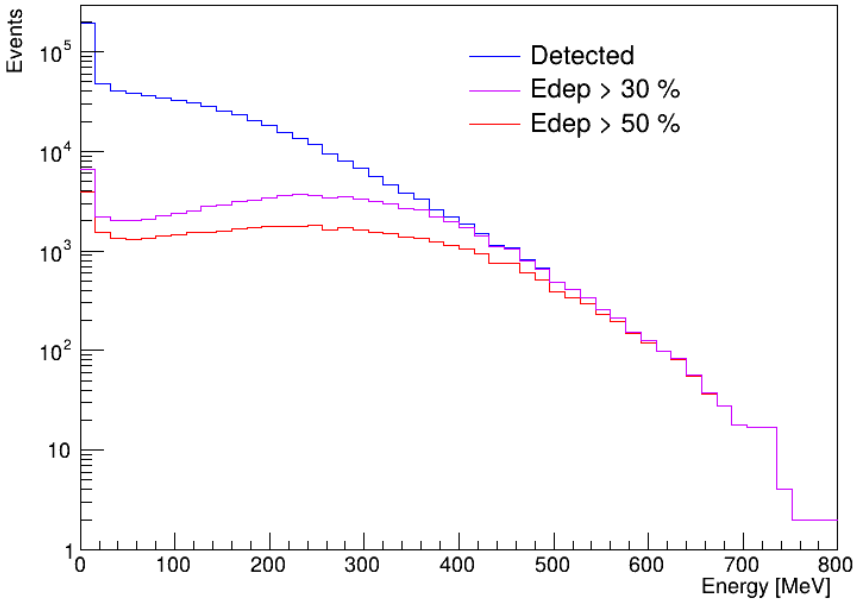
$\frac{E_{dep}}{E_{truth}}$ $(E_{dep} > 0)$

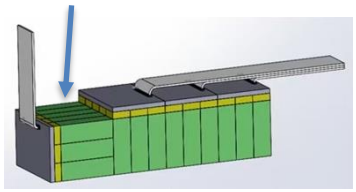


E_{dep} in ZDC

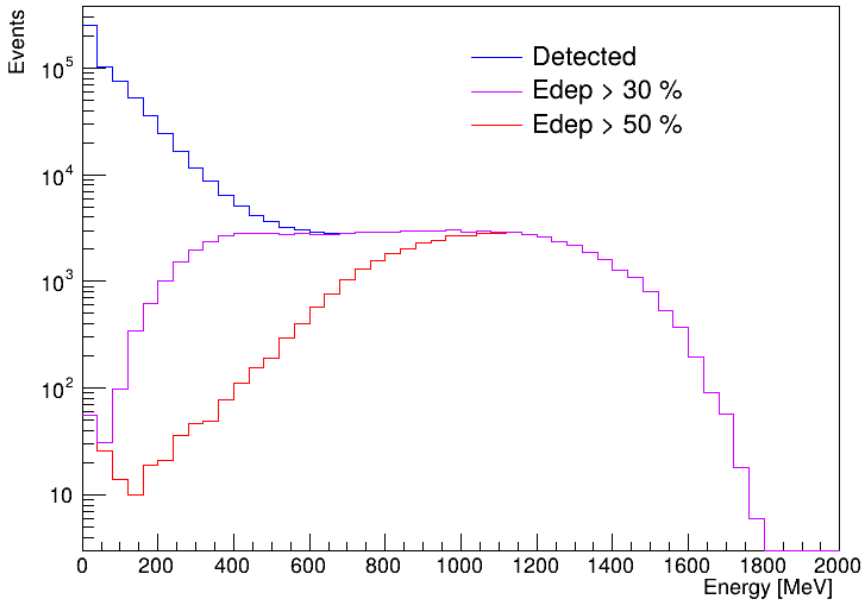


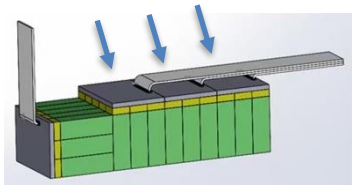
E_{dep} in first section of ZDC
with different total E_{dep}/E_{truth}



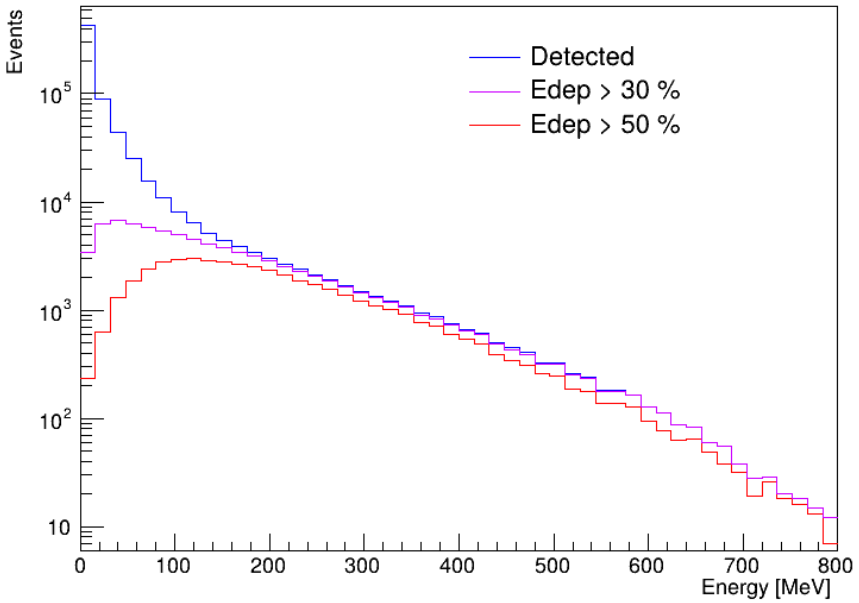


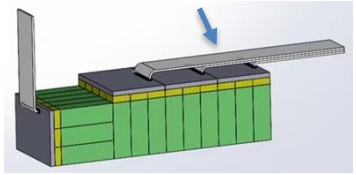
E_{dep} in 2 3 4 section of ZDC
with different total E_{dep}/E_{truth}



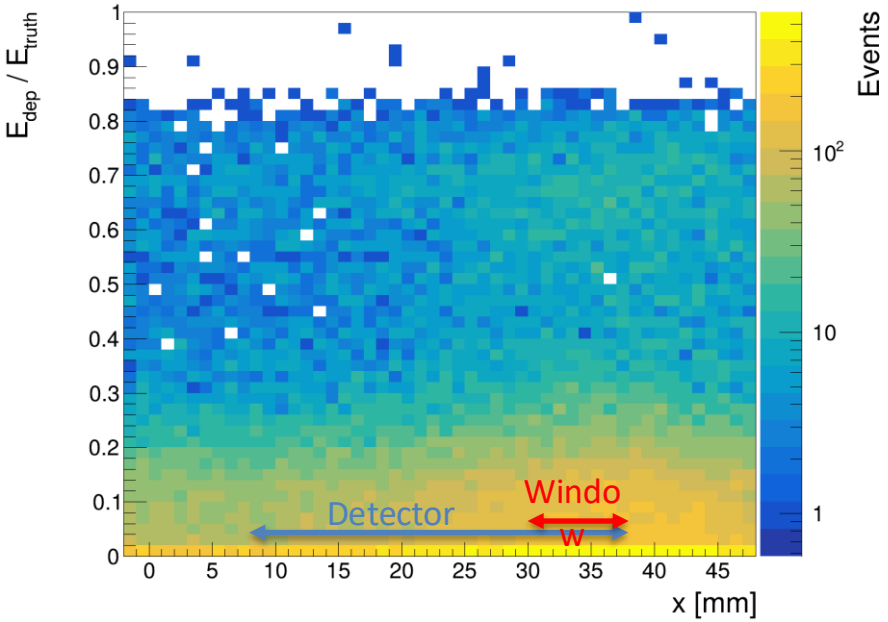


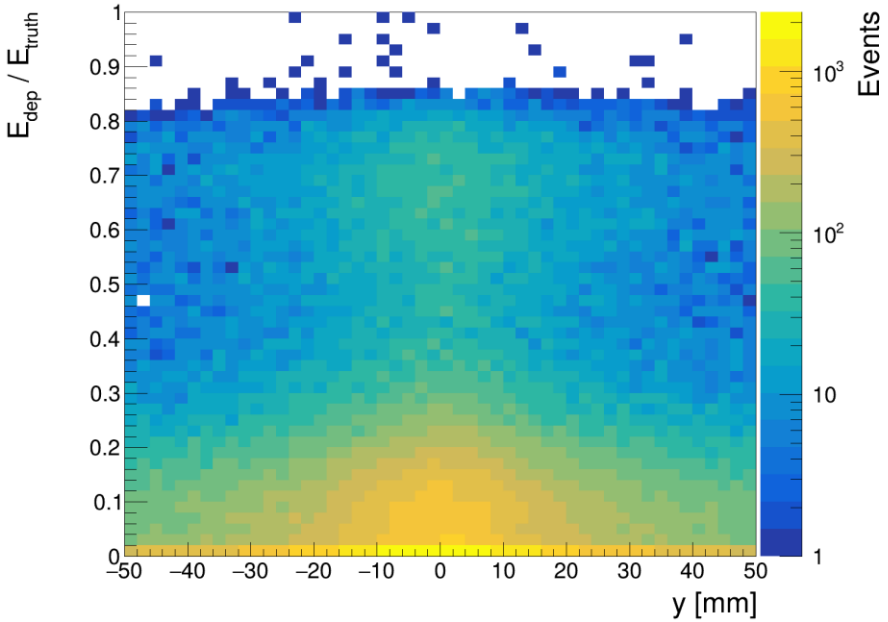
E_{dep} in last section of ZDC
with different total E_{dep}/E_{truth}





$\mu\mu$ recoil

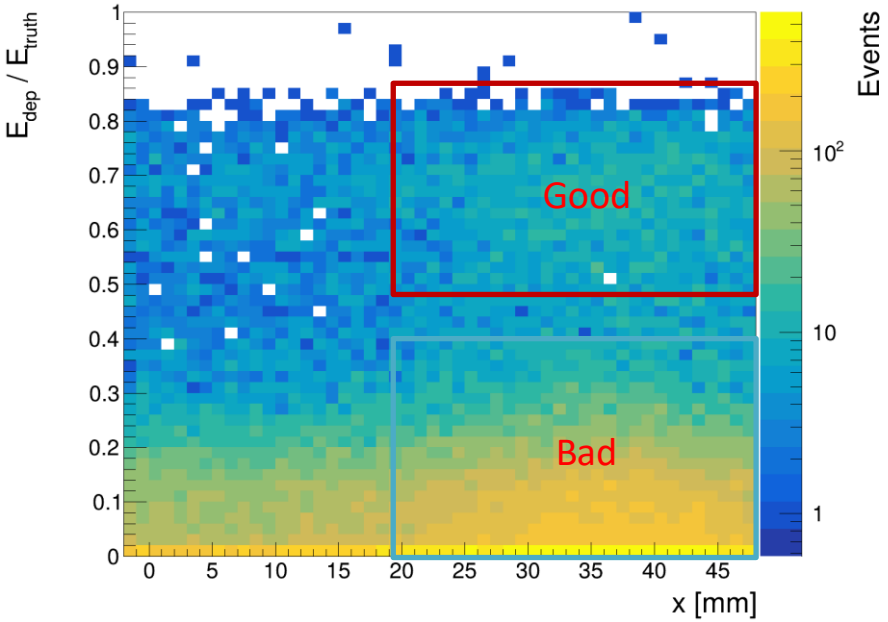


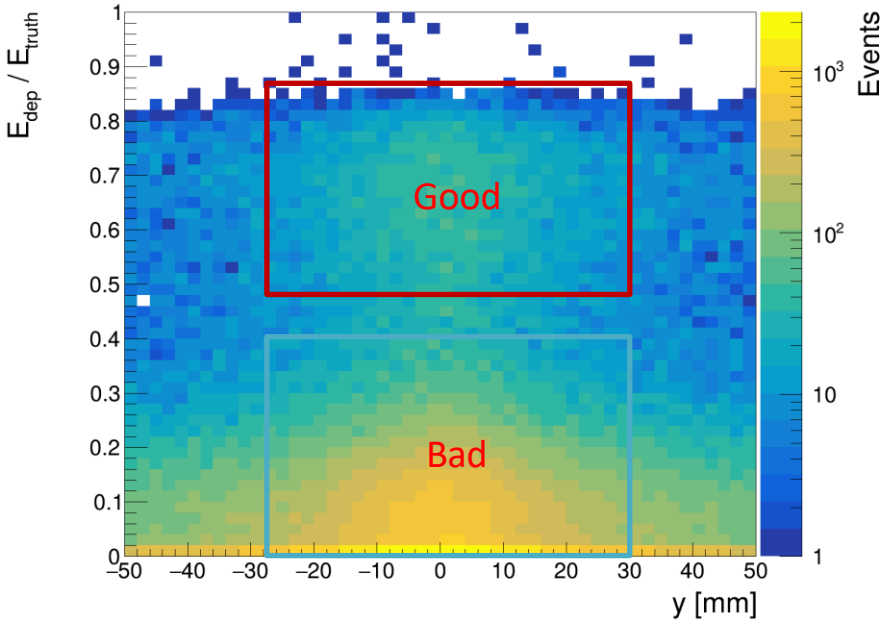


Recoil : $p_\gamma = p_{CM} - p_{\mu^+} - p_{\mu^-}$

$$x = \frac{p_{x(recoil)}}{p_{z(recoil)}} \times 3310\ mm, \qquad y = \frac{p_{y(recoil)}}{p_{z(recoil)}} \times 3310\ mm$$

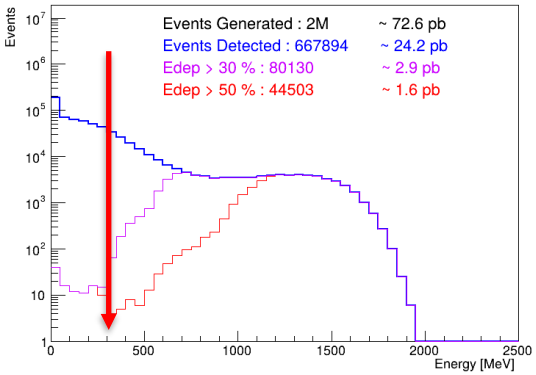
$\mu\mu$ recoil

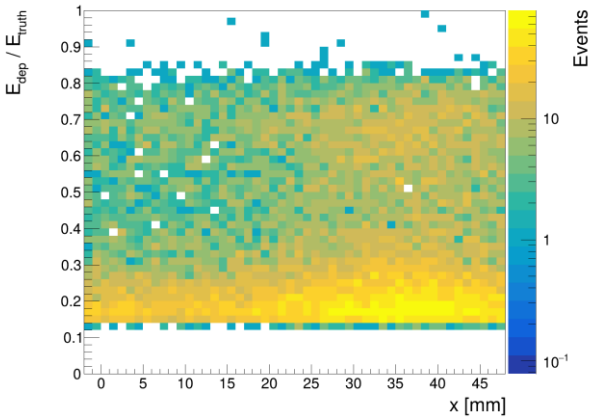


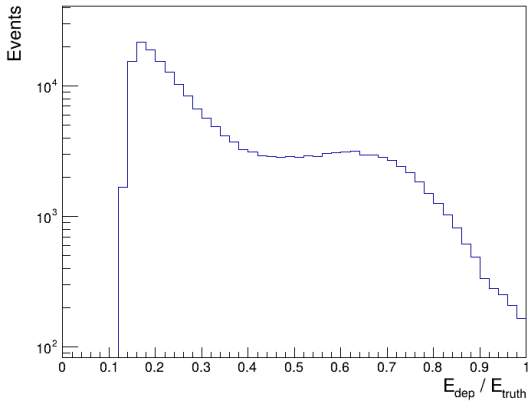


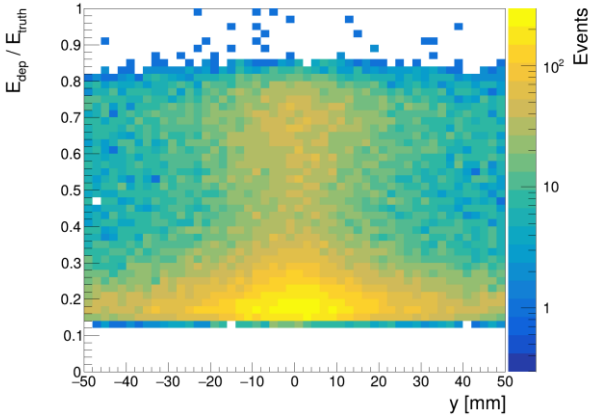
Positions of good events and bad events are the same

Cut 300 MeV

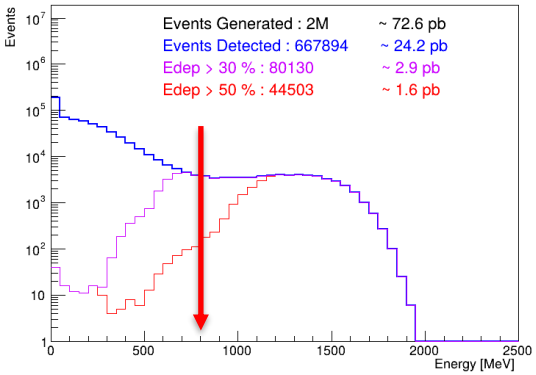

Events
Events Generated : 2M ~ 72.6 pb
Events Detected : 667894 ~ 24.2 pb
Edep > 30 % : 80130 ~ 2.9 pb
Edep > 50 % : 44503 ~ 1.6 pb
Energy [MeV]

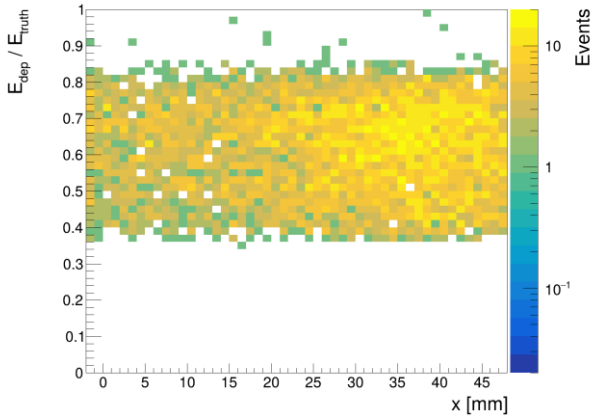

E_dep / E_truth
Events
x [mm]

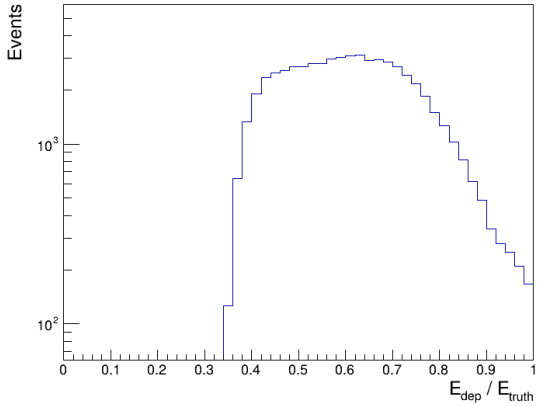

Events
E_dep / E_truth

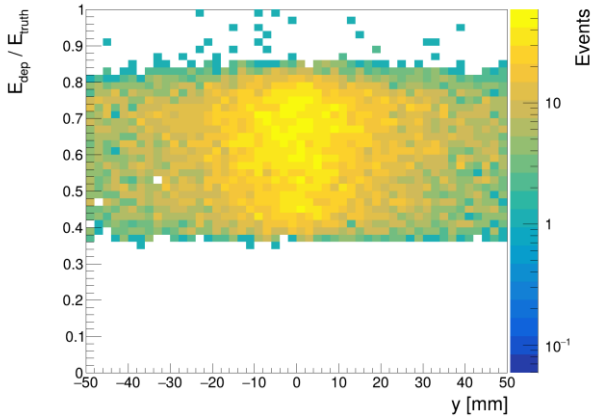

E_dep / E_truth
Events
y [mm]

Cut 800 MeV

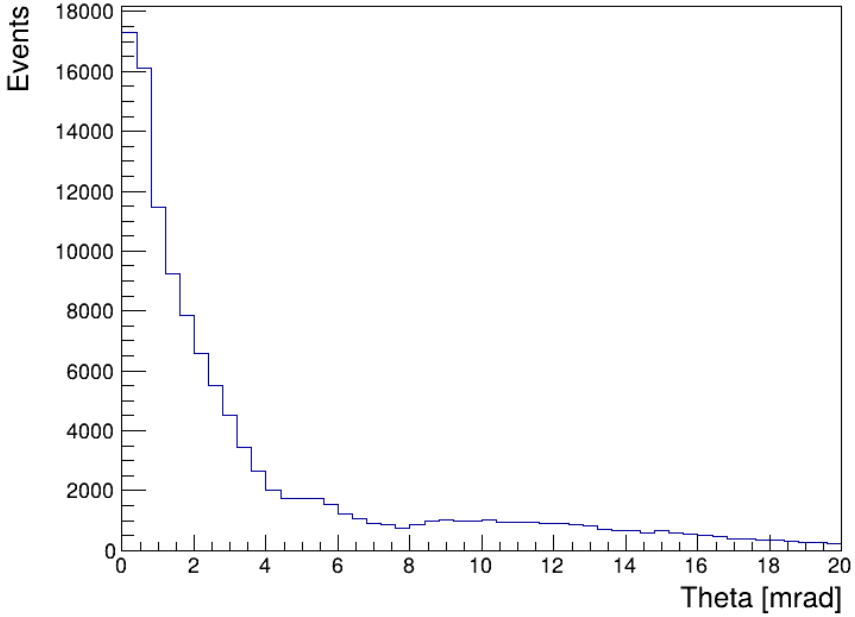

Events Generated : 2M ~ 72.6 pb
Events Detected : 667894 ~ 24.2 pb
Edep > 30 % : 80130 ~ 2.9 pb
Edep > 50 % : 44503 ~ 1.6 pb
Events
Energy [MeV]

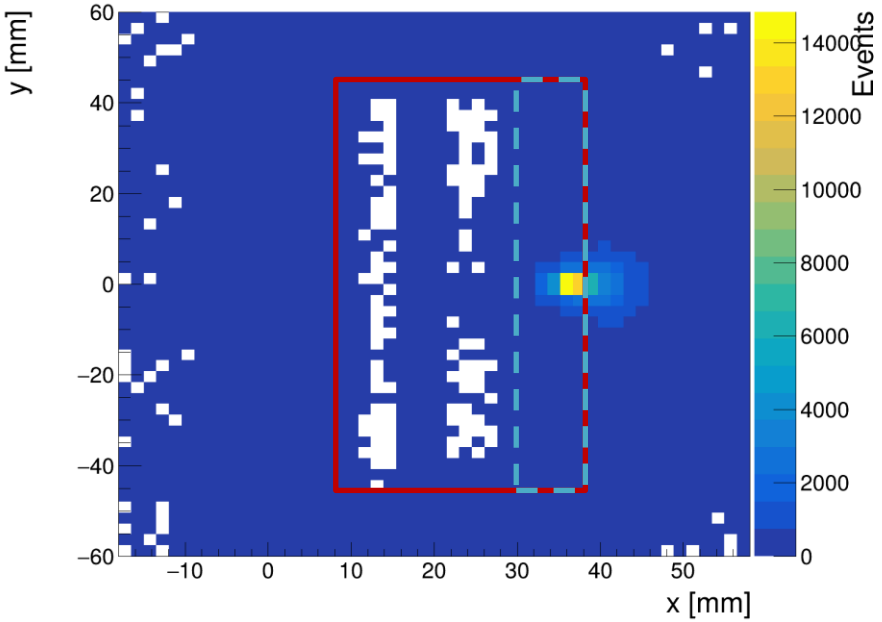

E_dep / E_truth
x [mm]
Events


Events
E_dep / E_truth

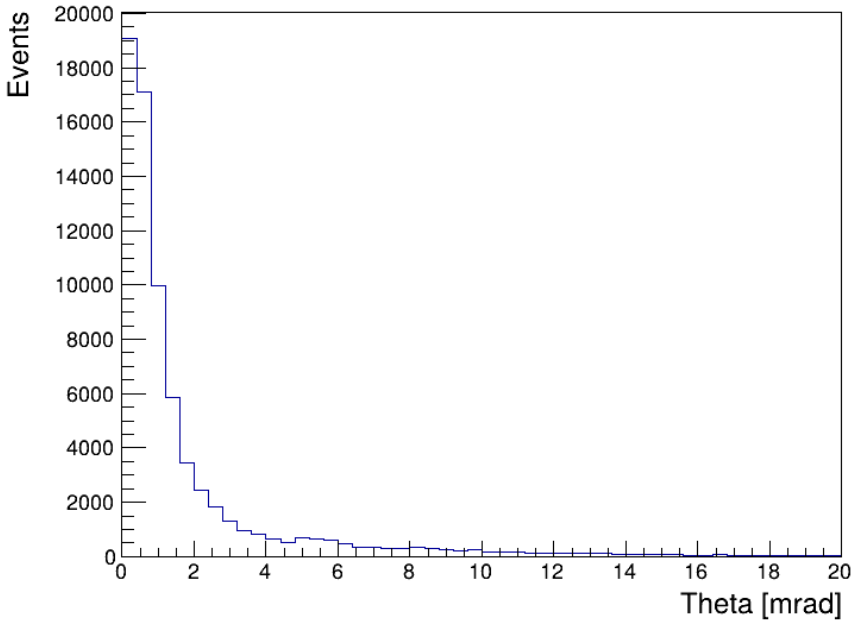

E_dep / E_truth
y [mm]
Events

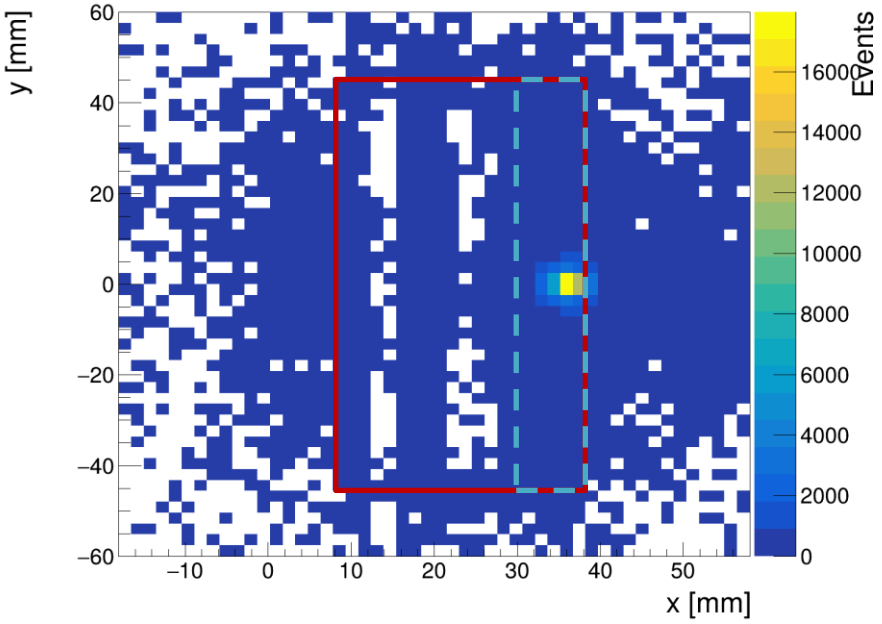
Theta & Position of truth hit, $\frac{E_{dep}}{E_{truth}} < 0.1$



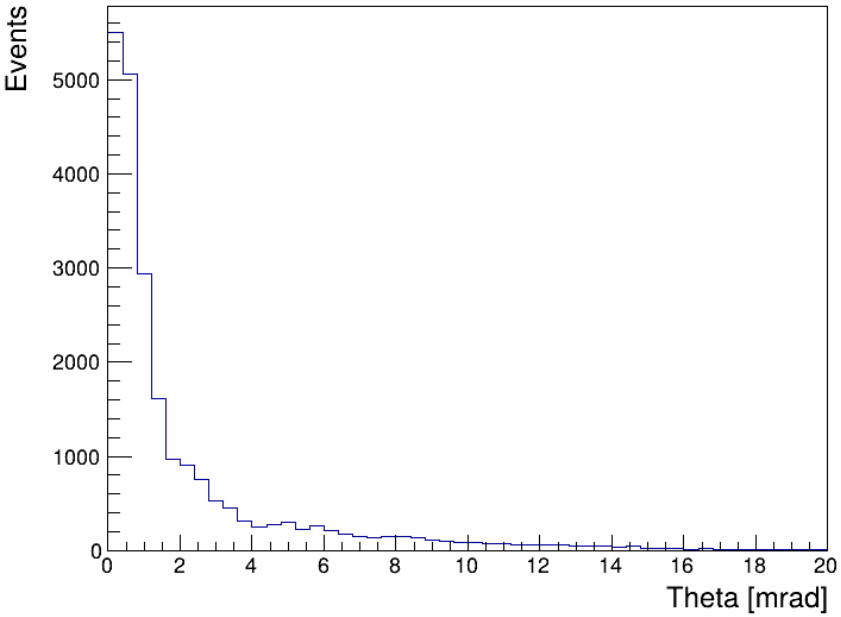


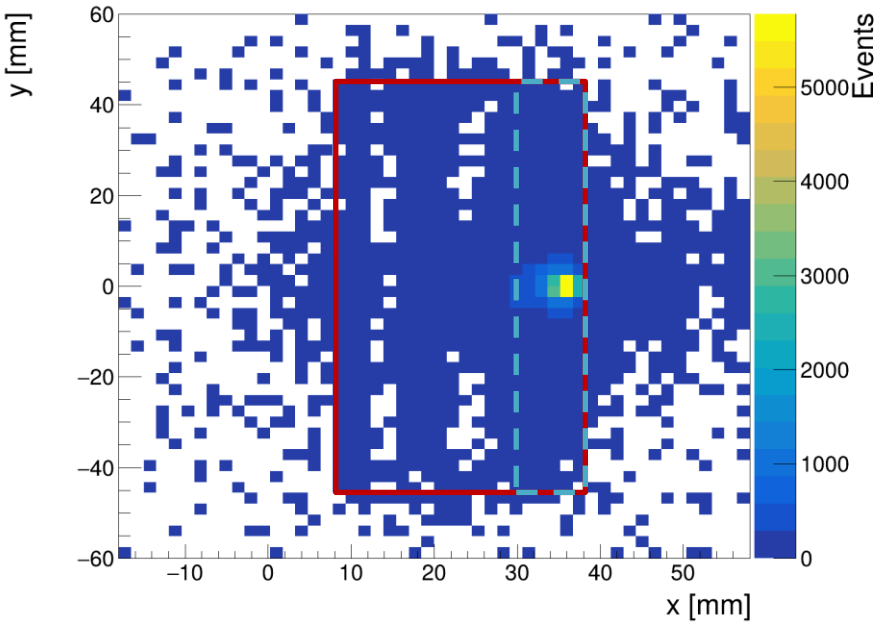
Theta & Position of truth hit, $0.1 < \frac{E_{dep}}{E_{truth}} < 0.2$



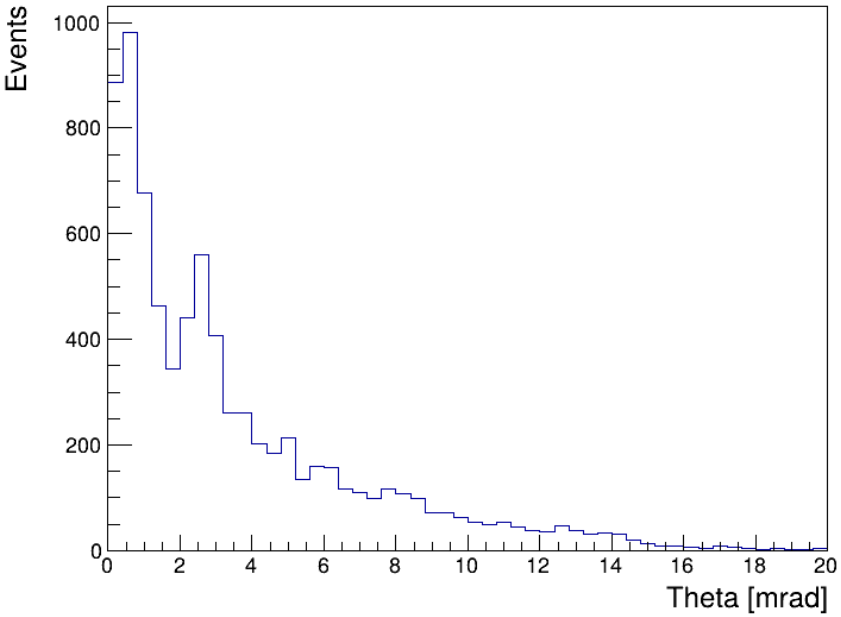


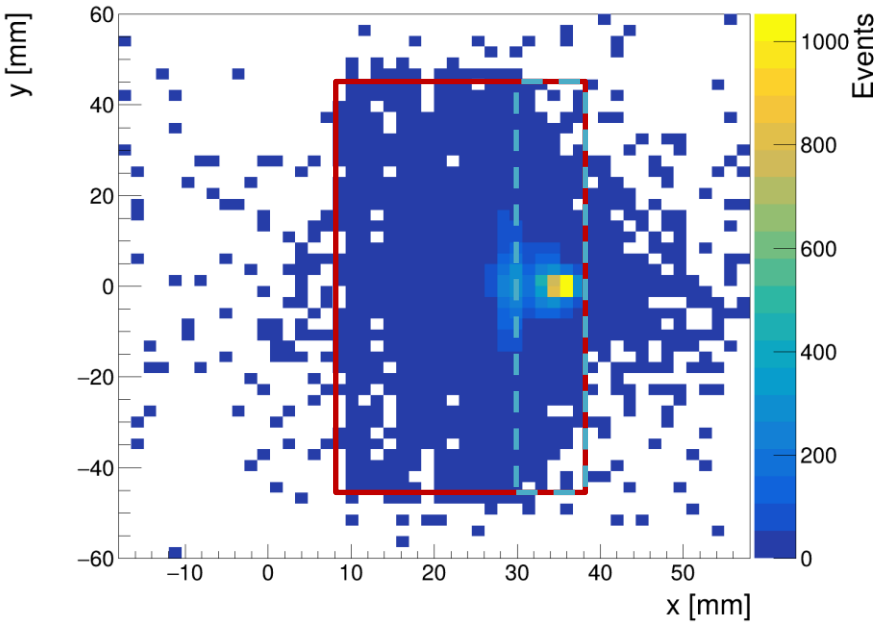
Theta & Position of truth hit, $0.2 < \frac{E_{dep}}{E_{truth}} < 0.3$



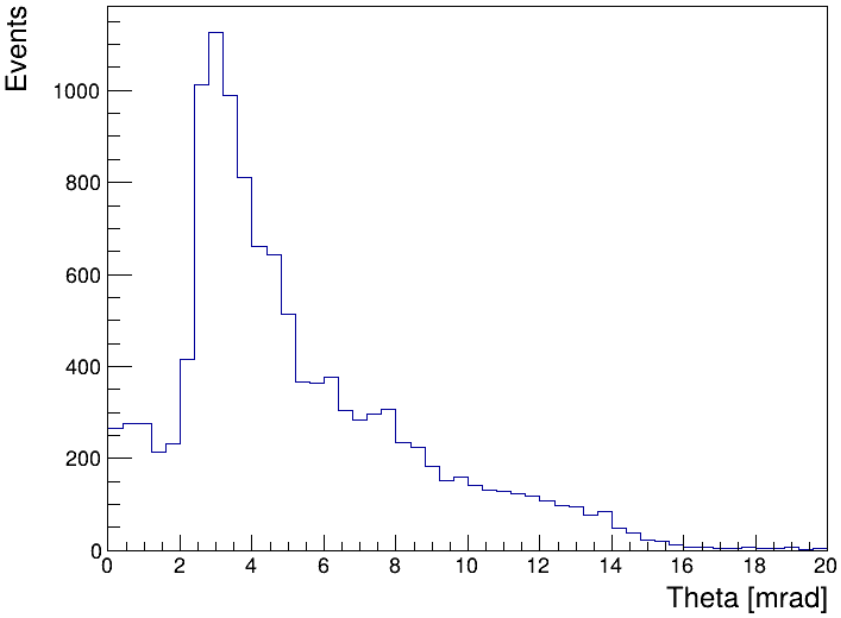


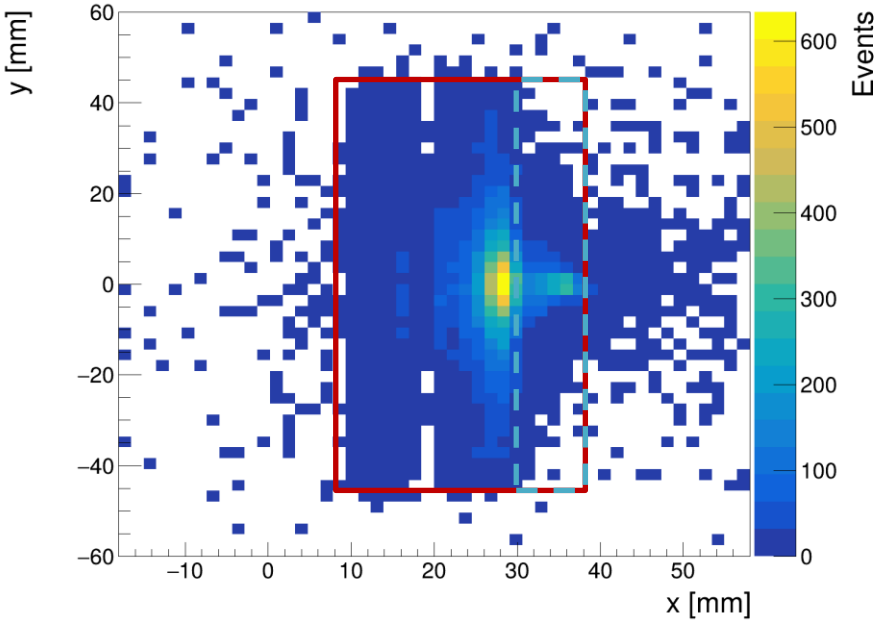
Theta & Position of truth hit, $0.3 < \frac{E_{dep}}{E_{truth}} < 0.4$



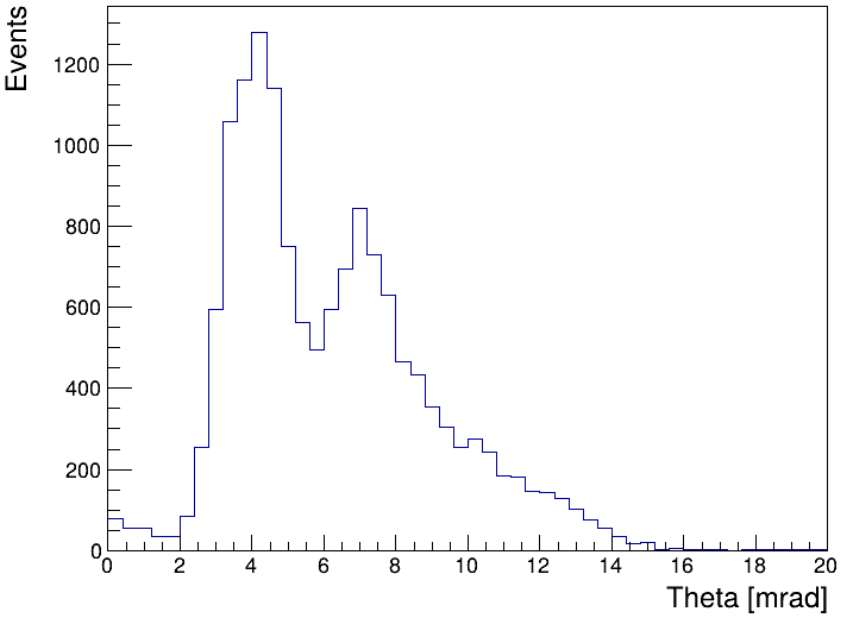


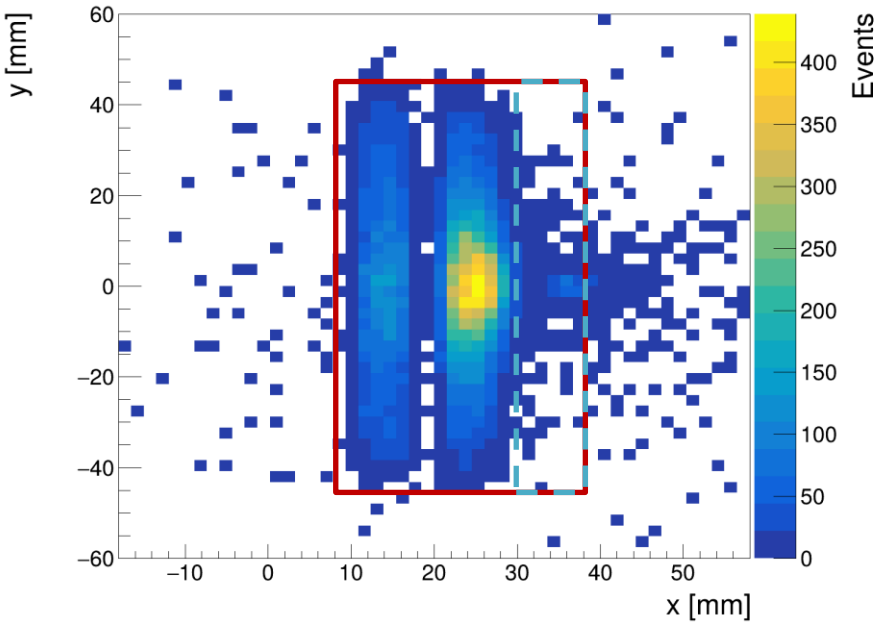
Theta & Position of truth hit, $0.4 < \frac{E_{dep}}{E_{truth}} < 0.6$



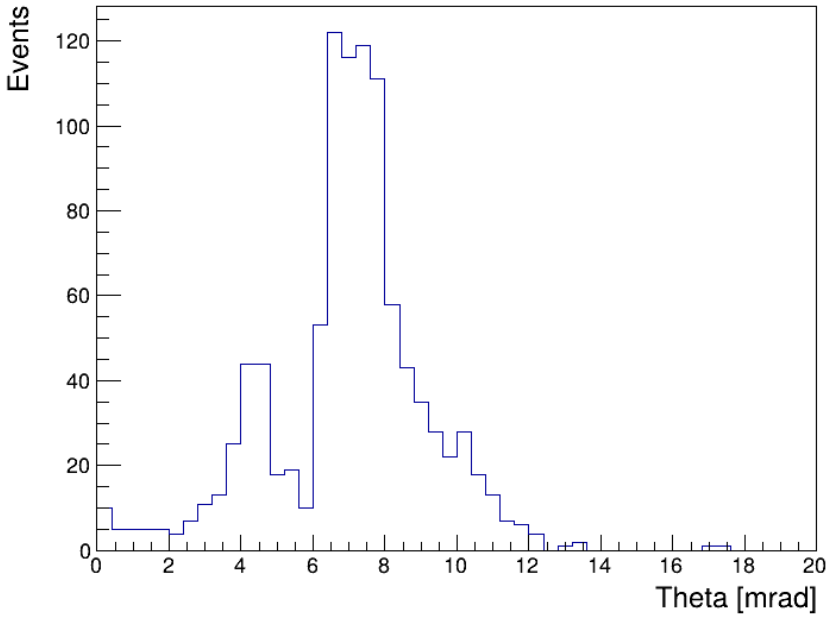


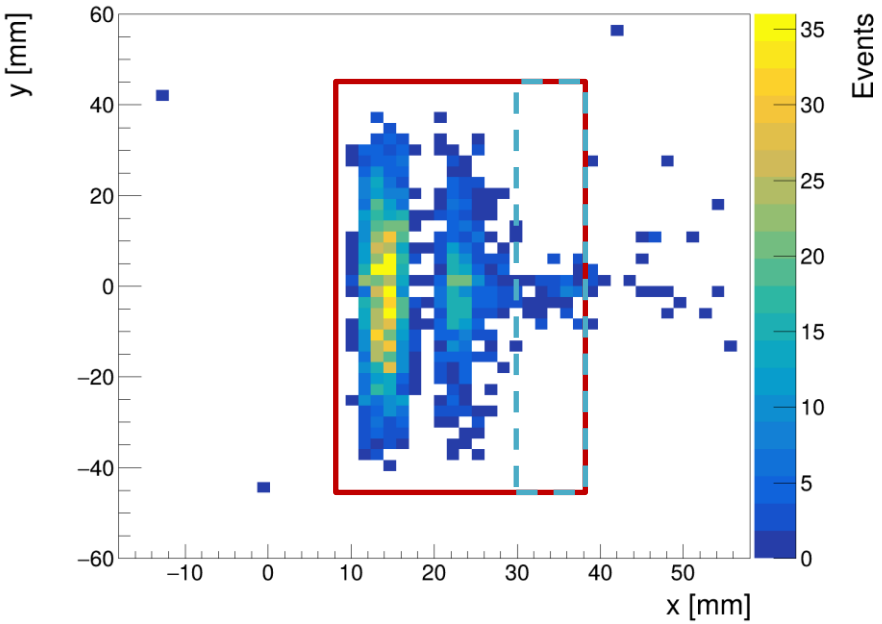
Theta & Position of truth hit, $0.6 < \frac{E_{dep}}{E_{truth}} < 0.8$





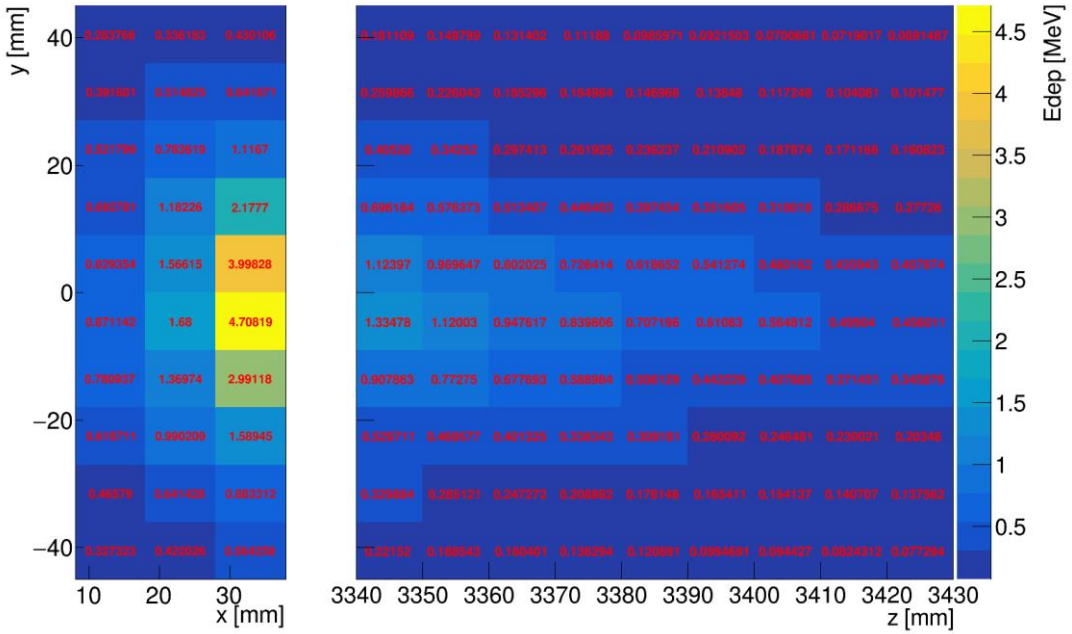
Theta & Position of truth hit, $0.8 < \frac{E_{dep}}{E_{truth}}$





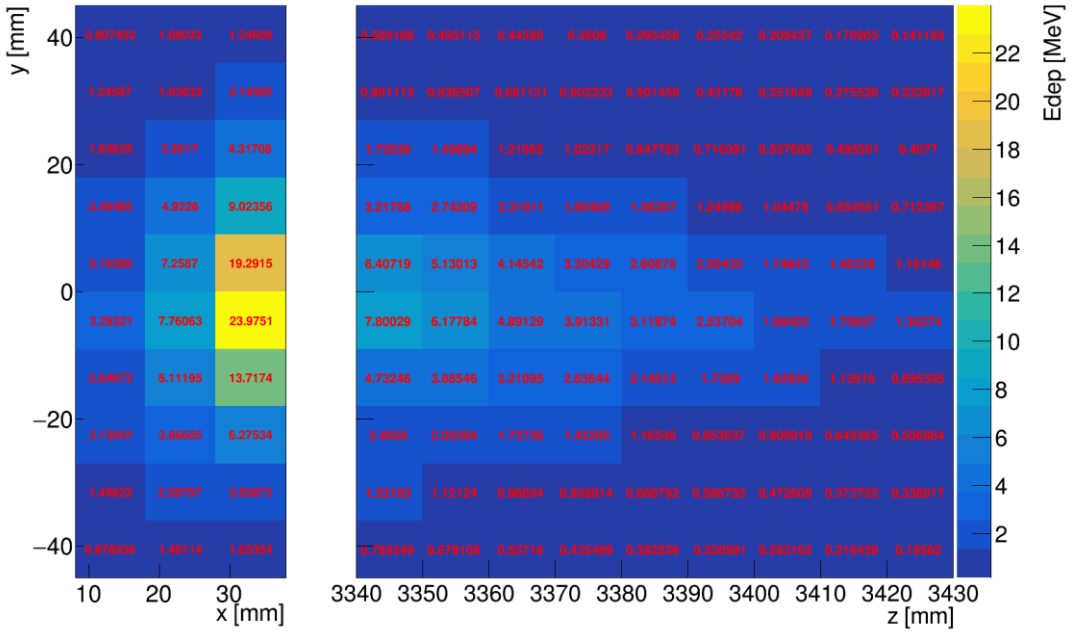
Average E_{dep} in each crystal for different $R = E_{dep}/E_{truth}$

$0 < R < 0.1$



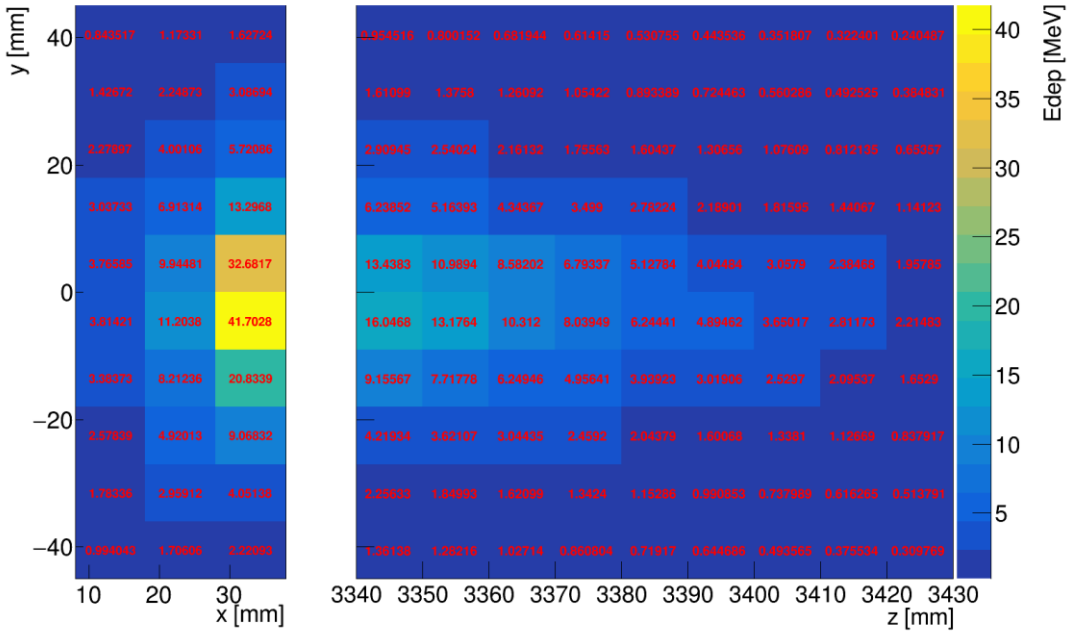
Average E_{dep} in each crystal for different $R = E_{dep}/E_{truth}$

$0.1 < R < 0.2$



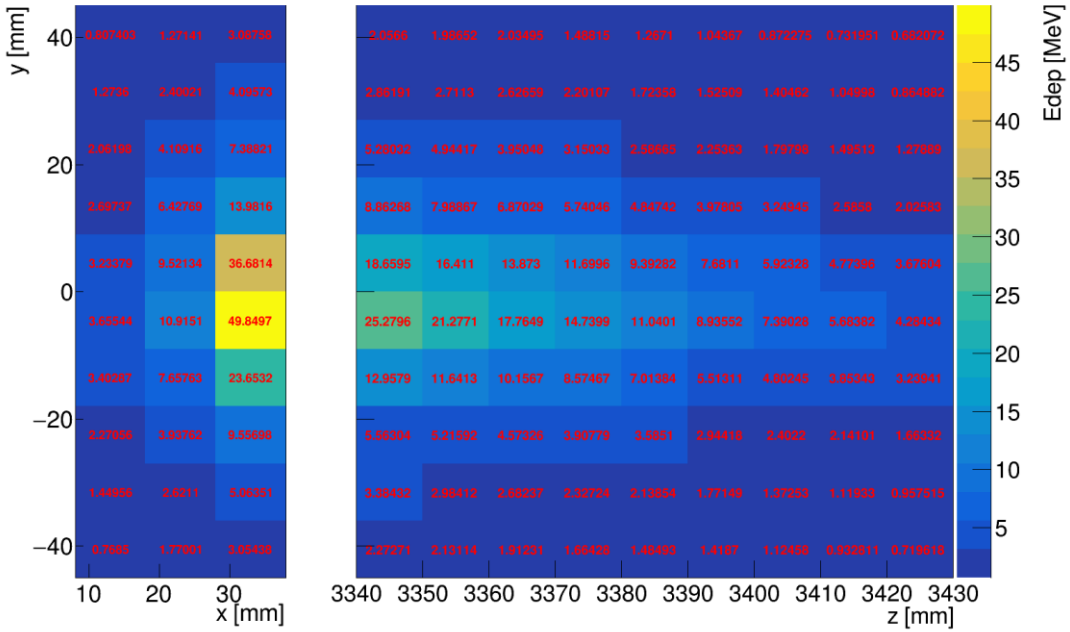
Average E_{dep} in each crystal for different $R = E_{dep}/E_{truth}$

$0.2 < R < 0.3$



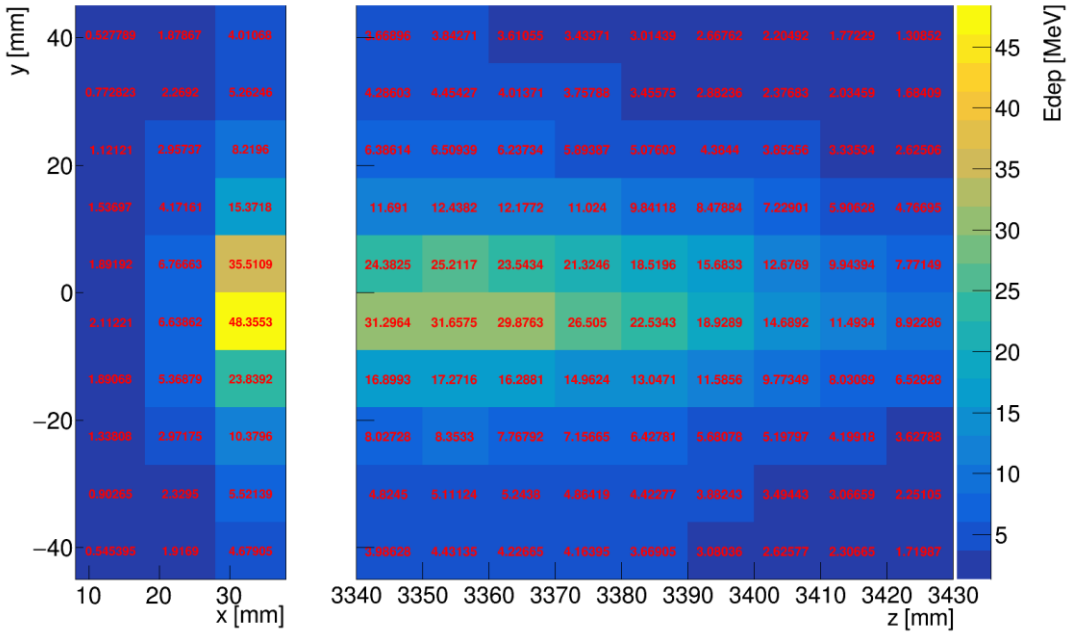
Average E_{dep} in each crystal for different $R = E_{dep}/E_{truth}$

$0.3 < R < 0.4$



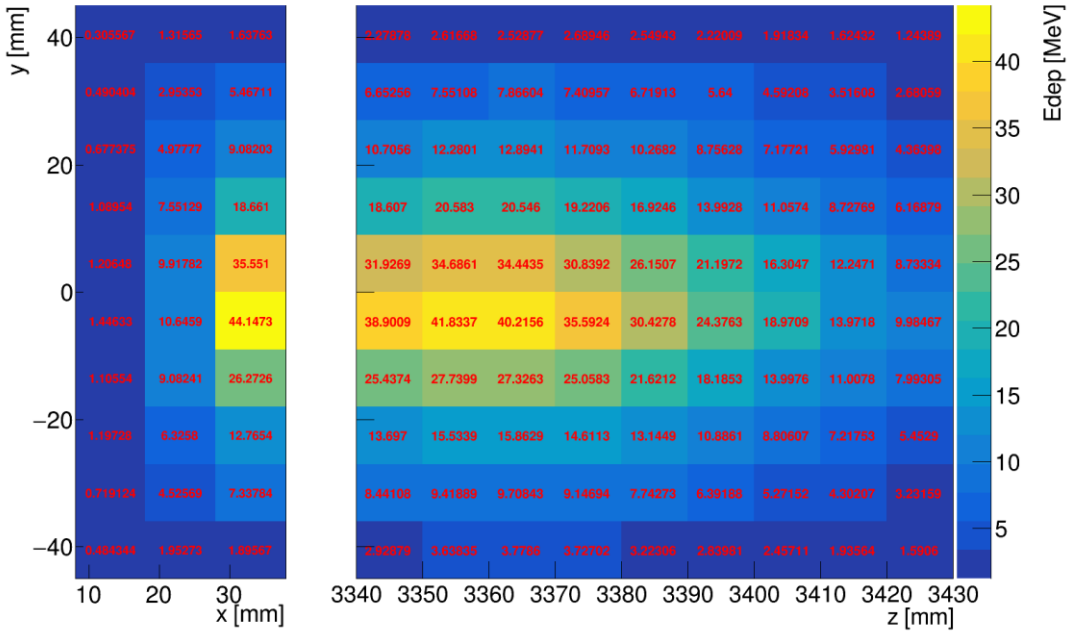
Average E_{dep} in each crystal for different $R = E_{dep}/E_{truth}$

$0.4 < R < 0.6$



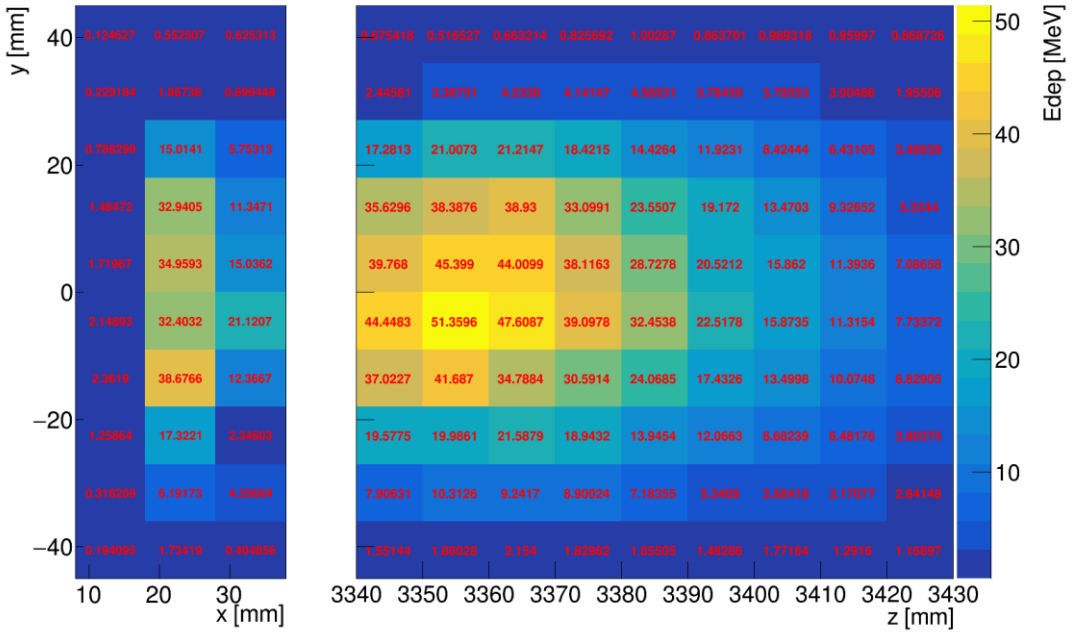
Average E_{dep} in each crystal for different $R = E_{dep}/E_{truth}$

$0.6 < R < 0.8$



Average E_{dep} in each crystal for different $R = E_{dep}/E_{truth}$

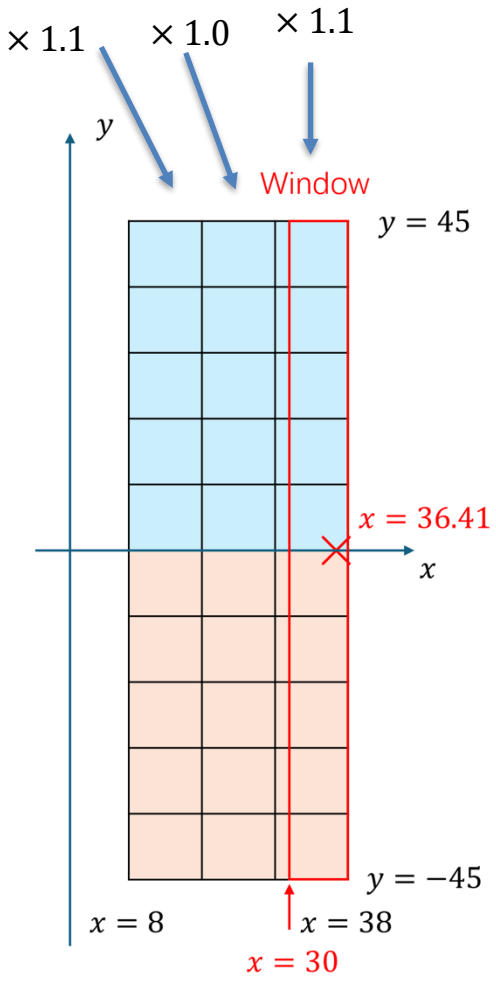
$0.8 < R < 1.0$



Reconstruction

- Position
- Use the center of crystal (if $E_{crystal} > E_{threshold}$) in first section as position
- $x = x_{cry},\ y = y_{cry},\ z = \pm 3310$
- If first section not hit, $x = 40,\ y = y_{cry},\ z = z_{cry}$
- Extra corrections based on results : $x = x - 9$

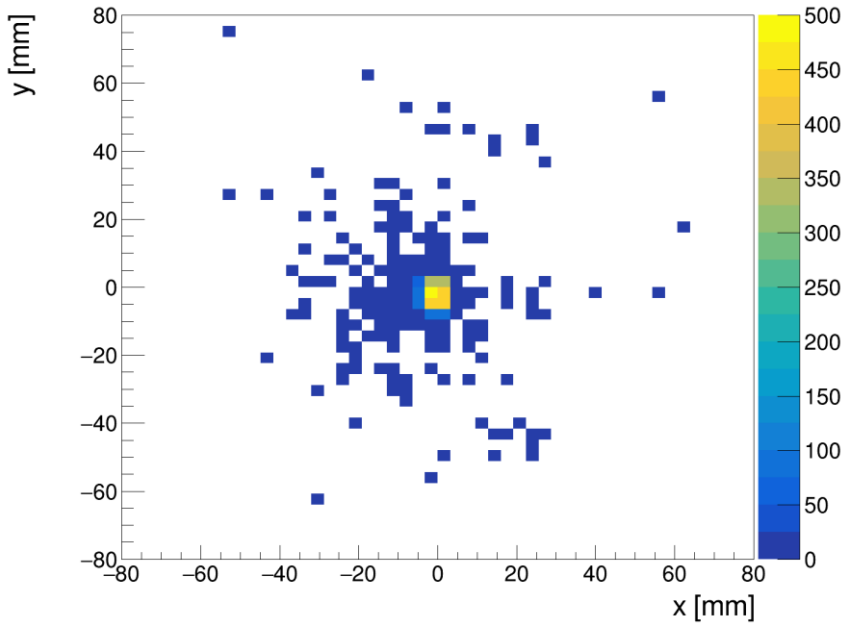
- Energy is corrected by the crystal position
  - Energy = $E_{totaldep} \times Corrections$
  - $Correction = 1.3 \times Corrections(x)$
  - $Corrections(x) = \{1.1, 1.0, 1.1\}$



Reconstruction – 3349 events with $\frac{E_{dep}}{E_{truth}} > 0.6$

Position

$(x_{rec} - x_{truth}, y_{rec} - y_{truth})$



Energy

E_{rec}/E_{truth}