Real-time analysis at LHCb

From Run 3 Operations to Upgrade II Prospects

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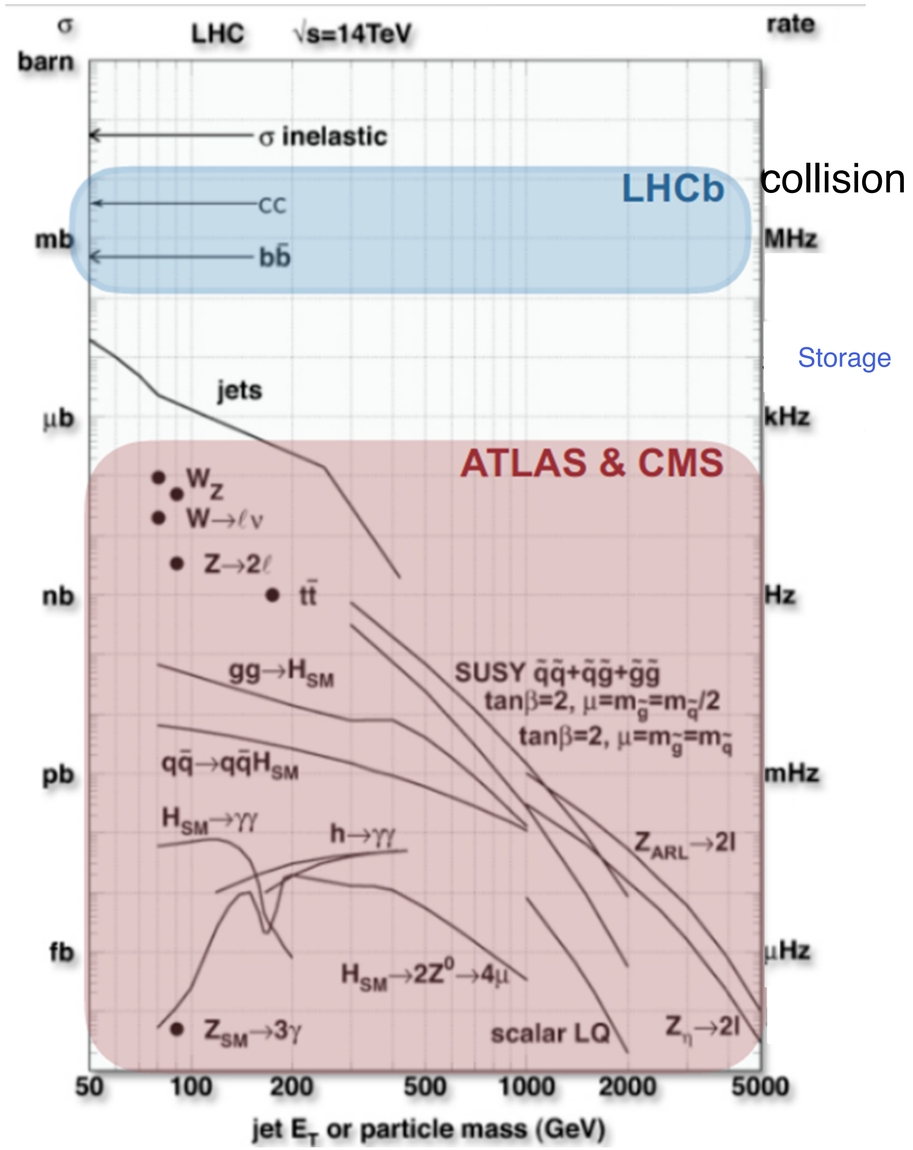
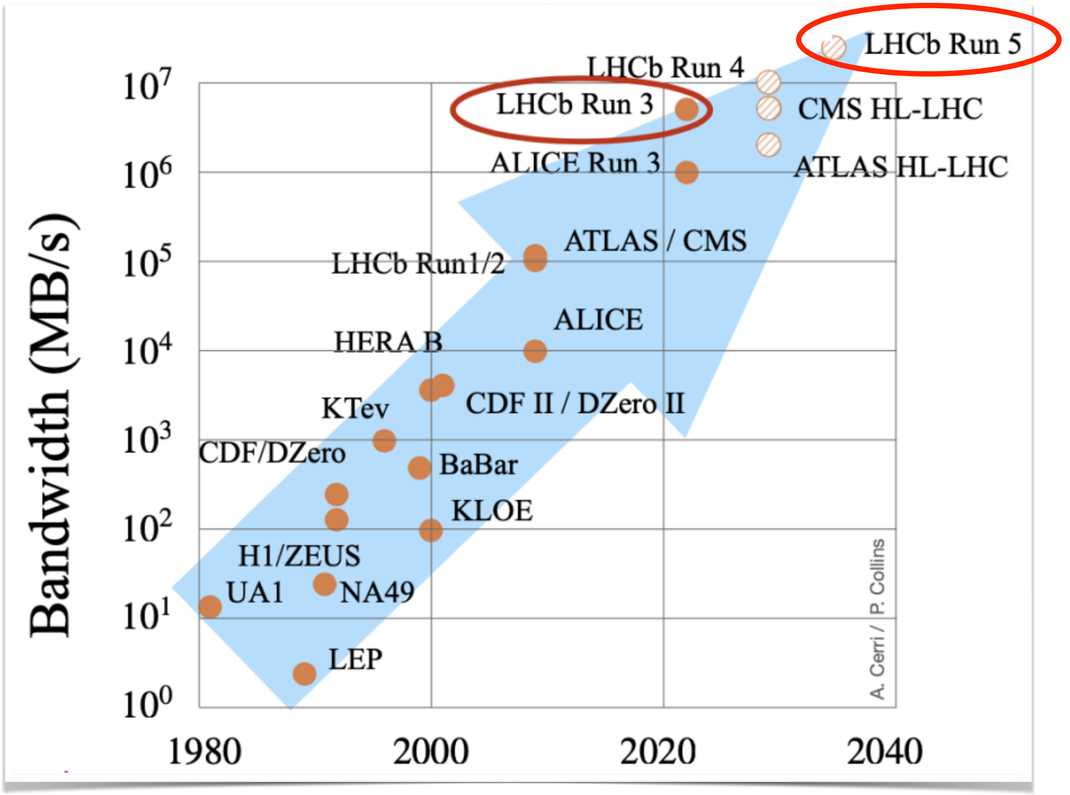
LHCb: flavour physics



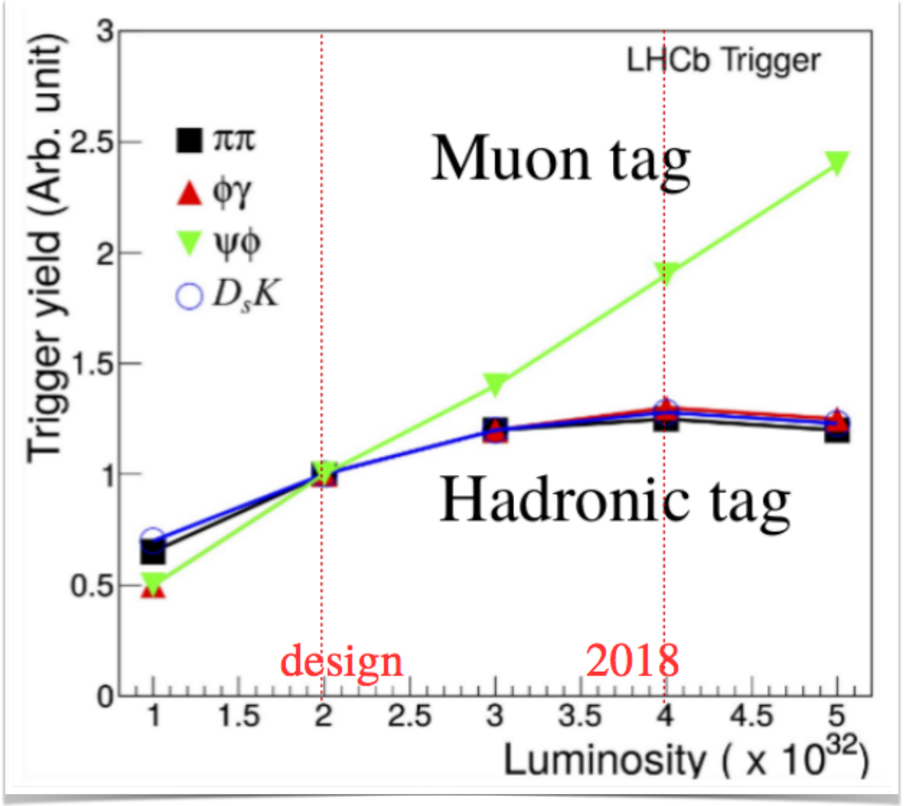
Pioneering in novel trigger strategies!

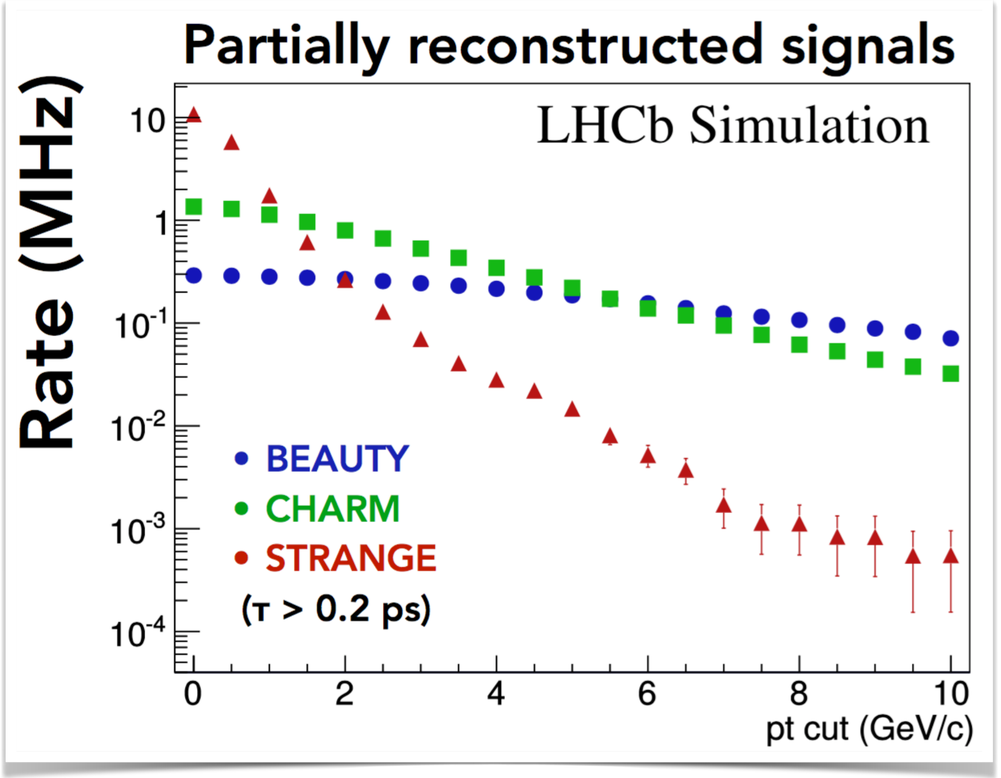


Highest data processing rate of any HEP experiment!

Trigger challenges for Run 3

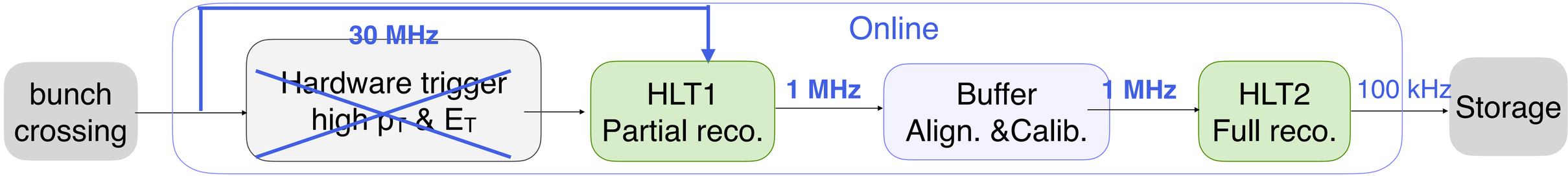
- Run 3: Luminosity of 2×10^{33} cm^{-2}s^{-1}, $\sqrt{s}$ = 13.6 TeV, visible collisions per bunch $\mu \sim 5$
- Hardware trigger saturation already with Run 2 luminosity
- Signal rate up to MHz





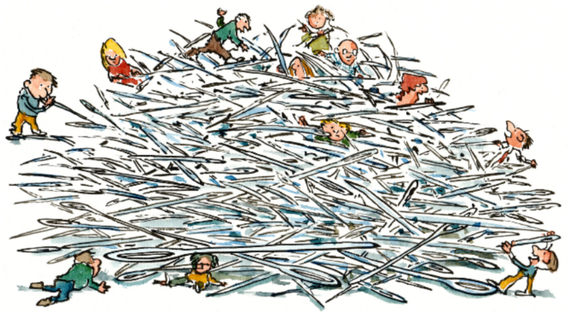
Trigger less strategy for Run 3

- Real-time analysis with full readout of the whole detector



Online - Real Time Analysis

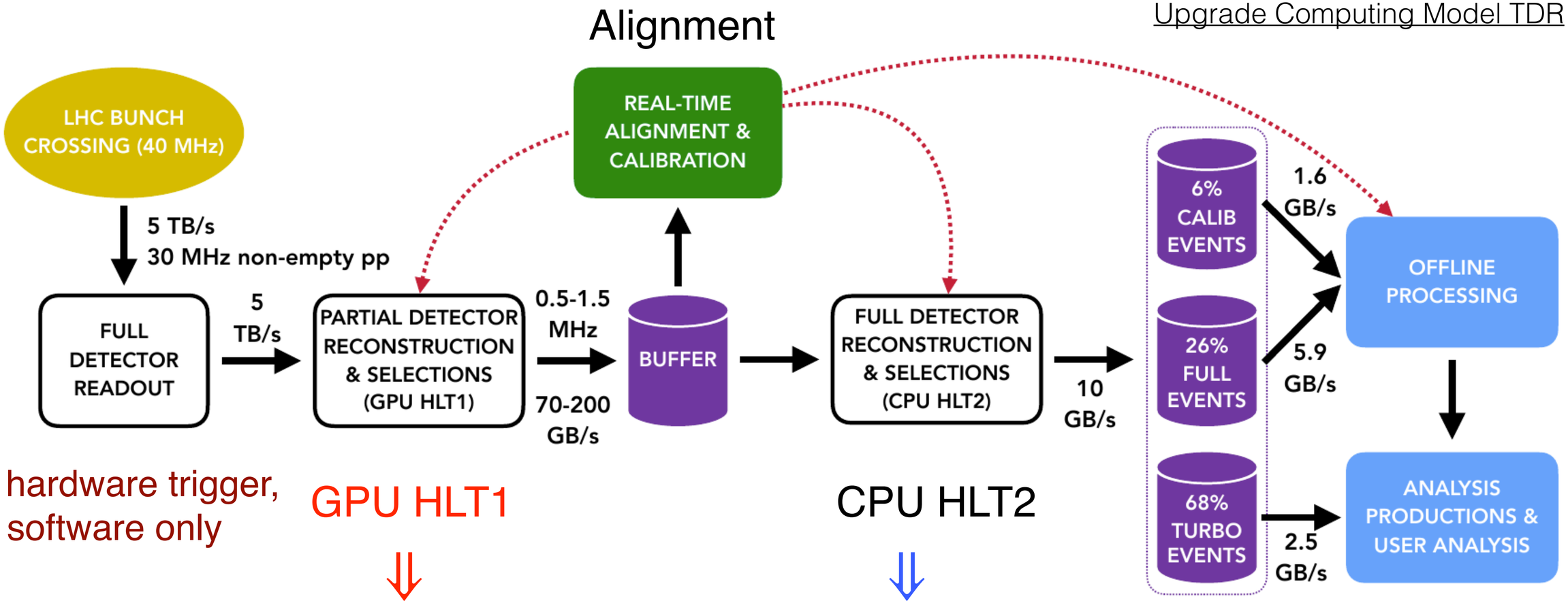
Run 1 & 2 trigger:
background rejection



Upgrade trigger:
background rejection & signals classification

LHCb Run 3 Data Flow

All numbers related to the dataflow are taken from the LHCb
Upgrade Trigger and Online TDR
Upgrade Computing Model TDR



No hardware trigger, software only

GPU HLT1

⇓

First complete high-throughput GPU Trigger for a HEP experiment!

CPU HLT2

⇓

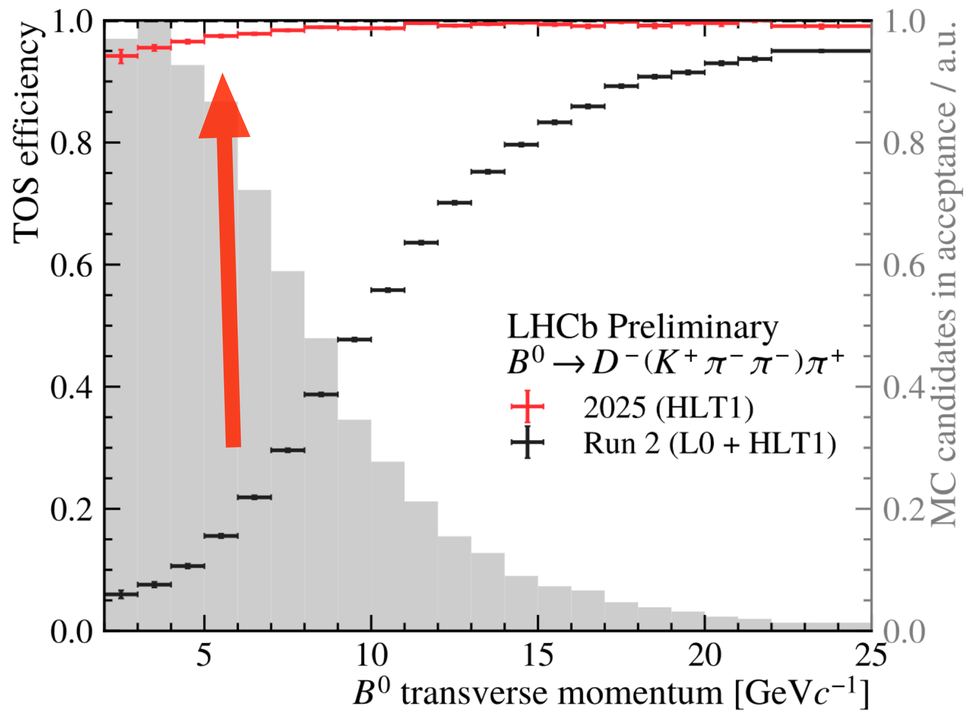
Offline-quality full reconstruction with exclusive selections ℴ (1000) lines

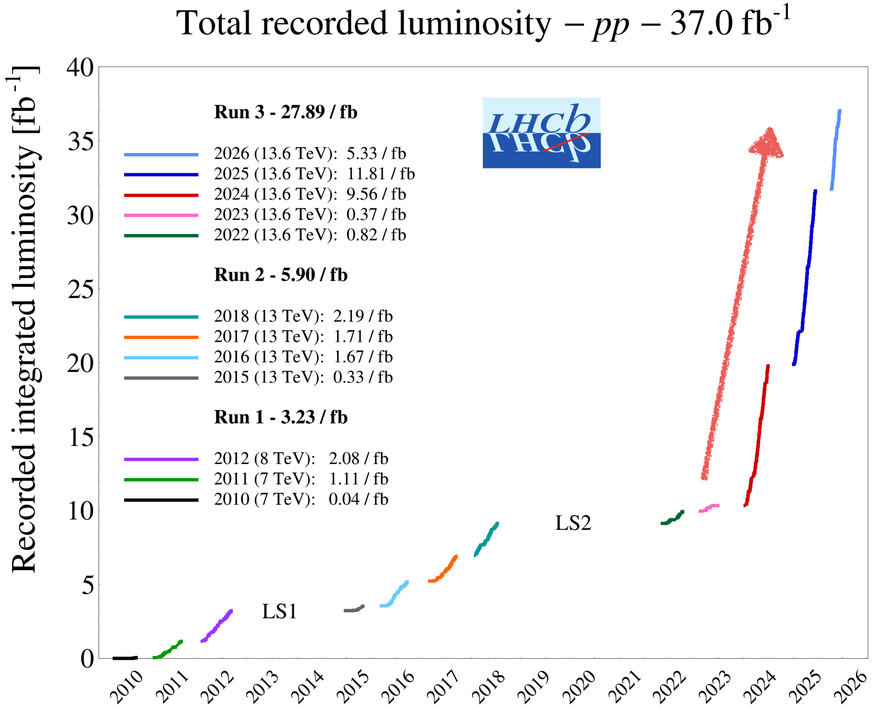
⇘

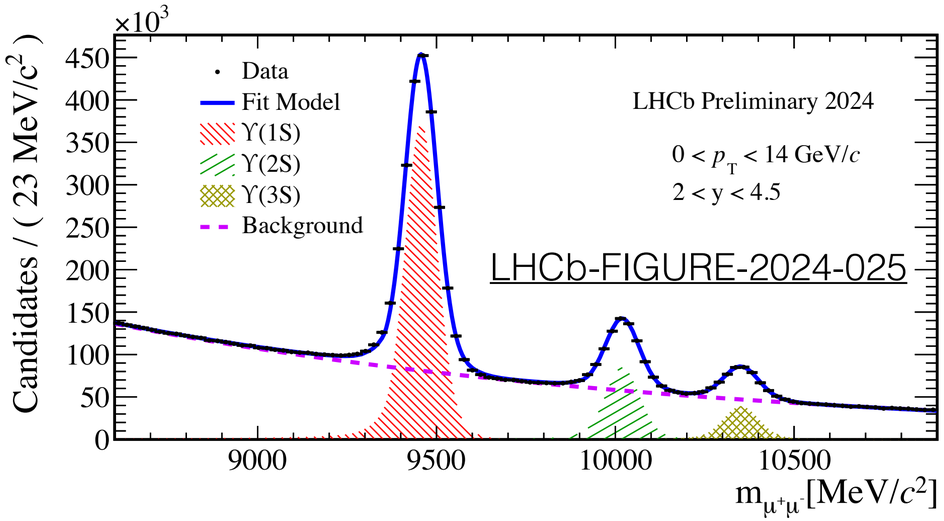
Selective persistence

LHCb Run 3 Performance

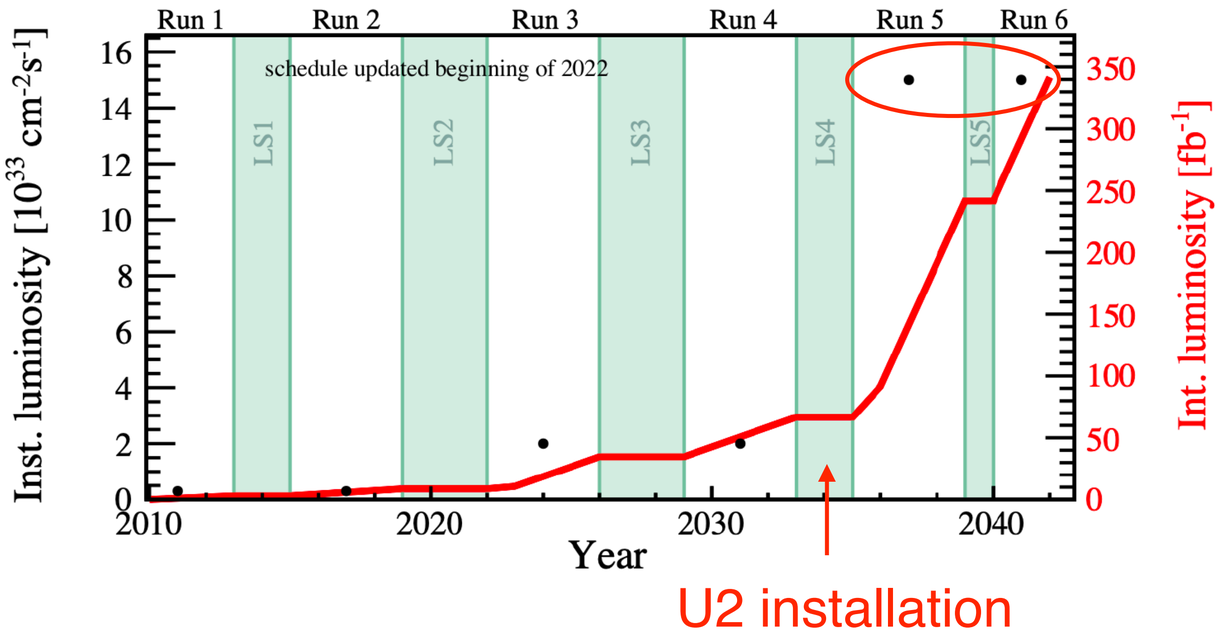
- Significant improvement in HLT1 efficiency (2-4x for hadronic modes)

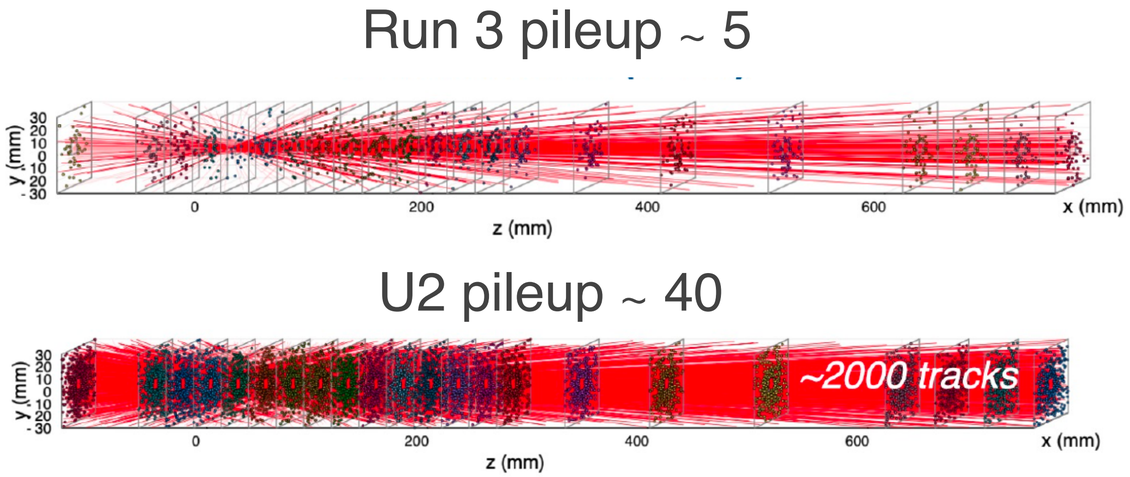






LHCb Upgrade II





[Scoping document, LHCb-TDR-026]

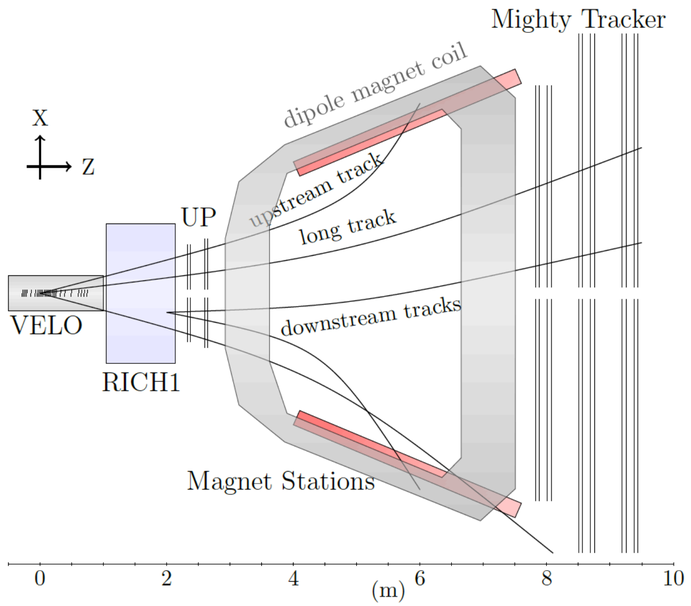
- 5x ~ 7.5x higher luminosity, up to 10^{-34} $cm^{-2}s^{-1}$
- Data rate: from 5 TB/s ⇒ 25 TB/s
- “triggerable” decay in every event
- Larger event size (more PVs + timing info)
- Computing and storage of HLT2 needs scale quadratically

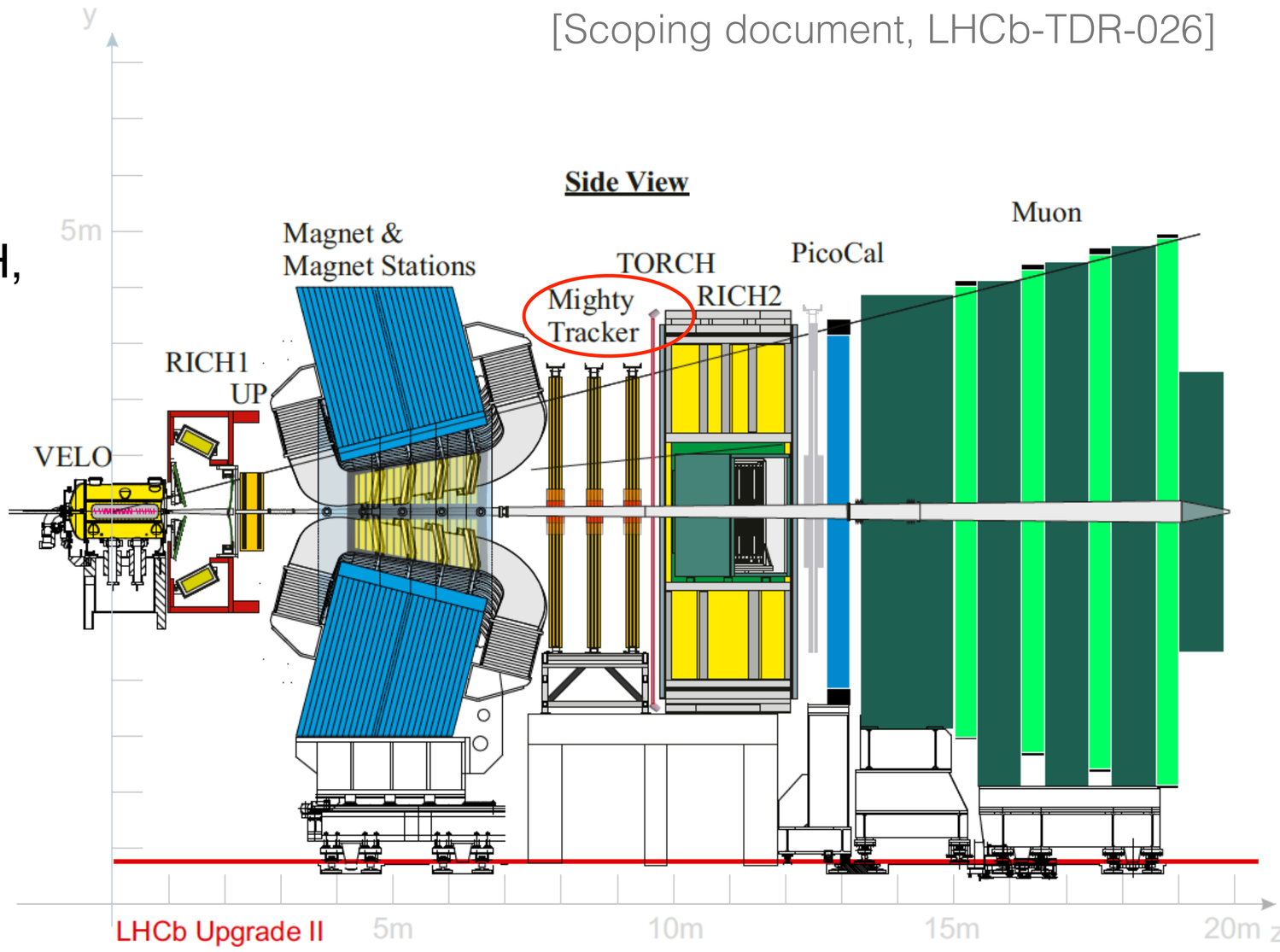
LHCb Upgrade II

[Scoping document, LHCb-TDR-026]

Same layout as Run 3, but with

- Pixels for VELO + UP + Mighty
- Timing information from VELO, RICH, PicoCal and possibly in SciFi

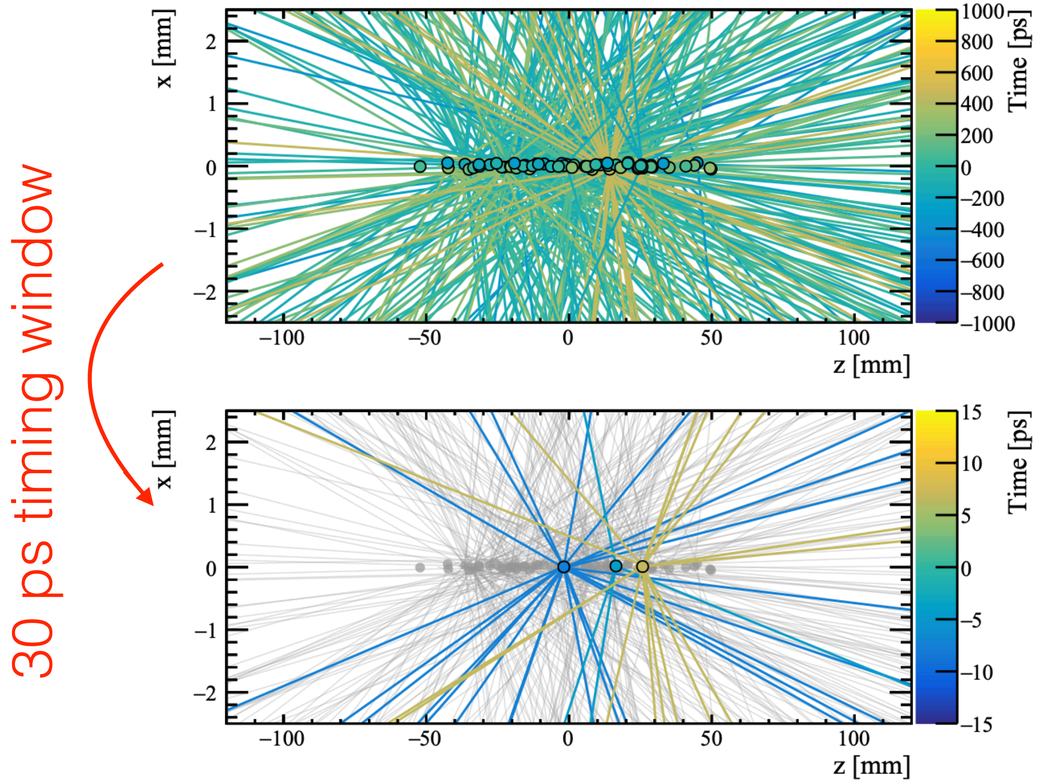


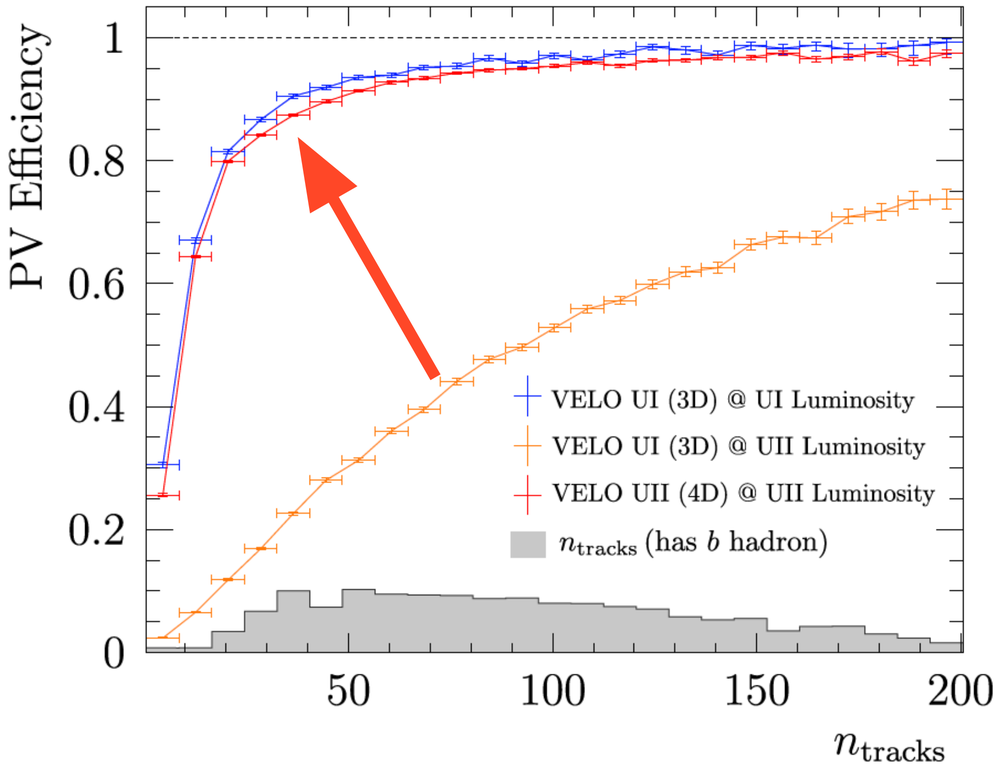


Pile up mitigation with timing

[Scoping document, LHCb-TDR-026]

- Timing is necessary for HL-LHC to mitigate the pile-ups
- 4D Tracking and Vertexing





Timing in Tracking (WIP)

[Scoping document, LHCb-TDR-026]

- 4D T-Tracking with timing in SciFi
  - timing windows in each step of hit search / adding
  - Scan of time resolution from 0.4 ns to 2.0 ns

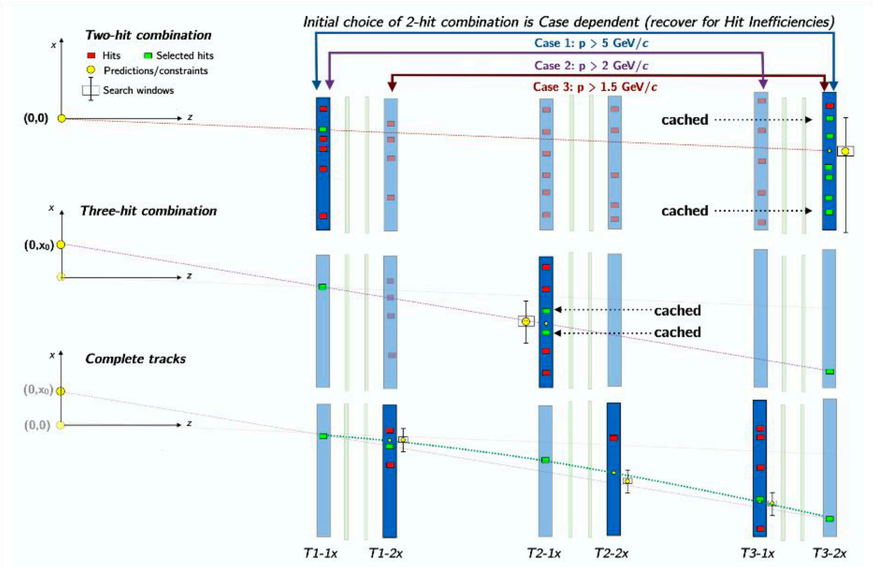
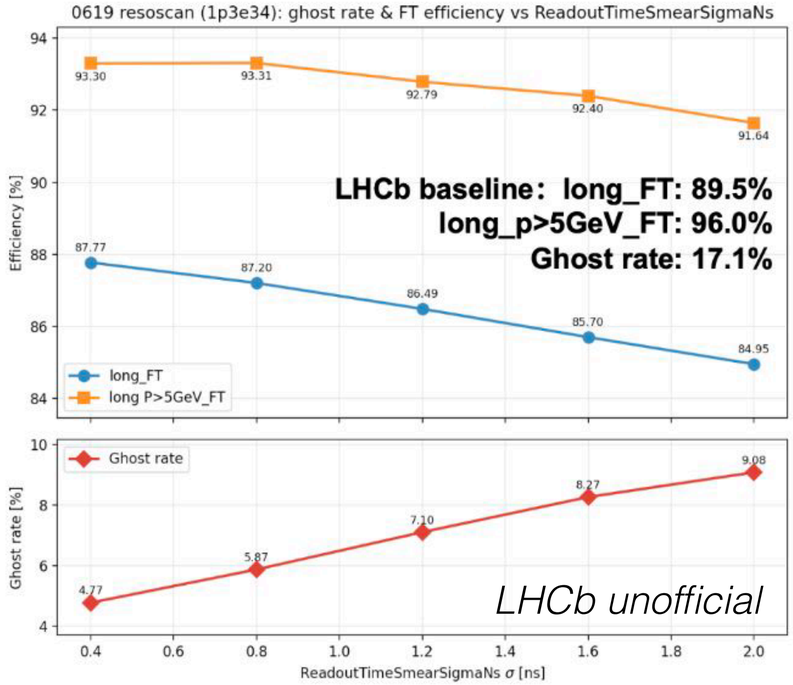
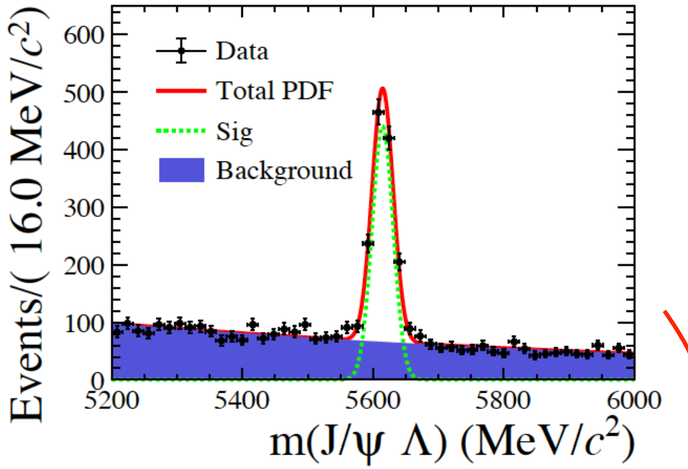


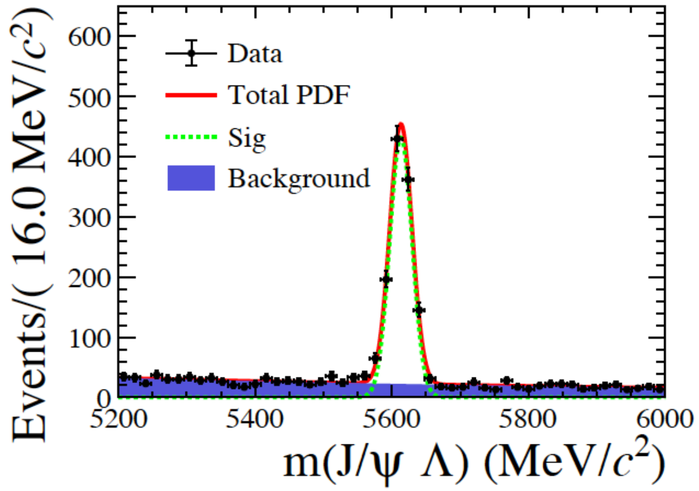
Figure 4.22: Logic implementation of the three main steps in the *x-z projections* track finding. Actual hits in the detector are shown in red while the green ones picked up in the track building are in green. Hits (actually iterators) at the border of tolerances are cached to speed up the look-up sequence given the order of hit processing. Two hit combinations are build considering combinations of hits in T1 and T3 forcing the track origin at $(x, z) = (0, 0)$. The three hit combination is built



Sample:1p3e34/MINBIAS_proto-v00.03_**L1p3E34**_Slot_0-30000000-100ev-20260129-Extended.digi
Number of evt: 100



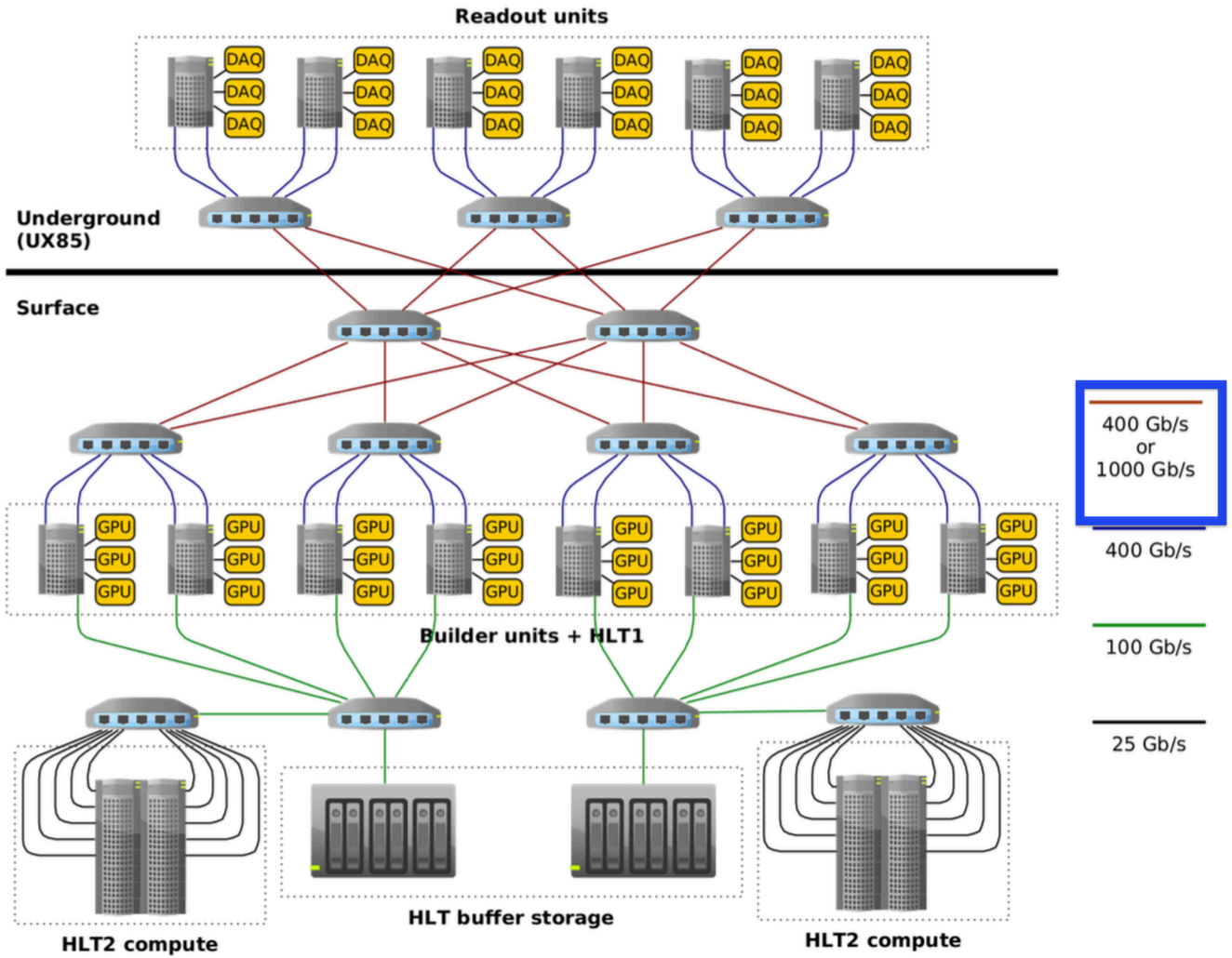
with downstream track timing



Event-builder architecture

[LHCb-FTDR-023]

- 5 times capacity of the Run 3 DAQ
- Assume 480 readout-boards at full speed



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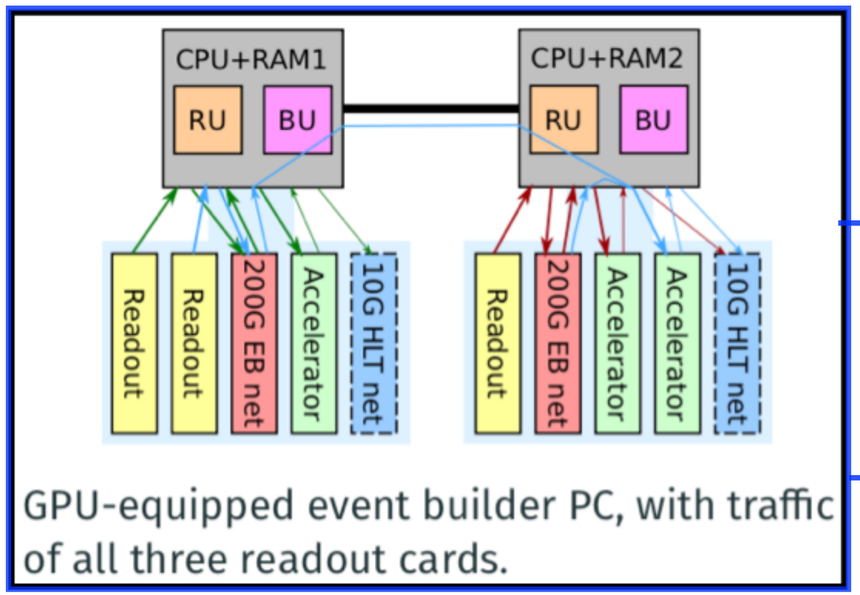

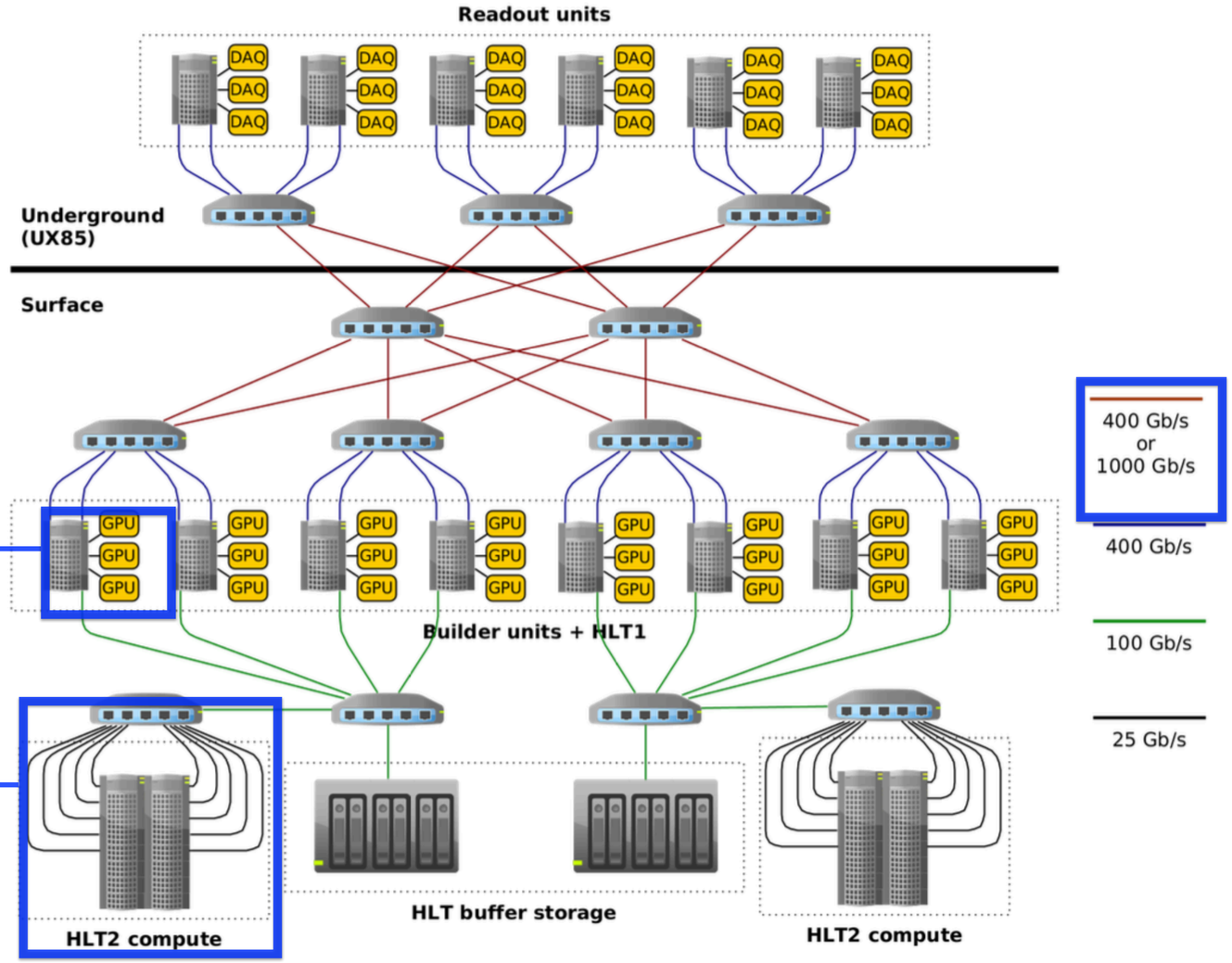

- Full detector reconstruction
- Two reconstruction stages (HLT1 + HLT2) on GPUs (Baseline)

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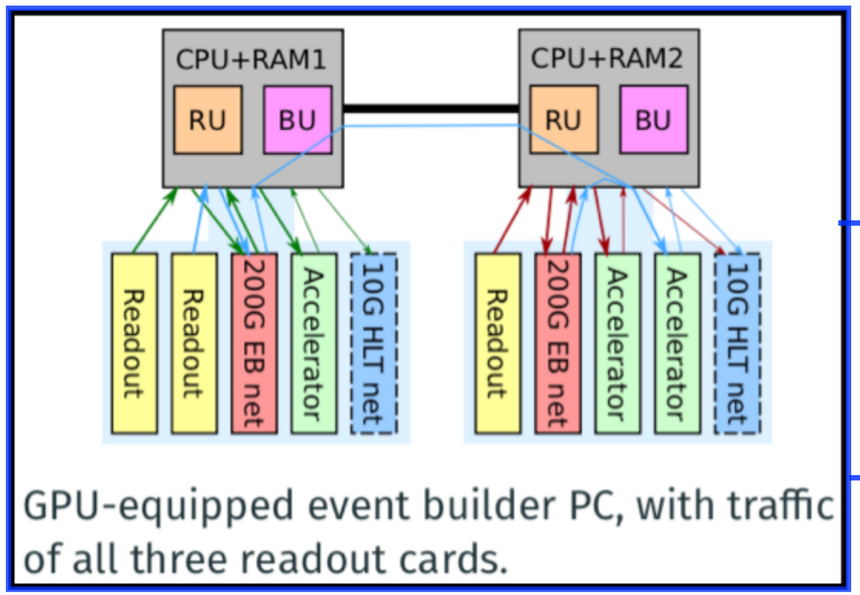

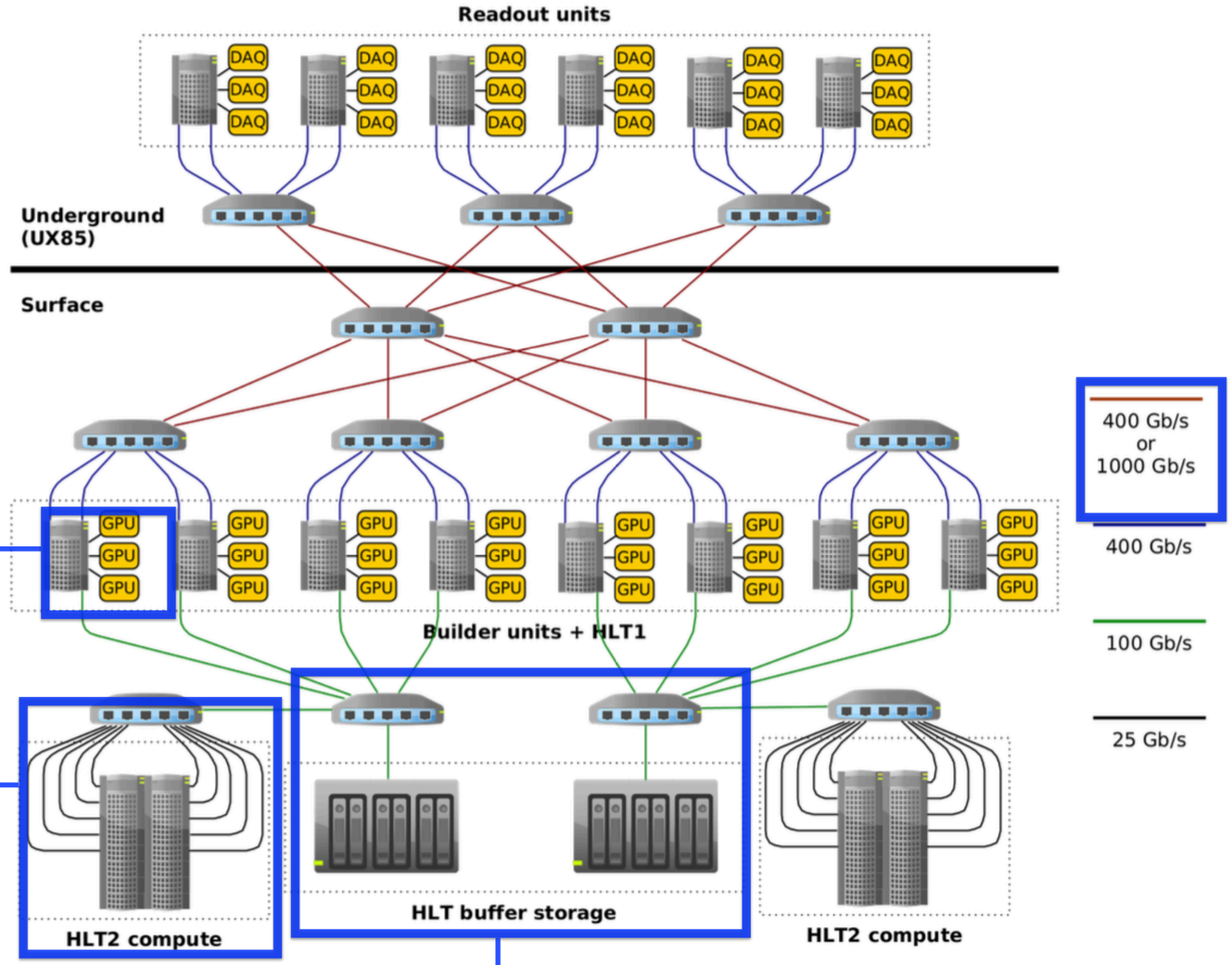

- Full detector reconstruction
- Two reconstruction stages (HLT1 + HLT2) on GPUs (Baseline)
- Disk buffer for alignment & calibration

U2 trigger strategy

All numbers related to the dataflow are taken from the LHCb
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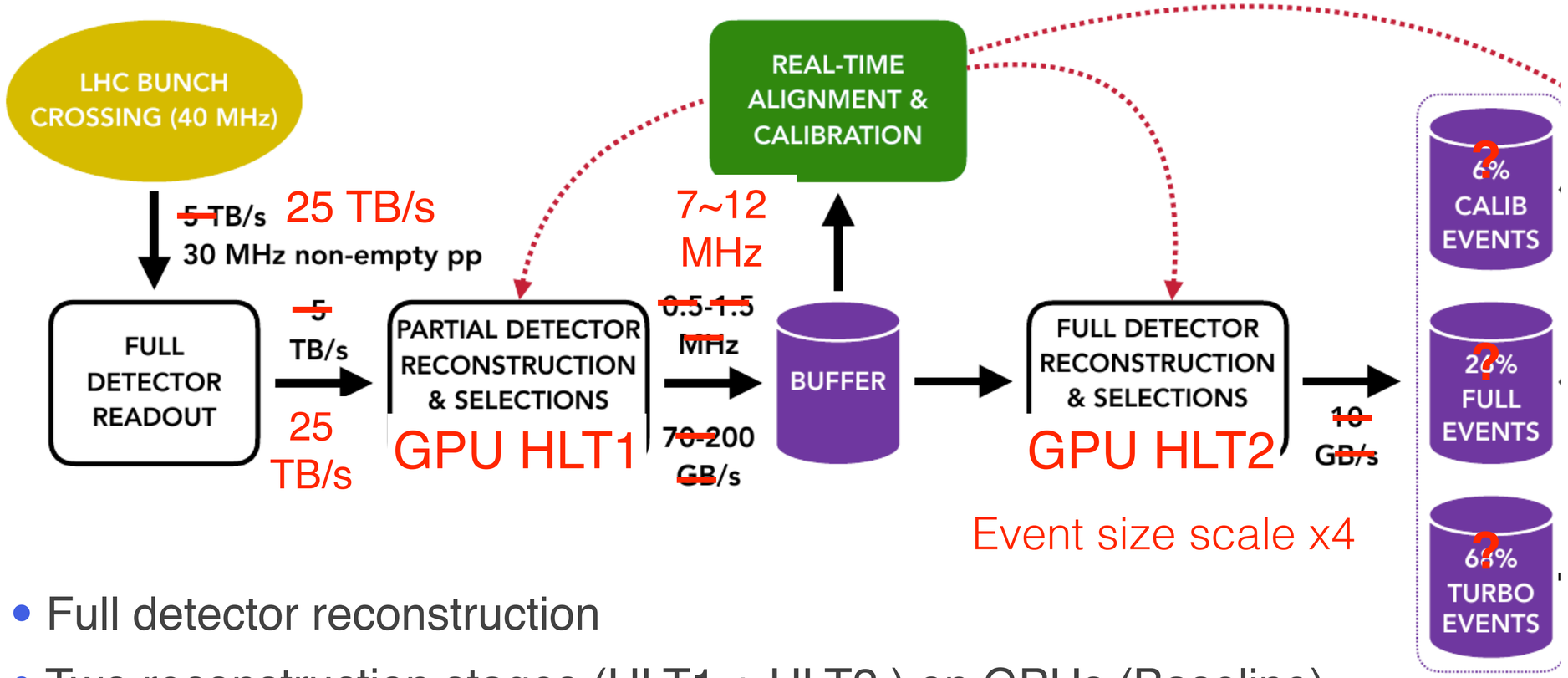
Upgrade Computing Model TDR



- Full detector reconstruction
- Two reconstruction stages (HLT1 + HLT2) on GPUs (Baseline)
- Clustering & track primitives on FPGAs
- Selective persistency

Summary

- LHCb successfully realised the pure software trigger paradigm in Run 3
  - ✓ Hybrid architecture (GPU+ FPGA +CPU)
  - ✓ Great performance & successful data taking
- Baseline strategy with both HLT1 and HLT2 on GPU for U2
  - 4D reconstruction with timing necessary
  - R&D in well progress
- Various ML / FPGA / IPU developments in progress

Thanks!