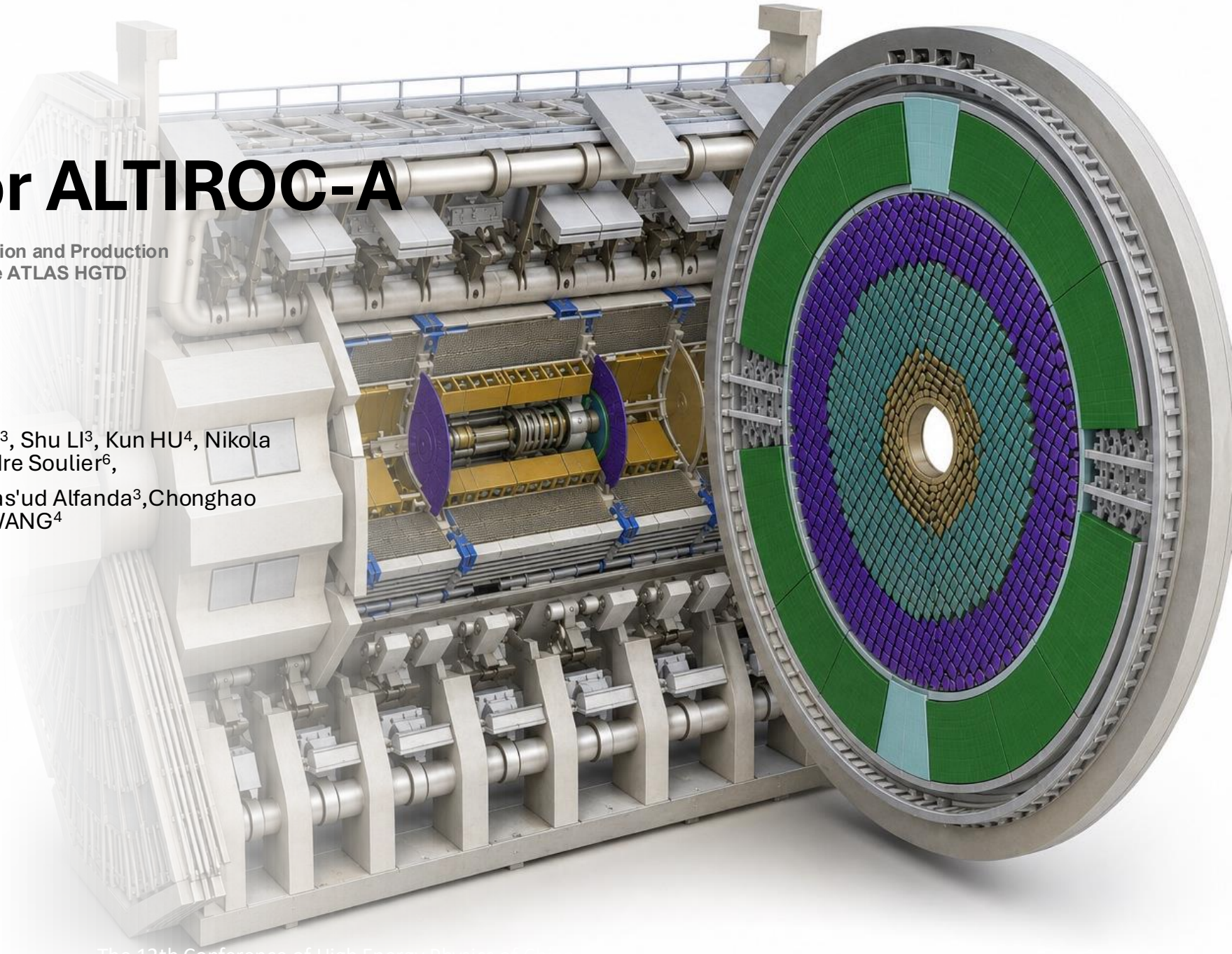
Wafer Probing for ALTIROC-A

Performance Characterization and Production Quality Control for the ATLAS HGTD



***Hancen LU*[1],**

Zhijun LIANG[1], Nathalie Seguin-Moreau[2] , Liang LI[3], Shu LI[3], Kun HU[4], Nikola Makovec[5], Laurent Serin[5], Alexandre Soulier[6],

Xiang CHEN[3], Jiahui WU[3], Zelin YAN[3], Haydar Mas'ud Alfanda[3],Chonghao WU[3], Jingru TANG[4], Jinghan WANG[4]

[1]Institute of High Energy Physics (IHEP)

[2]Organisation de Micro-Électronique Générale Avancée (Omega)

[3]Shanghai Jiao Tong University (SJTU)

[4]Shan Dong University (SDU)

[5]Laboratoire de Physique des 2 infinis Irène Joliot-Curie (IJCLab)

[6]Laboratoire de Physique de Clermont-Ferrand (LPC)

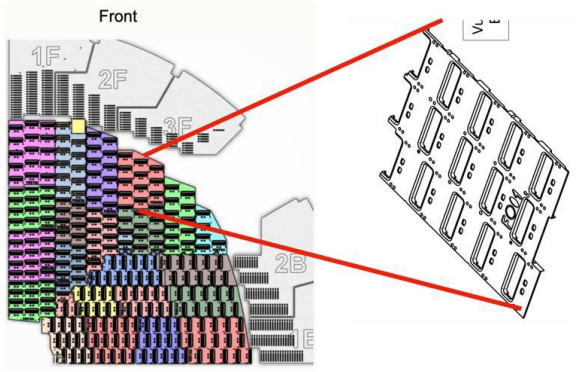
Outline

- **Motivation and test targets**
  - Introduction
  - Why wafer probing?
  - ALTIROC-A and test targets
- **Wafer probing workflow**
- **Pixel-level qualification**
  - Timing characterization
  - From pixel measurements to chip and wafer QC
- **Understanding yield spread**
- **Toward production**
  - Lessons from wafer probing
  - Toward production QC
  - Production schedule
- **Summary&Backup**

Introduction and Motivation

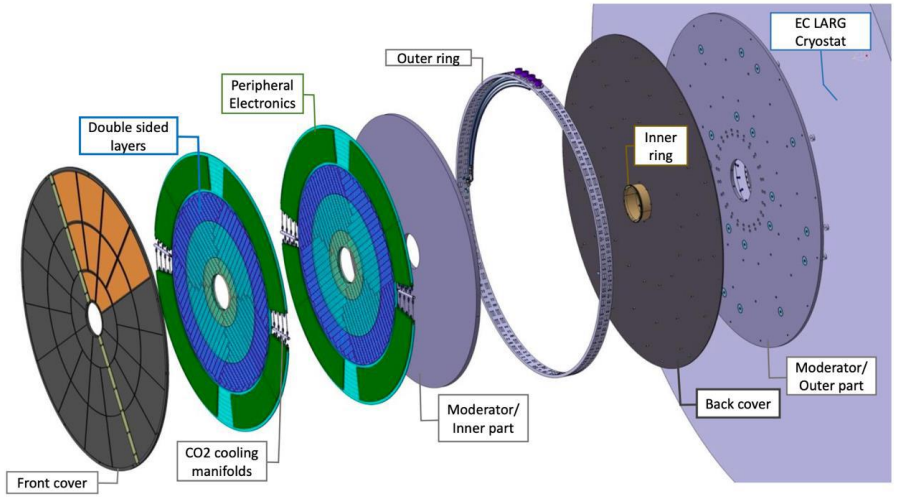
The High-Granularity Time Detector (HGTD) is to deal with the high pile-up environment for the future HL-LHC.

- Position: ± 3.5 m, Active area: $6.4\ \mathrm{m}^2$.
- 8032 HGTD modules in total.
- $2.4 < |\eta| < 4$, time resolution: 35ps (start), 70ps (end).



Contributions from China groups:

- LGAD sensor: 100%
- Module assembly: 44%
- Front-end electronics: 100%
- ASIC Probing: 50% (100%@China, >200 wafers)
- HV system: 16%

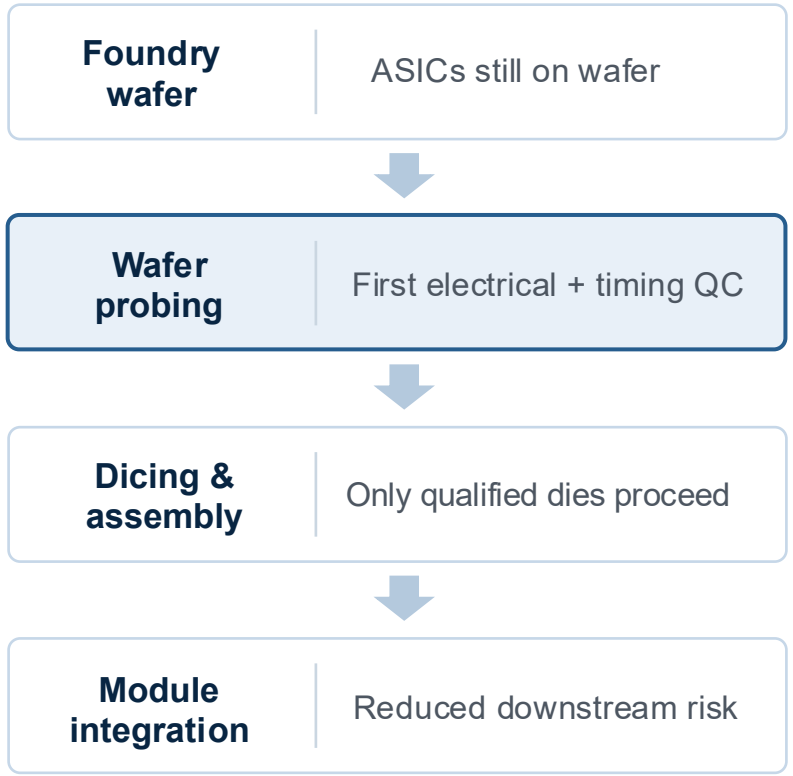


Simplified readout chain

LGAD sensor → Analog front-end → TDC / logic → DAQ / QC

Why Wafer Probing?

Production flow

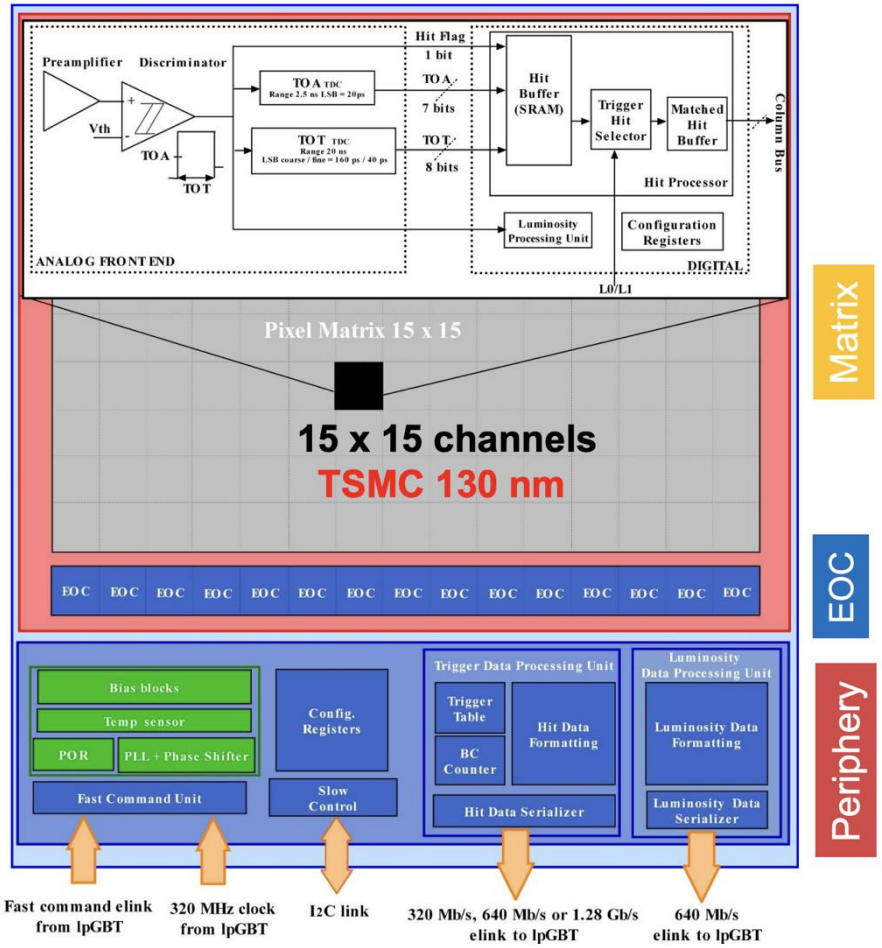


What wafer probing provides

- Early rejection of failed or marginal dies before costly downstream steps.
- Wafer maps that reveal yield spread, local patterns, and edge effects.
- Traceable database linking raw scans, derived metrics, and chip classification.
- Feedback on probing stability, contact quality, and production test robustness.
- A controlled basis for re-test policy and large-scale acceptance criteria.

Wafer probing is the first production-quality-control stage, not just a pass/fail chip test.

ALTIROC-A and the Main Test Targets



ALTIROC-A Overview

Feature	Value
Matrix	15*15 (225Channels)
Pixel Size	1.3*1.3 mm^2
FE	Transimpedance Amplifier
Timing	TOA (20 ps LSB), TOT (40 ps LSB)
Trigger Latency	38.4 μs
Threshold	10-bit VTH DAC+8-bit Local Trim DAC
Output	320/640/1280 Mbps e-link

Functional Blocks

- Matrix: AnalogFE, TOA/TOT DAC, Local Hit Buffer
- EOC: Column Readout, Trigger Matching
- Periphery: Clock & PLL, Slow Control, Data serialization

ALTIROC-A is a 225-channel timing ASIC developed for the ATLAS HGTD upgrade at the HL-LHC.

ALTIROC-A and the Main Test Targets

The wafer test is designed to screen every ASIC before downstream use.

The flow checks whether each chip is functional, electrically stable, and suitable for module production.

Basic function

SRAM test
FPGA communication
DAQ and readout chain

Analog calibration

Vdda / Vddd
Vth and DC pulser
Vctrl response

Pixel performance

Threshold and noise
Efficiency and jitter
TOT RMS and TOA / TOT LSB

QC output

Bad / marginal pixels
ASIC-level status
Wafer map and yield

The current workflow links probe-station control, FPGA scans, and offline QC.

Load config
wafer map
site / wafer code

→

Probe ASIC
move prober
contact chip

→

Run scans
SRAM, monitoring
VTHC, charge

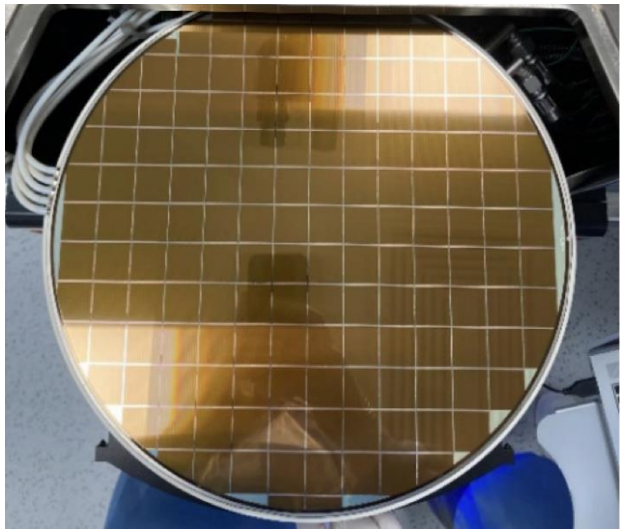
→

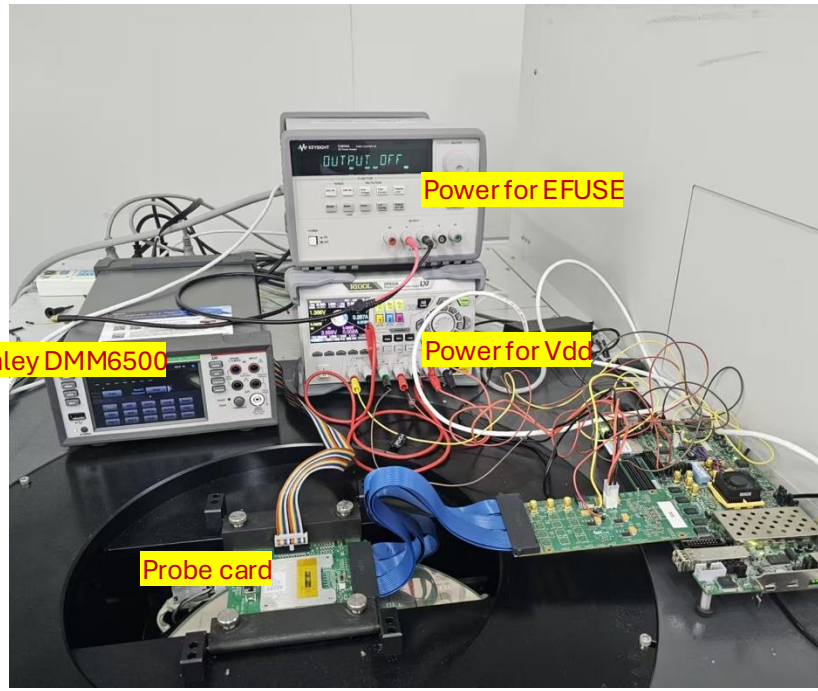
Analyze QC
For hybrid and module assembly

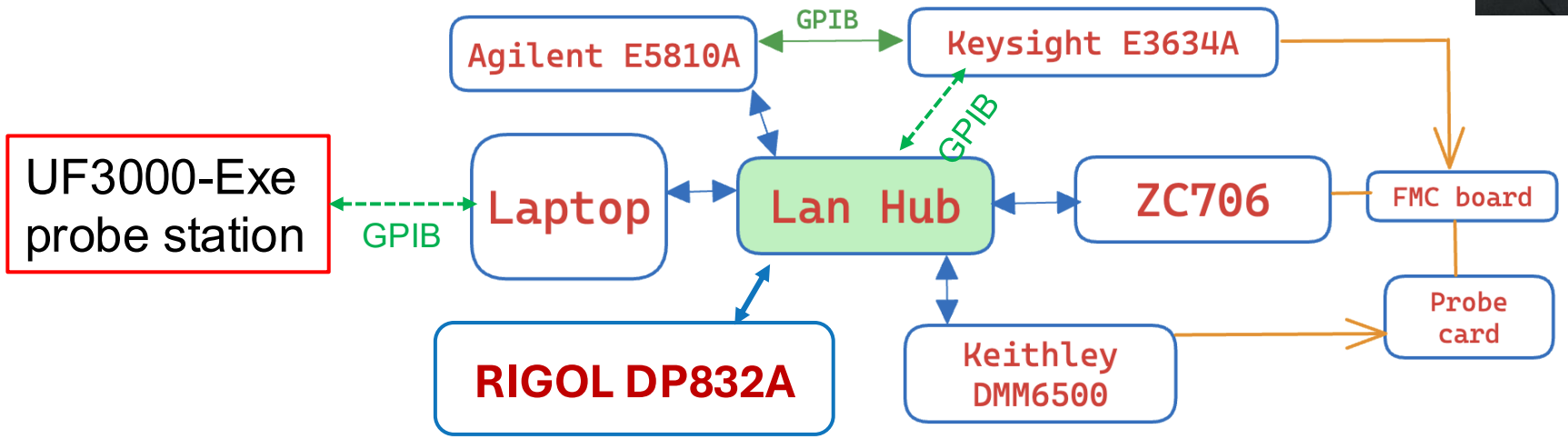
Probing System and Automated Test Workflow

Test environment setup

- Keysight E3634A: EFUSE power
- Keithley DMM6500: Measurement
- RIGOL DP832A: Vdd power
- UF3000Exe: Movement control
- Agilent E5810A: GPIB Gateway
- Laptop: Software & data processing

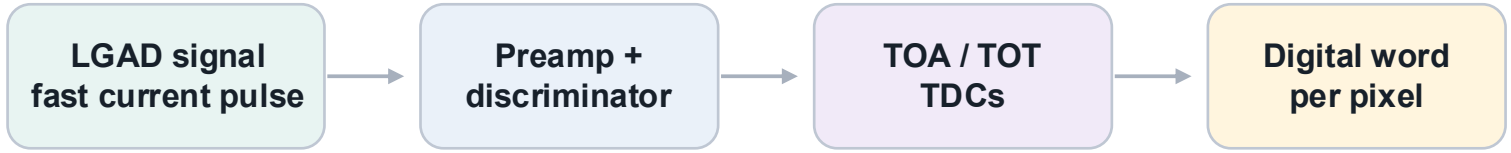






Timing Characterization: TDC and Jitter

Measurement chain



ALTIROC-A timing readout

- TOA and TOT information
- TDC binning reported as 20 ps
- Final pre-production ASIC under test

Jitter is driven by noise and signal slope

$$\sigma_t \approx N / (dV/dt) \approx \text{rise time} / (S/N)$$

Threshold choice trades efficiency/noise against the slope at crossing.

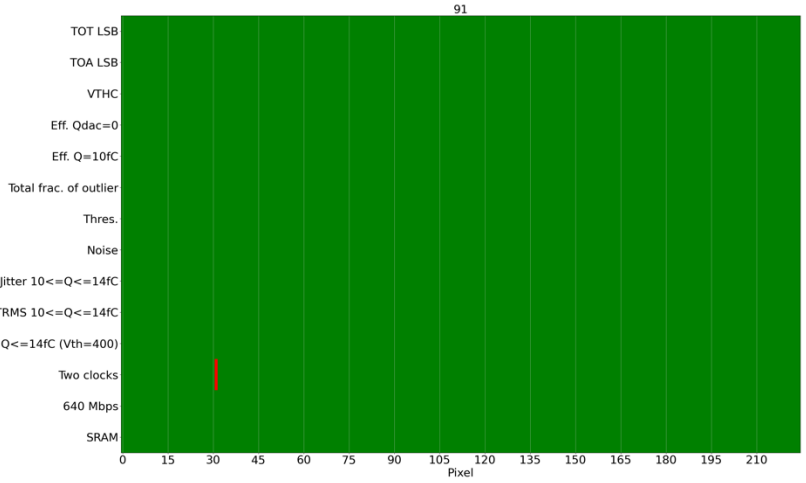
What wafer probing checks

TDC response — calibration, binning, linearity and overflow behavior
Timing RMS — jitter versus injected charge / threshold settings
Pixel spread — tails and outlier pixels rather than only the mean
Chip flag — timing anomalies enter chip-level qualification

Production relevance: timing qualification must control both average performance and pixel-level tails.

From Pixel Measurements to Chip and Wafer Qualification

Pixel-level observables



15 × 15 channels
1.3 mm × 1.3 mm LGAD pixels

Examples: threshold response, noise, injection response, TOA/TOT TDC, jitter, data integrity

Aggregation for QC

Pixel results
per-channel masks and distributions

↓

Chip summary
bad-pixel fraction + mandatory-test status

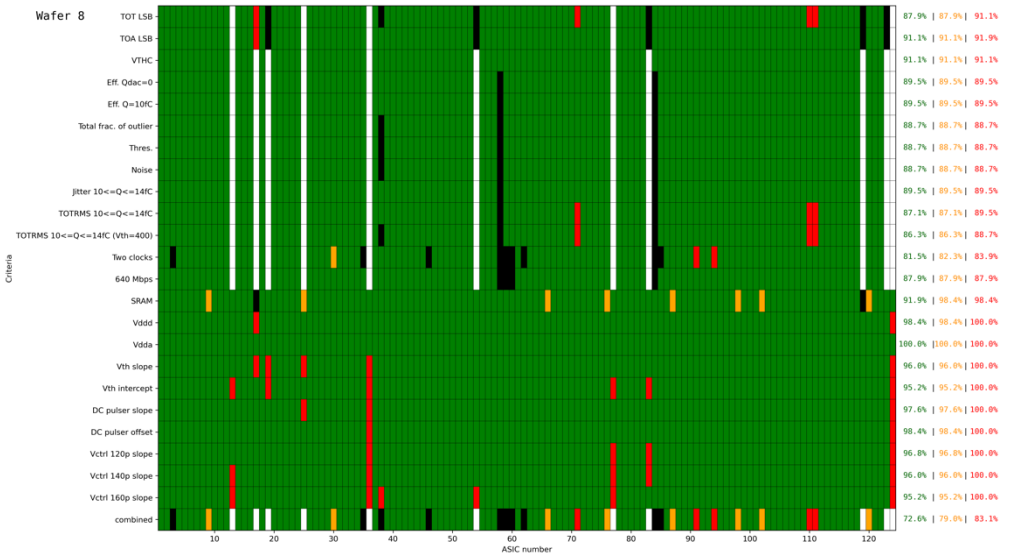
↓

Die class
qualified / marginal / failed / incomplete

↓

Wafer map
yield and spatial failure pattern

Wafer-level decision



QC principle: Separate intrinsic ASIC failures from probing-contact, DAQ, or analysis incompleteness before interpreting yield.

Pre-Production Campaign Results

20 wafers in total at preproduction stage

- 16 wafers were probed at IHEP
- 2 wafers are too old for module assembly, only for development
  - 14 wafers have been probed and efuse
- 2 wafers at IJCLab
- 1 wafer at TSMC
- 1 wafer for dicing

Brief summary

- Yields: 78%
  - 010 is one of the oldest wafer from IJCLab
- Average time cost: 1.5 days (15 hours) / wafer
  - Before automatic: 15 hours / wafer
    - Monitoring locally
    - 0.7 wafer/day
  - After automatic: 13 hours / wafer
    - Remote and testing during night is possible
    - 1.3 wafer/day (maxinum speed: 1.5 wafers/day)

Colored wafers are the wafers at China:
Red: Could be diced.
Blue: Old or not good enough for module.
Yields: Good+Ugly>=224

Wafer Number	Yields (%)	Wafer Number	Yields (%)
001 (18A4)	-- (For dev)	011 (19H2)	79
002 (1781)	77	012 (09E7)	81
003 (1686)	83	013 (06G6)	77
004 (15C3)	77	014 (05A0)	85
005 (14D0)	68	015 (04A5)	84
006 (13D5)	77	016 (02B7)	75
007 (12E2)	83	017	-- (IJCLab)
008 (11E7)	83	018	-- (IJCLab)
009 (03B2)	-- (For dev)	019	-- (TSMC)
010 (08F4)	62	020	-- (Dicing)

Understanding Yield Spread

Measured yield is a composite observable

The wafer-level decision combines true ASIC behaviour with the state of the probe contact, readout system and offline classification.

Intrinsic ASIC / wafer effects

- Non-functional pixels or local pixel clusters
- Threshold, TDC or timing outliers
- Power, I²C or digital failures
- Localized wafer-pattern signatures

Probe-contact-related effects

- Needle contamination and wear
- Contact-resistance variation
- Mechanical alignment and planarity
- Probe-card ageing / local damage

Test-system / analysis effects

- Communication or DAQ interruptions
- Incomplete scans and buffer instabilities
- FPGA / instrument state changes
- Software and criteria-version differences

Why this matters **Measured yield is a decision-quality metric, not a direct fabrication-yield measurement.**

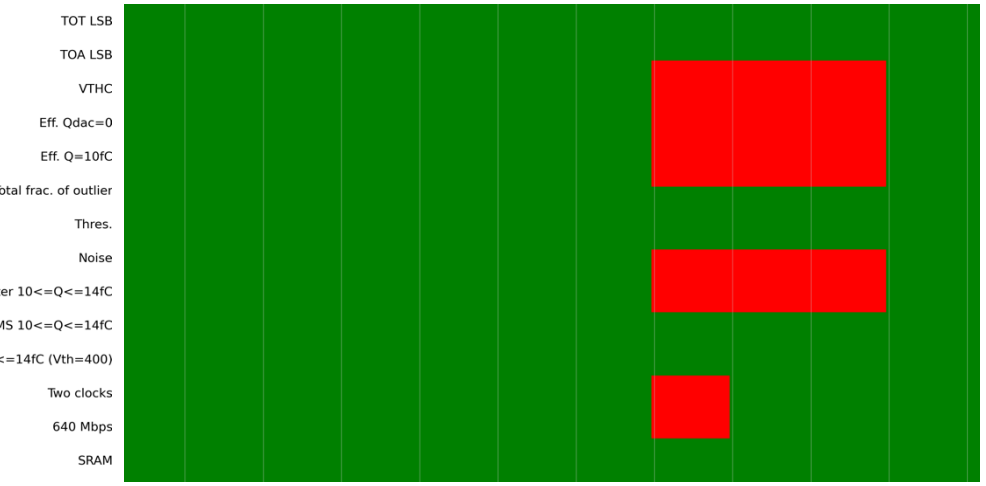
A low measured yield does not automatically imply a low intrinsic fabrication yield.

Understanding Yield Spread

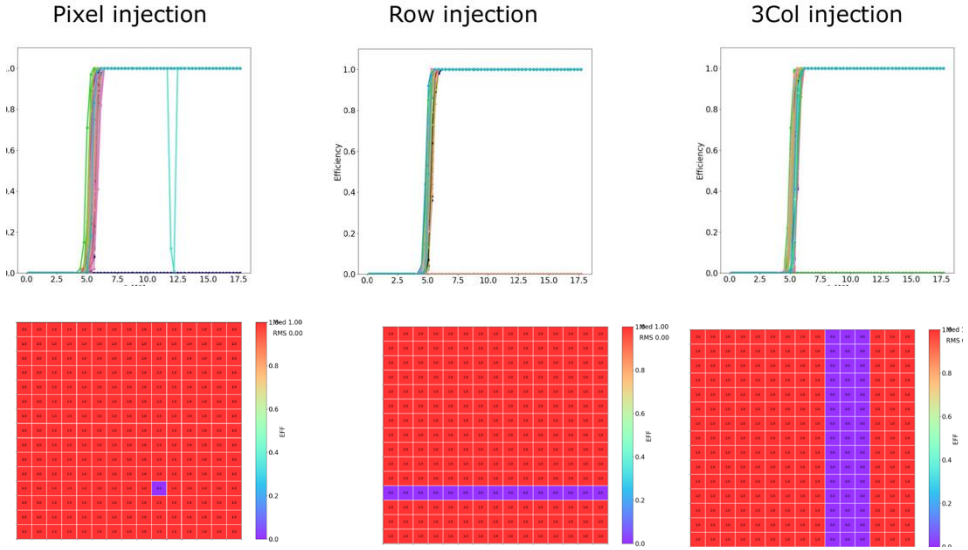
Single-pixel defect can expand through group injection

A single defective pixel was reproduced on a test board. The observed QC footprint follows the injection/acquisition granularity rather than the physical defect size.

Wafer QC map: ASIC 102



PCB injection comparison



Pixel injection
1 failed pixel

→

Row / column injection
15 failed pixels

→

Three-column injection
45 failed pixels

→

Wafer flow example
CHARGE: 135–179
SPEED: 135–149

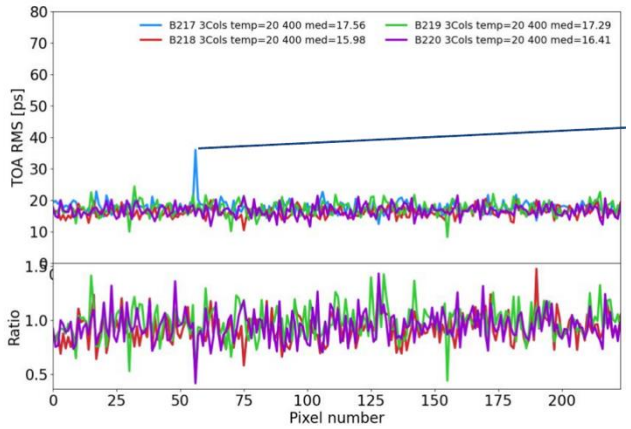
Injection mask → **Shared pulser / acquisition** → **Per-pixel QC result**

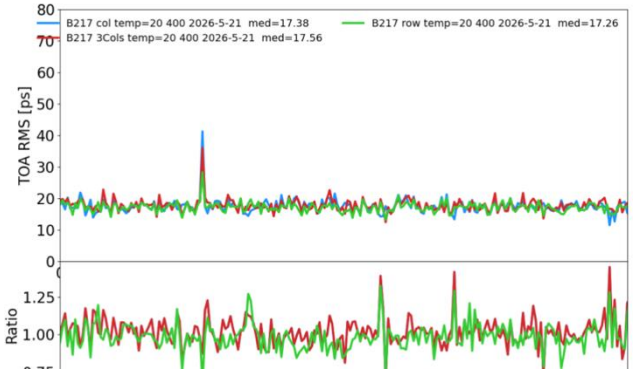
Possible couplings: shared pulser loading, busy/buffer effects, or group-level data loss. The exact mechanism is not yet uniquely identified.

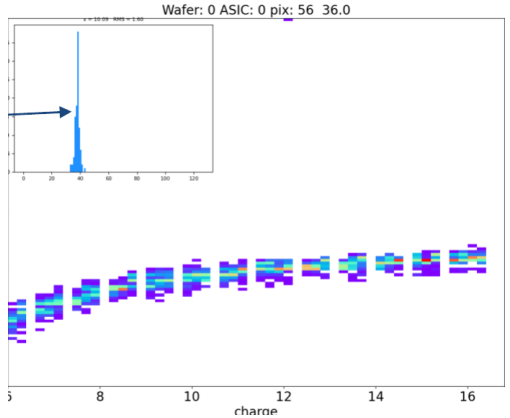
Physical defect size ≠ QC failure footprint.

Understanding Yield Spread

Retest checks whether the same pixel signature is reproduced







PCB retest: one local outlier observed at B217 pixel 56

Wafer-probing candidates

B217 / ASIC 9: pixel 208
B218 / ASIC 36: pixel 130
B219 / ASIC 75: pixel 202
B220 / ASIC 79: pixel 220

PCB observations

TOA RMS medians ≈ 16–18 ps
Originally flagged wafer pixels not reproduced
B217 pixel 56 showed ≈ 36 ps
Elevated under column, row and 3-column injection

Repeatable local outlier under the PCB condition—not a reproduction of the wafer-level pixel signature.

Analysis note: historical QC used Vth = 400, Q = 10 fC, 100 events and direct TOA RMS; ≈36 ps is above the historical ugly threshold of 35 ps but below the bad threshold of 50 ps. Later analysis averages Q = 10–14 fC and suppresses isolated TOA values.

Understanding Yield Spread

A traceable decision requires evidence beyond one scan

The goal is to classify the outcome—not simply the die—so that production data retain physical meaning and operational actionability.

Observed anomaly
pixel, timing, DC or scan failure

→

Validate scan integrity
health checks • logs • completion

→

Controlled re-test
reset / re-contact / repeat

→

Independent cross-check
testboard or later test stage

→

Final category

Traceable outcomes

Intrinsic failure
persistent pattern; reproduced independently

Contact / setup issue
changes with contact or instrument state

Incomplete test
scan interrupted or corrupted; not a physics decision

Retest required
evidence insufficient; condition and action recorded

Only results that survive this chain should contribute directly to the intrinsic-yield estimate.

Operational Lessons from Wafer Probing

The probing system is part of the instrument

Robust wafer probing is achieved by controlling the measurement chain with the same discipline applied to the ASIC under test.

1 Contact quality

Probe-card cleanliness, contact resistance, alignment and planarity must be monitored as operational variables—not treated as background conditions.

2 Online monitoring

Health checks and live diagnostics are needed to identify abnormal scans before they propagate into wafer-level classification.

3 Controlled re-test policy

Ambiguous cases require defined actions: re-contact, reset, repeat, flag incomplete, or escalate to independent cross-check.

4 Versioned decision chain

Test scripts, analysis code and acceptance criteria must remain synchronized, traceable and frozen for each production period.

Operational reliability protects both production throughput and the physical interpretation of the yield.

Toward Production-Scale Quality Control

Close the loop: measurement → evidence → action

The target is not only a wafer map, but a centralized and self-improving QC system that makes each production decision reproducible.

Probe wafer
Frozen production test sequence
Automated probing / DAQ health checks

→

Store evidence
Raw data, logs, plots and wafer maps
Derived quantities and version metadata

→

Analyse failures
Intrinsic vs contact vs incomplete
Pattern recognition across dies and wafers

→

Act and maintain
Probe-card inspection / cleaning
Criteria and software updates under version control

→

Stable QC
Traceable acceptance
Long-term trend monitoring

Production enablers

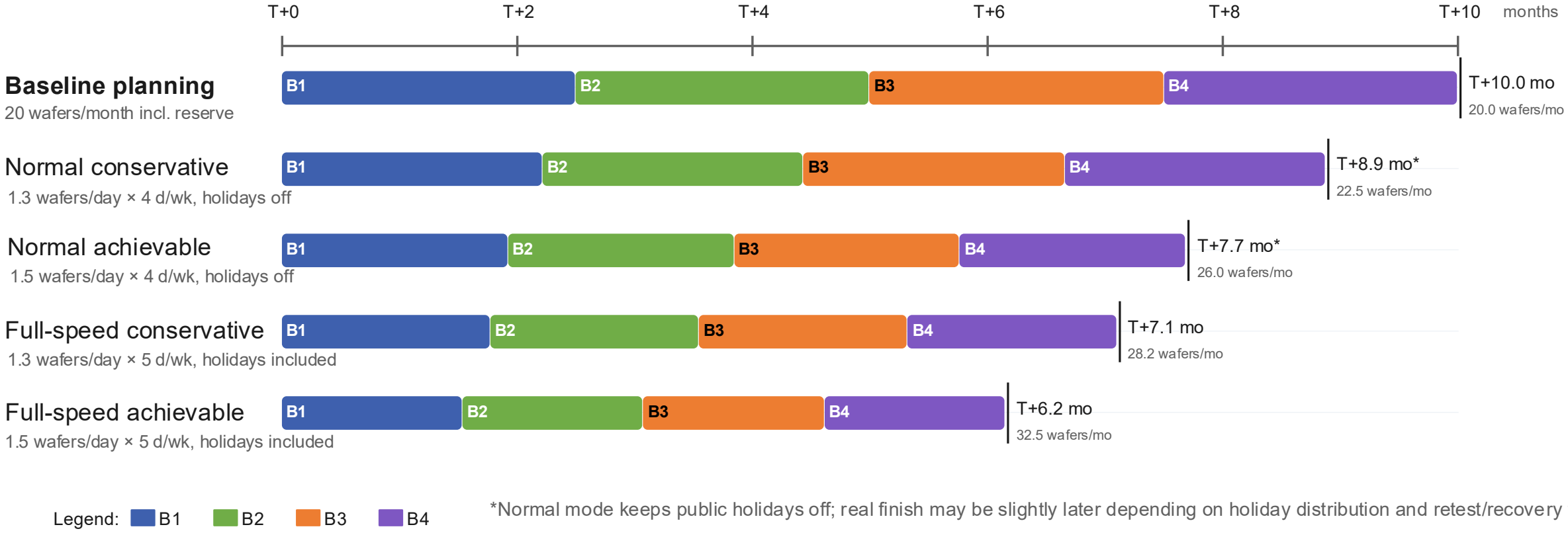
- Stable and traceable acceptance criteria
- Automated health checks for probing and DAQ
- Defined probe-card inspection and maintenance procedures
- Centralized database linking wafer maps, raw data and derived quantities
- Long-term trends across wafers and production batches
- Cross-checks with later chip / module-level tests

Production QC becomes robust when every wafer measurement feeds the next measurement decision.

Production Schedule

Assumptions

Per wafer: 124 ASIC × 6.5 min = 806 min ≈ 13.4 h; with overhead ≈ 14 h | **Practical rate:** 1.3–1.5 wafers/day | **Planning reserve:** ~20 wafers/month baseline



*Normal mode keeps public holidays off; real finish may be slightly later depending on holiday distribution and retest/recovery time.

- Estimated rate from current experience:
  - IHEP ~ 6.5 mins per ASIC -> 15 hours per Wafer
  - About 20 wafers per month as baseline, possible increasing to 25 wafers per month
- From latest schedule: Production probing started at 2026-05, lasting about 10 months

Summary

- An automated wafer probing workflow has been established for ALTIROC-A production QC.
- Pixel measurements are translated into chip- and wafer-level qualification through a traceable QC chain.
- Measured wafer yield is a composite observable, reflecting both intrinsic ASIC behavior and the probing/test environment.
- Group-based injection can amplify a local defect into a much larger QC failure footprint, motivating careful interpretation of wafer maps.
- Production-scale testing is now in progress with automated operation, version-controlled analysis and centralized QC.


Thanks!
Good probes make
good physics possible!
PROBE STATION
HGTD TEAM
ALTIROC-A
LGAD
HL-LHC
High time resolution
Reliable production
Better detector
Exciting physics
On the way!