

MVT (Multi-Voltage Threshold)

➤ 多阈值电压采样法

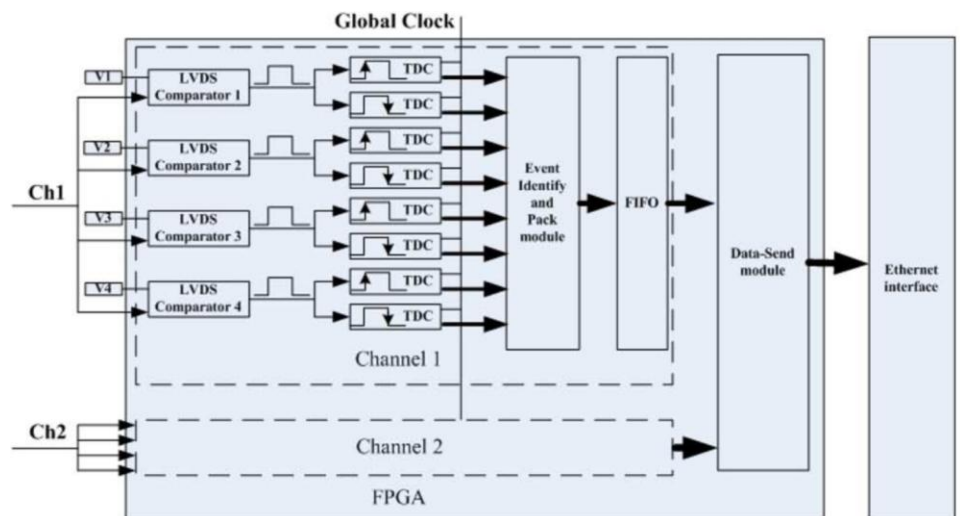
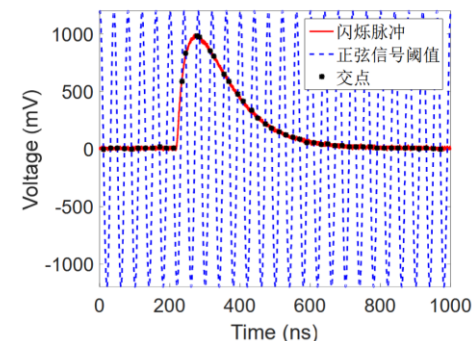
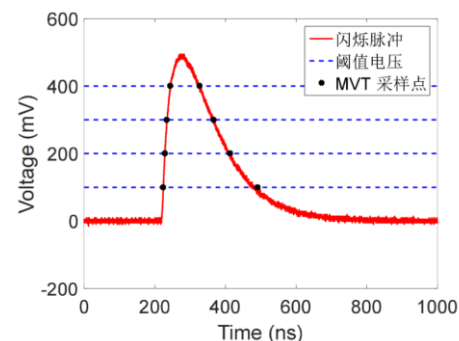
- 利用FPGA内部LVDS比较器进行采样
- TDC: FPGA内延迟链技术
- 固定阈值; 函数阈值

➤ 目前已有研究

- [1]:
 - FPGA: Altera EP2C70F896C7;
 - 时间分辨: ~ 310 ps
- [2]:
 - FPGA: Lattice ECP3
 - 时间分辨: ~ 20 ps

➤ 时间分辨取决于

- FPGA器件的LVDS比较器的建立时间
- TDC on FPGA算法
- 探测器



[1] IEEE Transactions on Nuclear Science, 2013, 60(5): 3253-3261.

[2] Journal of Instrumentation, 2011, 6(12): C12004.

固件开发

GIT storage: `git@code.ihep.ac.cn:yuanmk/mvt-evaluation-firmware.git`

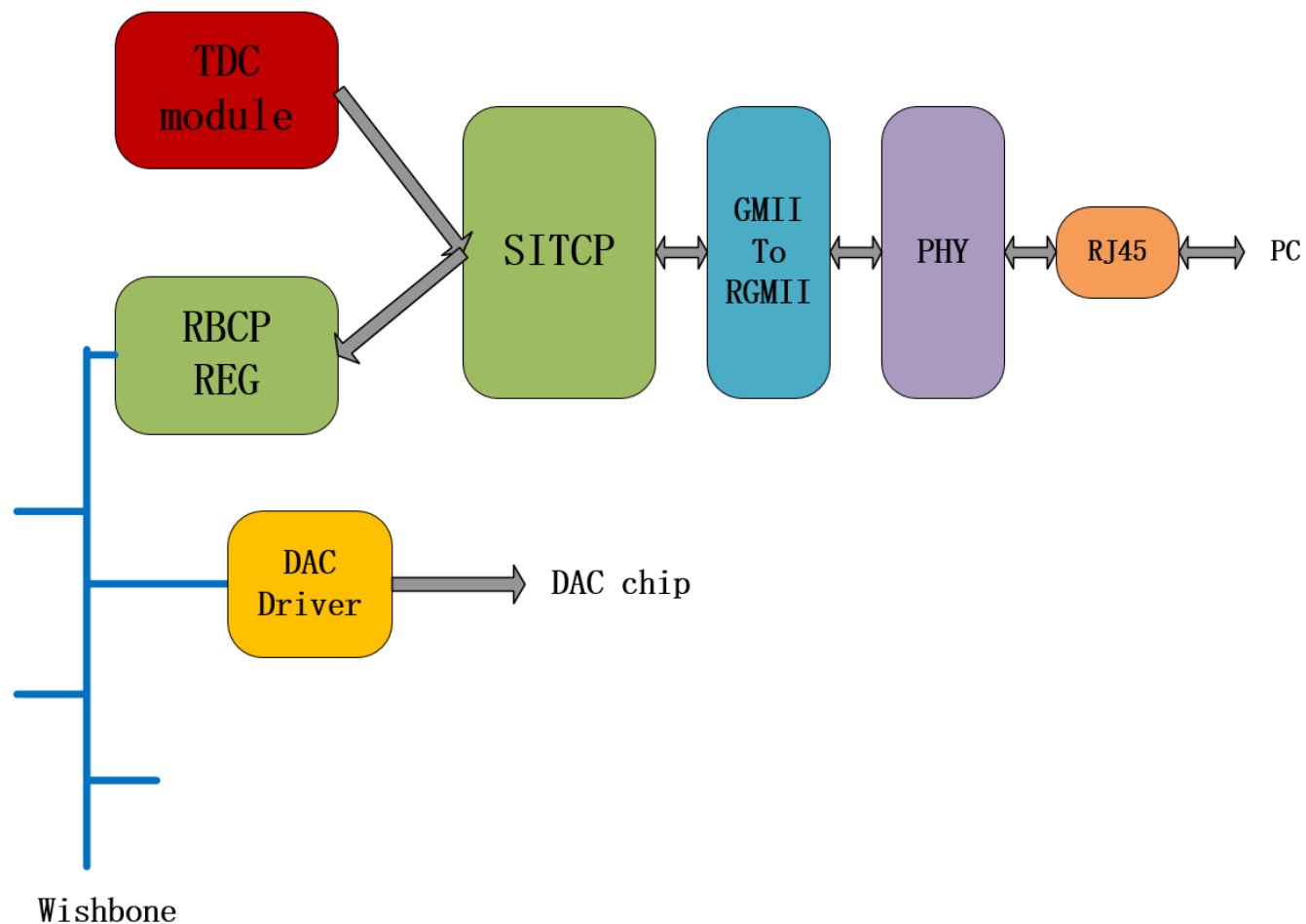
整体架构

- SiTCP

- 网口通信

- Wishbone总线控制dac芯片

- TDC模块

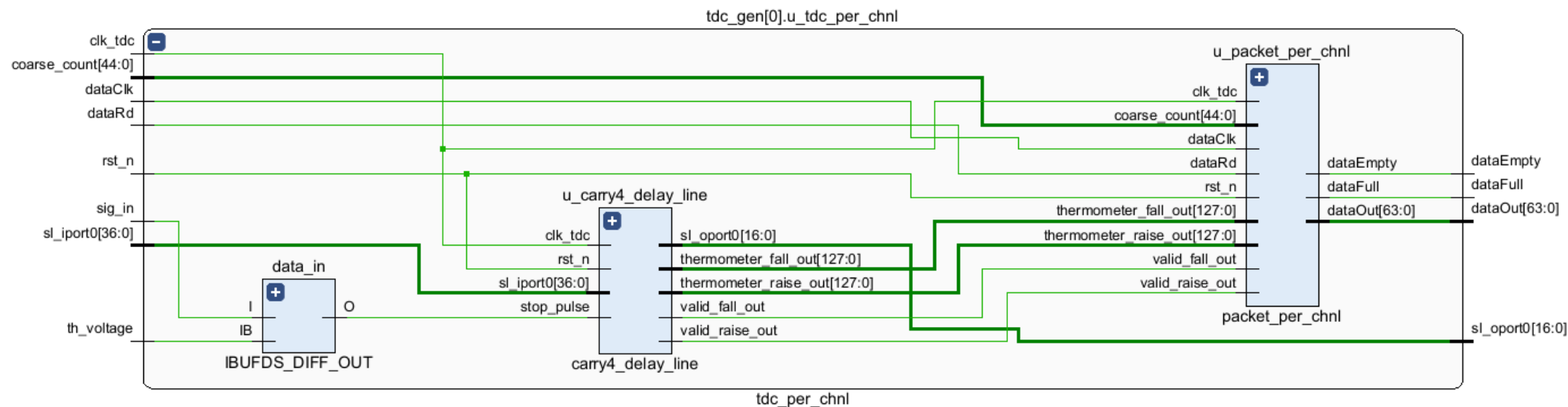
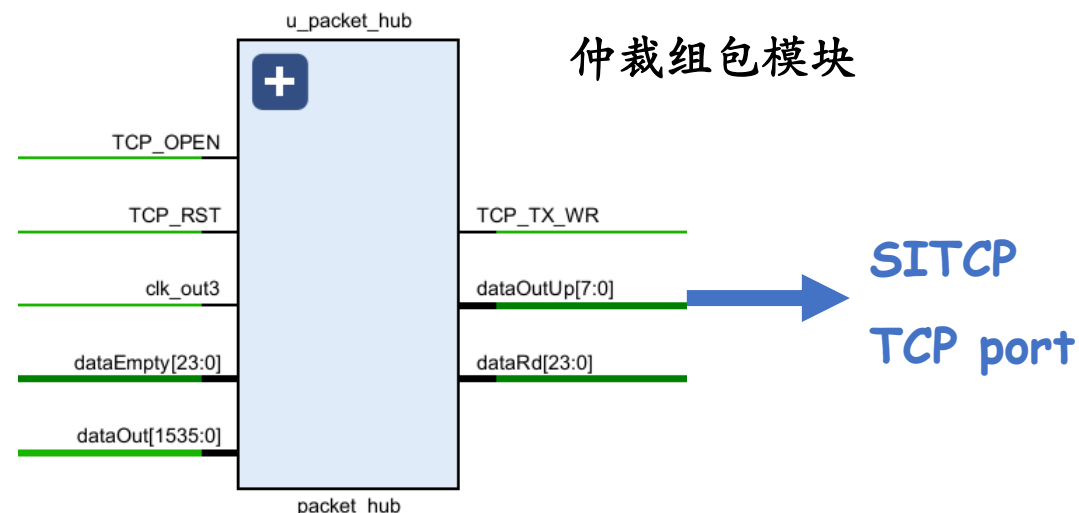


整体架构

固件开发

TDC模块开发-整体架构

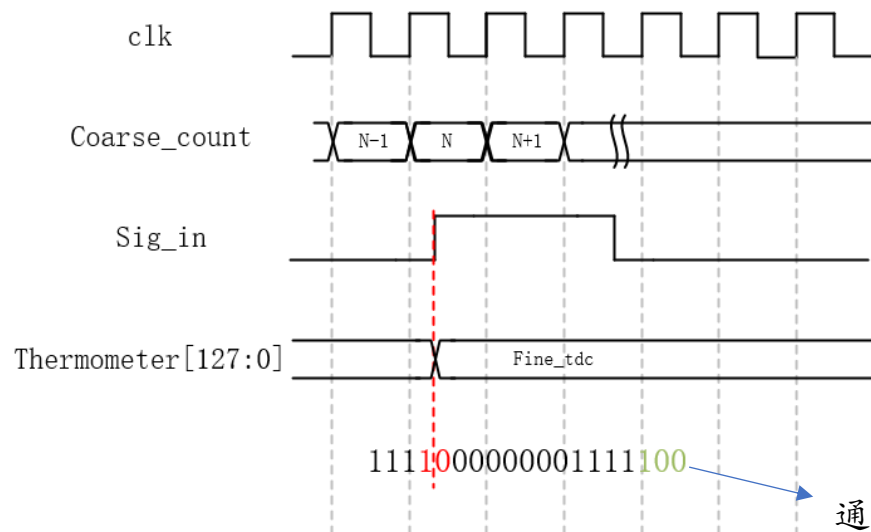
- Carry4_delay_line
- Packet_per_chnl
 - Thermometer_encoder
- Coarse_count



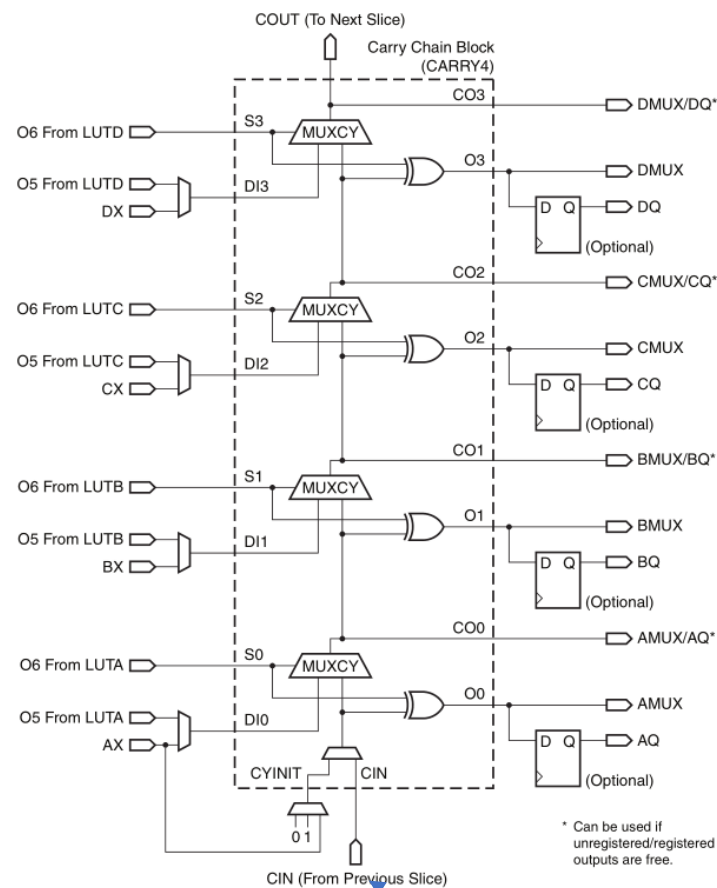
固件开发

CARRY4进位链

- 32个CARRY
 - 128级抽头
 - $128 * 20\text{ps} = 2.56\text{ ns}$
 - 覆盖粗时间戳范围
- 粗时间戳
 - 400 MHz
 - 2.5 ns



通过解码模块获得最终细时间戳



两个寄存器变为1的时间差~20 ps

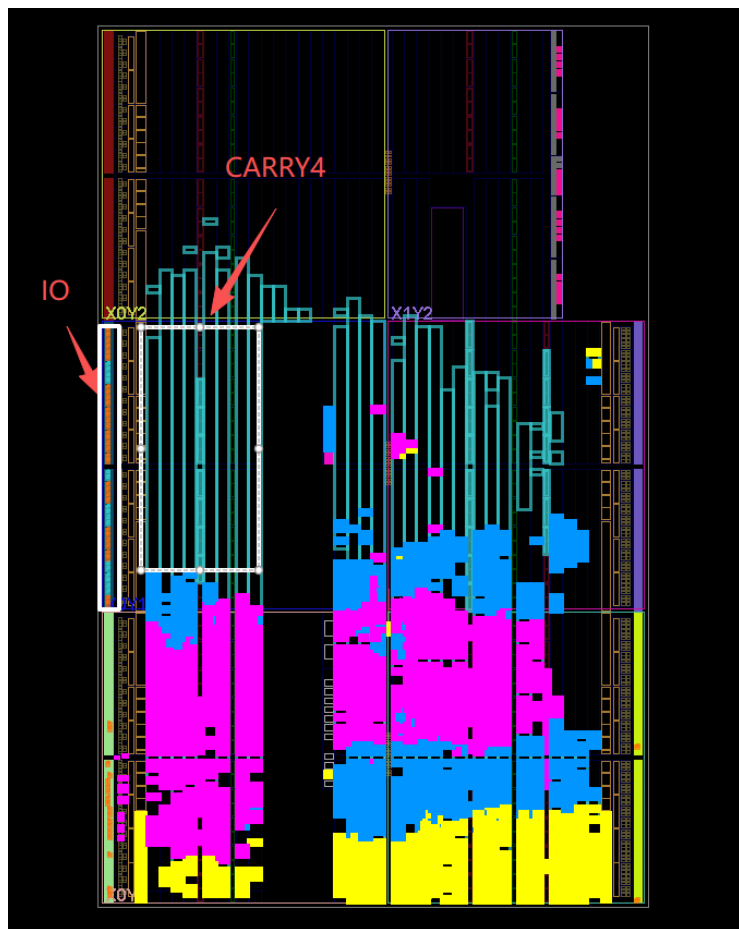
输入 1

CARRY4 原语

固件开发

CARRY4进位链位置约束

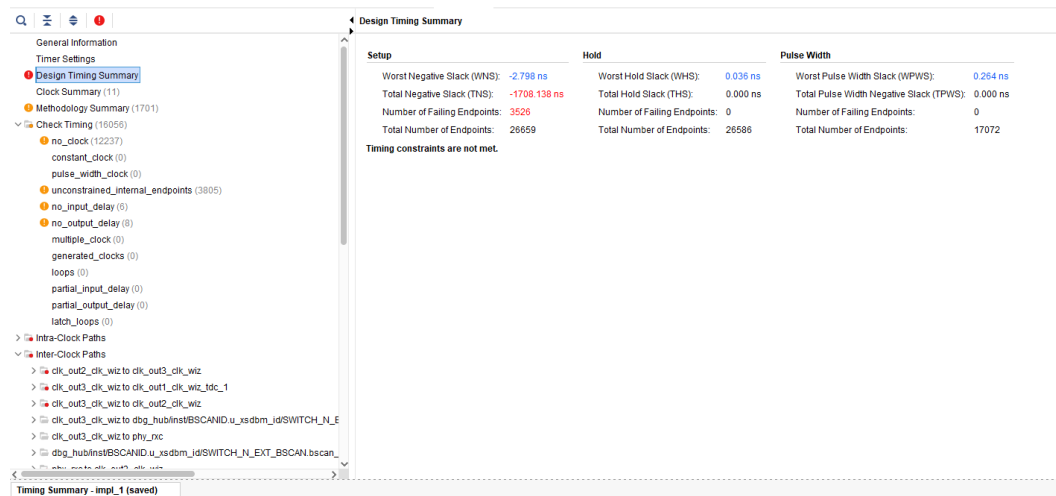
- 约束第一级CARRY4原语位置



TODO:

- 时序约束

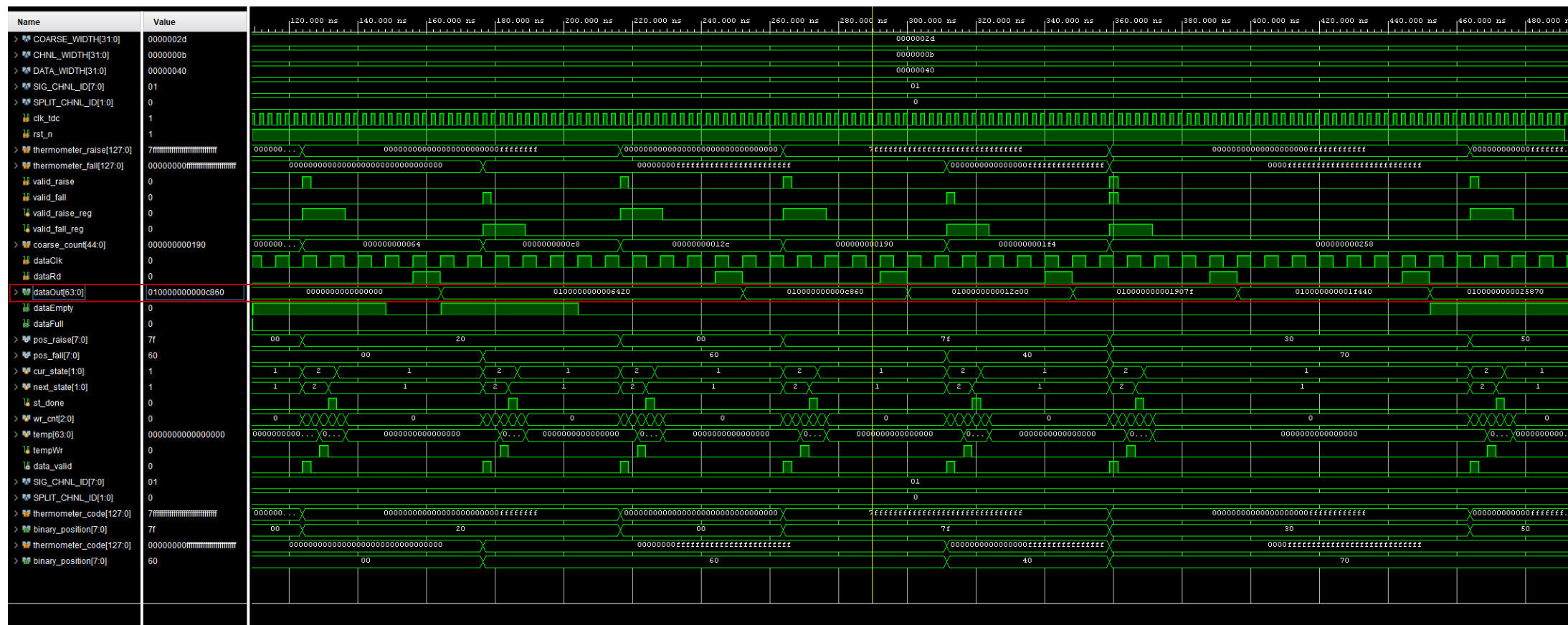
```
always @(posedge stop_pulse_bufh or negedge rst_n) begin
    if(!rst_n) begin
        thermometer_raise_async <= 0;
        valid_raise_async <= 1'b0;
    end
    else begin
        for (k = 0; k < NUM_CARRY4; k = k + 1) begin
            // Sample each CARRY4's 4 taps
            // Note: In actual implementation, each tap shou
            // specific outputs of CARRY4 (C00, C01, C02, C
            // Currently using carry[k] for all taps as a p
            thermometer_raise_async[k*4 + 0] <= carry[k];
            thermometer_raise_async[k*4 + 1] <= carry[k];
            thermometer_raise_async[k*4 + 2] <= carry[k];
            thermometer_raise_async[k*4 + 3] <= carry[k];
        end
        valid_raise_async <= ~valid_raise_async;
    end
end
```



固件开发

子模块仿真

➤ Packet_per_chnl



固件开发

数据传输结构

Packet_hub 模块

数据包格式（64位）：

- [63:56] - SIG_CHNL_ID（8位信号通道号）
- [55:54] - SPLIT_CHNL_ID（2位拆分通道号）
- [53] - 边沿标志（1：上升沿，0：下降沿）
- [52:8] - coarse_count[44:0]（45位粗计数器）
 - 400 MHz时钟，范围约为1.75 h
- [7:0] - position[7:0]（8位精细位置，0-127）

TODO:

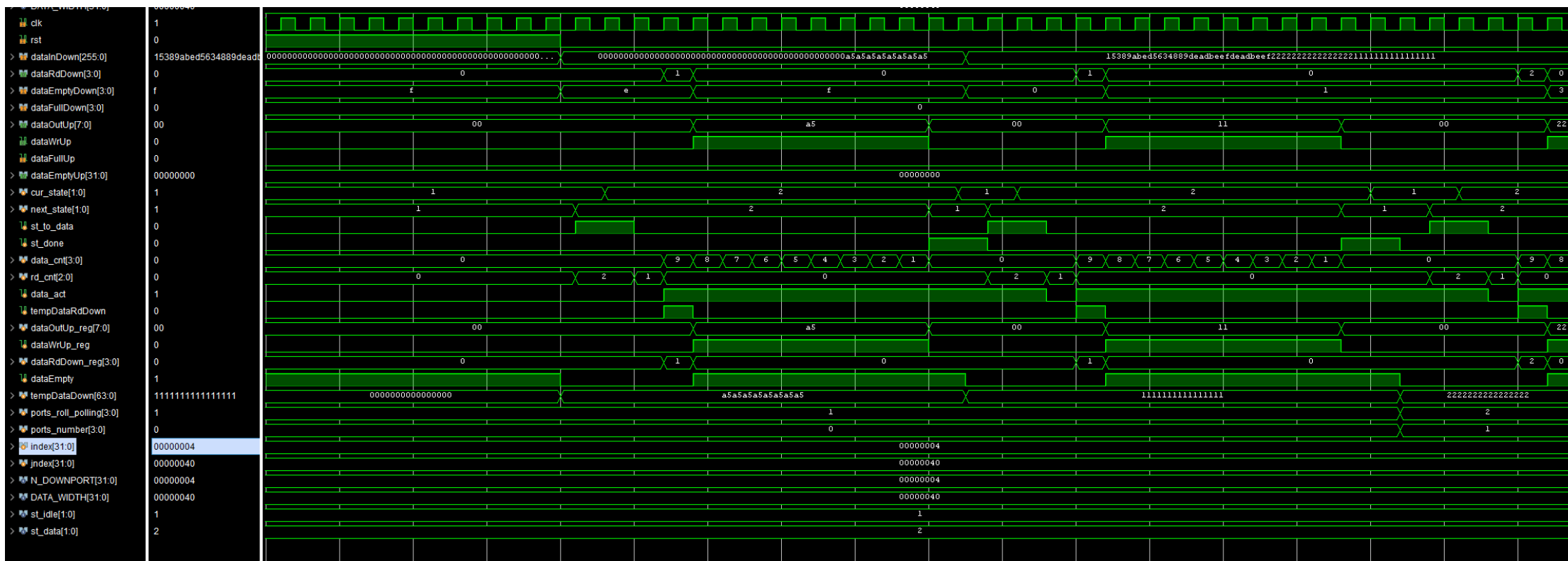
添加包头包尾定位符

固件开发

子模块仿真

➤ Packet_hub - task1

传输byte检查

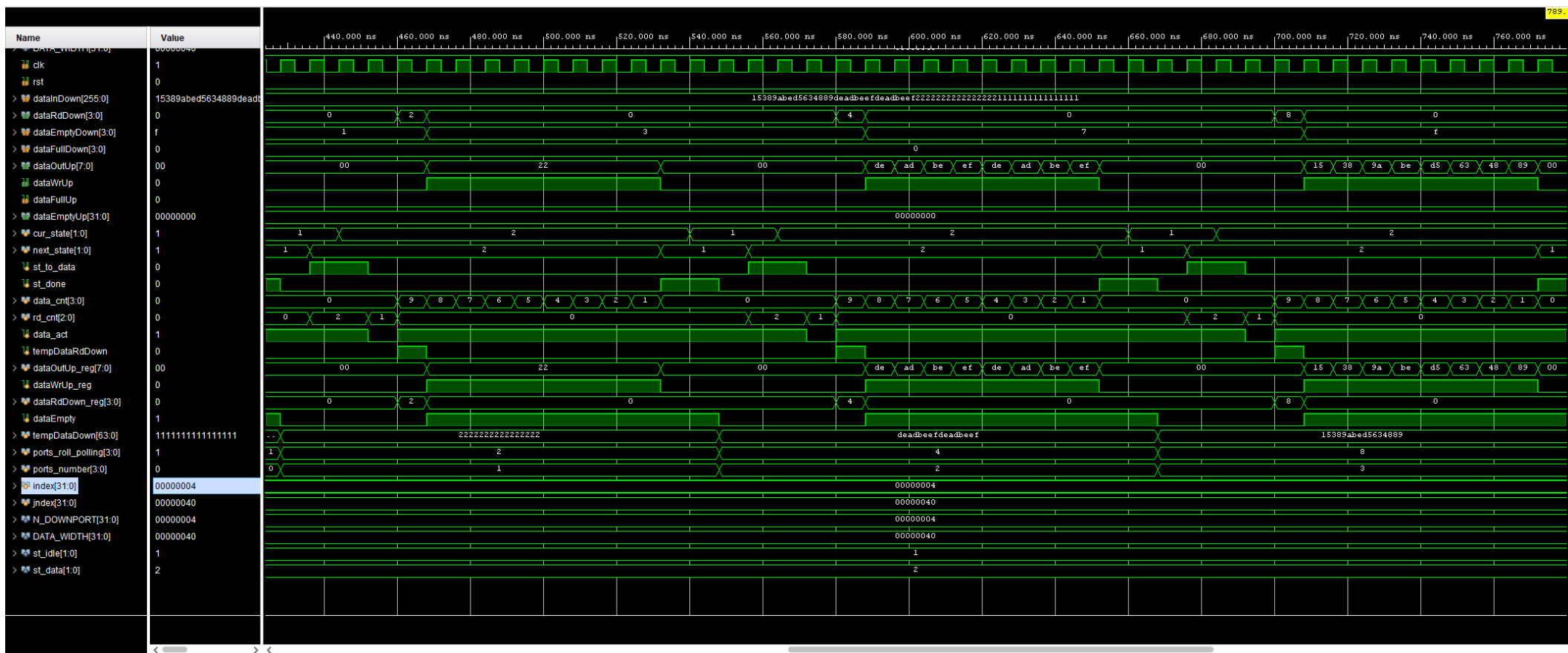


固件开发

子模块仿真

➤ Packet_hub - task1

传输byte检查



固件开发

子模块仿真

➤ Packet_hub - task3

传输中进行重置

