

# Progress of TPC module and prototype R&D

Huirong Qi

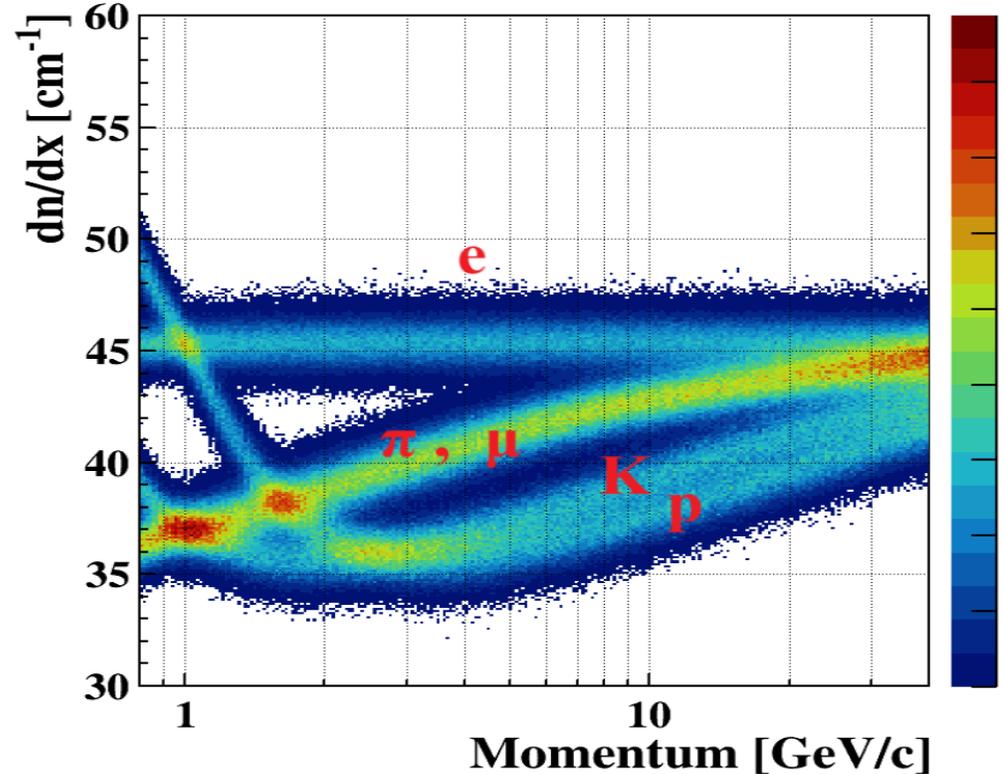
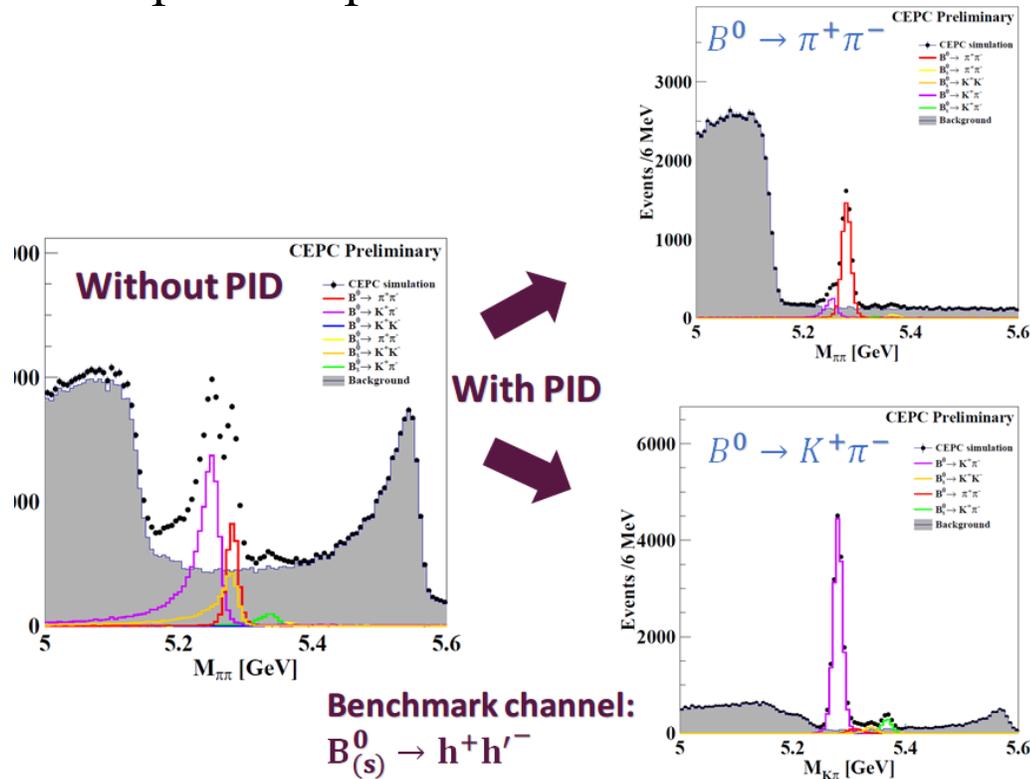
21 January 2026, IHEP

- **Motivation**
- **High granularity readout R&D**
- **Status of TPC module and prototype**
- **Work plan and summary**

# Motivation: Physics requirements in CEPC

- Circular e+e- collider operation stages in TDR: **10-years Higgs @3T** → **2-years Z pole** → **1-year W**
- Gaseous tracker leading contribution to PID and the high resolution: jet & differential
  - High granularity readout and better than  $2\sigma$  separation power between  $\pi$  and  $k$  for P using  $dn/dx$

**Calibration: Low luminosity Z at 3T**  
 Approximately  $10^{35} \text{cm}^{-2}\text{s}^{-1}$   
 20% of high luminosity Z



## TPC technology detector for e+e- collider

### Pad readout TPC

- To meet Higgs physics
- 1mm × 6mm of Pad
- < 100mW/cm<sup>2</sup>
- dE/dx
- Triple, double GEMs
- Micromegas

### Pixelated readout TPC

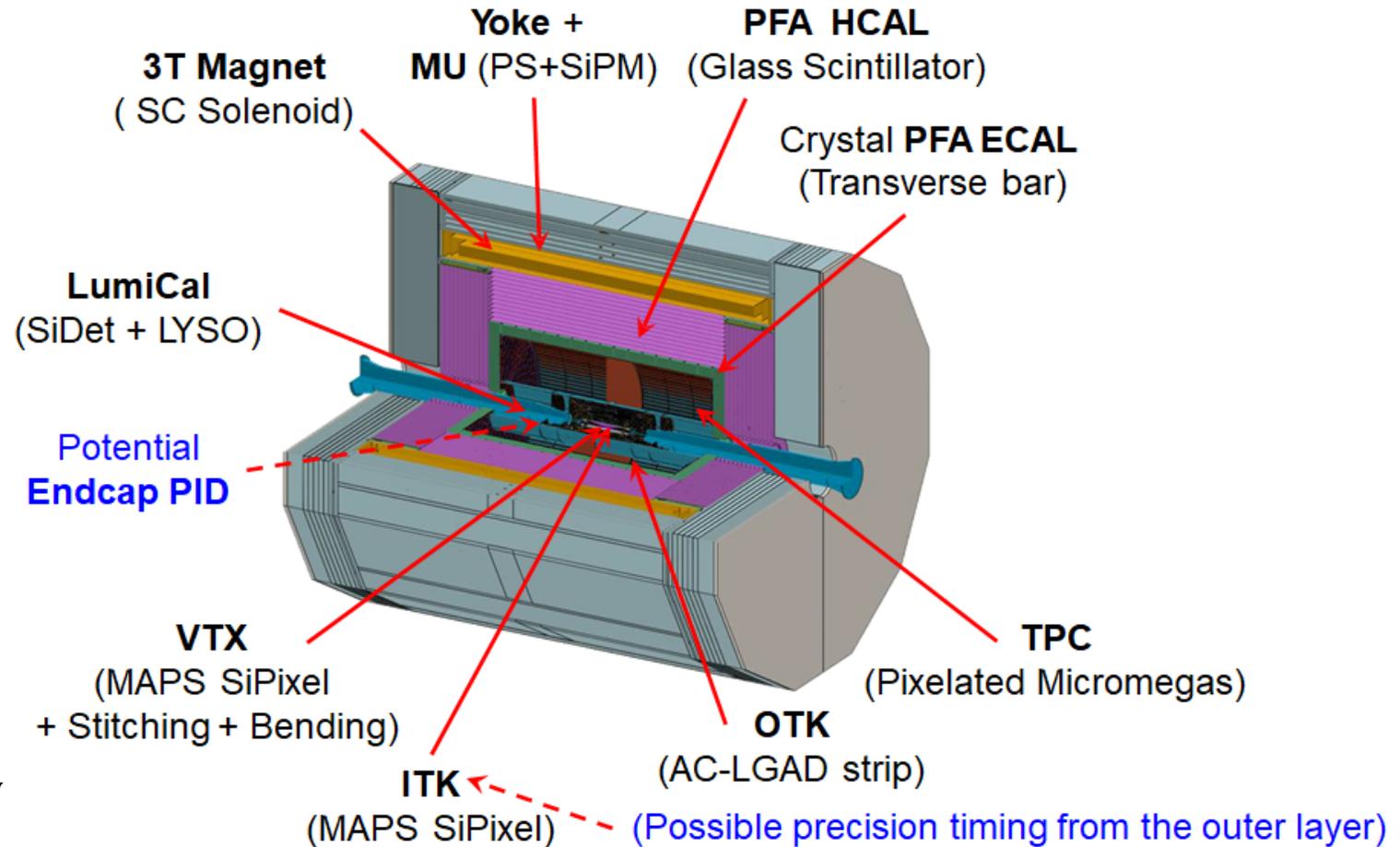
- To meet Low-lumi Z physics
- TPX3 and TPX4
- ~1W/cm<sup>2</sup>
- dN/dx+dE/dx
- GirdPix
- Interposer
- Direct mode



- CEPC community initiated the technical comparison and selection, balancing factors including **R&D efforts, detector performance, cost, power consumption and construction risks.**

# Baseline Detector Design in TDR

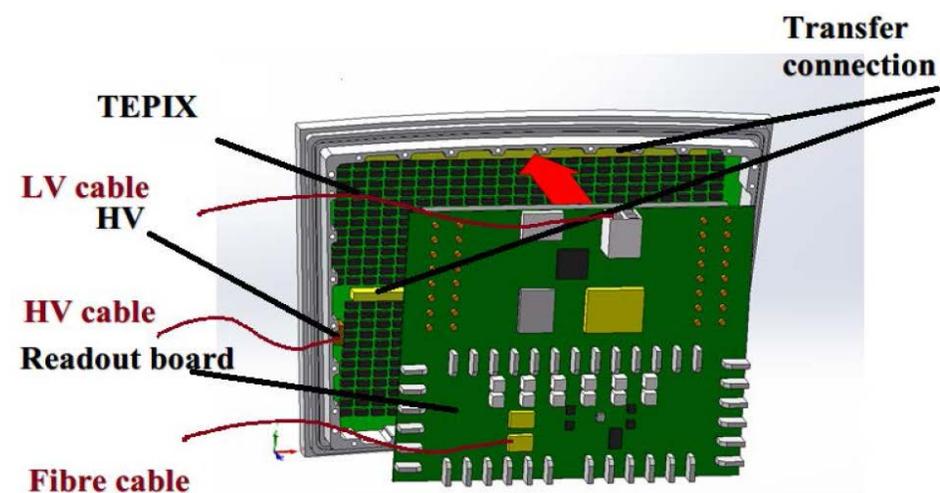
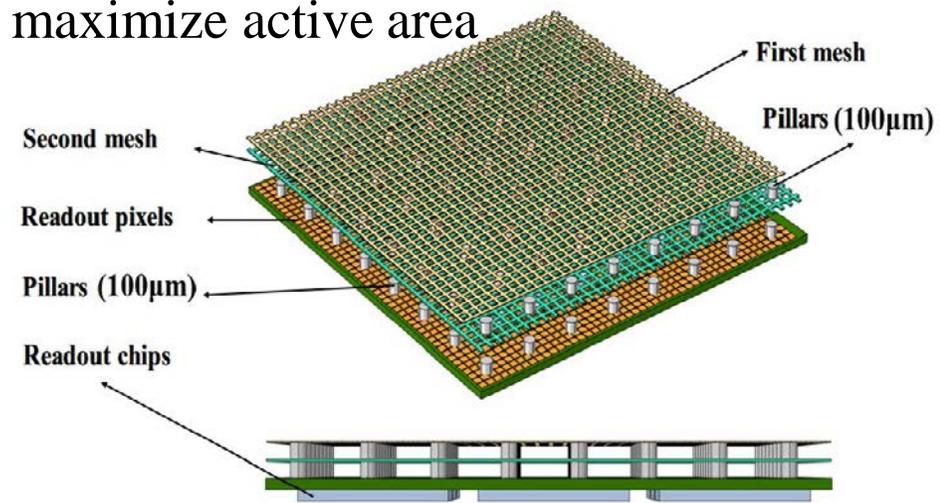
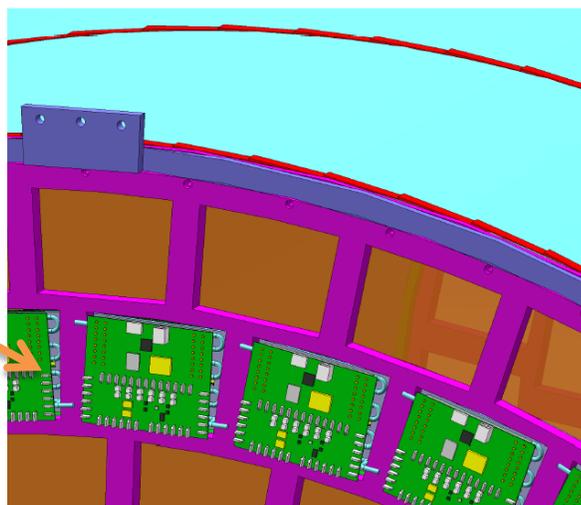
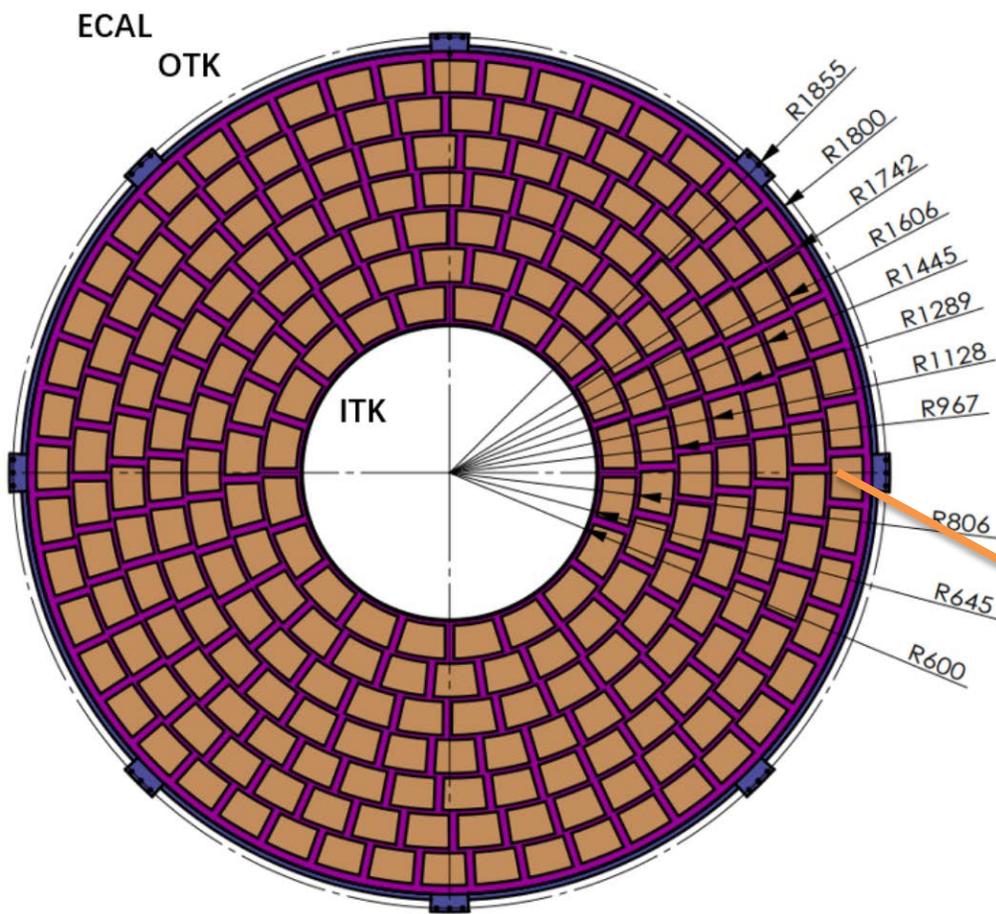
- Will explore the possibilities of
  - A forward PID detector inside TPC
  - The outer layer ITK also provides precision timing
- After 10-year operation, the majority will remain, a few may be upgraded, including
  - VTX: for a better performance and radiation tolerance
  - TPC: to deal with higher luminosity



<https://arxiv.org/abs/2510.05260>

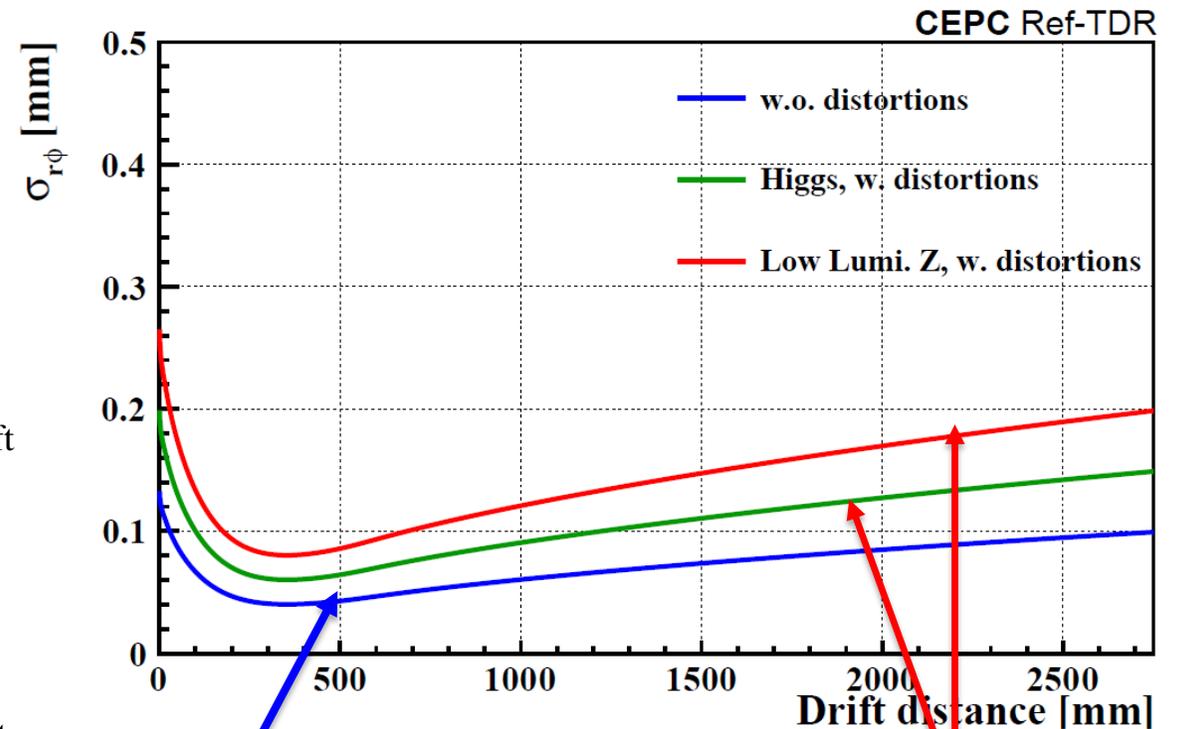
# Readout module design

- Readout modules on the endplate
  - 25mm thick aluminum endplate: 7 layers of windows along the radial direction
  - Readout modules with support frame installed in windows to maximize active area



# Full Simulation of High granularity readout TPC – Spatial resolution

- Impact of space-point distortions on spatial resolution
  - Space-point distortions can be corrected by the data-driven track-based calibration
  - Error contributions to the calibrated spatial resolution :
    - Space-charge distortion:  $< 80\mu\text{m}$  in Higgs,  $< 160\mu\text{m}$  in low-lumi. Z, dependent on  $L_{\text{drift}}$
    - NUMF effects on the drift process (after correction with B field map):  $< 65\mu\text{m}$
- Conservatively estimated, the calibrated spatial resolution degrades by  $\sim 50\%$  and  $100\%$  at the point with the longest drift distance in Higgs and low-luminosity Z modes respectively.

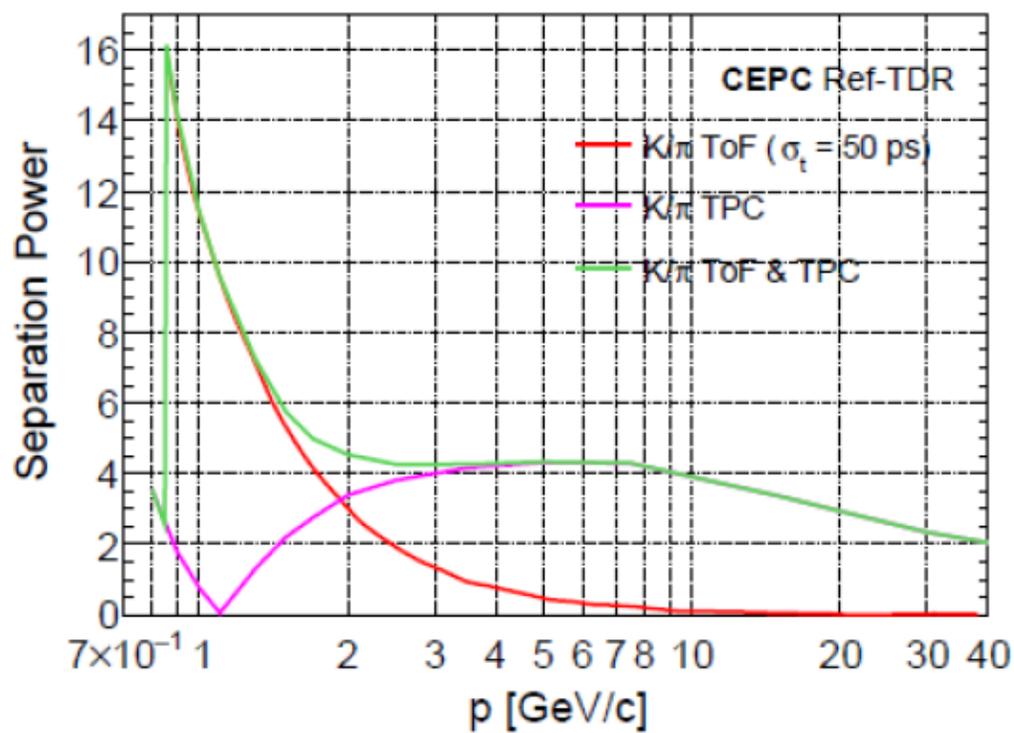


Taking into account space-point distortions with calibration and correction

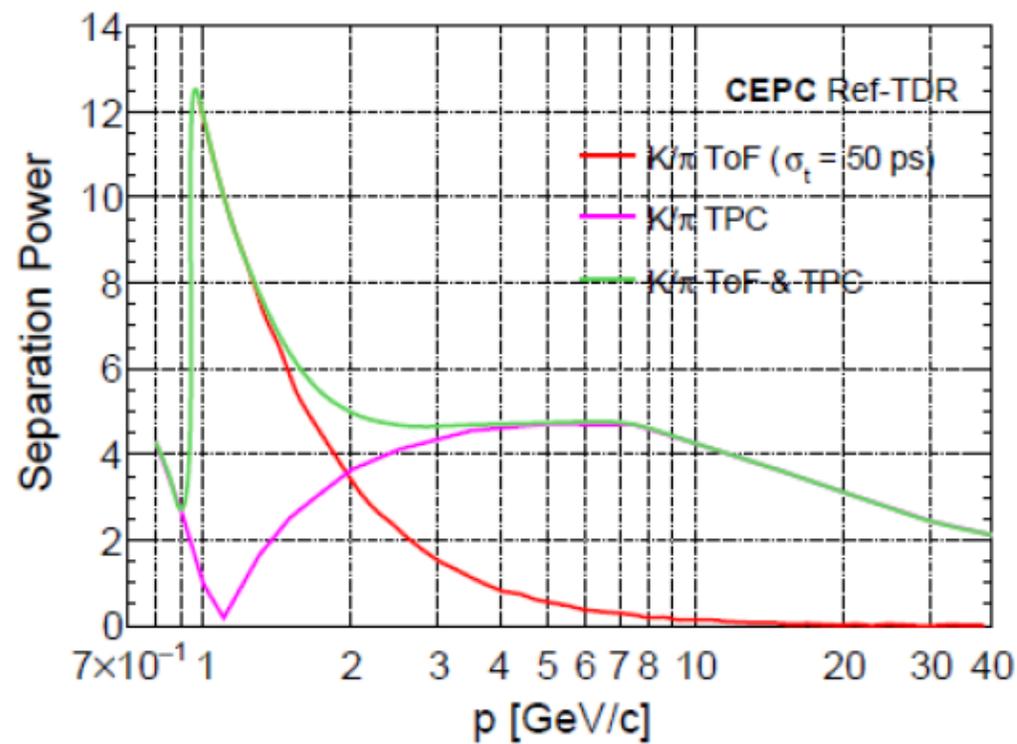
# Full Simulation of High granularity readout TPC – PID performance

- $K/\pi$  separation power using the combined information of ToF and TPC
  - ToF information compensates for momentum range of around 1 GeV/c
  - Larger than  $3\sigma$  separation between  $K/\pi$  with momentum up to 20 GeV/c

$$\eta_{A,B} = \frac{|\mu_A - \mu_B|}{\sqrt{(\sigma_A^2 + \sigma_B^2)/2}}$$



(a)  $\theta = 85^\circ$



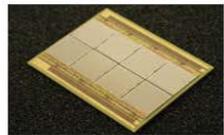
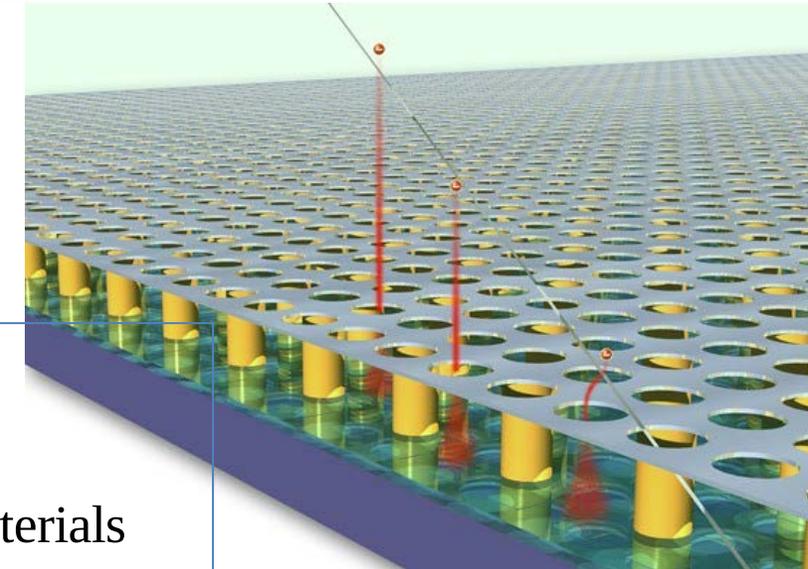
(b)  $\theta = 60^\circ$

# High granularity readout: Micromegas - GridPix

- GridPix from Timepix3 to Timepix4 ASICs. Tests with quad devices have been successfully done under  $B=1.0T$  at DESY.
- Very high detection efficiency results in excellent tracking and  $dE/dx$  performance. All results showed that a pixel TPC is realistic. ( $\sim 10^6$  events)

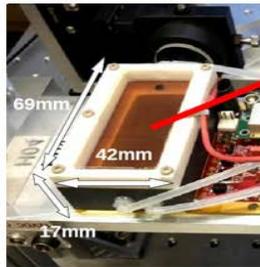
- **Key issues to address**

- High power consumption ( $2W/cm^2$ )
- Unable to self-develop, limited by high-end photolithography mask materials

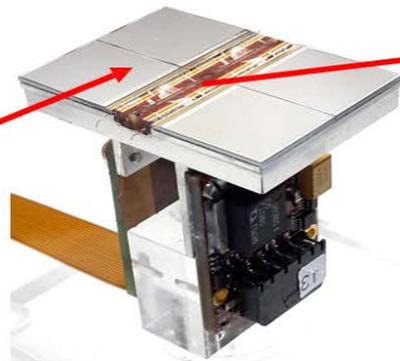


(Octopuce)

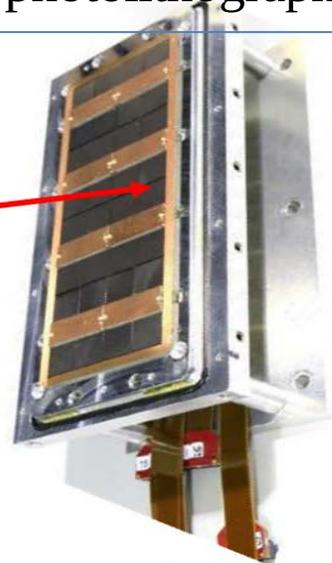
TimePix1  
2007



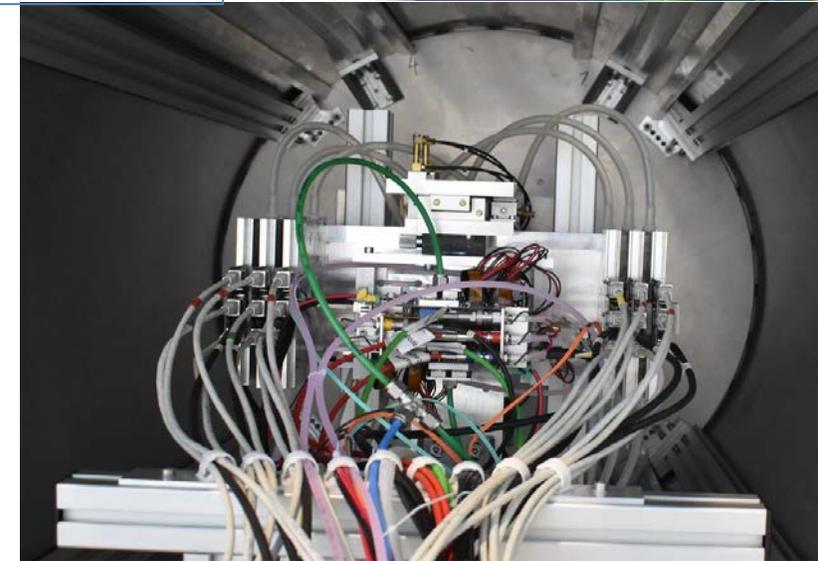
TPX3 chip  
2017



Quad  
2018



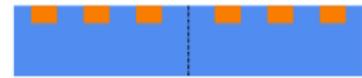
Module  
2019



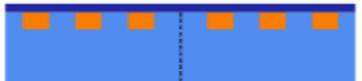
NIM A535 (2004) 506-510  
NIM A845 (2017) 233-235

# Production: Micromegas - GridPix

- The Timepix3's pixel pitch of  $55\ \mu\text{m} \times 55\ \mu\text{m}$  is matched by a grid with  $35\ \mu\text{m}$  diameter circular holes.
- The  $1\ \mu\text{m}$  thick aluminium grid is supported by  $50\ \mu\text{m}$  high SU8 pillars.



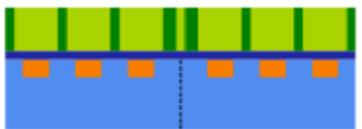
1. The wafer is prepared: the chips are probed to find electronic failures and the surface is cleaned



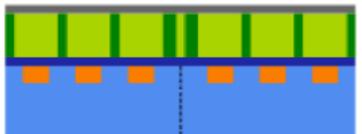
2. A high-resistive  $4\ \mu\text{m}$  thick SiRN protection layer is deposited on the chip in order to protect the chip from discharges. A protection layer on the bonding pads would hinder electrical connections, and is avoided by temporarily covering them with polyamide.



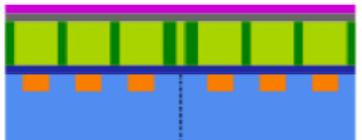
3. The wafer is covered with a  $50\ \mu\text{m}$  thick layer of SU-8 photoresist.



4. Using a special mask, part of the SU-8 is exposed to UV light, solidifying it to create the pillar structure.

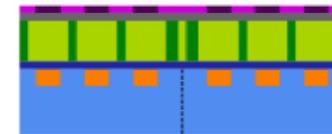


5. A  $1\ \mu\text{m}$  thick aluminium layer is deposited.

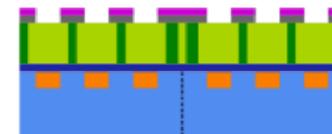


6. Another  $1\ \mu\text{m}$  thick layer of photoresist is applied.

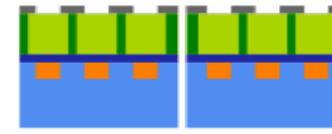
## NIKHEF and Fraunhofer Institute



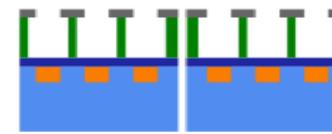
7. With UV light and another mask, a hole pattern is created.



8. The grid holes are chemically etched.



9. The wafer is diced into individual chips using a saw.

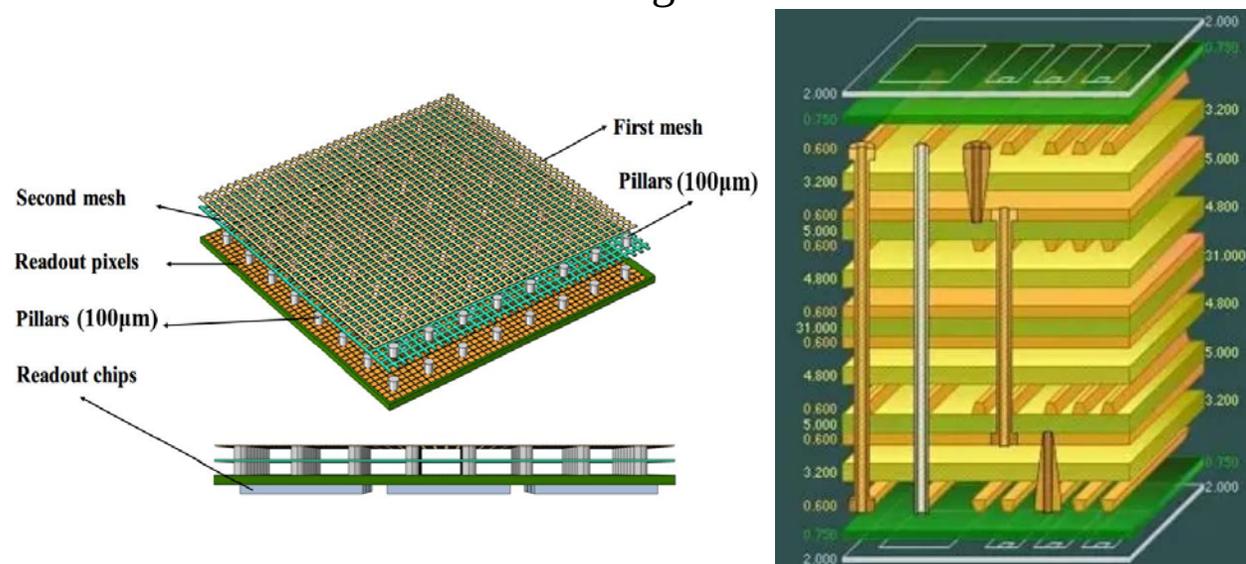


10. The unexposed SU-8 photoresist is resolved and the chips are ready.

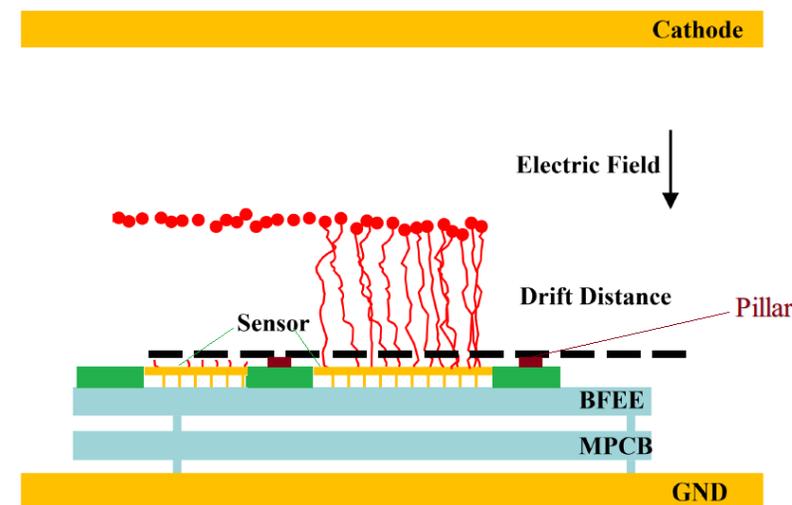
S. Tsigaridas, *New Generation GridPix: Development and characterization of pixelated gaseous detectors based on the Timepix3 chip*. PhD thesis, Amsterdam U., 2017.  
[http://www.nikhef.nl/pub/services/biblio/theses\\_pdf/thesis\\_S\\_Tsigaridas.pdf](http://www.nikhef.nl/pub/services/biblio/theses_pdf/thesis_S_Tsigaridas.pdf).

# High granularity readout: Micromegas – Interposer and direct mode

- #1: Interposer mode
  - Readout pads on top layer, readout chips on bottom layer, requiring multi-layer routing—high difficulty and high cost
  - 1.2mm PCB board with 12 layers routing
  - Potential for increased signal noise



- #2: Direct readout mode
  - Similar to GridPix but without photolithography masking
  - Readout sensor chips are used directly for readout, with Micromegas as the amplification layer above.

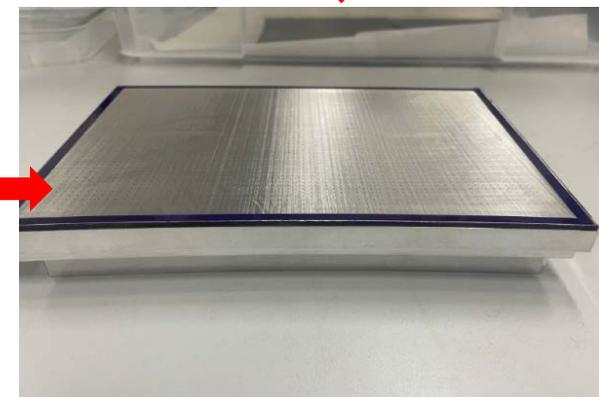
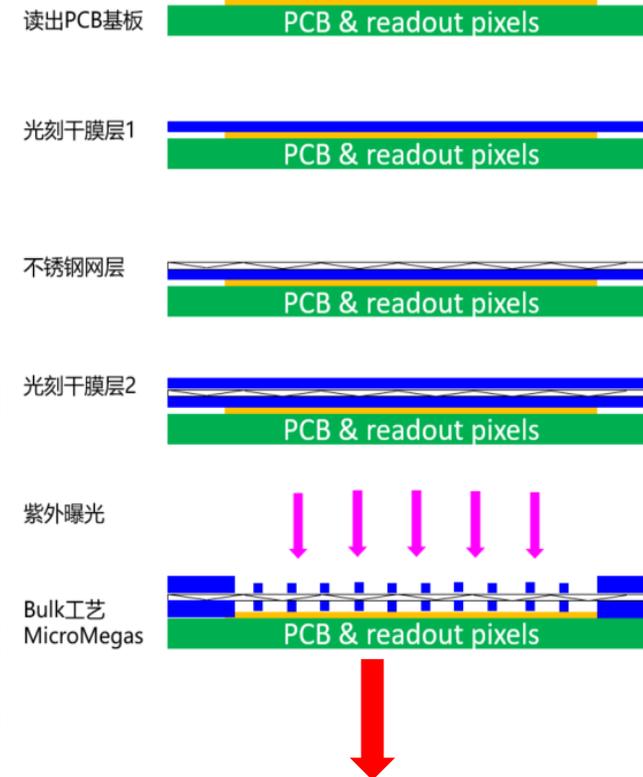
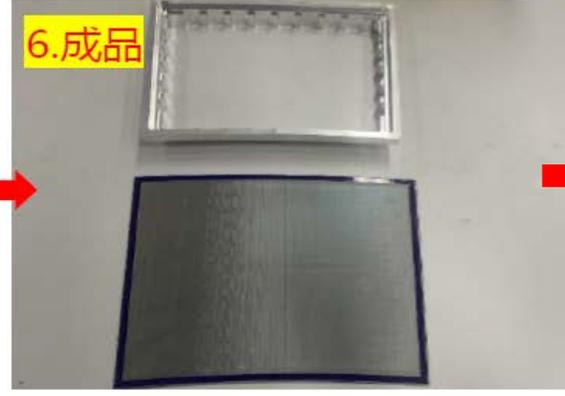
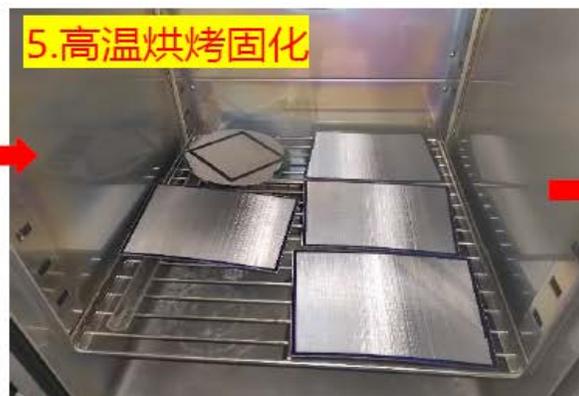
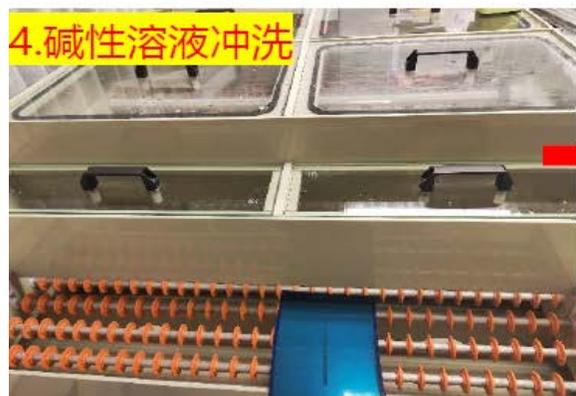
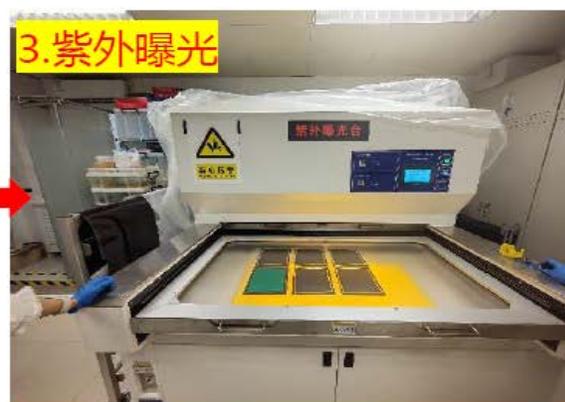
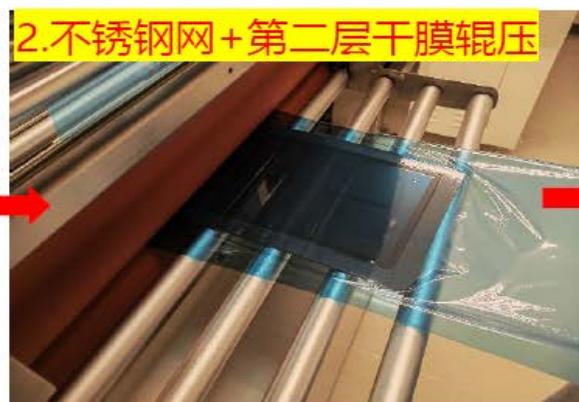
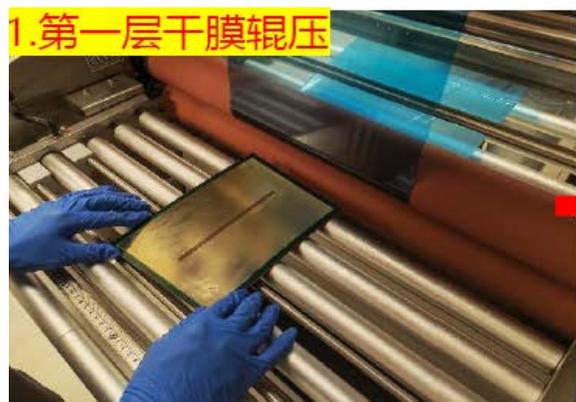


- **Key issues to address**
  - Requires low power consumption readout chips and further R&D.

- **Status of TPC module R&D**

# Production of TPC module: double-mesh Micromegas

- Achievements:
  - R&D on high granularity readout PCB board
    - 12-layer PCB inner routing, surface gold-plated flat finish
    - Top layer with Micromegas, bottom layer with the pixel readout chips

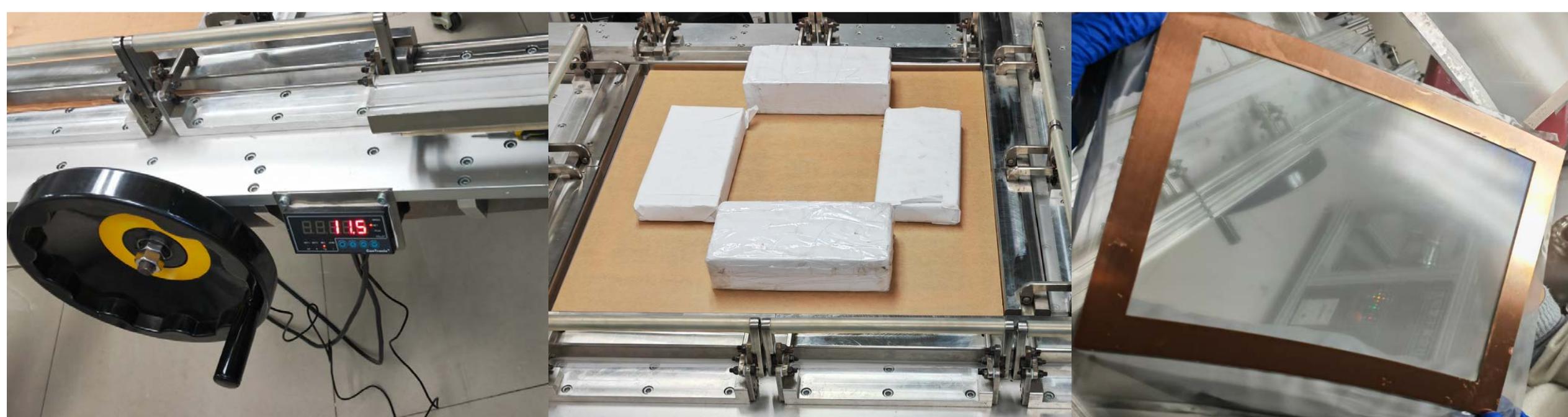


# Production of TPC module

- Key Issues to Address
  - Multilayer screen tension control ( $>10$  kg)
  - Flat roller pressing of mesh, mesh node control
  - Uniform  $100^{\circ}\text{C}$  baking control in the oven
  - Mutil-crimping of double-layer micromesh

- **Key issues to address**

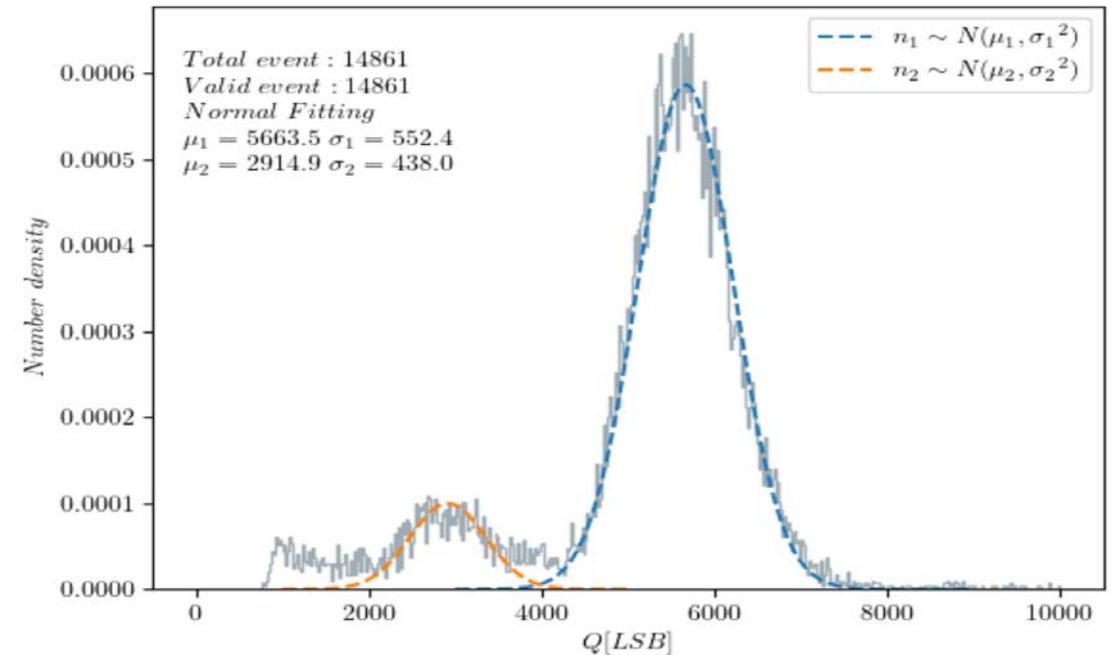
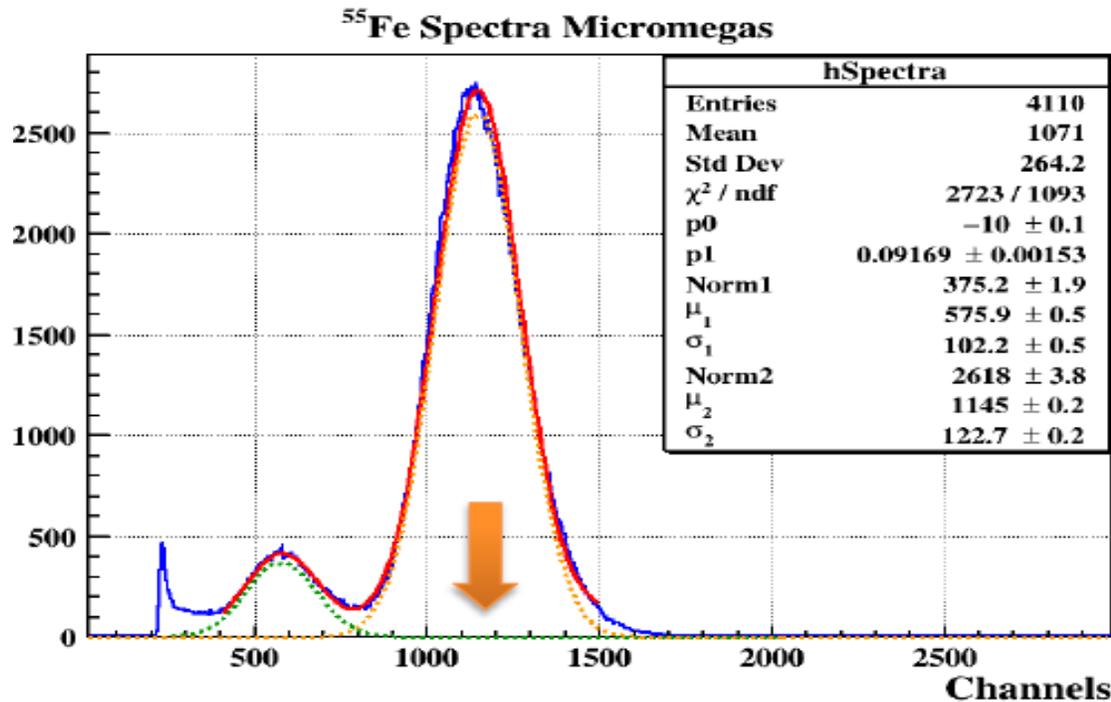
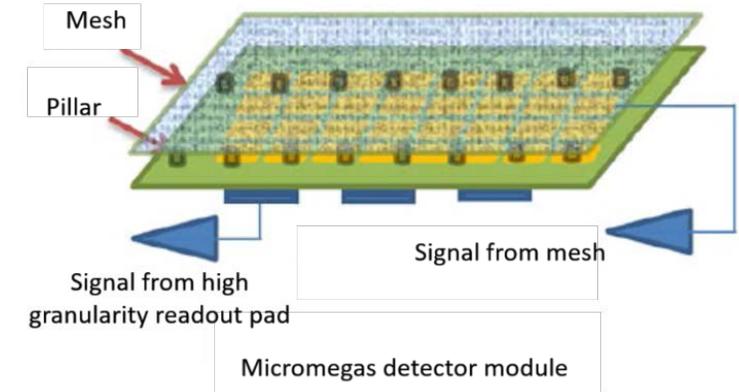
Improved detector gain, resolution, and overall performance.



# Fe-55 spectrum of TPC module

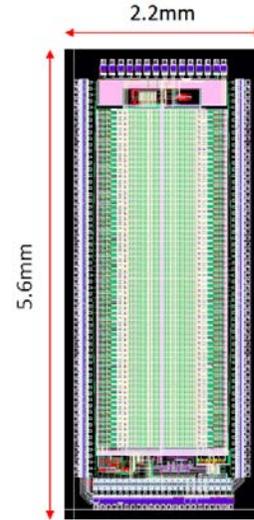
Achievement of TPC module:

- Used Fe-55 source to acquire energy spectrum on mesh; energy spectra obtained through the small pixel readout and the **two results are consistent**.
- Muon tracks under different pressures are under experimental investigation

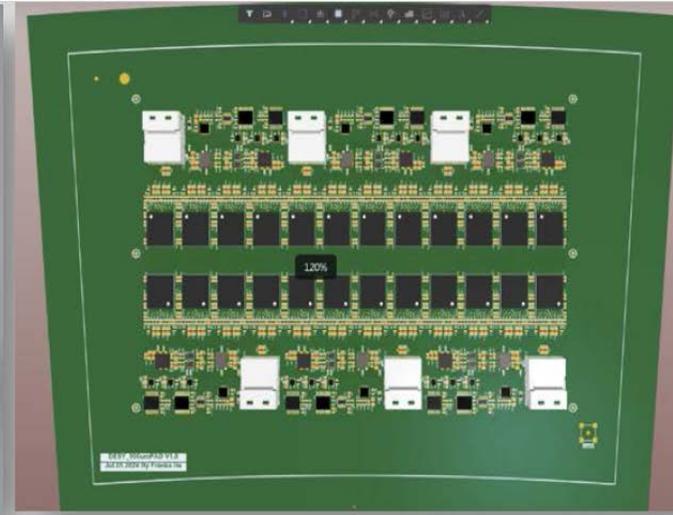
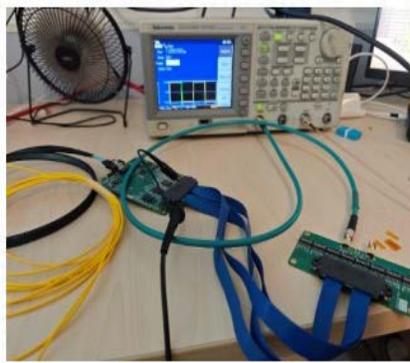


# Prototype of the **interposer mode** readout ASIC: TEPIX v1

- High granularity readout Electronics: TEPIX v1
  - Charge-sensitive preamplifier
  - Correlated double sampling shaper
  - 4-channel sample/hold circuits and 10 bit ADC
  - 128 channels using 180 nm process
  - Chip size: 2.2 mm × 5.6 mm
- Only 40 chip-in-package devices were tested in two batches; full-readout Micromegas readout has not yet been completed.



Total number of channels	30 Million per endplate
Pixel size	500 $\mu\text{m}$ × 500 $\mu\text{m}$
Equivalent Noise Charge (ENC)	100 $e^-$
Dynamic range	20 fC
Charge buffer dynamic range	8-10 bit
Event rate	12 kHz/cm <sup>2</sup> max. in low-lumi. Z mode
Event size	64 bit
Readout bandwidth	<10 Gbps per module with compression
Power consumption	<100 mW/cm <sup>2</sup>

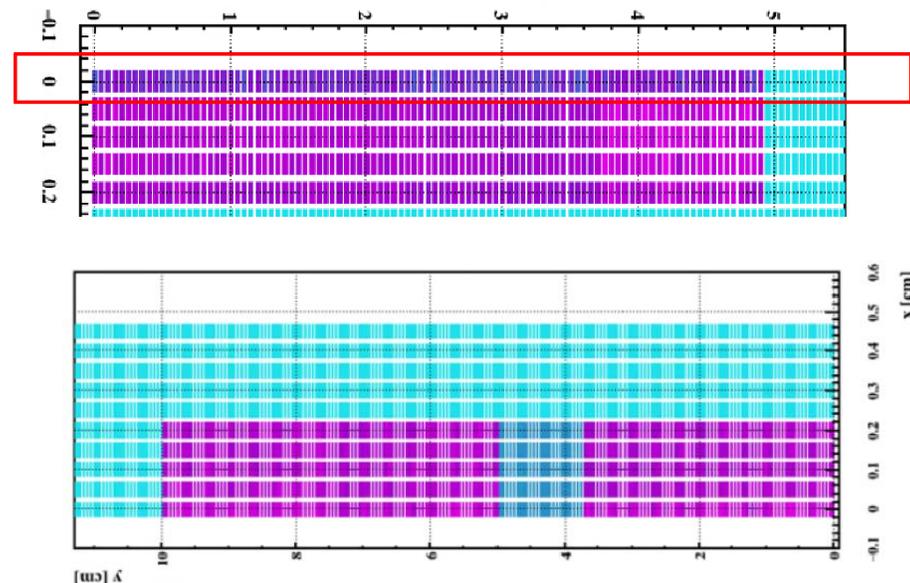
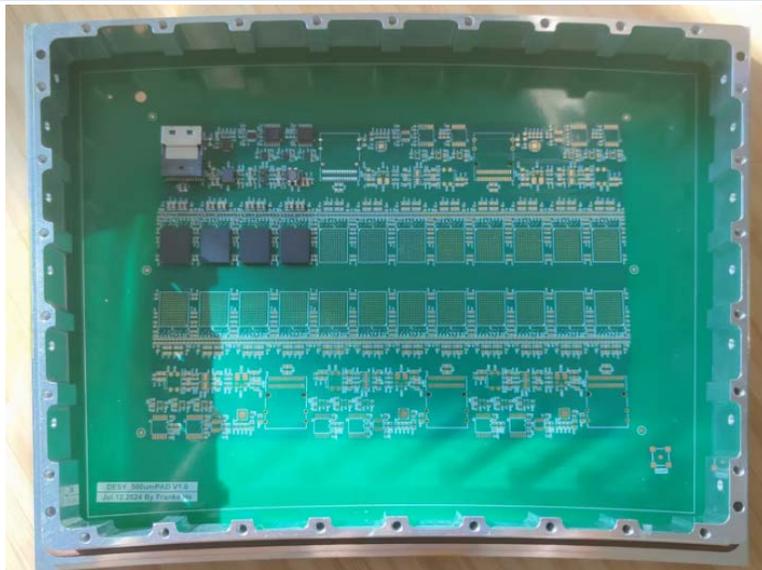


# Validation and commissioning of TPC prototype

- R&D on High granularity readout TPC readout using 4 chips integration.
  - ASIC chip developed and has been tested at IHEP.
- Energy/Time value of the channels according to the charged injected
  - Chip-to-chip threshold consistency varies greatly; some channels of the chip operate at excessively low thresholds.
- A TPC readout module has developed with  $10 \times 300$  readout channels (24 TEPIX v1 chips)

- **Key issues to address**

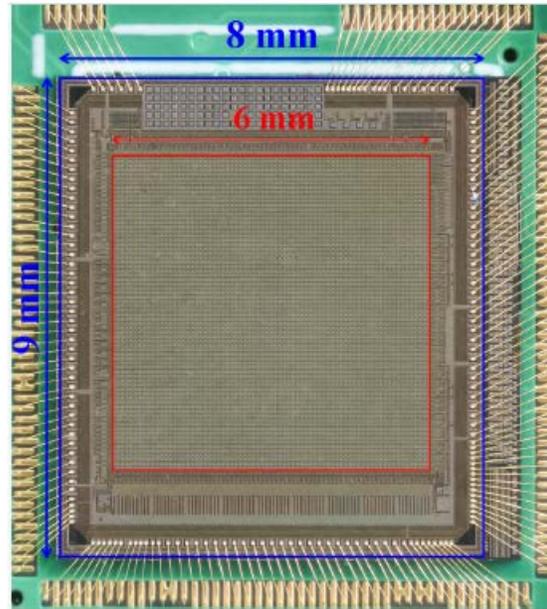
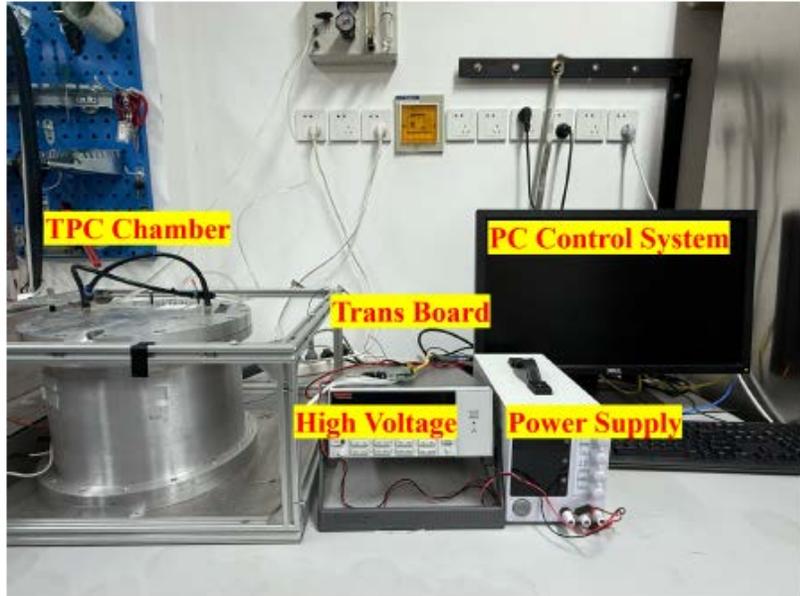
Micromegas detector requires further optimization, and the chip threshold inconsistency issue needs to be resolved, still needs more debugging and time.



Some test result of Micromegas detector integrated with TEPIX chip

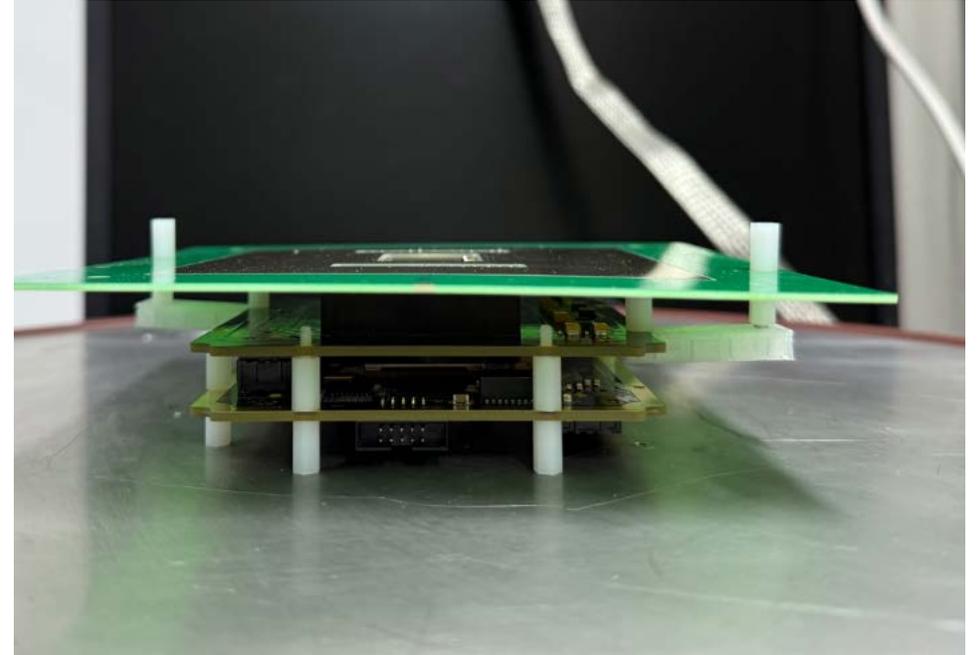
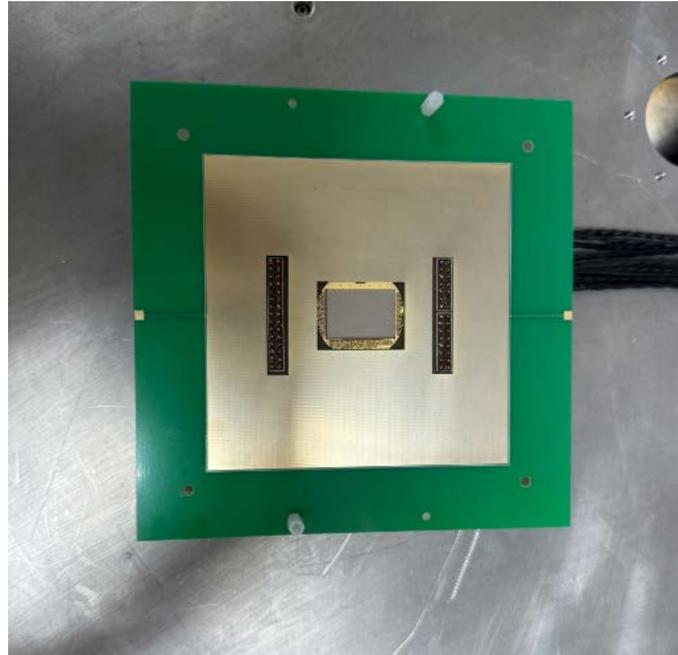
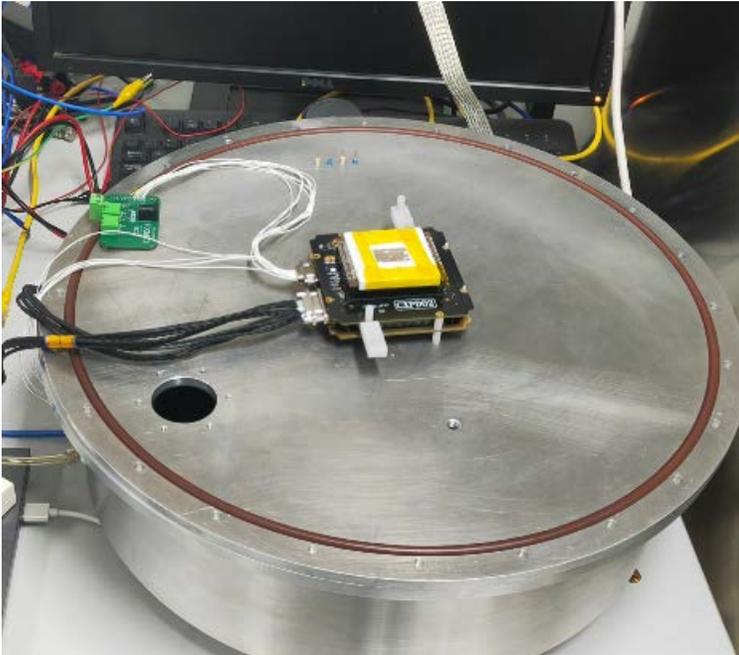
# Prototype of the **direct readout mode** readout ASIC: Topmetal II chips

- High granularity readout Electronics: Topmetal II
  - Switched-capacitor readout:  $72 \times 72$  array
  - The analog output of the Topmetal-II sensor is read out through a row/column time-multiplexed switching network to a single on-chip output buffer.
  - Time per pixel is 128 ns which corresponds to a full-frame readout time of 0.6 ms



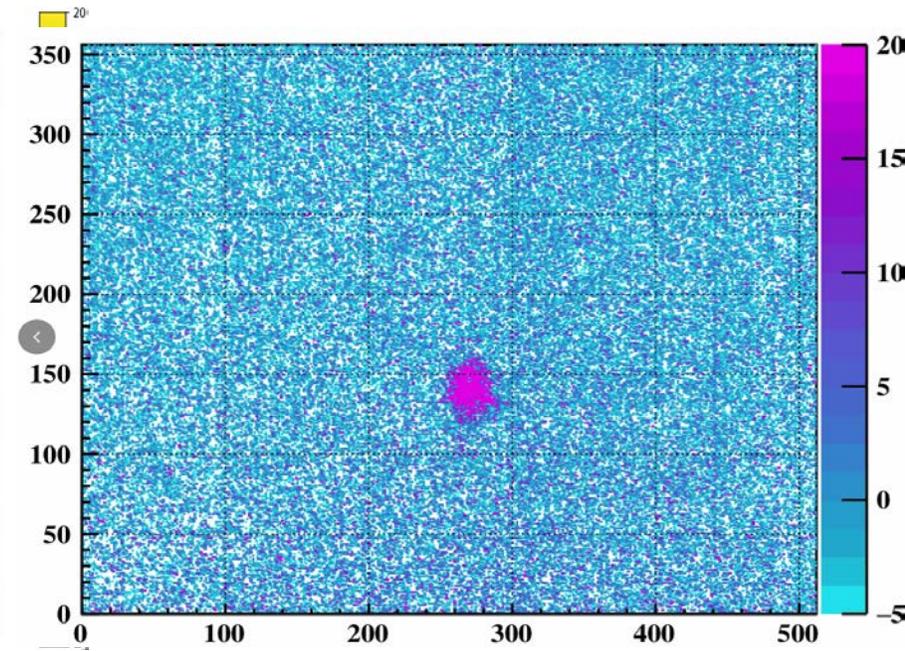
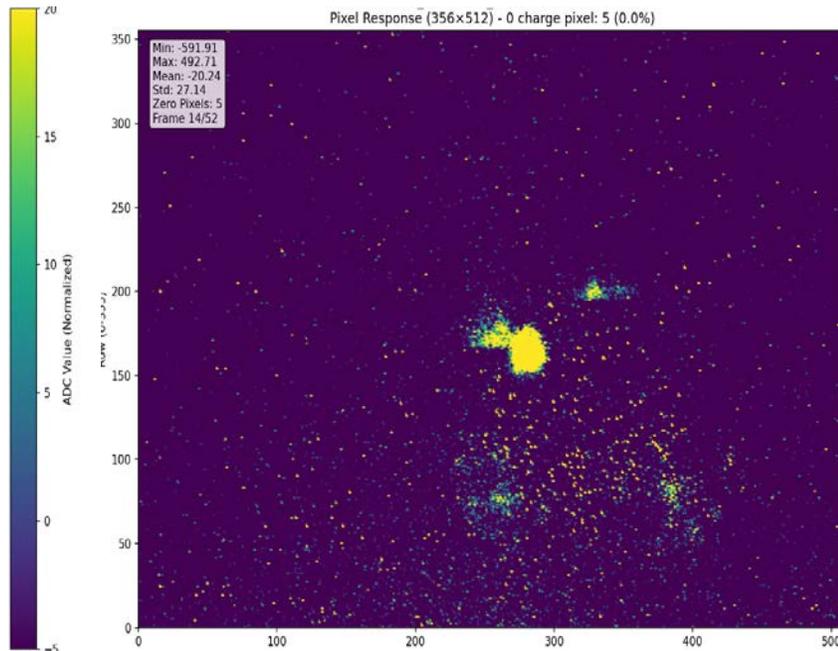
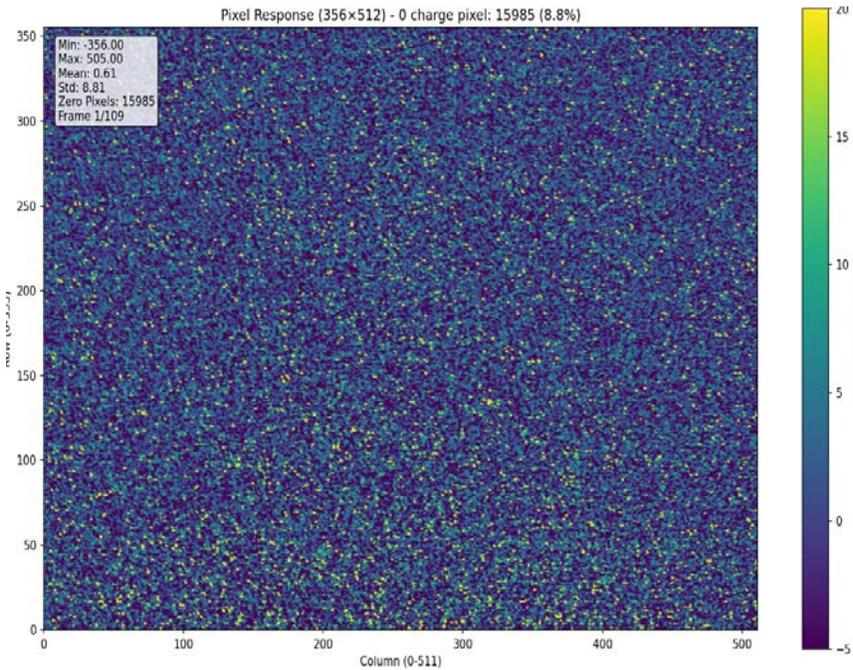
# Prototype of the **direct readout mode** readout ASIC: Topmetal II chips

- High granularity readout Electronics: Topmetal L
  - Switched-capacitor readout:  $72 \times 72$  array (module:  $356 \times 512$ )
  - The analog output of the Topmetal L sensor is read out through a row/column time-multiplexed switching network to a single on-chip output buffer.
  - Time per pixel is 128 ns which corresponds to a full-frame readout time of 0.6 ms



# Prototype of the **direct readout mode** readout ASIC: Topmetal II chips

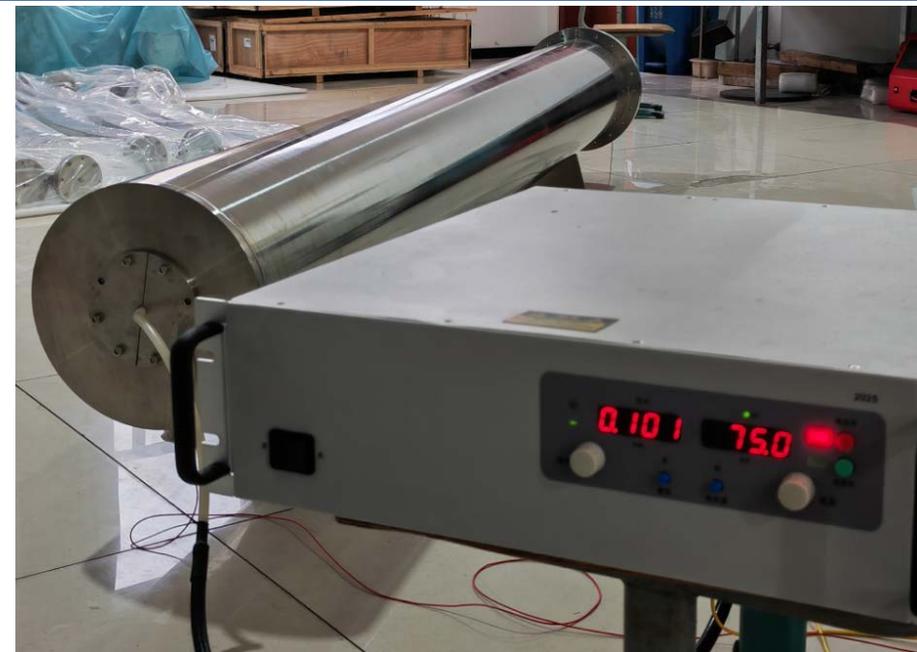
- High granularity readout Electronics: Topmetal L
  - 2 mm aluminium collimator
  - 1 mCi Fe-55 source
  - GEM detector for amplification were used
  - Next steps, a Micromegas detector is being fabricated and will be tested with Bi-207 tracks.



- **Status of TPC prototype R&D**

# Plans of TPC R&D

- Development of TPC prototype with low power consumption FEE
  - Collaboration with LCTPC and DRD1 group
- Prototyping R&D and validation with the test beam
  - mechanics, manufacturing, beam test, full drift length prototype
- Development of the full drift length prototype
  - Drift velocity. Attachment coefficient, T/L Diffusion, etc.
- Performance of the simulation and Machine Learning algorithm



Milestones achieved	Short term	Long term
Ion backflow suppression	<b>IBF × Gain &lt; 1 (Gain=2000)</b>	<b>Graphene technology</b>
High granularity readout readout prototype	<b>Validation with beam test</b>	<b>Prototype with Multi-modules</b>
Power consumption ASIC	<b>~100mW/cm<sup>2</sup> (60nm ASIC)</b>	<b>Optimization readout size</b>
PID resolution	<b>3% (dN/dx)</b>	<b>&lt;3% (dN/dx)</b>
Material budget (barrel)	<b>Carbon Fiber</b>	<b>Full size prototype</b>

- High granularity readout TPC is chosen as the baseline detector as main track in CEPC TDR. The simulation framework has been developed using Garfield++ and Geant4.
- The TEPIX chip v1 based on the Interposer readout has been developed. Some chips have undergone joint debugging with the Micromegas detector, though consistency in noise and threshold still requires further resolution.
- Experiments using the Topmetal L chip with pixel-by-pixel readout have been conducted. The chip has undergone joint calibration with the GEM detector, yielding well-calibrated information from the Fe-55 radiation source.
- Further commissioning and optimization are required to validate the technical application of high-granularity readout for future circular colliders. **Funding and recourse are also urgently needed.**

**Many thanks!**