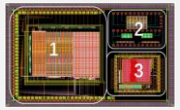
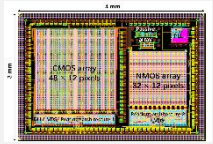
55nm HV-CMOS pixel sensor development status

-- Specifications for CEPC ITK： ~10ns time resolution、~150mW/cm^2 power dissipation、< 8um position resolution

Zhou Yang 2026_2_3

CMOS sensOr in Fifty-Five nm process

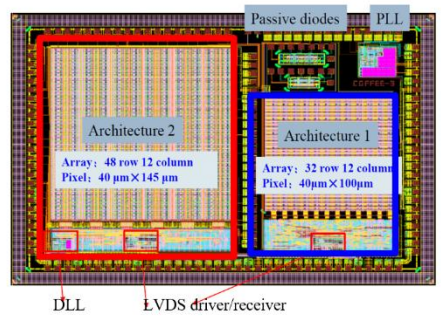
COFFEE1	COFFEE2	COFFEE3	CHiR 1.0	CHiR_x	Final version
SMIC 55nm Low Leakage process	 55nm HV-CMOS process	 Small prototype	Process modification and validation	0.5cm × 2cm ¼ full size sensor	2cm × 2cm Full size sensor

COFFEE series development — 2022 — 2023.08 — 2025.01 — 2026.01 — Future

Main goal:

- Verification of technical principles
- Chip design architecture verification
- Process modification and verification

Layout and Targets of COFFEE3



COFFEE3 layout，3×4 mm², designed in a 55nm HV-CMOS process. Submitted Jan.2025. Returned May 2025.

Main design:

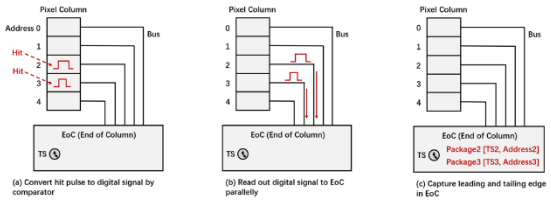
- **Two independent readout architecture**, both could be scaled to large sensor (~2×2 cm²);
- Necessary digital and analogue Peripheral Function Modules;

To answer:

1. **If it possible to meet**（**Time resolution** ~ ns；**Spatial resolution** ~10 μm; **Power dissipation** < 200mW/cm²） **at the same time;**
2. **What's more can 55 nm process bring to DMAPS?**

Readout Architectures

Architecture 1： In-pixel NMOS design, after digitization, each pixel data is transmitted in parallel to the bottom of the array, where time stamps are added.

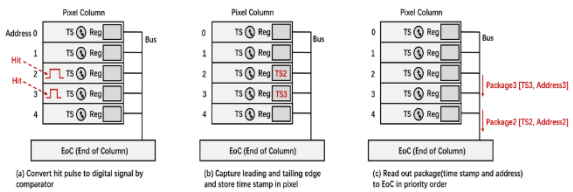


Readout concept of Architecture 1, similar with ATLASPix, MightyPix, MuPix, etc

Targets:

- *Potential for Low power consumption and high position accuracy*

Architecture 2： employs a TDC within each pixel. Particle hit information (arrival time, end time) is recorded locally in each pixel and then read out to the bottom of the array in priority order.

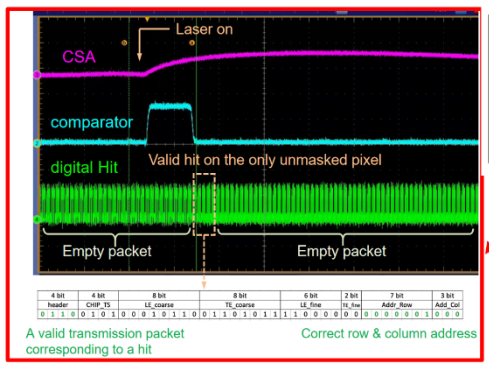


Readout concept of Architecture 2, similar with Timepix, RadPix, MonoPix, etc.

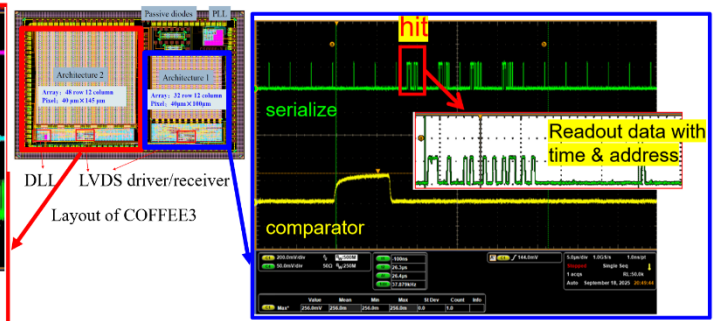
- *More possibilities & High hit density processing capability*

Response of Full Readout Chain with Laser Test

Architecture 2: in-pixel TDC



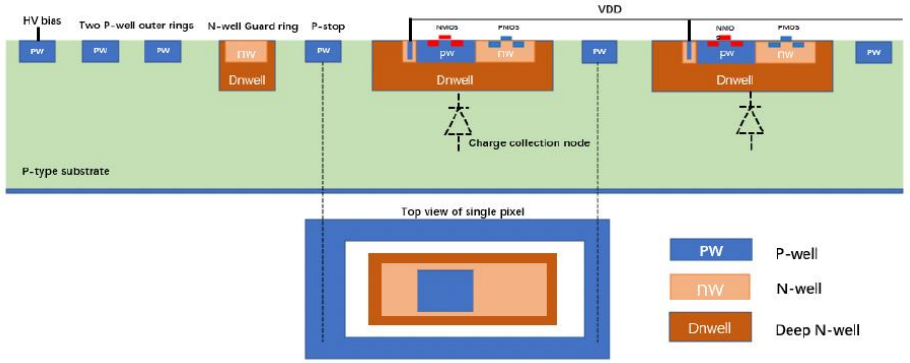
Architecture 1: in-pixel NMOS design

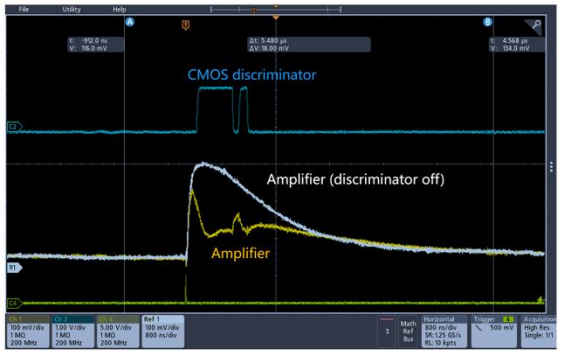


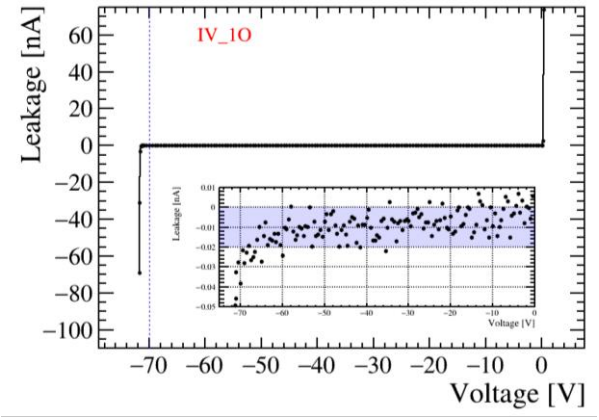
The full readout chain works for both of the two readout architectures.

Sensing diode → in-pixel (CSA\comparator\TDC) → EOC (digital peripheral) -> data link-> DAQ

Limitations of Commercial 55nm HV-CMOS Process



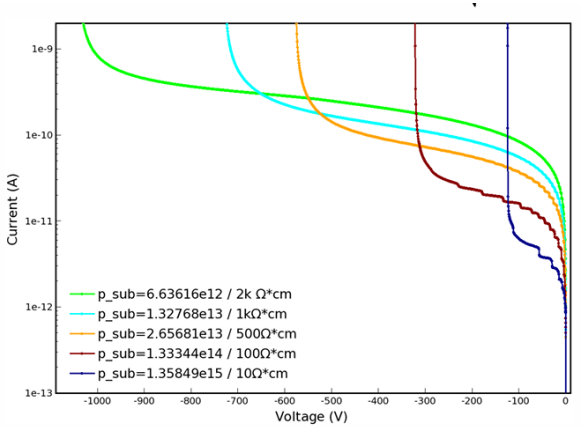




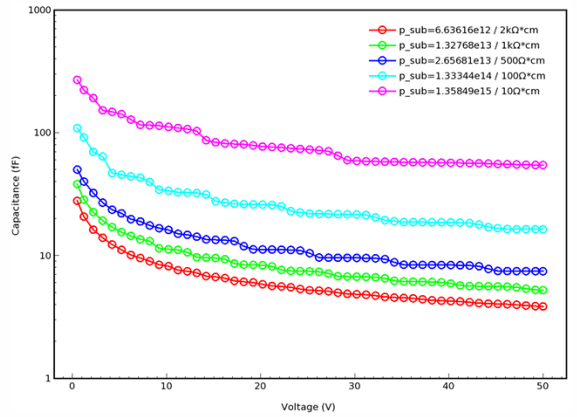
1. Triple-well process → cross-talk between sensor (deep-n) and PMOS circuit;
2. Break down at -70V;
3. No access of high-resistivity wafers;

Process Modifications for HV-CMOS MAPS in 55nm process R&D

Modifications：

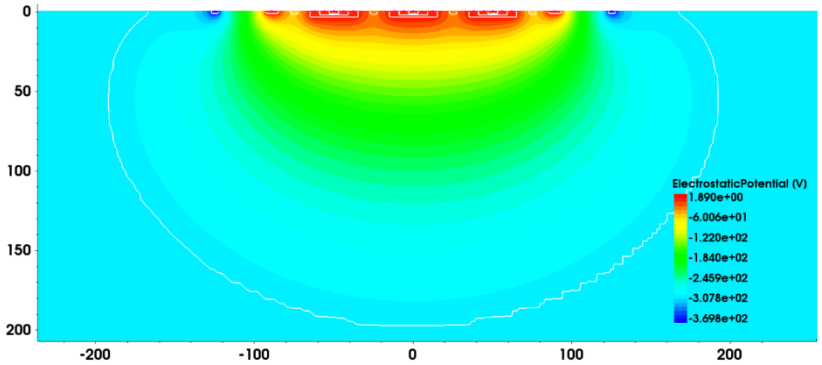


➢ Breakdown V: **70 --> > 400V**



➢ Capacitance of VDNW/p-sub:
~ hundreds fF --> ~ tens of fF

- ◆ Add layers: Deep-PW & Very-deep-NW;
- ◆ Replace wafer: from 10 Ω·cm --> 1k/2k/4k Ω·cm;
- ◆ Change doping rules affecting breakdown voltage;



➢ Depletion depth: ~10 μm → >200 μm

The first submission has been made!

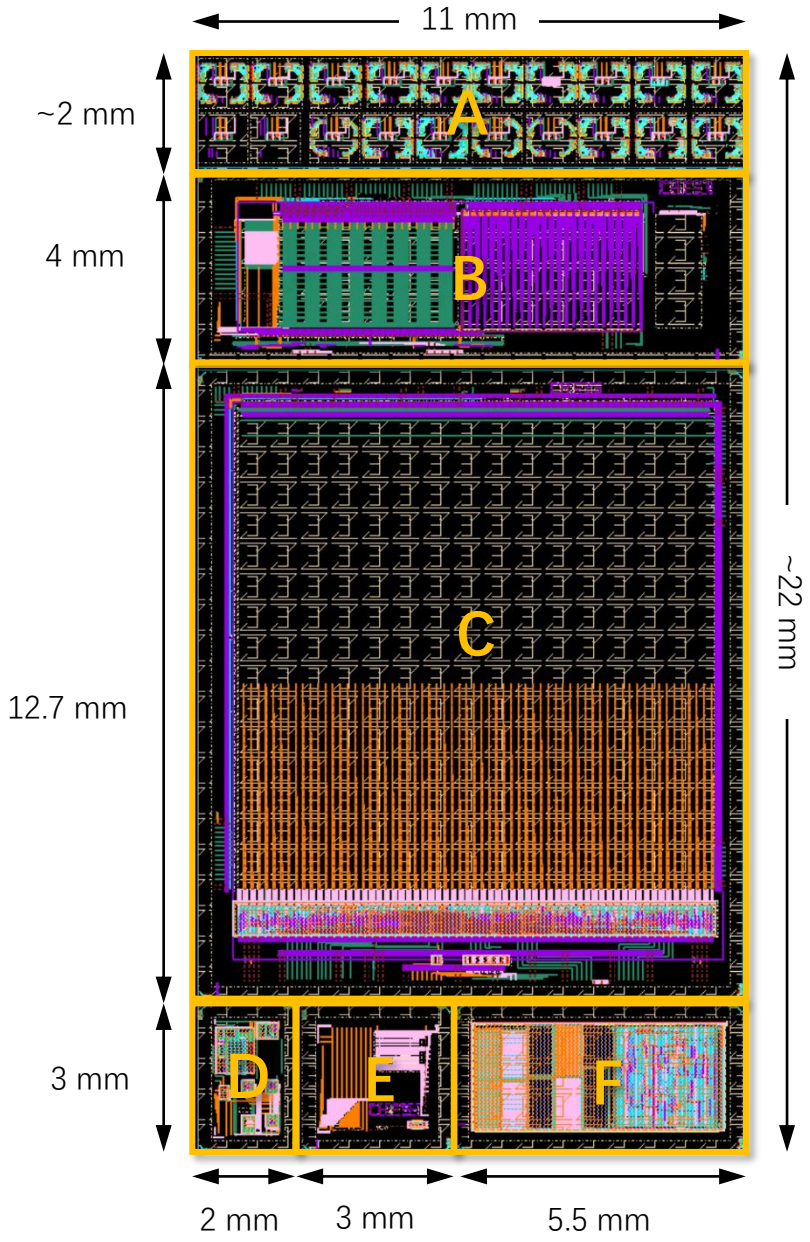
Answers to many key questions can be expected!

Huge S/N gain: Signal increase >10 times, while C_{diode} reduce

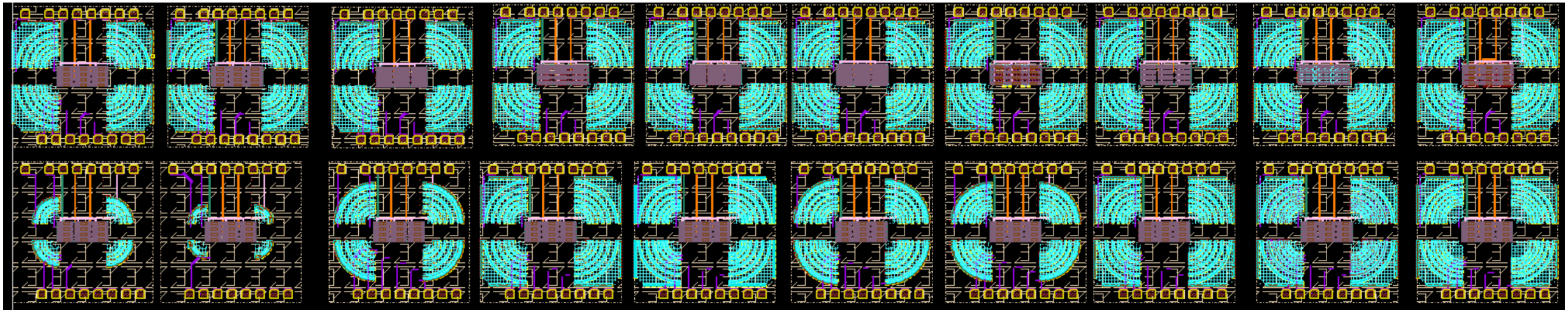
CHiR 1.0 chip(s)

*CHiR (COFFEE-HiRes)

- Can be diced into a number of chips serving various goals
- Passive sensor validation:
  - (A) 20 arrays of 3x4 passive pixels with diff guard ring designs, each can be diced into individual 1x1 mm^2 chip
  - Pixel size: 38 um x 150 um
- Pixel array design
  - (B) 9 variations of in-pixel frontend designs
  - (C) main pixel array of 256 x 64 pixels with digital periphery
- IP validations
  - (D) necessary analog Ips: PLL, DLL, LVDS transceivers …
  - (E) alternative small pixel arrays and two more shunt-LDO versions
  - (F) digital modules and transistors for TID and SEE studies



A

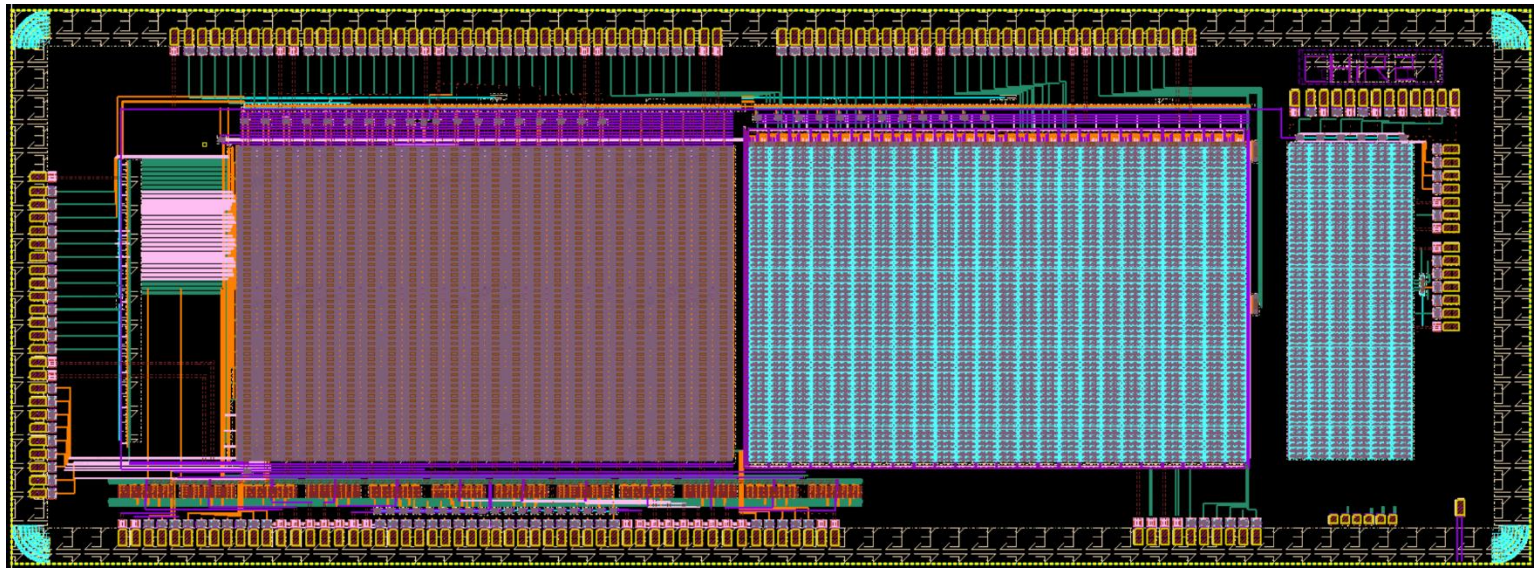


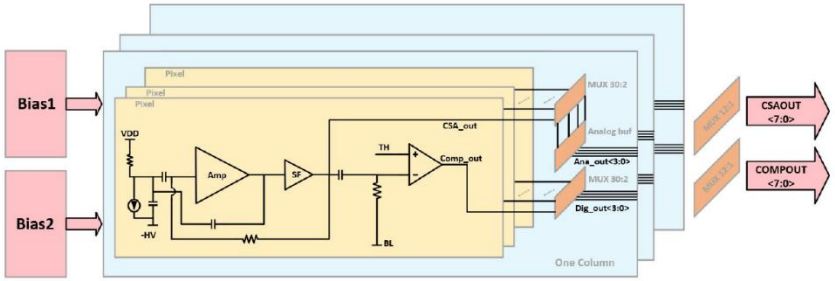
◆ Design goals of the Guardrings:

- ➢ Improve the breakdown voltage before and after irradiation， $V_{breakdown}$ > 400V
- ➢ The smallest possible dead zone area；

◆ Different types of passive sensors: size, structure, etc.

B

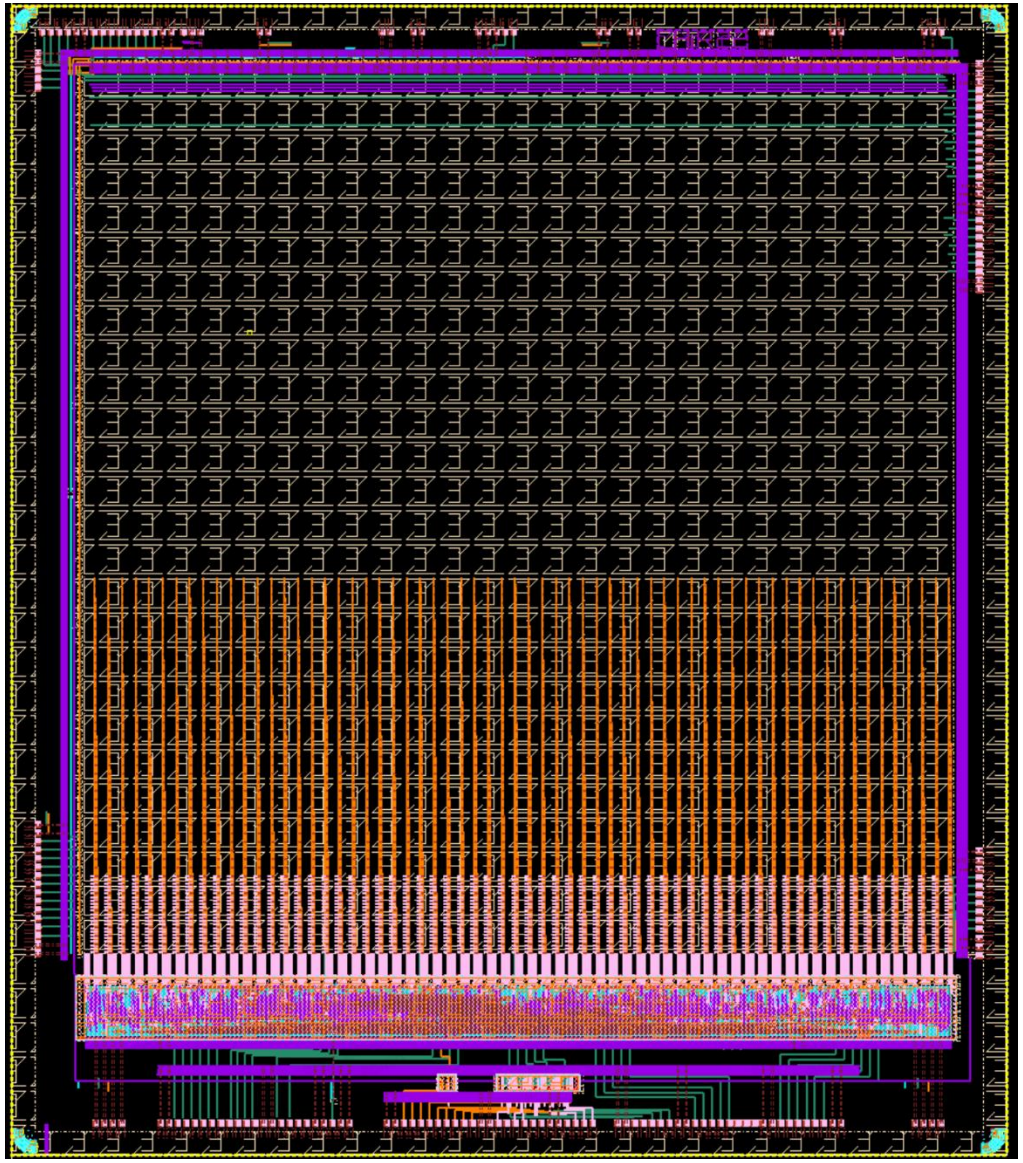


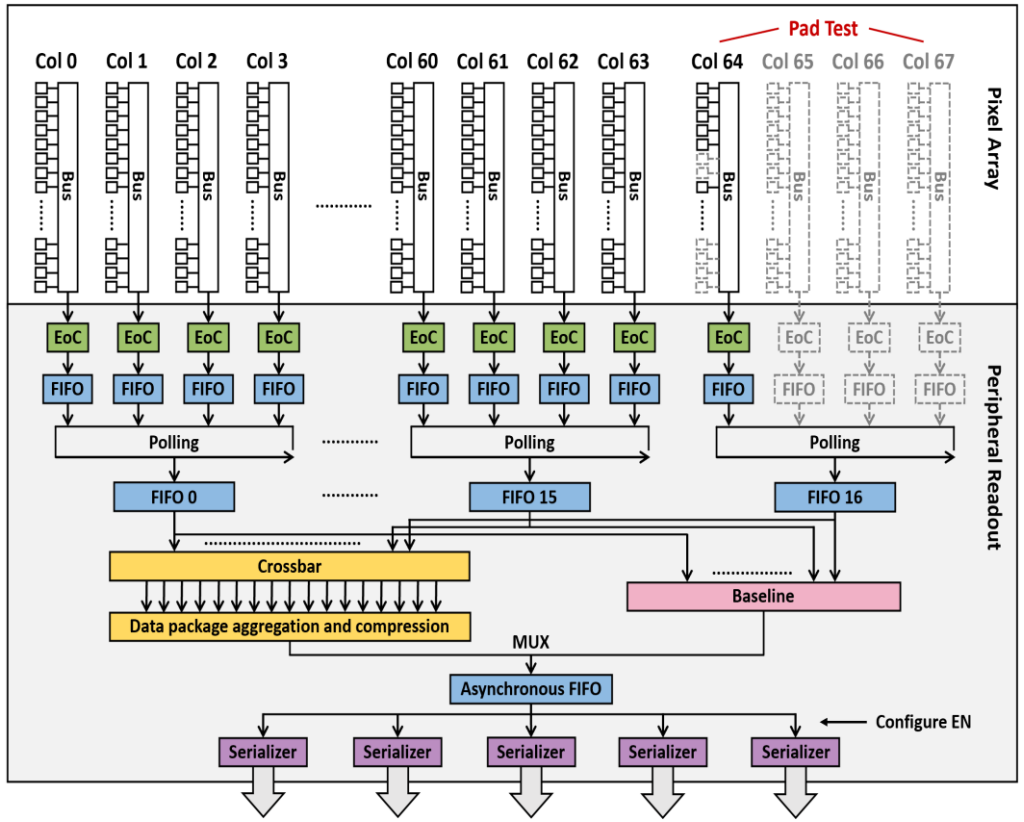


Different pixel sizes and front-end design verification:

- 9 variations of in-pixel frontend designs;
- 12 variations of pixel size, smallest pixel pitch @ 18 μm

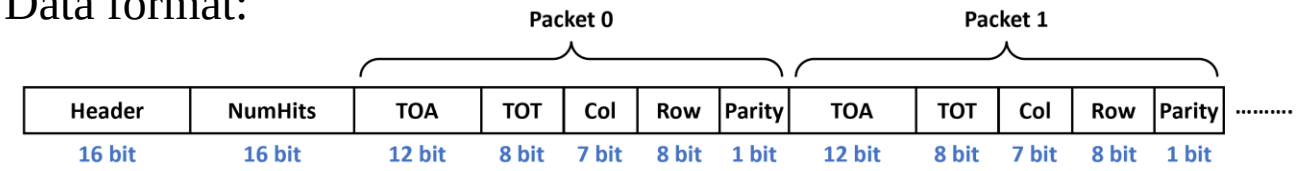
C Pixel array of 256 x 64 pixels with digital periphery





5 parallel LVDS differential output channels with a speed of 320MHz

Data format:

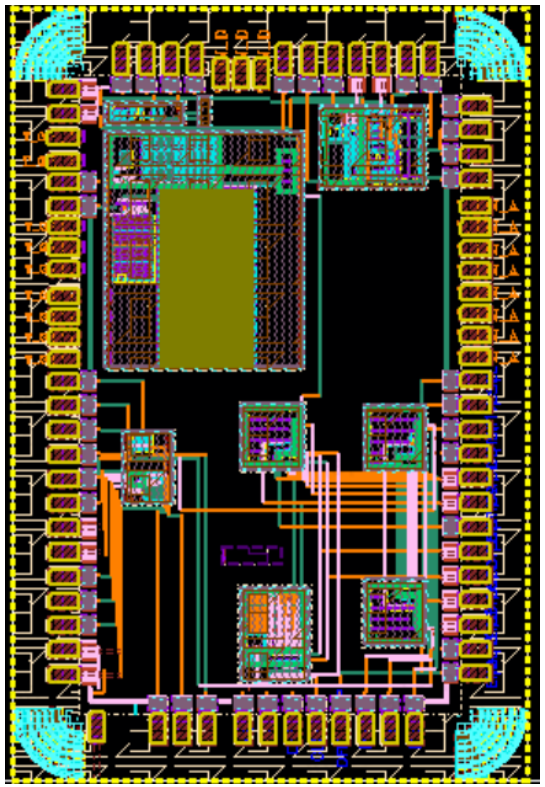


D

Necessary analog Ips for next step integration:

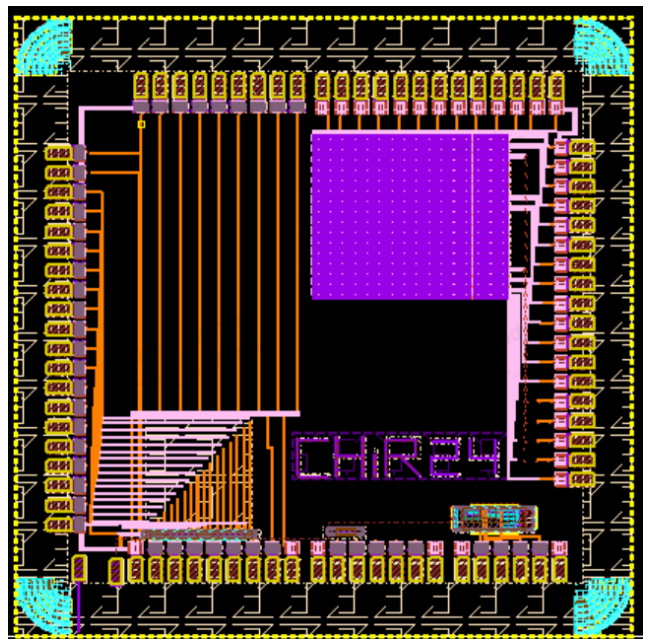
- SLDO
- LVDS
- Bandgap
- PLL
- DAC

……

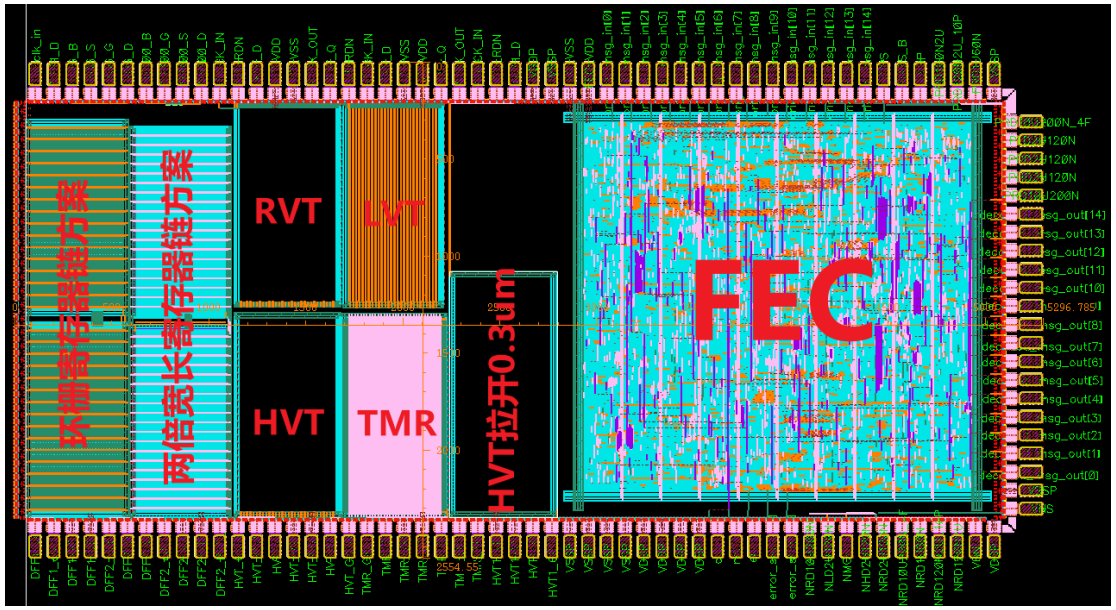


E

Alternative small pixel arrays and two more SLDO versions



F



Digital modules and transistors for TID and SEE studies

A total of 8 schemes were designed to verify the radiation resistance of the Register chain of this process

1、With ELT； 2、Twice the width and length； 3、HVT； 4、RVT； 5、LVT； 6、HVT with larger distance； 7、TMR； 8、FEC;