Heating film design and temperature-sensing methods for VTX thermal mockups

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Abstract

We have developed resistive heating films to simulate the heat loads generated by pixel sensors and readout electronics in the vertex detector. Two designs have been fabricated for thermal mockups of the first and fourth detector layers. The films consist of high-resistivity heating elements encapsulated in polyimide and operate at low supply voltages. Dedicated flexible printed circuit (FPC) boards attached to the films carry PT100 platinum thin-film resistance temperature detectors (RTDs). Adapter boards connect the sensing channels to data-acquisition modules. We present the experimental setup and preliminary air-cooling results for two assembly configurations. In parallel, we are developing silicon dummy chips as an alternative for thermal studies.

Heating film design

We designed two heating films for the first and fourth vertex-detector layers. The first-layer sensor module (Figure 1) routes all power connections, I/O signals and services through the Left-end Readout Block (LRB), forming a localized high-heat region. The first-layer film therefore contains high- and low-heat regions (Figure 2a). The fourth-layer film comprises two independently powered sections, each with a high-heat region at one end (Figure 2b).

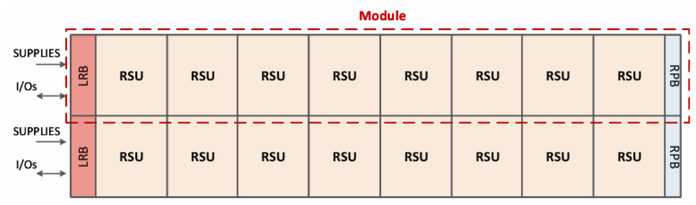
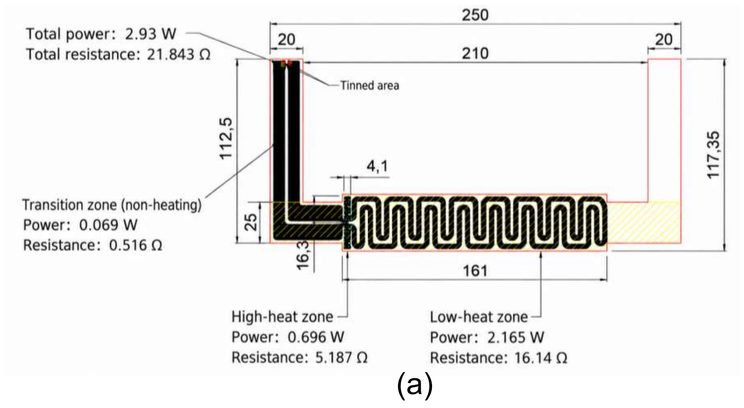
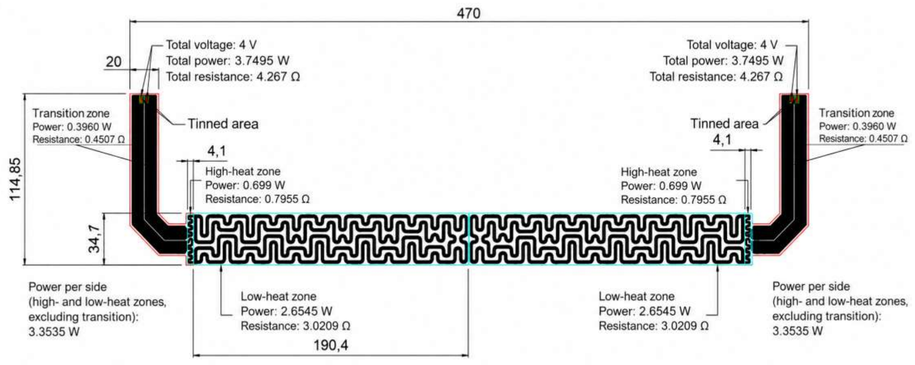


Figure 1. Sensor module for the first vertex-detector layer



(a)



(b)

Figure 2. First- and fourth-layer heating film layouts

FPC sensor board design

We designed two FPC boards using Vishay PTS060301B100RP100 platinum RTDs. Their Class F0.3 tolerance is ±(0.3 + 0.005|T|) °C, where T is the temperature in °C.

The first-layer board has 11 sensing points (Figure 3a) for temperature profiling with airflow from the left. Three-wire connections use two traces on one RTD terminal and one on the other to reduce lead-resistance errors. Signals pass through 24-pin FPC connectors. Polyimide stiffens both FPC tails, and stainless steel reinforces the connector regions. The fourth-layer board has 18 sensing points (Figure 3b), with nonuniform spacing based on simulation results.

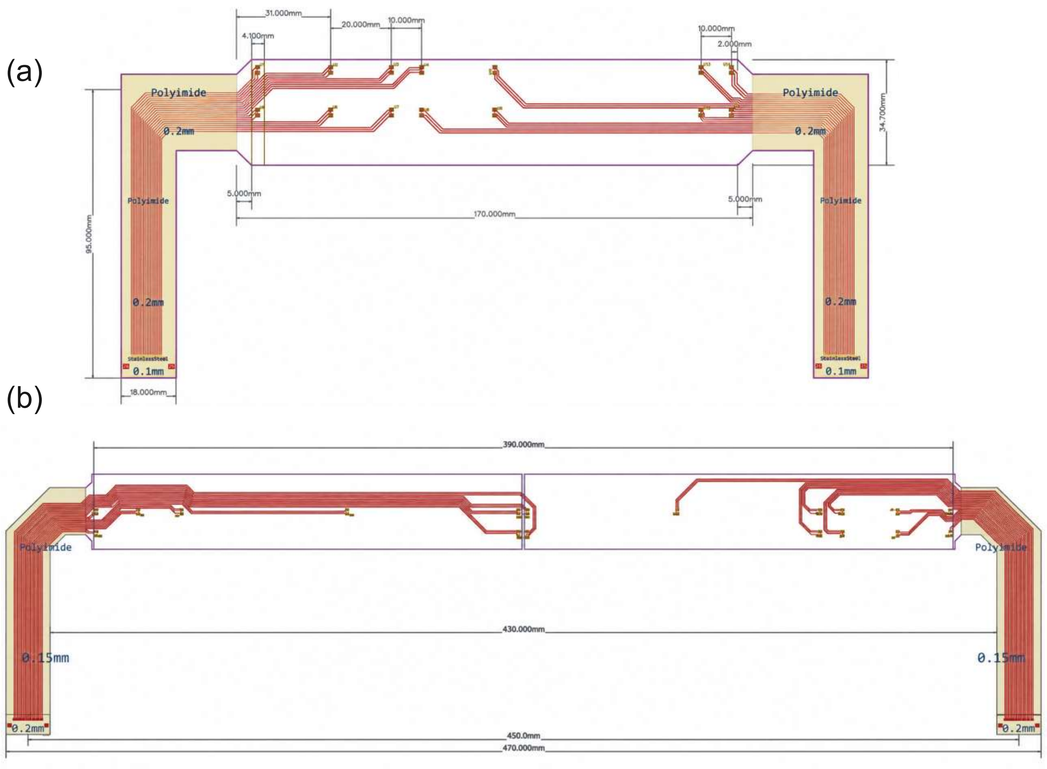
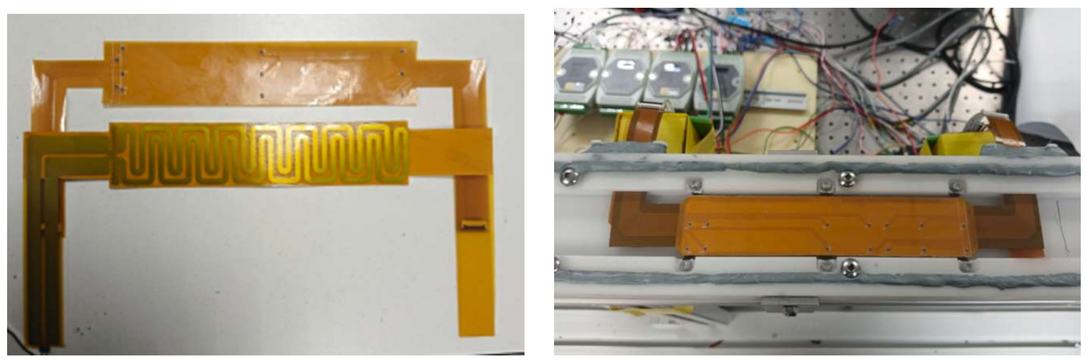


Figure 3. First- and fourth-layer FPC layouts

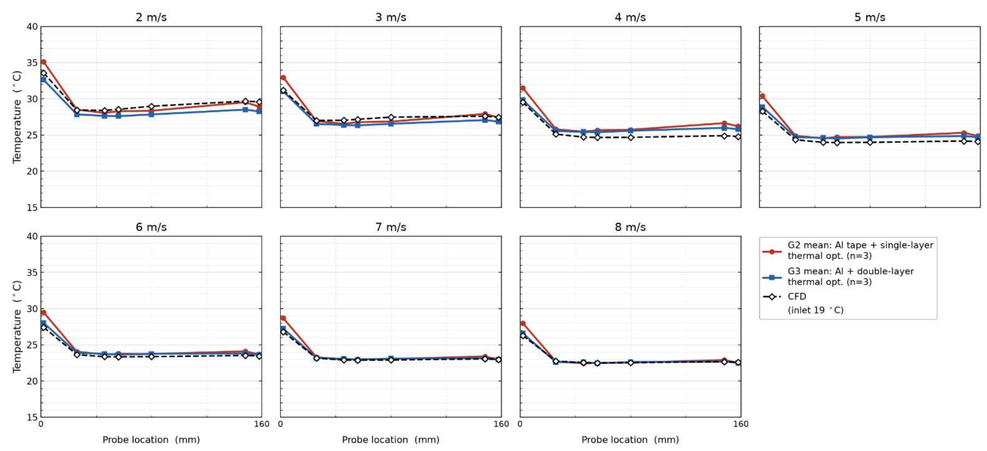
Air-cooling test

We conducted preliminary air-cooling tests with the first-layer heating film and FPC sensor board (Figure 4). After assembling the heater using aluminium and adhesive layers, we installed it in a thermal mockup. We compared two configurations: aluminium tape with 3M 9448A double-sided tape, and aluminium with two layers of 3M 8805 thermally conductive tape. We tested both configurations at different air velocities and compared the measured temperature profiles with computational fluid dynamics (CFD) simulations.



(a)

(b)



(c)

Figure 4. Air-cooling test setup and test results

Silicon dummy chip design

We are developing two silicon dummy chips, A and B (Figure 5), each measuring 34.7 mm × 80 mm, to better reproduce the thermal behavior of actual sensors. Both designs use serpentine aluminium heaters with a nominal thickness of 2 μm. Each chip contains four independently powered low-heat sections, each with two parallel branches. At 12 V, these sections provide a nominal average power density of 40 mW/cm². Chip A also includes a separately powered, 4.1 mm-long high-heat region designed to dissipate 696 mW at 9.3 V. Chip B provides low-heat coverage across its full area.

Table 1 summarizes the trace geometry and nominal current densities.

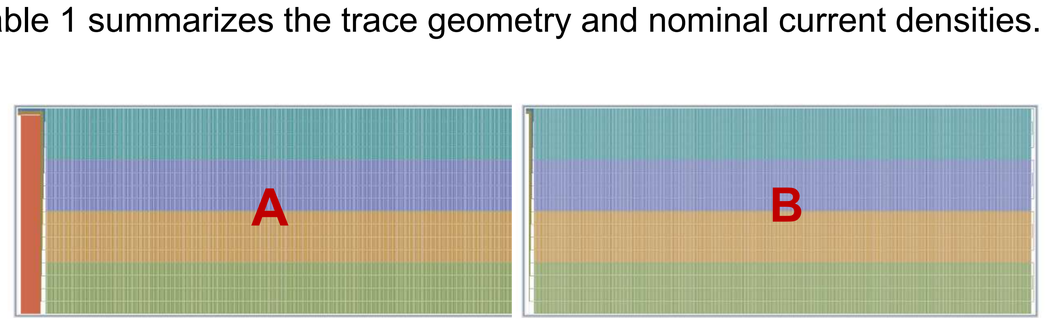


Figure 5. Silicon dummy chips A and B

Parameter	High-heat region	Chip A low-heat	Chip B low-heat
Trace width, w (μm)	97.28	40	40
Clear spacing (μm)	11.42	53.734	63.074
Cross-sectional current density, J (kA/cm²)	38.47	13.72	14.46
Linear current density, K (mA/μm)	0.7693	0.2743	0.2892

Table 1. Trace geometry and nominal current densities