A Compact Silicon Microstrip Tracking System

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Abstract

Silicon microstrip detectors offer high spatial resolution and scalable architectures, making them attractive for charged-particle tracking, beam monitoring, and detector prototyping. We present the development and initial characterization of a compact p-on-n silicon microstrip detector system. A module comprises a 192-channel sensor with a sensitive area of approximately 26 mm × 40 mm, three 64-channel IDE1140 front-end ASICs, dedicated bias and control electronics, and FPGA-based data acquisition using a Xilinx ZCU102. The current single-module prototype supports front-end configuration, calibration, programmable sampling delay, and internal or external triggering. At a bias voltage of 50 V, the typical common-mode-reduced channel noise is approximately 3.5 ADC counts, and cosmic-ray measurements show clear particle-induced clusters.

System Architecture

The readout system integrates a silicon microstrip sensor, a dedicated front-end board (FEB), and a Xilinx ZCU102-based DAQ platform. The FEB provides sensor biasing, leakage-current monitoring, and analog signal digitization. The ZCU102 implements front-end control, trigger handling, and data acquisition.

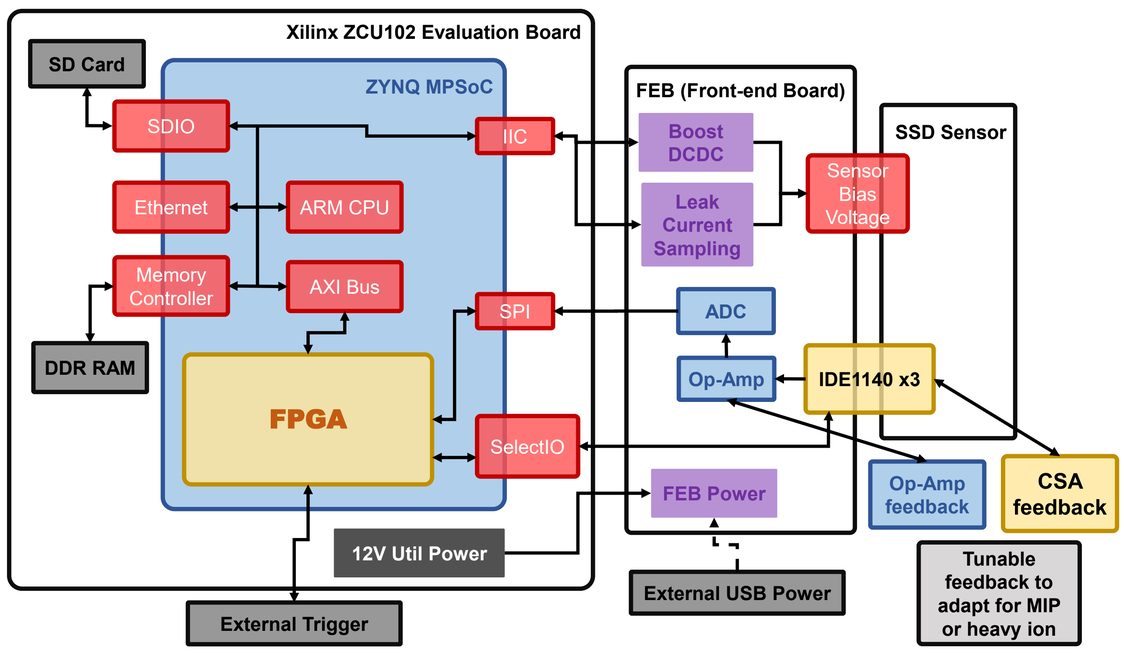


Figure 1. Architecture of the single-module readout system, showing the ZCU102 DAQ platform, front-end electronics, sensor interfaces, and power and trigger connections.

Detector Module and Front-End Electronics

The detector module integrates a 192-channel p-on-n silicon microstrip sensor (AMS L0 baby sensor) with an active area of about 26×40 mm² and three 64-channel IDE1140 front-end ASICs. The front-end electronics provide signal conditioning, digitization using a 14-bit ADC rated at 2.5 MSPS, and adjustable sensor biasing over 0–80 V. An FMC-to-RJ45 adapter board is alternative for connecting the readout electronics to the ZCU102-based DAQ system.

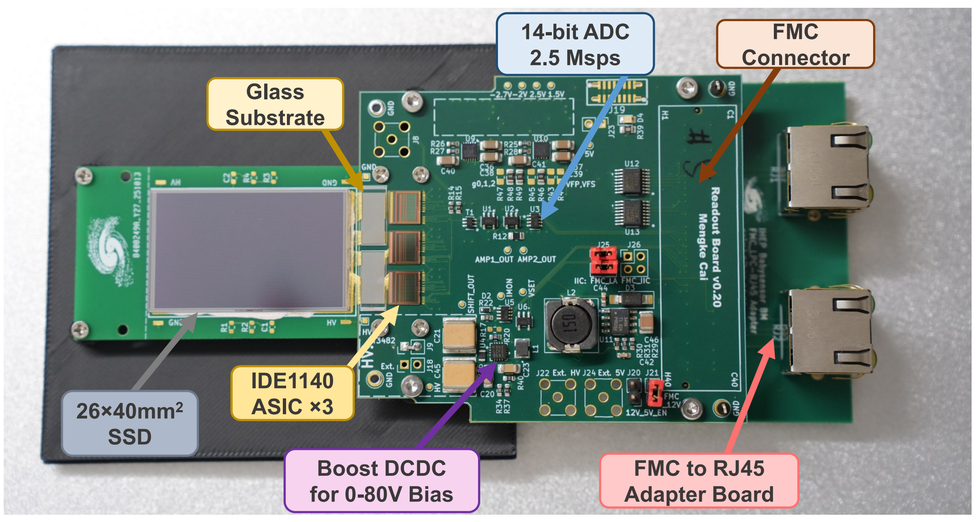


Figure 2. Assembled silicon microstrip detector module and front-end electronics.

ADC Signal Decomposition and Correction

The raw ADC value comprises a channel pedestal, an event-dependent common-mode offset, random noise, and signal:

$$ADC_i^j = Pedeatal_i + CM_{a(i)}^j + Noise_i^j + Signal_i^j$$

where i and j are the channel number and event number. $a(i)$ represents the ASIC channel i connects to.

Pedestals are determined from dedicated pedestal runs. For each event, the common-mode offset is estimated separately for each ASIC using the median pedestal-subtracted channel value.

After pedestal and common-mode noise subtraction, the corrected strip response retains the particle signal and residual noise.

Electronics Characterization

Pedestal data were acquired with the sensor shielded from light in auto-trigger mode at a sensor bias of 50V using 20,000 triggers. Common-mode offsets were estimated separately for each ASIC using the median channel value. The typical channel RMS after common-mode correction was approximately 3.5 ADC counts.

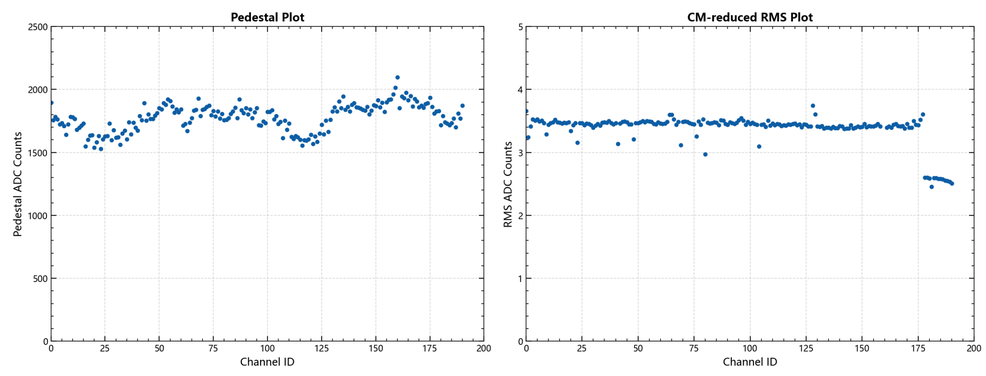


Figure 3. Pedestal and common-mode-reduced RMS distributions measured in auto-trigger mode at a sensor bias of 50 V.

Cosmic-Ray Measurements

Cosmic-ray measurements were performed with a single silicon microstrip module operated at a bias voltage of 50 V. A coincidence signal from two scintillators provided the external trigger. The sensor was shielded from ambient light during data acquisition.

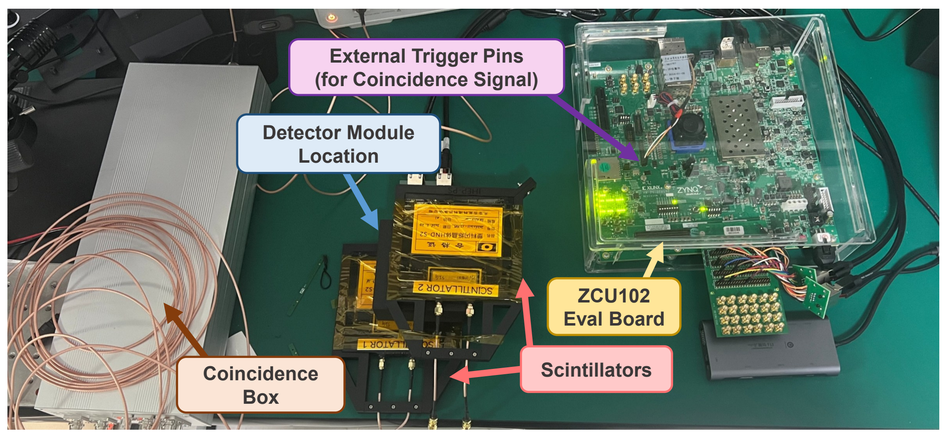


Figure 4. Cosmic-ray test setup shown with the light shielding removed. The sensor was shielded from ambient light during data acquisition.

Signals were corrected for pedestal and common-mode offsets. Cluster selection used a 5σ seed threshold and a 3σ side threshold, where σ is the mean common-mode-reduced RMS of channels remaining after bad and dead channels were excluded.

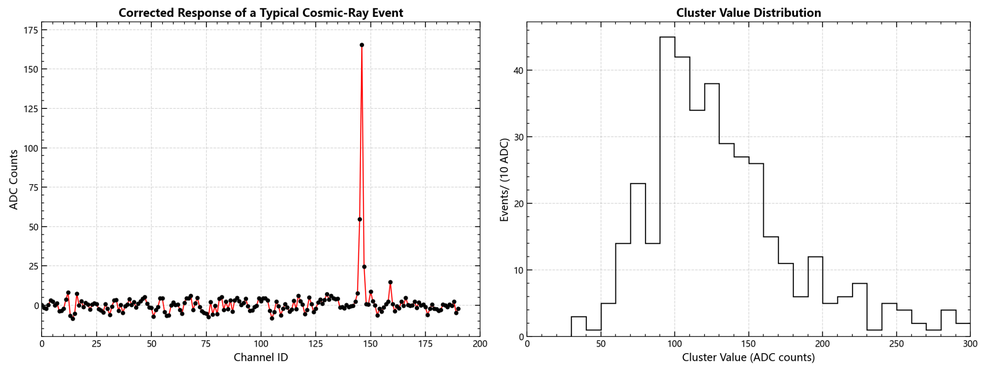


Figure 5. Representative cosmic-ray event and cluster value distribution in the cosmic-ray data. The cluster signal is the sum of the corrected strip signals within each selected cluster

Conclusions & Outlook

- Silicon-microstrip-DAQ system for cosmic-ray, testbeam, and education purpose.
- A very compact design: SSD+FMC+FPGA-board.
- Looking for more economic solutions for readout ASIC and DAQ platform.

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