

L1 trigger Hardware design progress on CEPC ref-Detector

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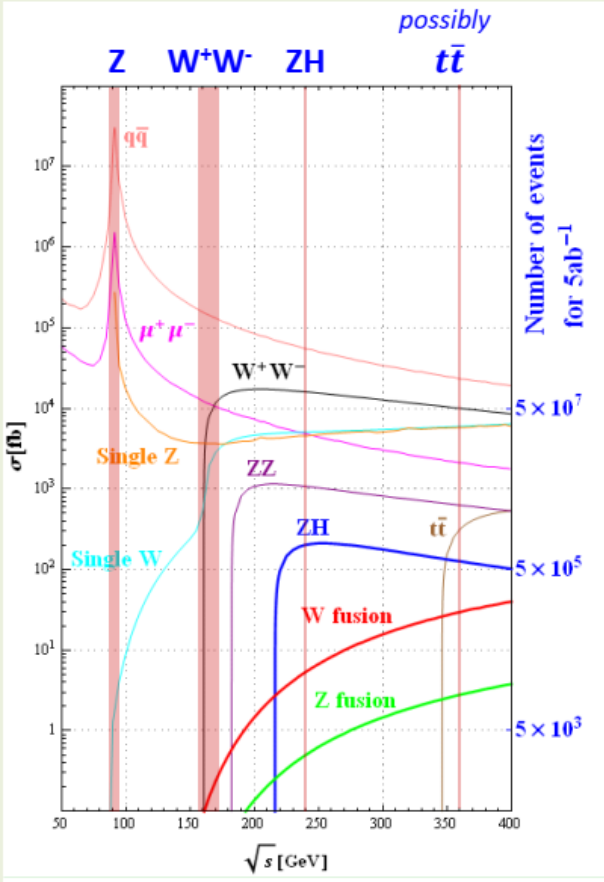
IHEP, Beijing

Content

- Introduction
- TDAQ structure
- L1 trigger design
- R&D progress on Trigger common board
- Summary

Introduction

- The project employs a two phase operational strategy – baseline and upgraded – to accelerate its readiness and maximize its scientific output
- The CEPC is designed to operate at center of mass energies that scale from the Z-pole at 91 GeV to WW at 160 GeV, ZH at 240 GeV, and up to $t\bar{t}$ at 360 GeV.



Baseline operation plan

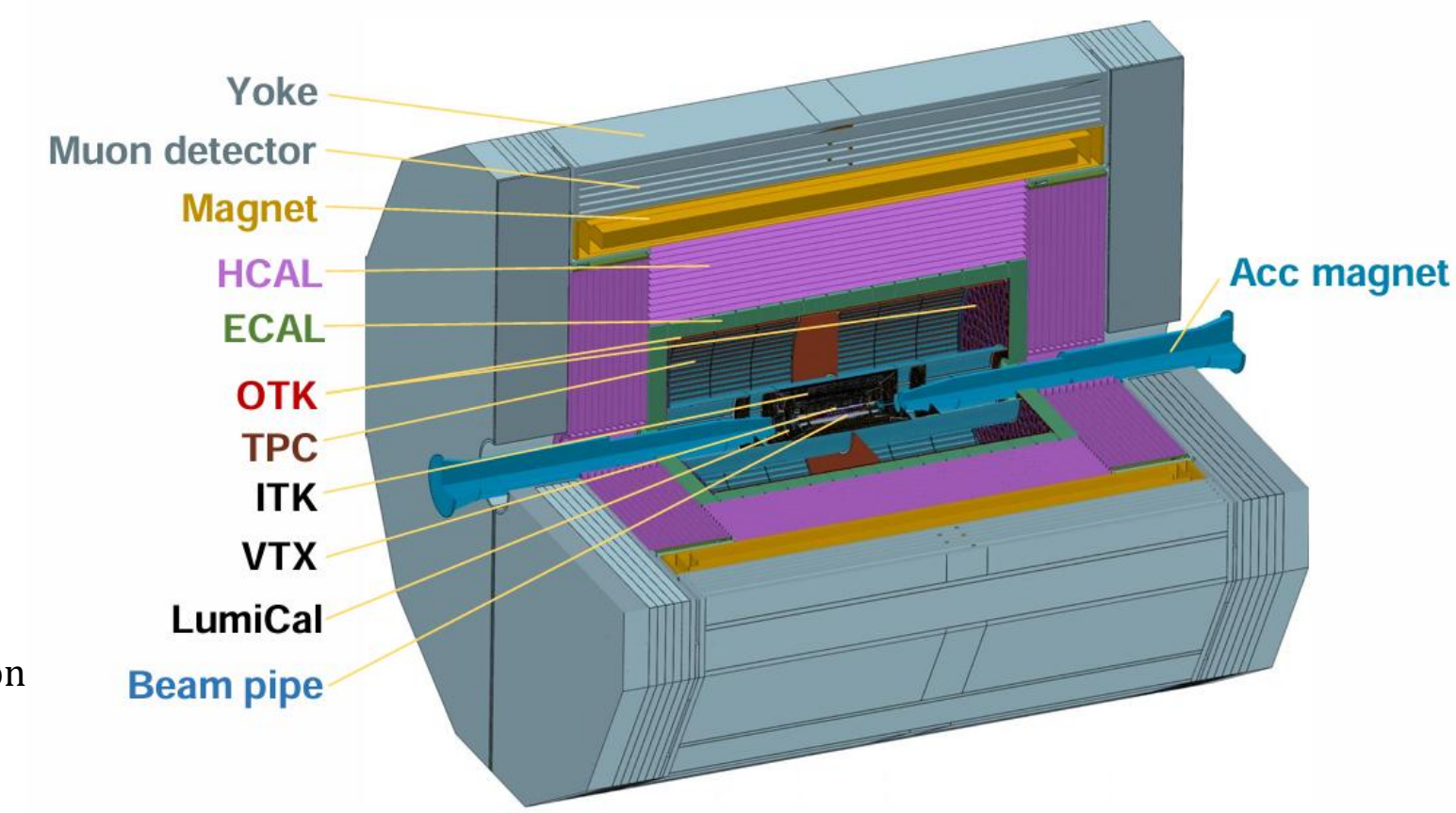
Operation mode	$\sqrt{s}$ (GeV)	SR power (MW)	$\mathcal{L}$ (10^{34} cm^{-2}s^{-1})	$\int \mathcal{L}$/year (ab^{-1})	Years	Total $\int \mathcal{L}$ (ab^{-1})	Event yields
H	240	30	5	0.65	15	10	2.0×10^6
Z	91	12.1	26(*)	3.2	4	13	5.6×10^{11}
W^+W^-	155-170	30	16	1.2	1	1.2	1.0×10^7(†)

Upgrade operation plan

Operation mode	$\sqrt{s}$ (GeV)	SR power (MW)	$\mathcal{L}$ (10^{34} cm^{-2}s^{-1})	$\int \mathcal{L}$/year (ab^{-1}, 2 IPs)	Years	Total $\int \mathcal{L}$ (ab^{-1}, 2 IPs)	Event yields
H	240	50	8.3	2.2	10	21.6	4.3×10^6
Z	91	50	192(*)	50	2	100	4.1×10^{12}
W^+W^-	155-170	50	26.7	6.9	1	6.9	5.5×10^7
$t\bar{t}$	360	50	0.8	0.2	5	1.0	0.6×10^6

Detector Introduction

- Tracking system
  - VTX
    - 6 layers ,5μm resolution
  - ITK
  - TPC
    - Maximum drift time: 34us
  - OTK
    - Maximum drift time: 34us
- Calorimeter system
  - ECAL
    - BGO crystals,18layers,3%/$\sqrt{E(GeV)}$ resolution
  - HCAL
    - 16 sectors, 48 layers
- Muon
    - 6 superlayers,1ns resolution



CEPC Reference detector

Introduction

- Physical Event Rate
  - ~500Hz @ Higgs (1.34Mhz)
  - ~10 kHz @ Low lumi Z (12Mhz)
- Trigger aim is to Retain as many physics events as possible
  - By a Coarse filtering of relevant objects (jets, e, μ, τ, γ...) and their combinations.
  - Based on energy, cluster, track and time relation

Table 12.1: Expected Standard Model processes event rate at the Higgs mode for 50 MW.

Higgs mode processes	Cross section (fb)	Event rate (Hz)
Physical events (top priority)		
Higgs production	203.7	0.017
Two Fermions processes (exclude Bhabha)	6.4×10^4	5.3
Four Fermions processes	1.9×10^4	1.6
Bhabha	1.0×10^6	80
Diphoton process (low priority)		
$\gamma\gamma \to b\bar{b}$	1.6×10^6	136
$\gamma\gamma \to c\bar{c}$	2.1×10^6	173
$\gamma\gamma \to q\bar{q}$	6.0×10^7	4963
$\gamma\gamma \to \mu^+\mu^-$	2.1×10^8	17210
$\gamma\gamma \to \tau^+\tau^-$	2.3×10^6	193

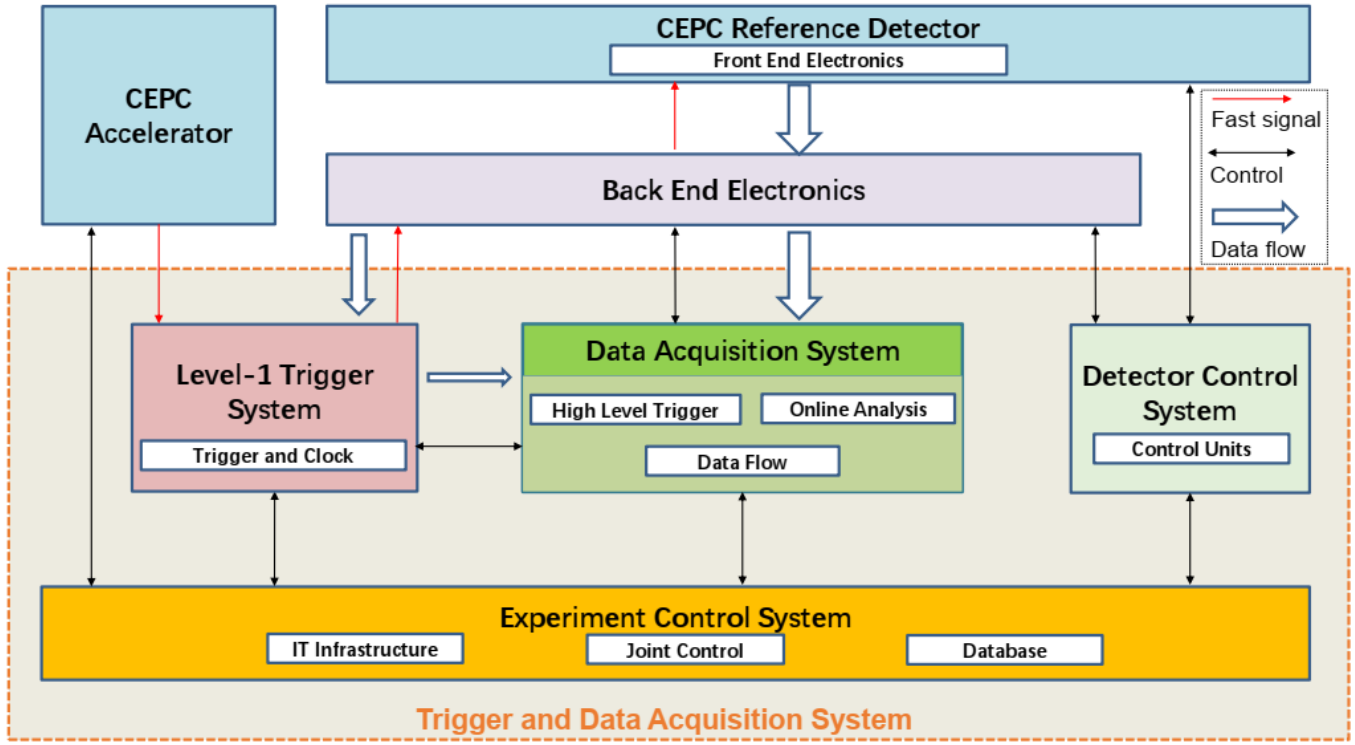
Table 12.2: Expected Standard Model processes event rate at the Z mode for 12.1 MW.

Z mode processes	Cross section (fb)	Event rate (Hz)
Physical events (top priority)		
$q\bar{q}$	3.1×10^7	7970
$\mu^+\mu^-$	1.5×10^6	400
$\tau^+\tau^-$	1.5×10^6	396
Bhabha	6.6×10^6	1714
Diphoton process (low priority)		
$\gamma\gamma \to b\bar{b}$	2.7×10^5	71
$\gamma\gamma \to c\bar{c}$	5.1×10^5	132
$\gamma\gamma \to q\bar{q}$	3.5×10^7	9014
$\gamma\gamma \to \mu^+\mu^-$	1.3×10^8	33696
$\gamma\gamma \to \tau^+\tau^-$	6.3×10^5	163

TDAQ structure

- Electronics framework schema
  - Transmit full raw data from FEE. to BEE Trigger connect with BEE
- Trigger solutions
  - Hardware trigger(L1) + high level trigger(HLT)
  - Expect to reduce beam BG to <1% of BX rate at L1,and <0.1% at HLT

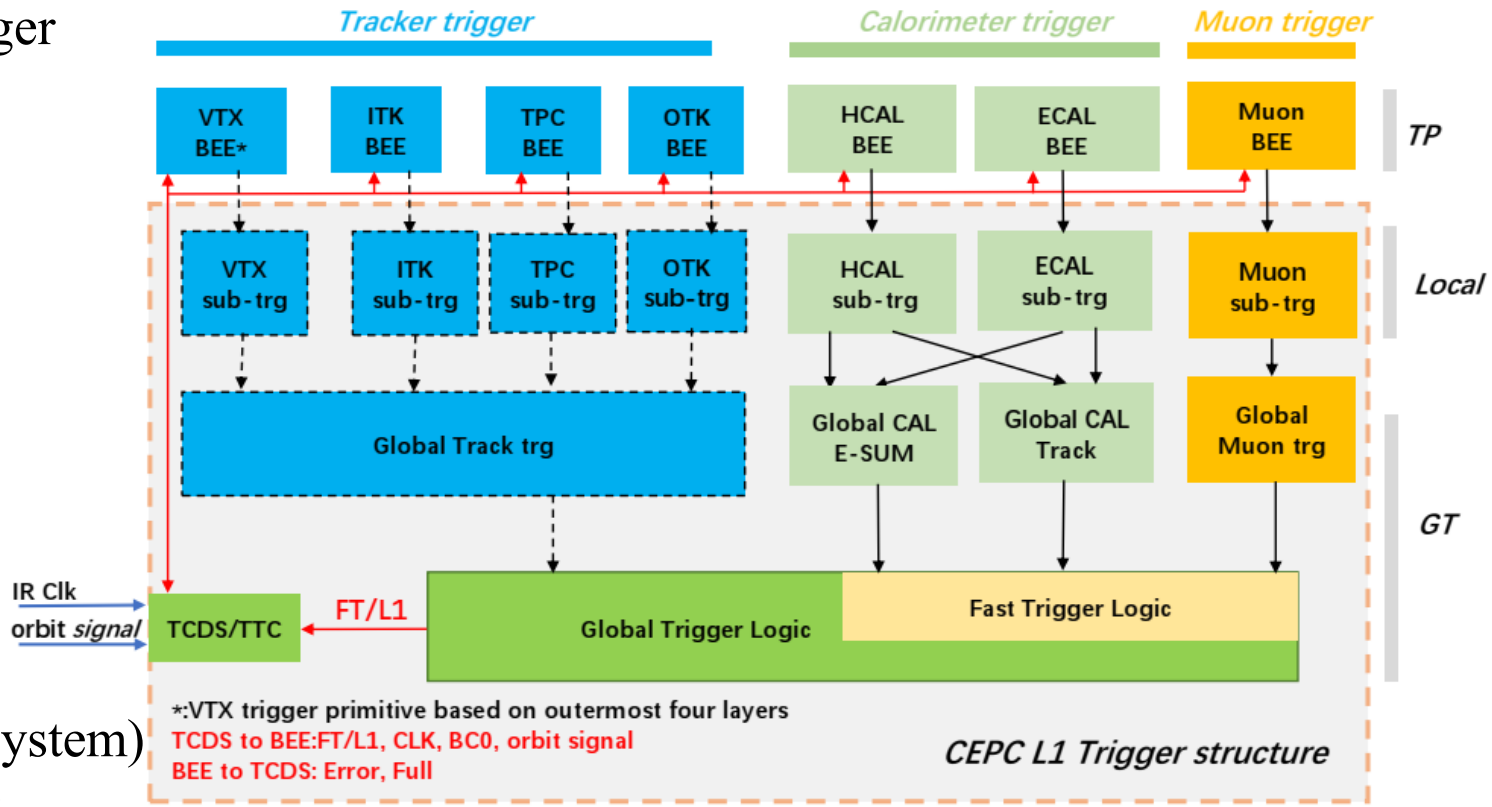
Running mode SR power	Higgs 50 MW	Z 12.1 MW
Non-empty bunch crossing rate(MHz)	1.34	12
Luminosity (10^{34}/cm^2/s)	8.3	26
Physical event rate (kHz)	0.5	10
L1 triger rate (kHz)	20	120
DAQ readout rate (Gbyte/s)	5.34	11.9
HLT rate (kHz)	1	20
Raw event size (kbyte)	405	333
DAQ storage rate (Gbyte/s)	0.405	6.66



Overall structure of TDAQ and Online system for Reference Detector

Hardware Trigger Structure

- Detectors contributing to Hardware trigger
  - ECAL+HCAL+MUON is baseline ,Tracking detectors are optional
- Trigger Primitive
  - Extracted by BEE
- Local detector trigger
  - Local Esum and tracking
- Global trigger
  - Global Esum and tracking match
  - Fast trigger and L1A generation
- TCDS(Trigger and Clock Distribution System)
  - Fast control signal and clock distribute to BEE



L1 Trigger architecture diagram

Each sub-trigger system needs a reliable platform on which to run its trigger algorithms. To reduce duplicated development and support different algorithms on the same hardware, the platform is designed as a common board.

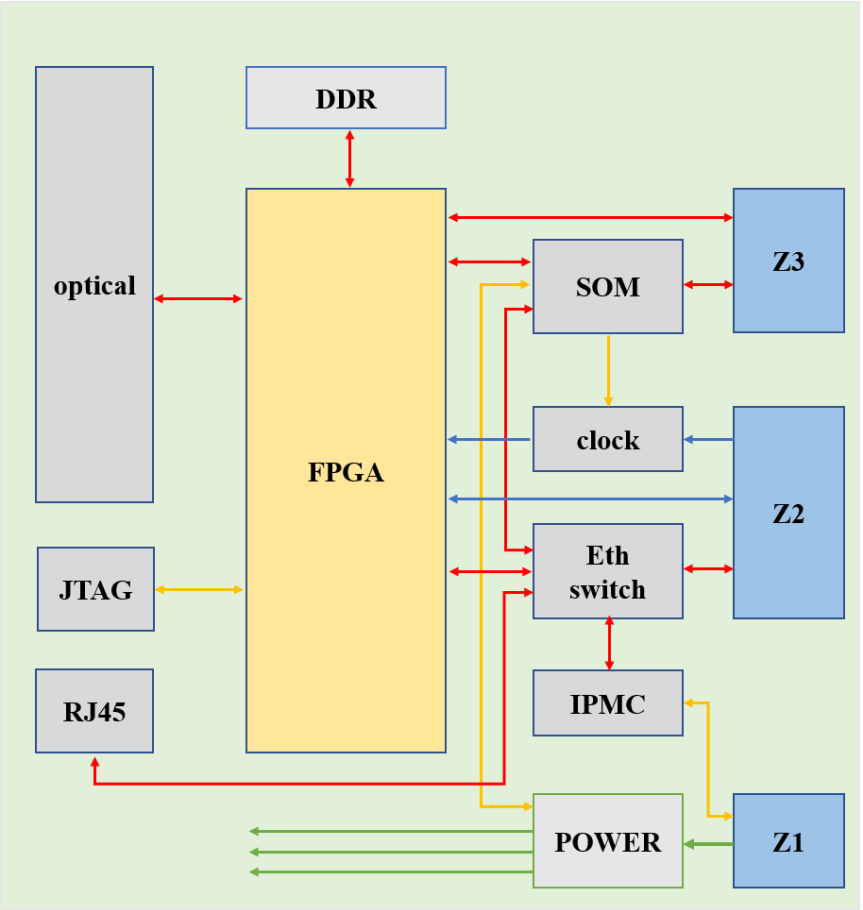
Structure of the common Trigger Board

■ Requirements

- High-speed optical interface
- On-board data buffering(~ms)
- Clock synchronization and configurable clock resources
- Abundant logic resources

■ Board function list

- ATCA standard
- Xilinx Virtex Ultrascale Plus FPGA
- Optical :10-25Gbps@44channel
- DDR4 for mass data buffer
- SOM for board management
- Ethernet Interface connection
- IPMC for Power management
- Clock distribution

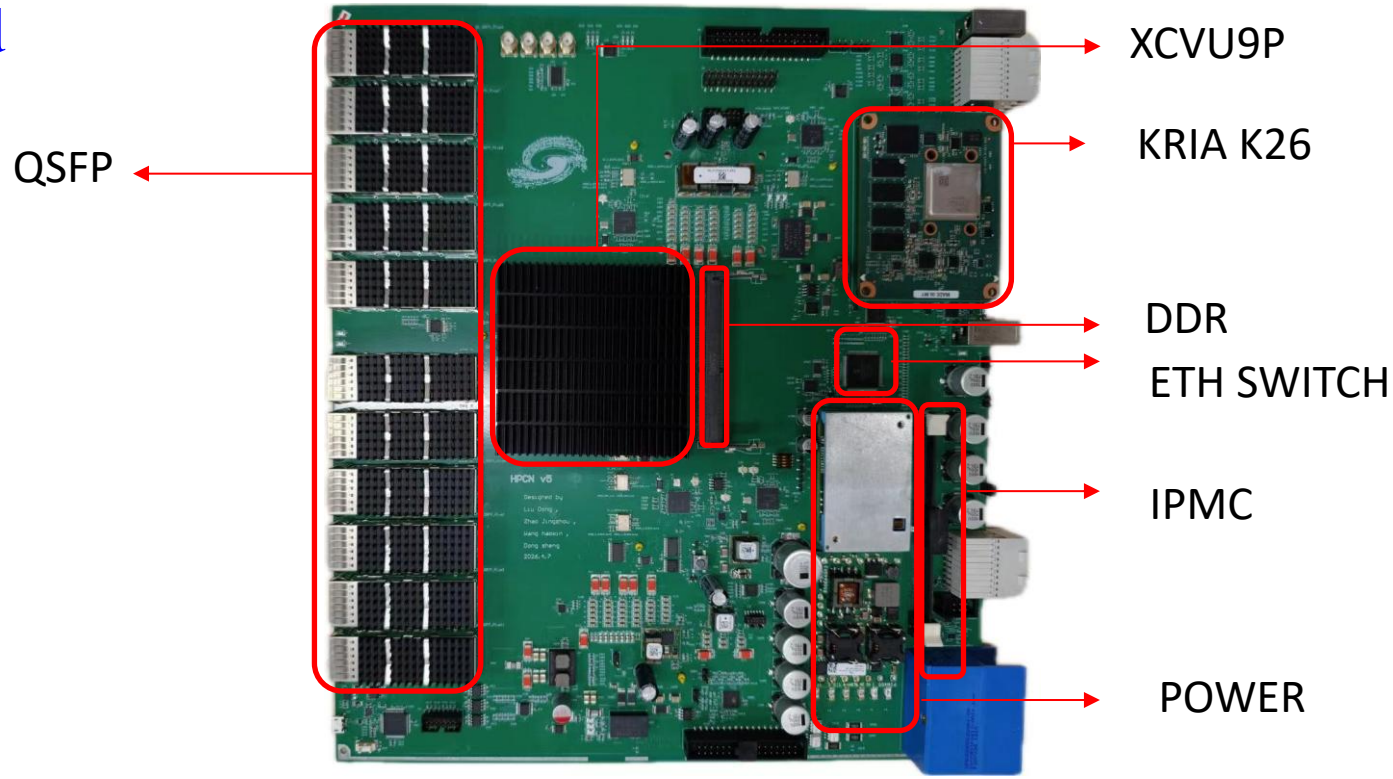


Trigger Common board diagram

Progress on Trigger module R&D

Architecture Definition	Component Selection	Schematic Design	Layout and Routing	PCB Assemble	Board-Level Testing
Done	Done	Done	Done	Done	In Progress

- First version designed and fabricated
  - Component selection
  - Schematic and pcb design
  - Pcb assemble
- Board-Level Testing is ongoing
  - Ground impedance measurement
  - Power & Clock Test
  - FPGA firmware configuration test
  - GTY Test
  - DDR4 Test
  - Board management



Trigger Common board first version prototype

Key components Selection

FPGA

- Xilinx XCVU9P-FLGB2104-2-I
- Package compatible with VU5P / 7P / 11P / 13P and Fudan Microelectronics devices

DDR4

- 64bit ,16GB





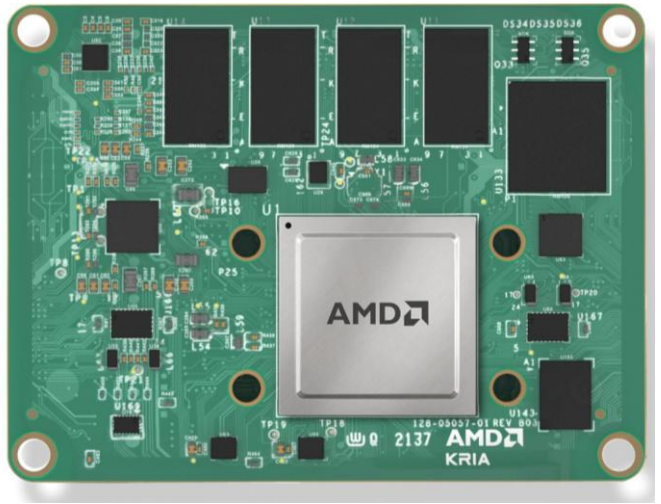


QSFP

- 4 TX/RX module
- 25Gbps/ch

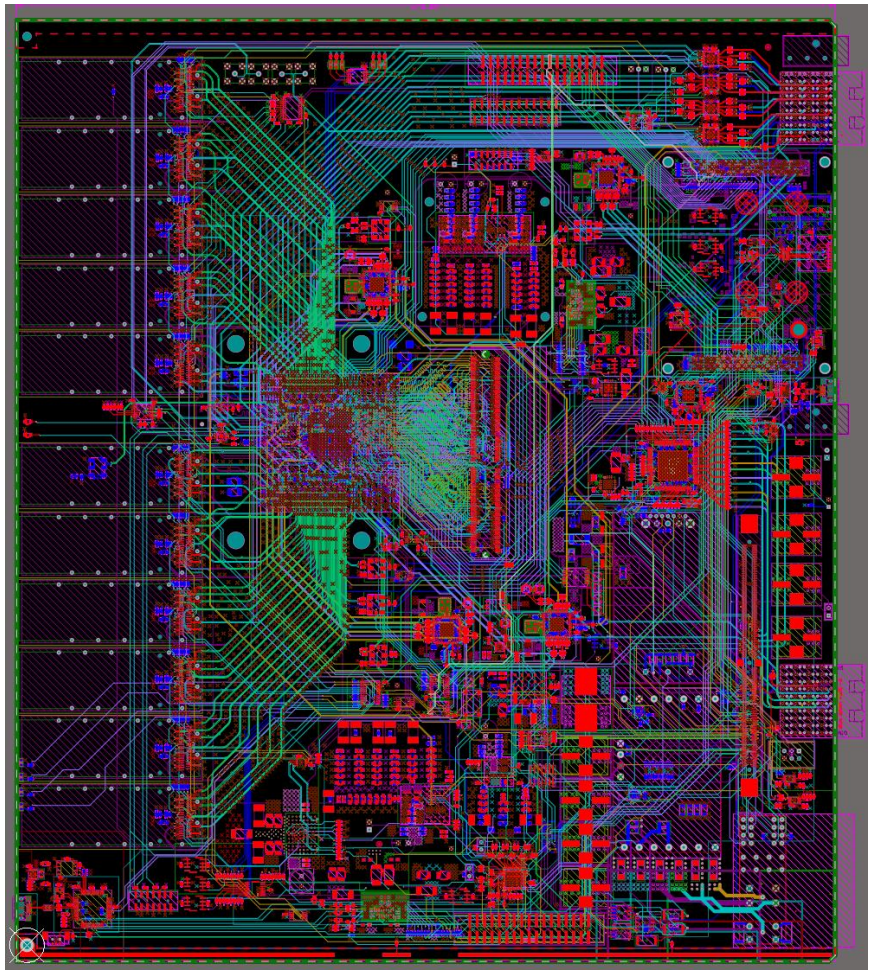
SOM

- Xilinx Kria k26 SOM module
- Linux-based management



PCB Design

- Stack-up
  - 18layers:8 signals,4 gnd,6 power
- High-Speed Interface Arrangement
  - Optimized for impedance control and low loss
  - Back-drilled vias
  - matched-length
- Power
  - Low ripple — FPGA, GTY
  - Current carrying capability
  - Thermal design- layout and heat dissipation for high-current rails



PCB layout of the first prototype

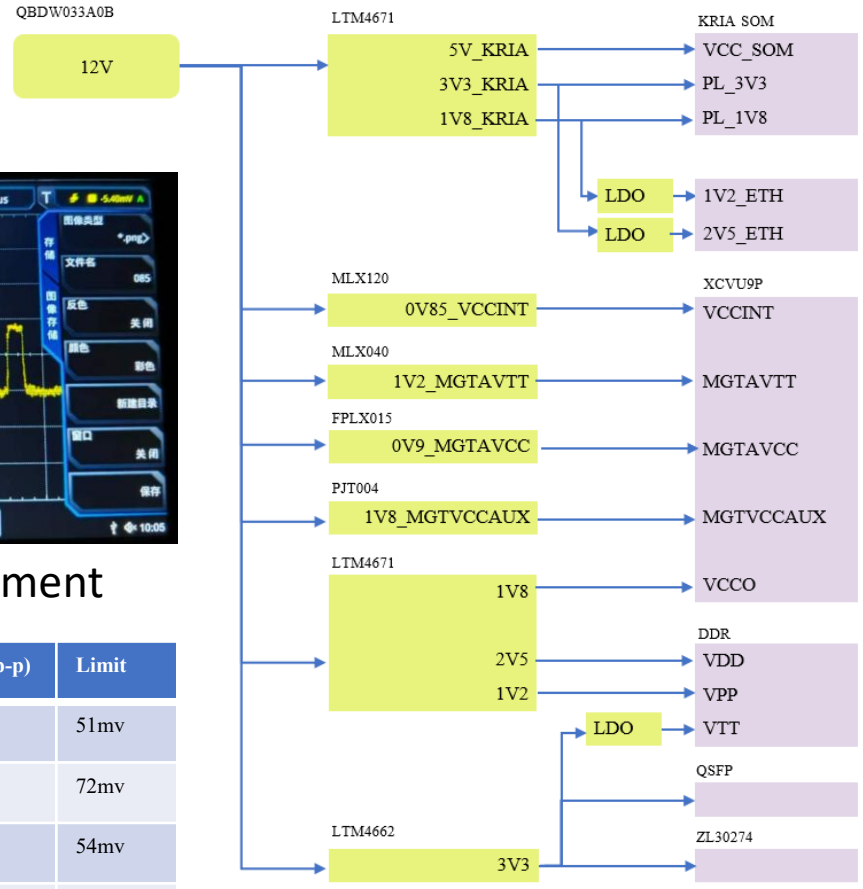
Power Design and test

- Design Requirements
  - Power consumption
    - Estimated max power consumption~200W
    - Designed Power Consumption~280W
  - Low ripple
    - FPGA DDR SOM
- Power Design
  - Multi-stage power architecture
  - Power sequencing
- Testing results
  - Pre-power-up impedance-to-ground test passed
  - All power rails output normally, values as expected
  - Output ripple meets requirements on critical rails



VCCINT ripple measurement

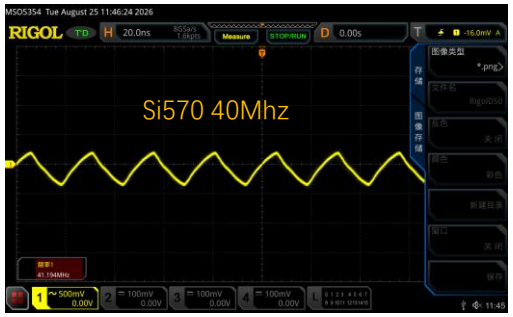
Power rail	Measured(p-p)	Limit
VCCINT_0V85	23mv	51mv
MGTAVTT_1V2	18mv	72mv
MGTAVCC_0V9	19mv	54mv
MGTVCCAUX	17mv	108mv
VCC_SOM	10mv	50mv

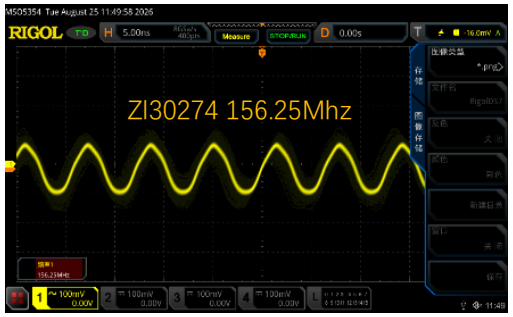


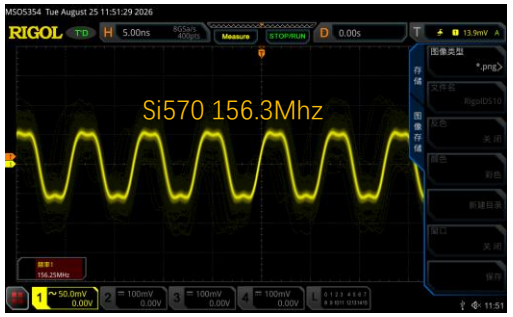
Power structure

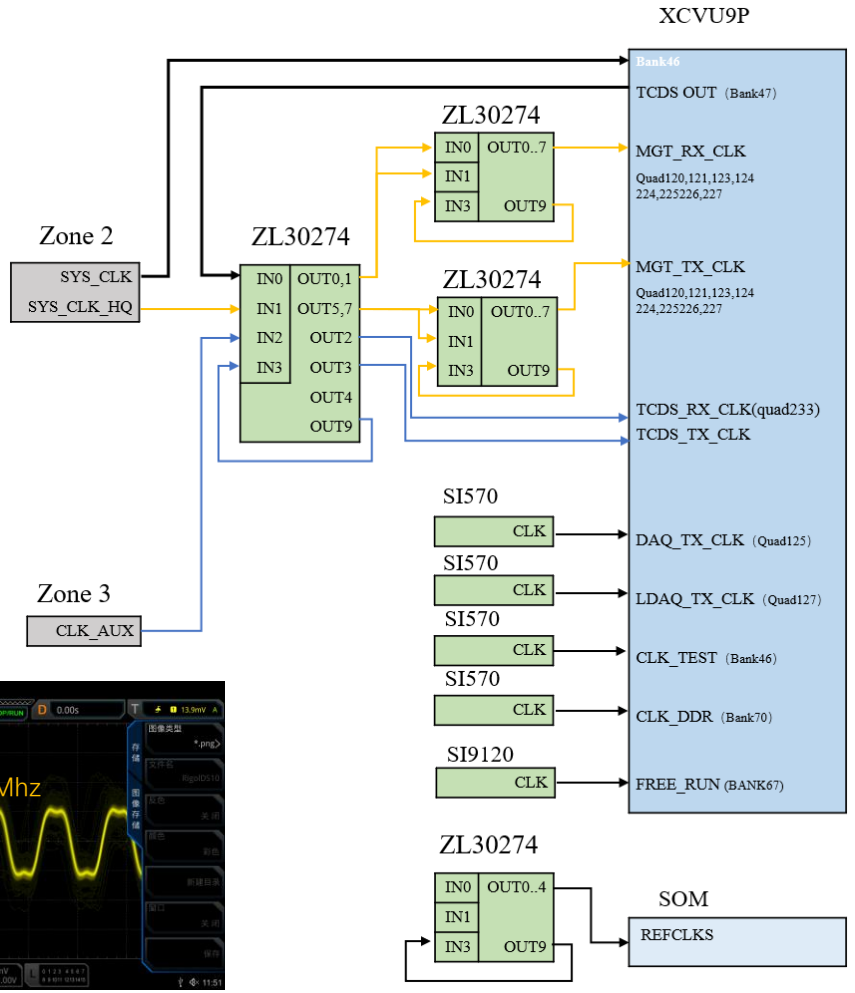
Clock Design and test

- ZL30274
  - 10 output channel
  - zero-delay jitter-cleaner
- Si570
  - I2C programmable— 10 MHz–1.4 GHz, <1 ppb resolution
- Flexible configuration to support diverse applications.
- All clock output frequencies and levels are as expected





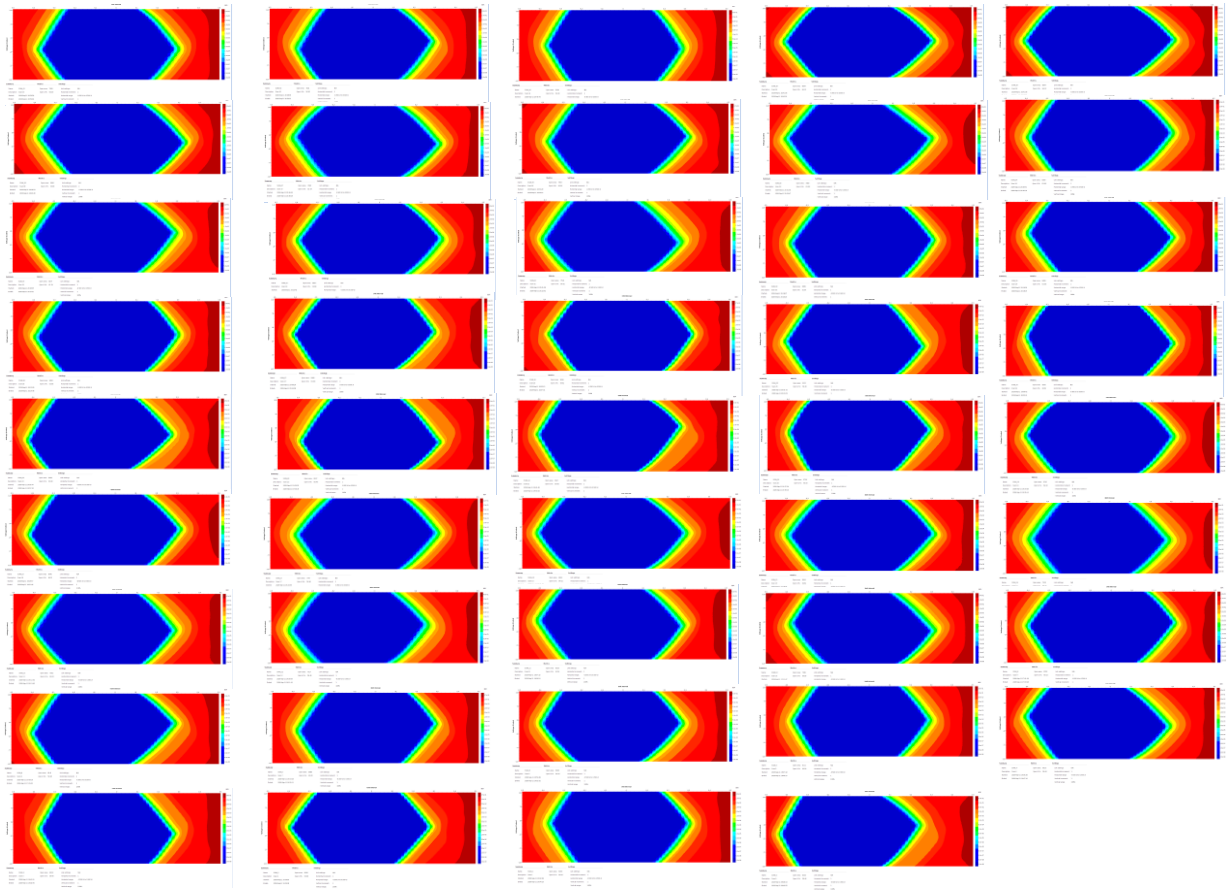




Clock distribution

High speed Transceiver test

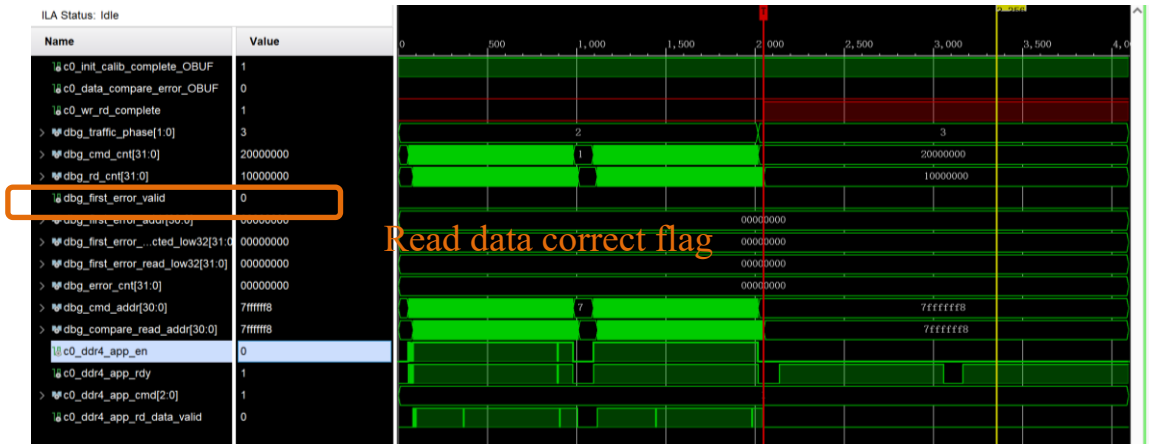
- Test Purpose
  - Verify link reliability over the GTY transceivers
- Test Setup
  - IBERT external fiber loopback@25Gbps
  - 44 channel ,one week
  - Monitor BER and eye opening
- Test Results
  - No errors observed over one week
  - BER better than 10^{-16}
  - Eye opening > 55% on all 44 lanes



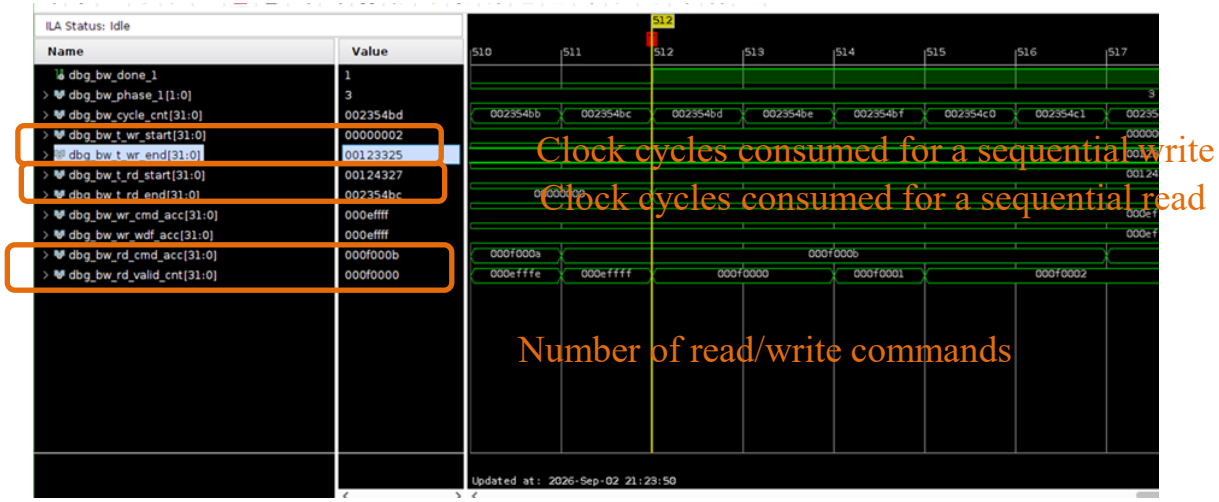
GTY eye-opening measurement

DDR test

- Requirements
  - **Capacity** — ms-level data buffering
  - **Throughput** — > 100 Gbps
- Component Selection
  - MTA16ATF2G64HZ-2G3E1
  - 16GB,64bit max frequency@2400MT/s
- Test results
  - Full-address-space data write/read passed, no anomalies
  - Continuous write bandwidth 112 Gbps, read bandwidth 120 Gbps.
  - Read latency shows a relatively wide distribution



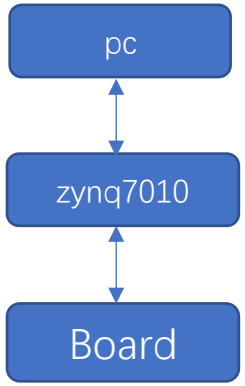
Full-address write/read test

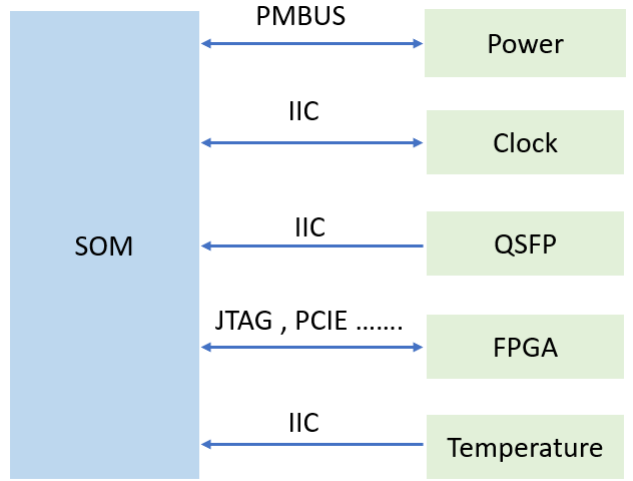


Measured DDR continuous read/write bandwidth

Board management

- **Based on linux**
- **Configuration and monitor**
  - ◆ Power
    - Status monitor ,output value configuration, power sequencing
  - ◆ Clock
    - Stataus monitor ,output configuration
  - ◆ QSFP
    - Status monitor
  - ◆ FPGA
    - Firmware configuration
  - ◆ Temperature
    - Status monitor
- Kria K26 not yet brought up. On-board configuration & monitoring temporarily performed via external ZYNQ-7010 board






```
root@Num6:~/i2c_test/i2c_bus_0# ./max34451.sh
PAGE 0x02 (RS2) 电压: 0x076a
PAGE 0x03 (RS3) 电压: 0x02c0
root@Num6:~/i2c_test/i2c_bus_0# ./max34451.sh
PAGE 0x02 (RS2) 电压: 0x076a
PAGE 0x03 (RS3) 电压: 0x02c1
```

```
root@Num6:~/i2c_test/i2c_bus_0/zl30274# ./zl30274_config 10_zl30274.mfg
Connected to ZL30274 at I2C address 0x70
Parsing configuration file: 10_zl30274.mfg

Configuration completed successfully!
Total I2C write commands executed: 1134
```

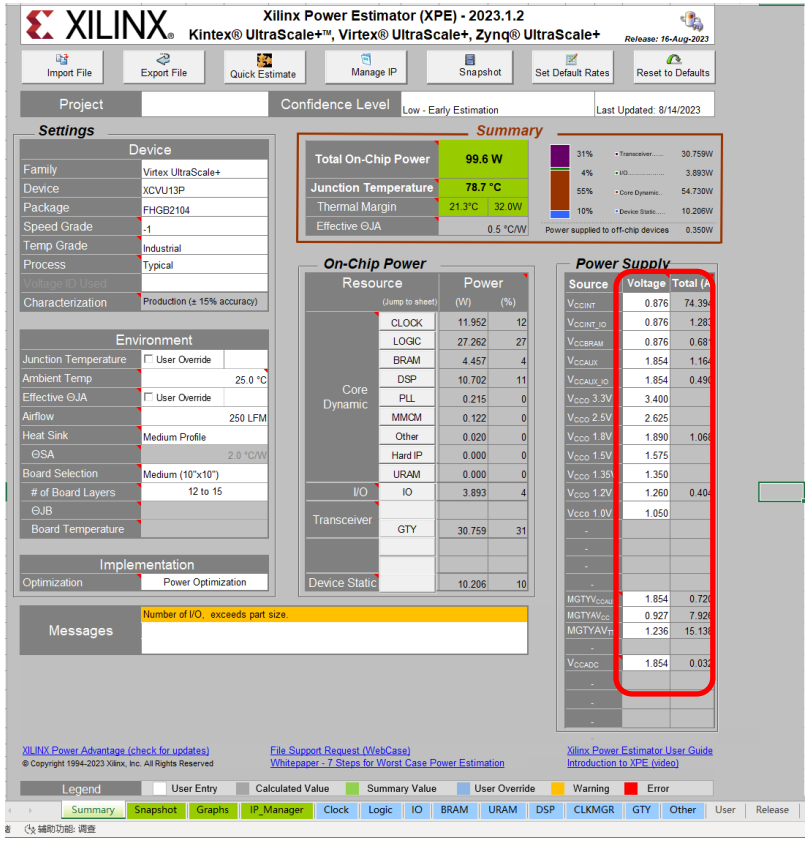
Summary

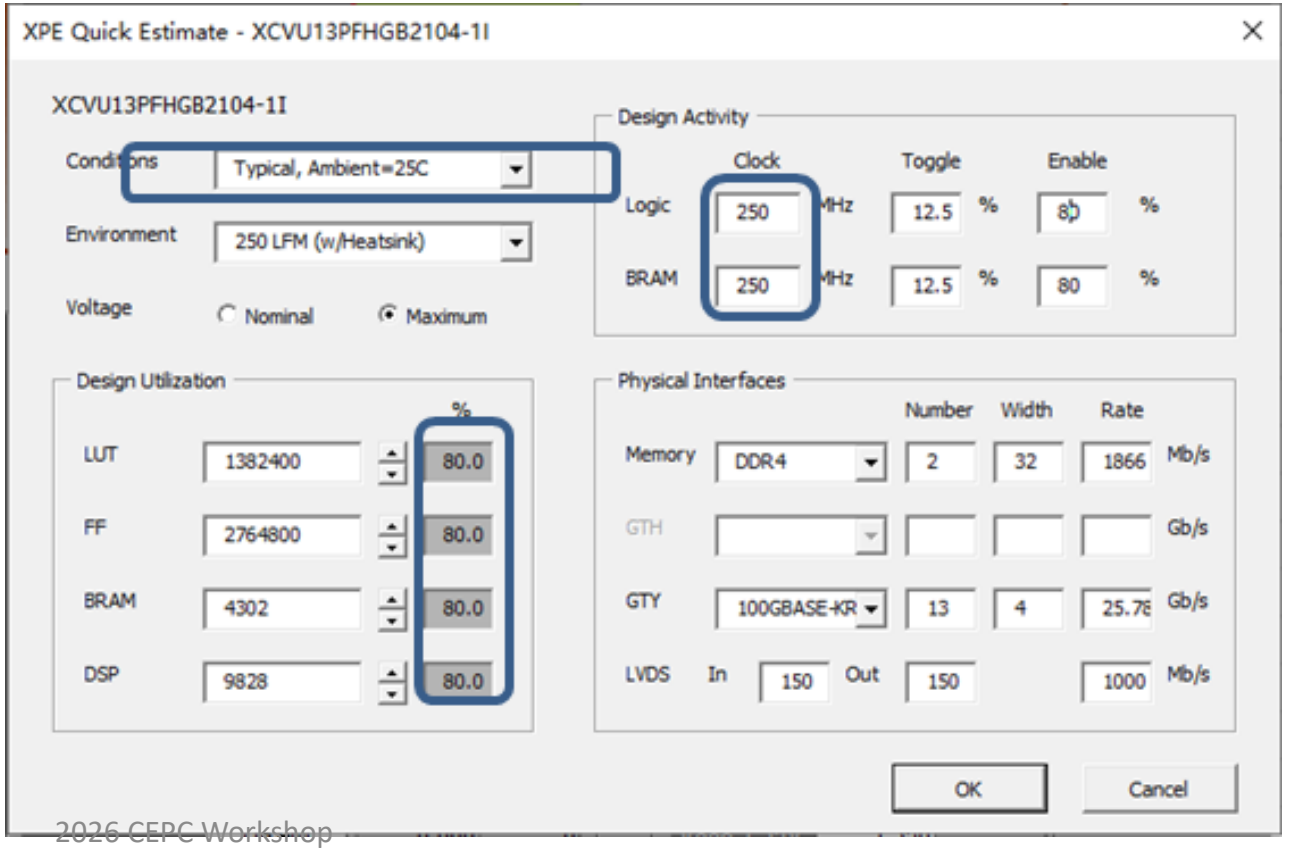
- L1 Trigger is a key system for CEPC ref-detector.
- Trigger strategy : Hardware trigger(L1) + high level trigger(HLT)
- Baseline L1 trigger strategy: Ecal+Hcal+Muon
- L1 trigger system structure is designed. Common trigger board will be used for trigger algorithm.
- R&D on the trigger board is ongoing. The first prototype has been designed and fabricated, and board-level functional tests are largely completed. The test results meet expectations and indicate that the board's key functions operate properly.

Thank you.

BACK UP

- Power consumption estimation using XPE
  - FPGA： XCVU9P or XCVU13P(Compatible with domestic chips)
  - Evaluate the power consumption of the Xilinx XCVU13P FPGA under specified operating conditions to guide optimal power supply design.





BACK UP

- QSFP power consumption
  - Optical transceiver :36-48 channels
  - Recommand :QSFP*10 (40 channels)
  - 3.3V Power Rail Current Estimation 1.2*10 = 12A

Performance	
SFP transceiver type *	Fiber optic
Maximum data transfer rate *	100000 Mbit/s
Interface type *	QSFP28
Single-mode fiber (SMF) supported	✕
Multi-mode fiber (MMF) supported	✔
Fiber optic connector	MPO-12
SFP transceiver standard	SR4
Maximum transfer distance	100 m
Wavelength	850 nm
Ethernet LAN	✔
Ethernet interface type	100 Gigabit Ethernet
Fiber ethernet cabling technology	100GBASE
Digital Diagnostics Monitoring (DDM)	✔
Features	
Product colour	Silver
Housing material	Metal
Plug and Play	✔
Hot-Plug support	✔
Hot-swap	✔
Easy to install	✔
Brand compatibility	Arista Networks
Power	
Input voltage	3.3 V
Maximum voltage	3.5 V

Power	
Power consumption (typical)	4 W
Certificates	
Compliance certificates	TÜV mark, UKCA, UL, US FDA, REACH, Federal Communications Commission (FCC), RoHS, CE
Certification	CE, FCC, RoHS, REACH
Sustainability	
Sustainability compliance	✔
Doesn't contain	Lead
Operational conditions	
Minimum operating temperature	0 °C
Maximum operating temperature	70 °C
Operating temperature (T-T)	0 - 70 °C
Storage temperature (T-T)	-40 - 85 °C
Operating relative humidity (H-H)	0 - 95%
Storage relative humidity (H-H)	0 - 95%
Weight & dimensions	
Width	13.5 mm
Depth	72.4 mm
Height	18.4 mm
Weight	100 g
Packaging content	
Quantity per pack	1 pc(s)
Packaging data	
Package type	Box
Logistics data	
Country of origin	United Kingdom

- Clock and Ethernet switch power consumption
  - ETH switch :
    - 6 or more ports
    - Recommend : KSZ9897R(7 ports) Estimation 2A
  - Clock fan out : QSFP*10 ,FPGA.....
    - Recommend : ZL30274 *2 (8*2) Estimation 1A

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Supply Current - Full 1000 Mbps Operation						
I_{DD_AH}	**AVDDH** supply current	**VDDIO** @ 3.3V Ports 1-5 in 1000BASE-T Ports 6 & 7 in RGMII (1000 Mbps) All ports 100% utilization		330		mA
I_{DD_IO}	**VDDIO** supply current			80		mA
I_{DD_CA}	**AVDDL** supply current			460		mA
I_{DD_CD}	**DVDDL** supply current			750		mA

TABLE 9-3: ELECTRICAL CHARACTERISTICS: SUPPLY CURRENTS

Characteristics	Symbol	Min.	Typ. (Note 1)	Max.	Units
Total power, two CMOS REF inputs, Synth1 and six LVDS outputs enabled	P_{DISS}	—	0.8	—	W
Total current, 3.3V supply (VDD33+VDDOx pins)	I_{DD33}	—	160	322	mA
Total current, 1.8V supply (VDD18 pins)	I_{DD18}	—	207	519	mA