A Unified Sensor-Front-End Optimization Framework for 55nm HV-MAPS

Bingchen Yan[1], Yang Zhou[1], Leyi Li[1,6], Jianpeng Deng[3], WeiGuo Lu[1], Pengxu Li[3], Xiaoxu Zhang[1,4], Xiaomin Wei[2], Mei Zhao[1], Yu Zhao[2], Zheng Wei[2], Yang Chen[5], Yujie Wang[5], Zhan Shi[5], Hongbo Zhu[3], Meng Wang[6], Jianchun Wang[1], Yiming Li[1]

[1]Institute of High Energy Physics, CAS, Beijing, China [2]Northwestern Polytechnical University, Xi'an, China
[3]Zhejiang University [4]Nanjing University, Nanjing, China [5]Dalian Minzu University, Dalian, China [6]Shandong University, Qingdao, China

Introduction

The CEPC Inner Tracker targets a timing resolution of approximately 3 ns and a power consumption below 150 mW/cm². This work presents a sensor–front-end co-optimization framework for MAPS in a domestic 55nm HV-MAPS process, where deep-well parasitic capacitance (Cw) dominates the front-end load.

A calibrated TCAD model decomposes the sensor capacitance and provides 3×3-pixel electric-field data, which is imported into Allpix² to simulate the collected charge and charge collection time. The AFE is optimized via gm/ID methodology under the extracted parameters to achieve sub-1 ns jitter with minimal power. This establishes a practical sensor-AFE co-optimization flow for CEPC ITK pixel chip development.

TCAD Capacitance Analysis

A 3 × 3 pixel array was modeled and simulated in TCAD to identify the contributions to the sensor capacitance. Capacitance decomposition shows that coupling to the P-well and deep P-well within the central pixel dominates, contributing approximately 229 fF out of a total of 262 fF (87%) .

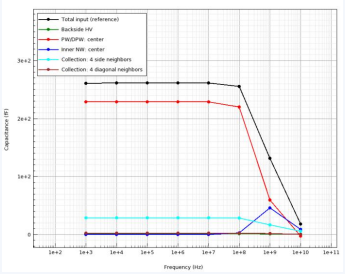


Fig. Dominant capacitance contributions.

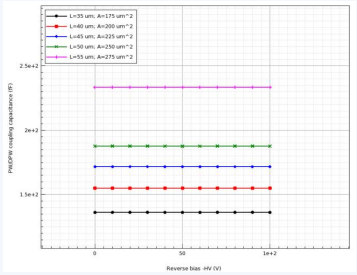


Fig. DPW area dependence.

The dependence on deep P-well area was further investigated through a geometry scan. The results clearly show that reducing the deep P-well area effectively lowers the sensor capacitance.

Allpix² Charge Collection Simulation

Signal collection was simulated in Allpix² using TCAD electric fields from a 3 × 3 pixel array, with normally incident 3 GeV protons, a −200 V bias, and a substrate resistivity of 2000 Ω·cm.

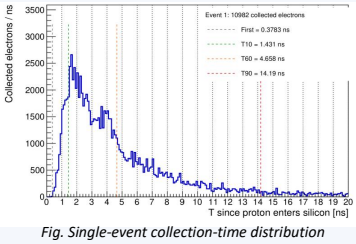


Fig. Single-event collection-time distribution

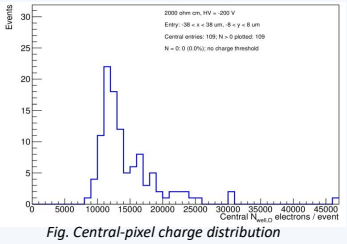


Fig. Central-pixel charge distribution

The collection-time distribution features a fast leading edge followed by a long tail. In a representative event, approximately 60% of the charge is collected within 5 ns. The collected-charge distribution for direct central-pixel hits mainly spans 8–25 ke⁻ , with a typical signal of 11–13 ke⁻ .

The rapid charge collection sets requirements on AFE bandwidth and response speed, while the collected-charge range guides the required input sensitivity and dynamic range.

From Requirements to AFE Design

$$C_{eq} = C_d + \frac{C_c C_i}{C_c + C_i}$$

The Ceq, used throughout the following analysis, represents the effective capacitive load referred to the sensor collection node. Cd,Cc,Ci, and Cfb are the total sensor, coupling, amplifier input, and feedback capacitances, respectively.

1. Open-loop gain requirement

For a maximum relative gain loss δ_{max}

$$G_Q = \frac{1}{C_{fb} + \frac{C_{eq}+C_{fb}}{A\alpha}} \qquad \delta = 1 - \frac{G_Q}{G_{Q,ideal}} \le \delta_{max} \qquad A \ge \frac{1-\delta_{max}}{\alpha\delta_{max}}\left(1 + \frac{C_{eq}}{C_{fb}}\right)$$

Larger Cd requires higher open-loop gain for the same tolerated signal loss.

2. Timing requirement and transconductance

For a single-pole response, timing jitter is approximately

$$\sigma_t \approx \frac{ENC}{N_{min}} \frac{\tau}{1-\eta}$$

With ENC = 200 e⁻ , N_{min} = 2000, and threshold fraction η = 0.5, subnanosecond jitter requires τ < 5 ns.

$$\tau \approx \frac{C_{eff,A}}{\alpha\kappa g_{m,in}\beta} \qquad C_{eff,A} = C_{L,A} + \frac{C_{fb}C_{eq}}{C_{eq}+C_{fb}} \qquad g_{m,in} \gtrsim \frac{C_{L,A}\left(1+\frac{C_{eq}}{C_{fb}}\right)+C_{eq}}{\alpha\kappa\tau_{max}}$$

Larger C_{eq} demands higher g_m to preserve timing performance.

3. Low-noise requirement

For sufficient loop gain, the series-noise contribution and the input-transistor noise spectra are approximately given by:

$$ENC_{series} \approx \frac{C_{noise}}{q} e_{n,rms} \qquad C_{noise} = (C_d + C_{fb})\left(1 + \frac{C_i}{C_c}\right) + C_i \qquad S_{v,th} \approx \frac{4kT\gamma}{g_m} \qquad S_{v,1/f} \approx \frac{K_{eff}}{WLf}$$

4. Power constraint

$$g_m \approx \sqrt{2\mu C_{ox}\frac{W}{L} I_D}, \qquad I_D = \frac{g_m}{g_m/I_D}, \qquad P_{AFE} \approx V_{DD}\sum I_D.$$

Improving timing performance and reducing noise often require higher power consumption. Reducing Cd simultaneously relaxes gain, speed, and noise constraints, making capacitance reduction a key route to power-efficient sensor–AFE co-optimization.

AFE Simulation Results

Simulations are performed with a 200 fF input sensor capacitance, covering 2k–20k electrons.

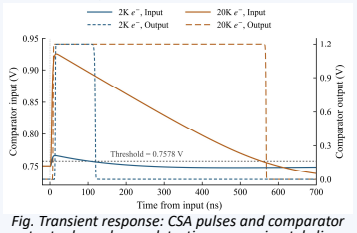


Fig. Transient response: CSA pulses and comparator outputs show charge detection, approximately linear discharge, and no saturation at 20k electrons.

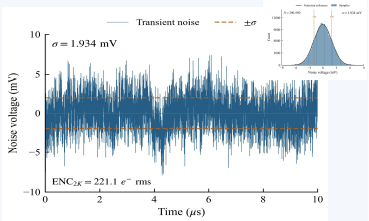


Fig. Noise: The output RMS noise is 1.934 mV, corresponding to ENC ≈ 221 electrons.

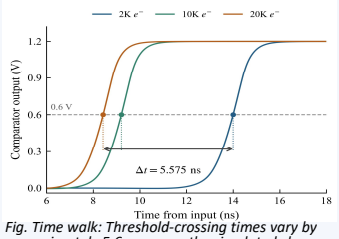


Fig. Time walk: Threshold-crossing times vary by approximately 5.6 ns across the simulated charge range.

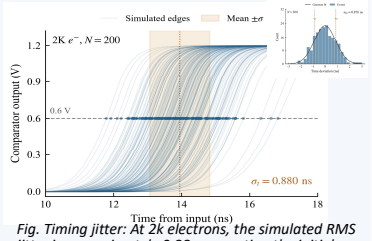


Fig. Timing jitter: At 2k electrons, the simulated RMS jitter is approximately 0.88 ns, meeting the initial subnanosecond target.

Summary & outlook

This work establishes a sensor–AFE co-design flow linking TCAD, Allpix², and analog front-end simulations. With sensor capacitance as the key design variable, the analysis identifies its dominant contributions (DPW) and evaluates its influence on AFE gain, response speed, and noise. The work also defines a systematic path from experimental requirements to circuit performance targets and transistor sizing, providing a methodological foundation for further parameter optimization and design iterations.

Email: yanbc@ihep.ac.cn