First beam test results of COFFEE3, an HV-CMOS Pixel Prototype for the CEPC Inner Tracker

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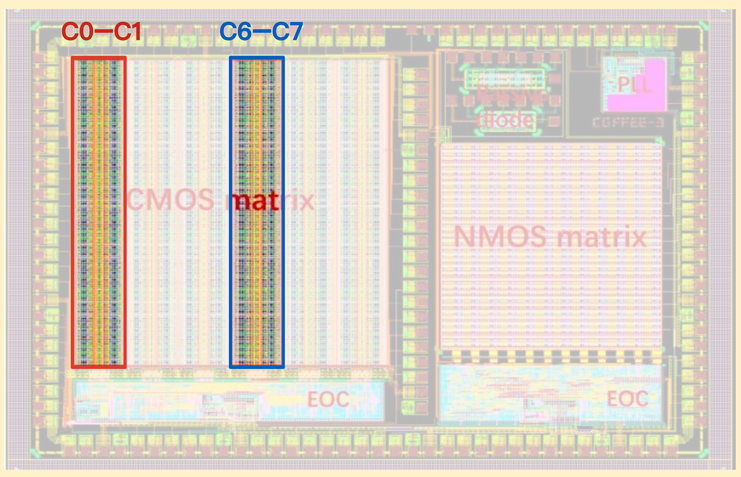
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Introduction

COFFEE3 is a 55 nm HV-CMOS pixel sensor prototype developed for the CEPC inner tracker. Following laboratory characterization, two beam-test campaigns were carried out at the CERN SPS in May and July 2026. This poster presents particle response in two double-columns, timing and timewalk measurements on a test pixel, and tracking with a silicon-strip beam monitor. Laboratory threshold tuning and high-threshold hit bursts motivate further calibration and design studies.

COFFEE3 Chip Design

- Chip size: 4000 × 3000 μm²
- CMOS array: 48 rows × 12 columns
- Pixel pitch: 36 × 130.5 μm²
- Tested double-columns: C0–C1 and C6–C7
- Two CSA variants and 4-bit pixel TDACs
- In-pixel timing and peripheral readout

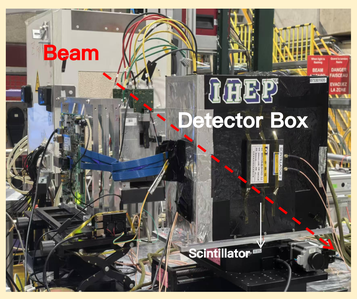


COFFEE3 chip layout

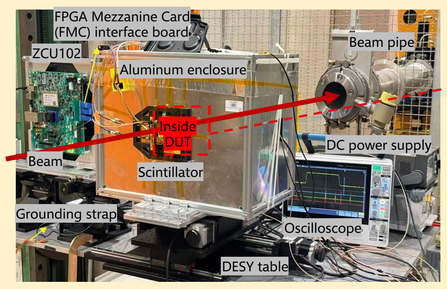
Beam-Test Setup

- May 2026: SPS H6, 200 GeV hadrons
- Tracking references: 6-layer silicon-strip beam monitor
- Trigger: two scintillators in coincidence with COFFEE3

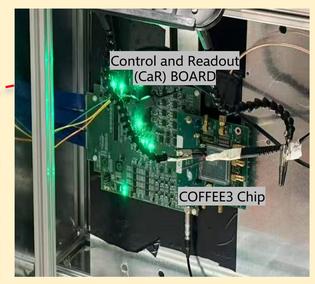
- July 2026: SPS H8, 180 GeV hadrons
- Timing references: three scintillators
- Beam intensity: ~2 × 10⁶ particles/spill



May: tracking setup



July: beam-test setup

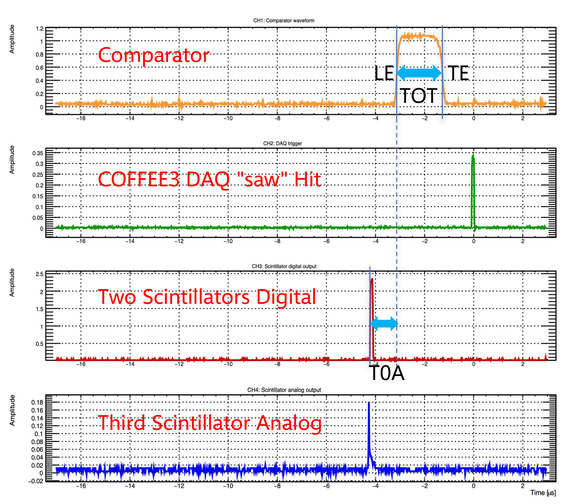


DUT and CaR board

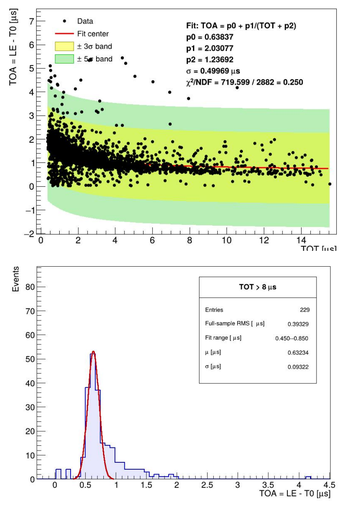
Test Results

1 Single-pixel timing and timewalk

Timing measurements are performed on a test pixel: TOA = LE − T0 and TOT = TE − LE. For TOT > 8 μs, the fitted TOA core has σ ≈ 93 ns. Measured times include test-system delays and do not represent intrinsic chip timing.



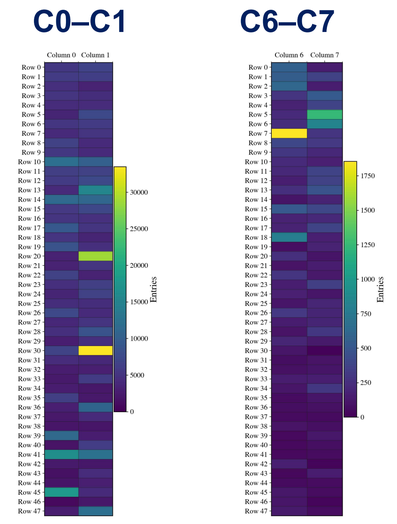
Beam-test waveforms and timing definitions



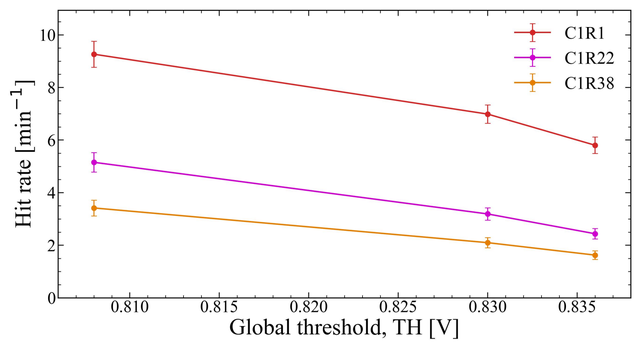
Test-pixel timing

2 Multi-pixel response and threshold scan

All 192 pixels in the two tested double-columns, C0–C1 and C6–C7, respond to particle hits. For representative pixels, the particle-hit rate decreases as the global threshold increases.



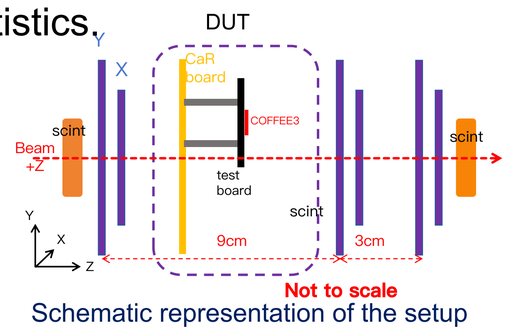
Beam-test hit maps
96 pixels per double-column



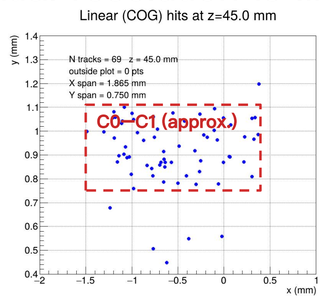
Particle-hit rate versus global threshold
Three representative pixels

3 Tracking with the silicon-strip monitor

Tracking confirms the expected pixel geometry: X pitch = 36.5 ± 0.8 μm (design: 36 μm); Y separation is consistent with the 130.5 μm design pitch. Further study on spatial resolution is limited by statistics.



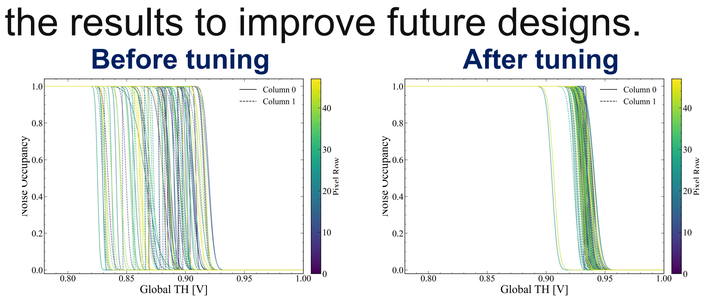
Schematic representation of the setup



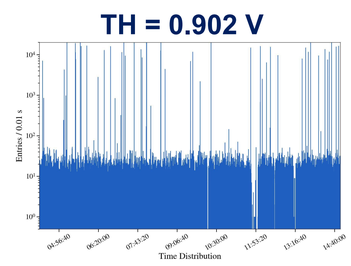
Projected track positions

4 Future study for COFFEE3

Laboratory TDAC tuning on the first double-column (96 pixels) reduces the S-curve spread from ~0.10 V to ~0.02 V. Next: tune before beam tests, investigate high-threshold hit bursts and use the results to improve future designs.



Laboratory TDAC tuning on the first double-column



High-threshold hit bursts

Summary & Outlook

COFFEE3 demonstrates particle response and array readout in all 192 tested pixels. Test-pixel measurements show timewalk and a ~93 ns TOA core width for TOT > 8 μs, including test-system contributions. Laboratory TDAC tuning improves threshold uniformity in the first double-column, reducing the S-curve spread from ~0.10 V to ~0.02 V. Track projections agree with the pixel geometry. Further work will investigate high-threshold hit bursts and quantify efficiency and intrinsic timing performance.

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