



Development Status & Plans of Serial Powering at IHEP

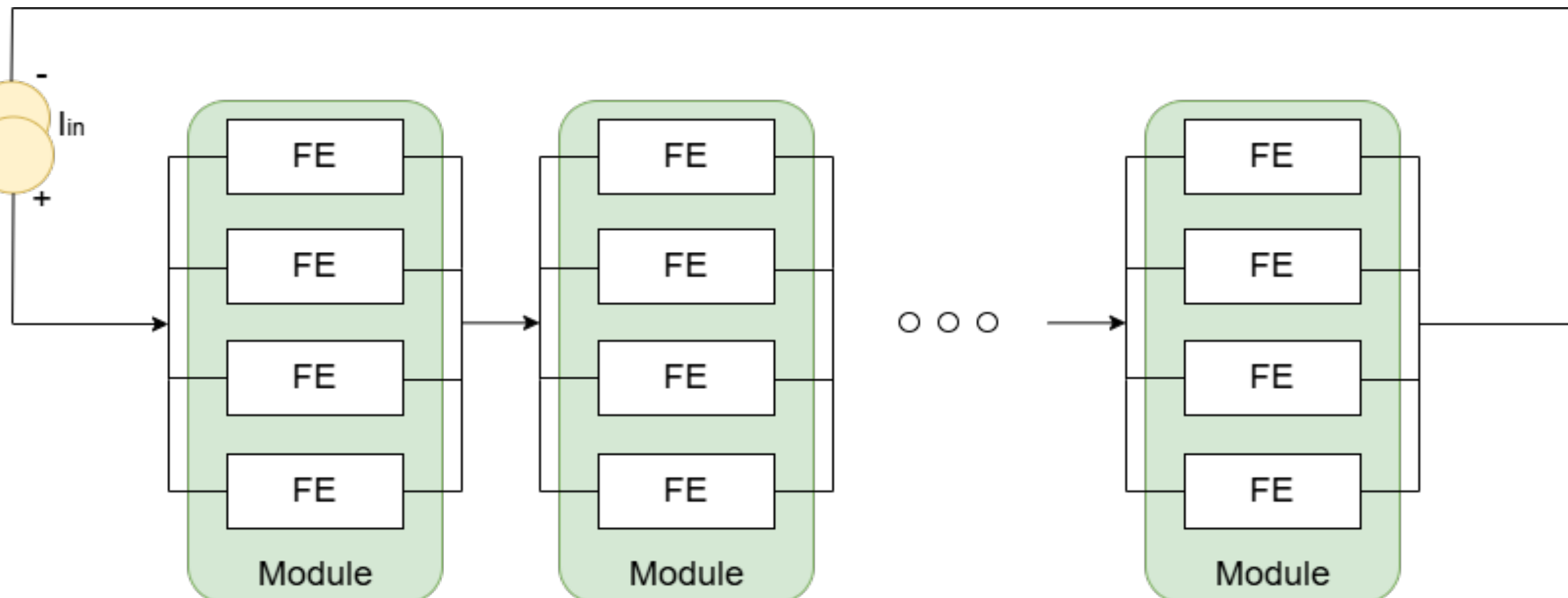
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Abstract

The increasing level of front-end integration in particle detector has placed new requirements for powering system, particularly in terms of material budget, power distribution, and system scalability. Serial powering, based on a constant current scheme with shunt-LDO regulars (SLDO), has been an attractive solution for large-scale detector systems and future collider upgrades. This contribution presents the development status and future plans of serial powering R&D at the Institute of High Energy Physics (IHEP), with applications to the LHCb Upstream Tracker and future Higgs-factory experiments such as CEPC.

Serial Powering Concept



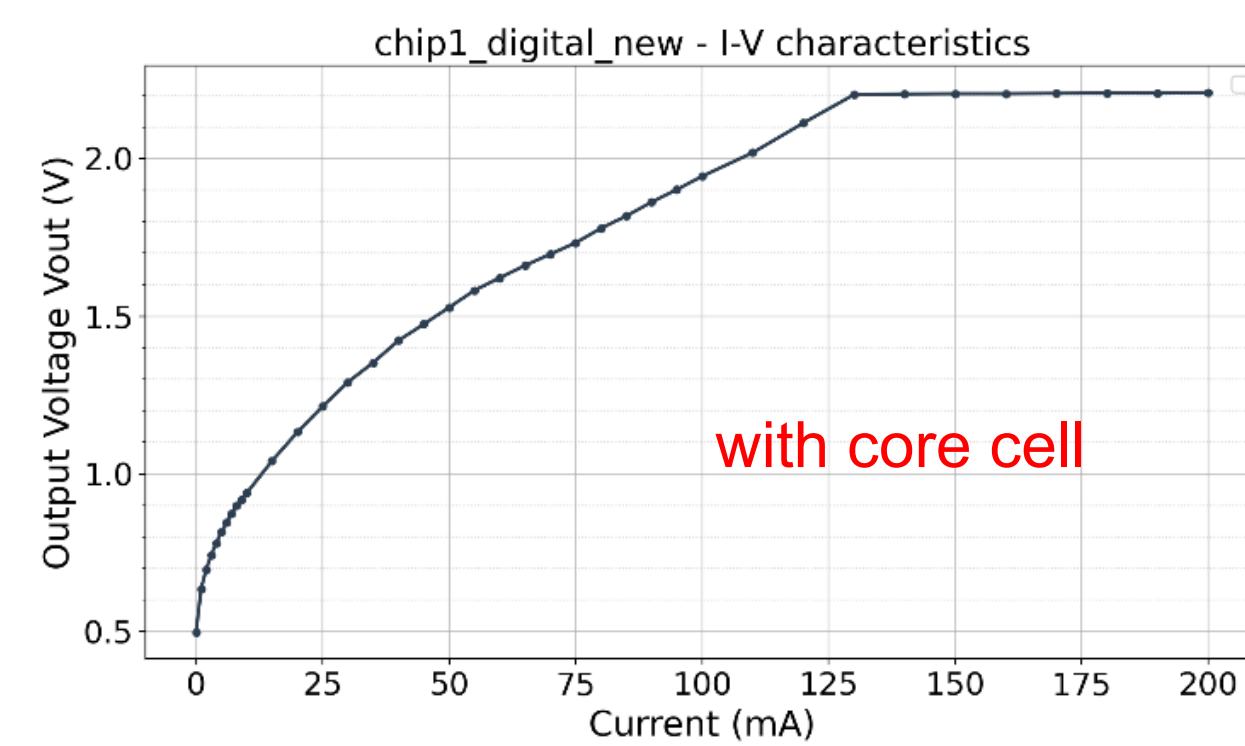
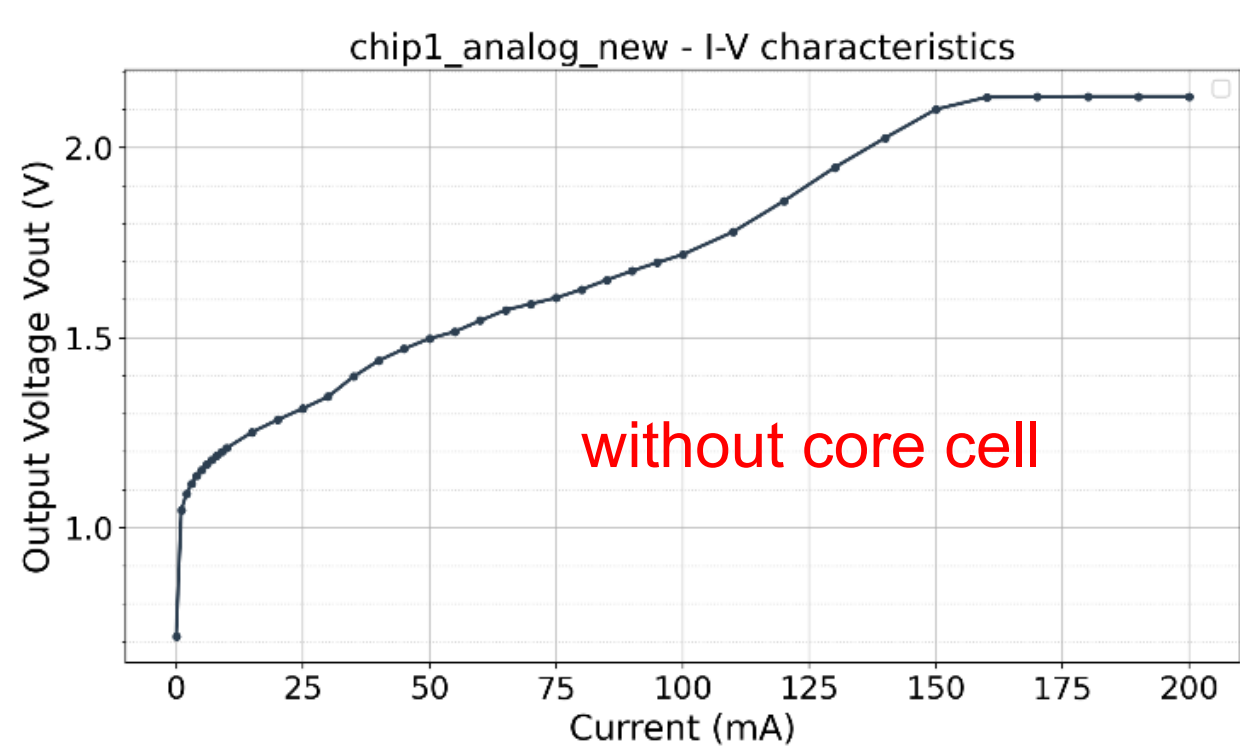
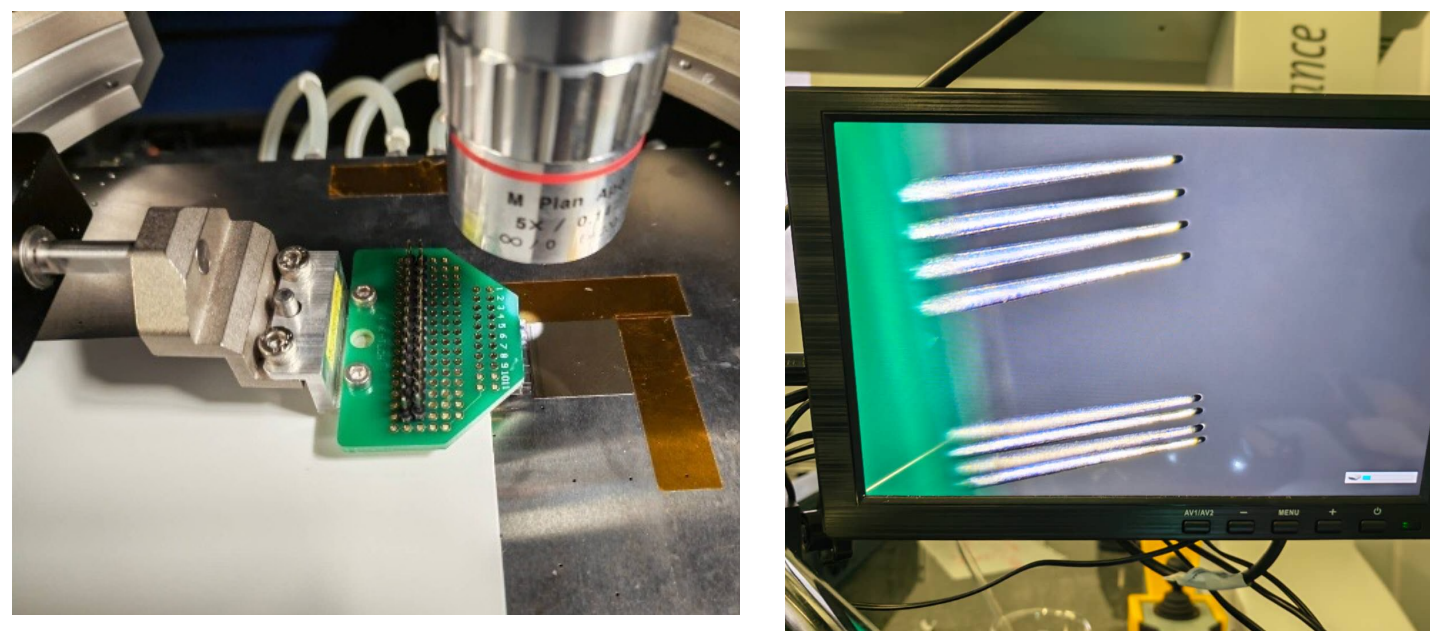
Serial powering diagram

ATLASPix3-based SLDO Tests

The SLDO performance of ATLASPix3 chips has been systematically investigated using dedicated probe card and Single-Chip Carrier (SCC) setups. Both **bare chip** and chip with **core cell** configurations have been characterized. Four ATLASPix3 chips assembled on SCCs have been operated in series, demonstrating stable voltage regulation and functional outputs. Besides, A 1×4 PCB based on a quad-flex layout has also been designed and produced for module-level serial-powering studies, with wire bonding and functional testing in progress.

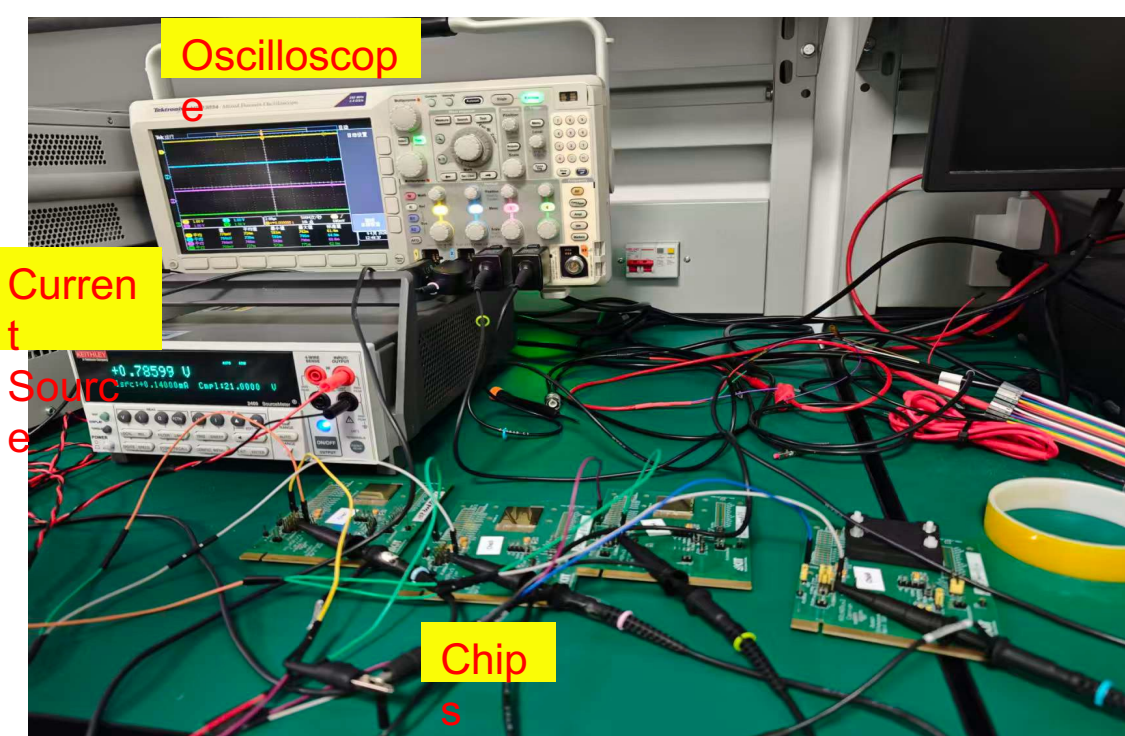
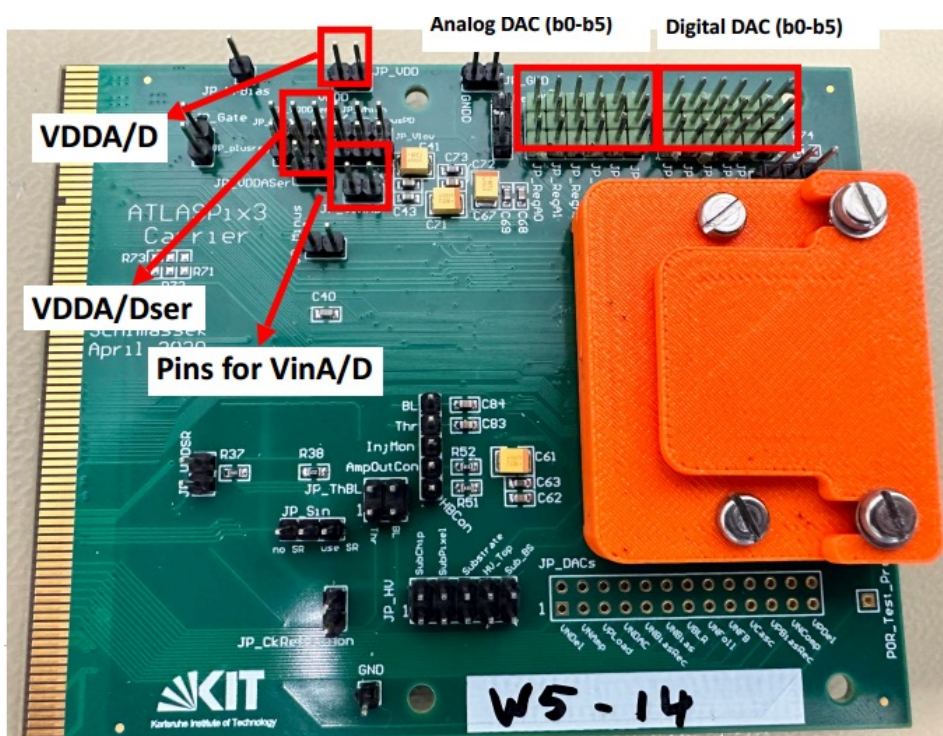
Prob card test

- Testing bare chips with the probe card.
- Analog and digital output are both tested.
- Six chips are tested and show excellent I-V characterization.



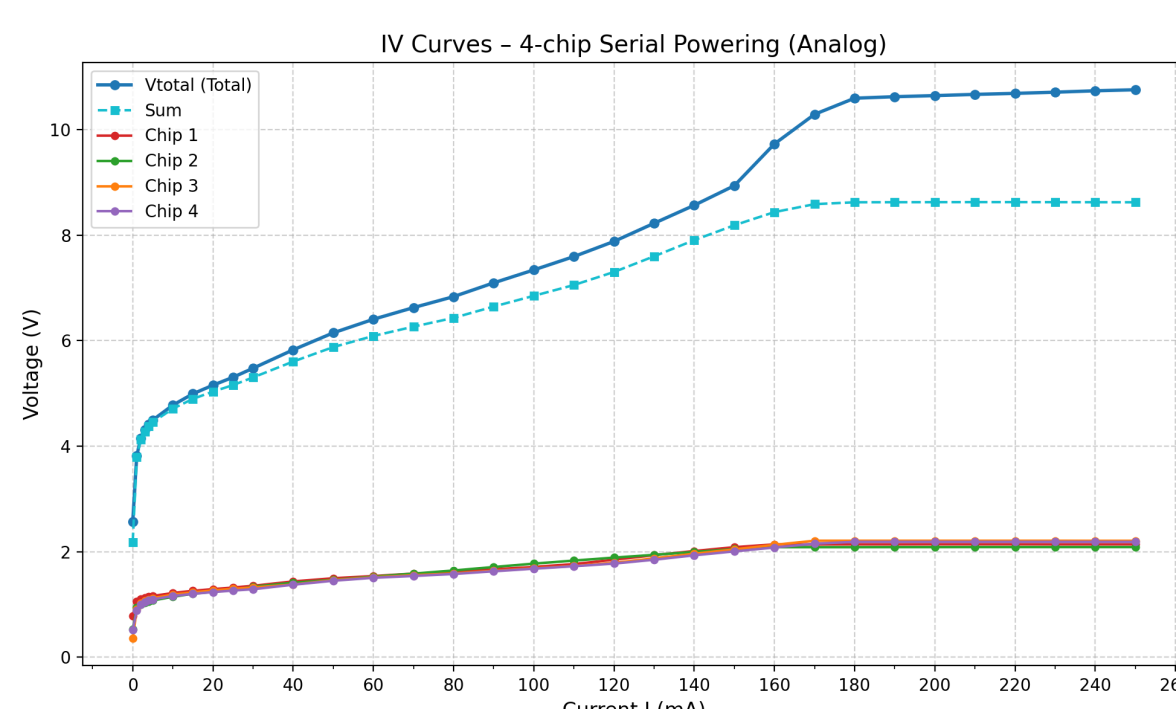
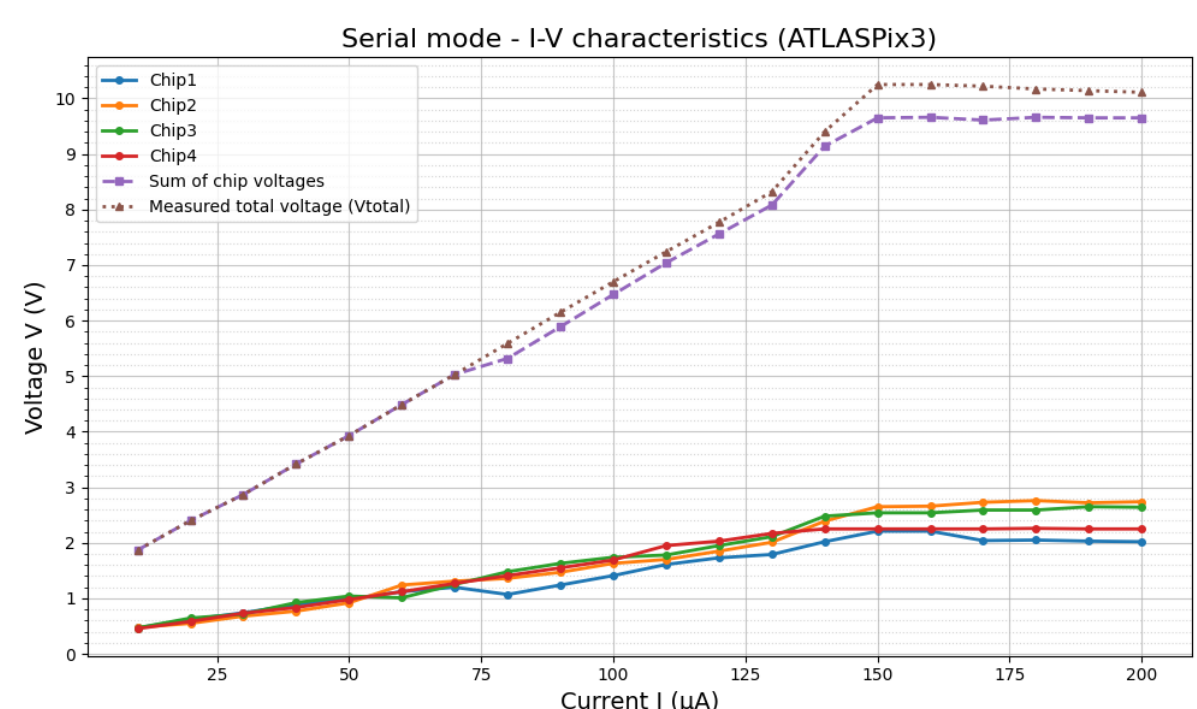
I-V Curve for a random chip

Single-Chip (multi) Carrier(s) test



Photos of test setup

- Stable regulation is achieved in both cases
 - ✓ ~150 mA input current yields 2.2–2.8 V (without core cell)
 - ✓ ~160 mA input current yields 2.0 V (with core cell)
- Both scenarios demonstrate good regulation and fully meet our expectations

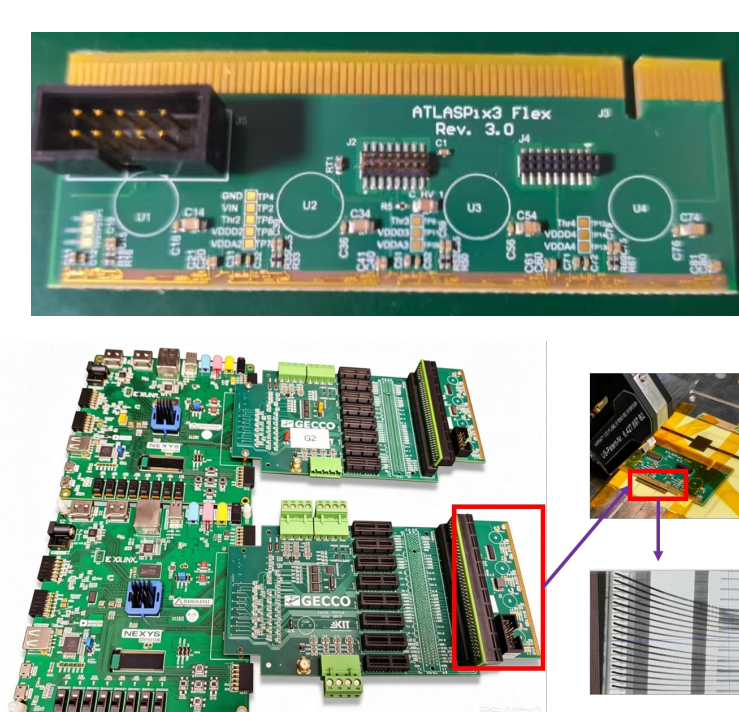


I-V Curve for 4 serial modules

1 x 4 PCB design and production

- A new layout 1×4 test board has been designed and produced suitable for LHCb experiment geometry based on Quad flex.
- ATLASPix Chip will wire bonded on 1 x 4 PCB and test the serial powering functionality

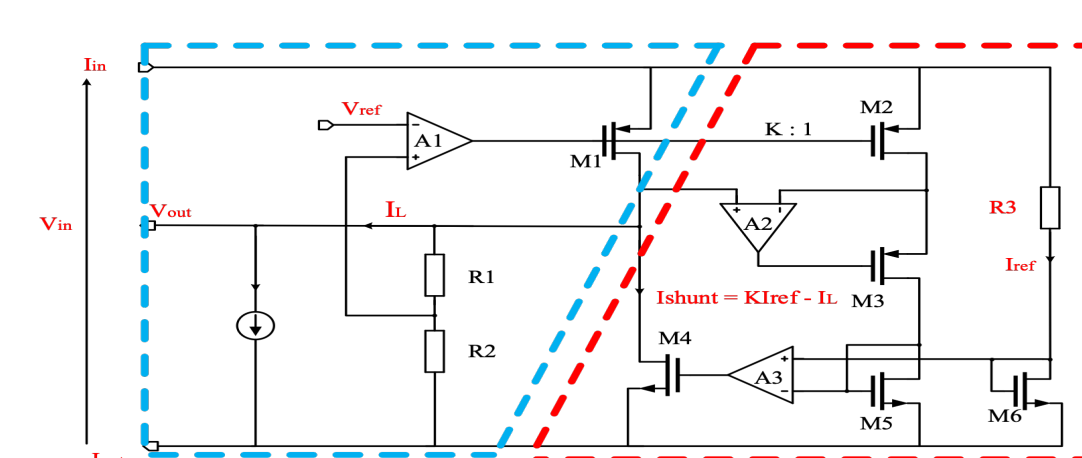
Photo of test board



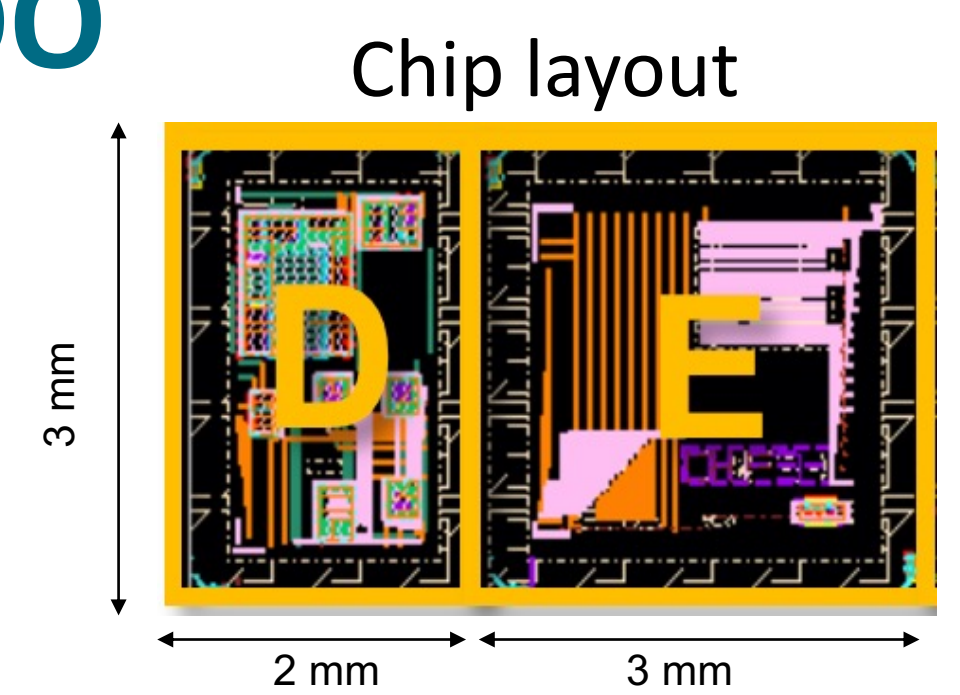
COFFEE/CHiR Chips with SLDO design

To develop CMOS pixel sensors in a 55-nm HVCMOS processing with serial powering module, two different SLDO architectures have been implemented in the CHiR chip, including an approach following the ATLASPix3 design and another based on the RD53 architecture. Device sizes and types have been optimized for the shunt and pass devices, while an overvoltage tolerant design extends the applicable input voltage range beyond the nominal 1.2~V technology limit to approximately 2~V. Simulations have demonstrated stable regulation for both a single SLDO and a four-chip serial chain. A dedicated CHiR test PCB has been designed, with measurements planned to characterize SLDO output regulation, serial-chain operation, and load-transient response.

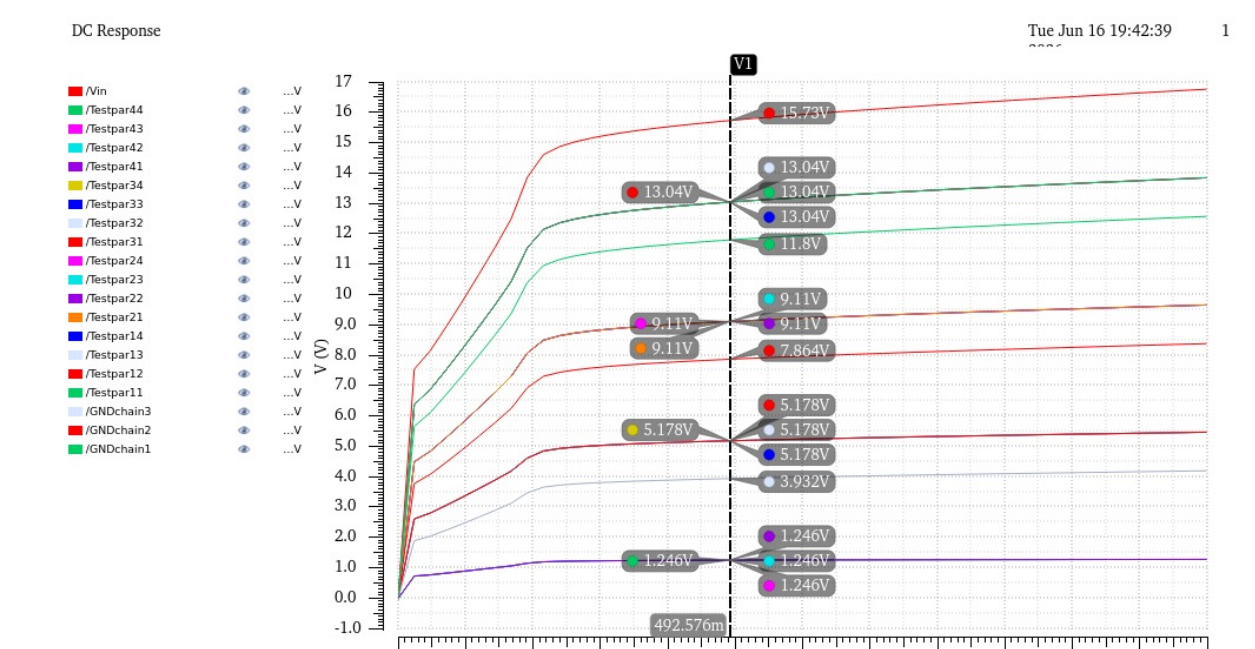
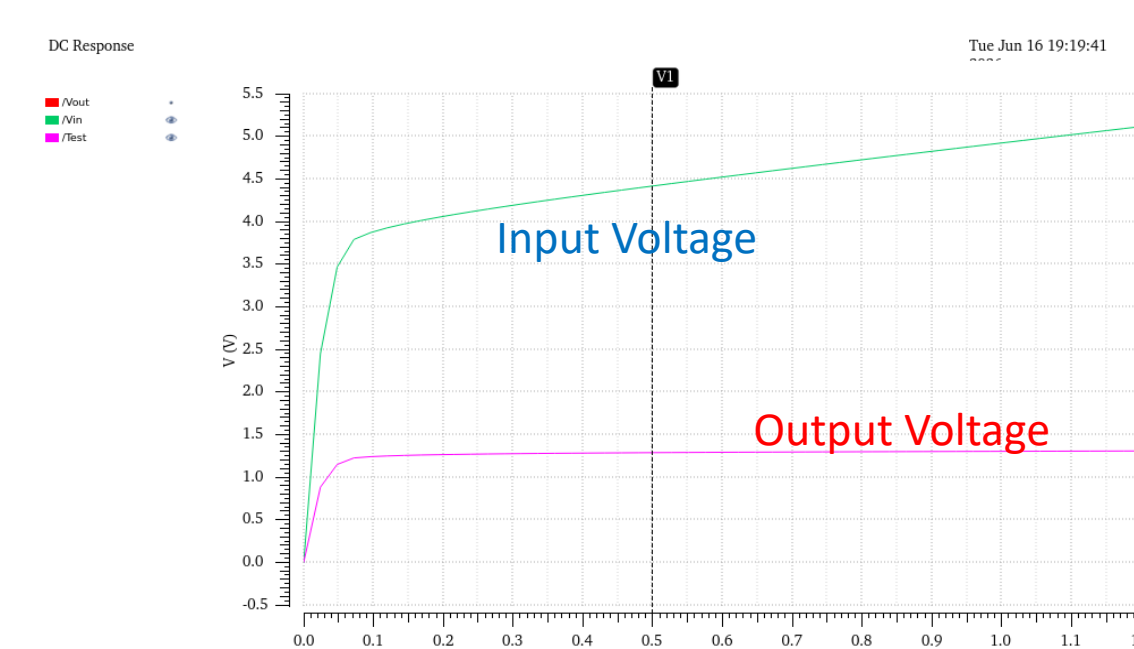
Sensor development with SLDO



SLDO structure diagram

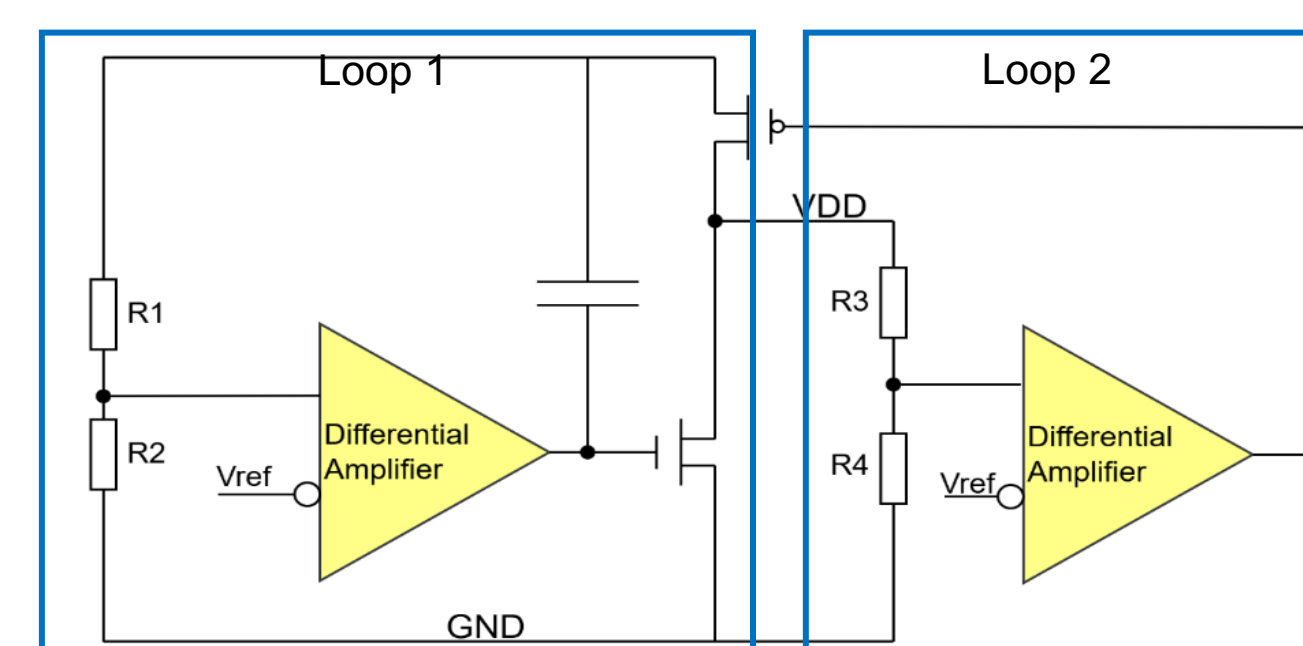


- Two different designs of SLDO implemented in CHiR with 55 nm HVCMOS process (latest COFFEE submission with modified process)



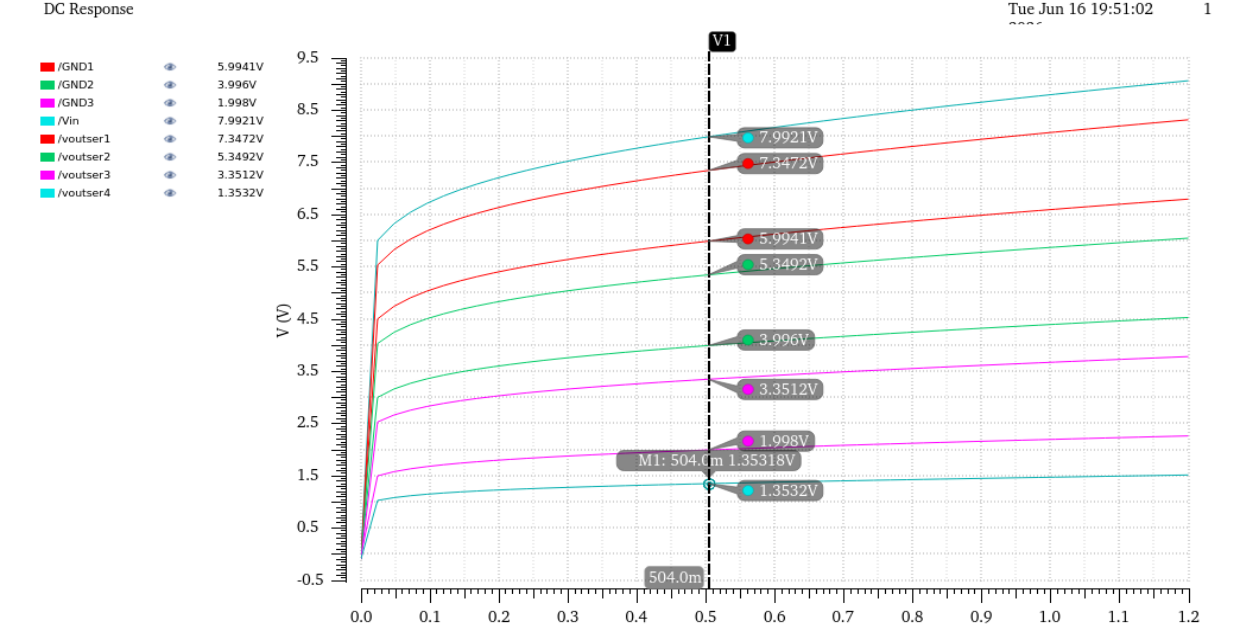
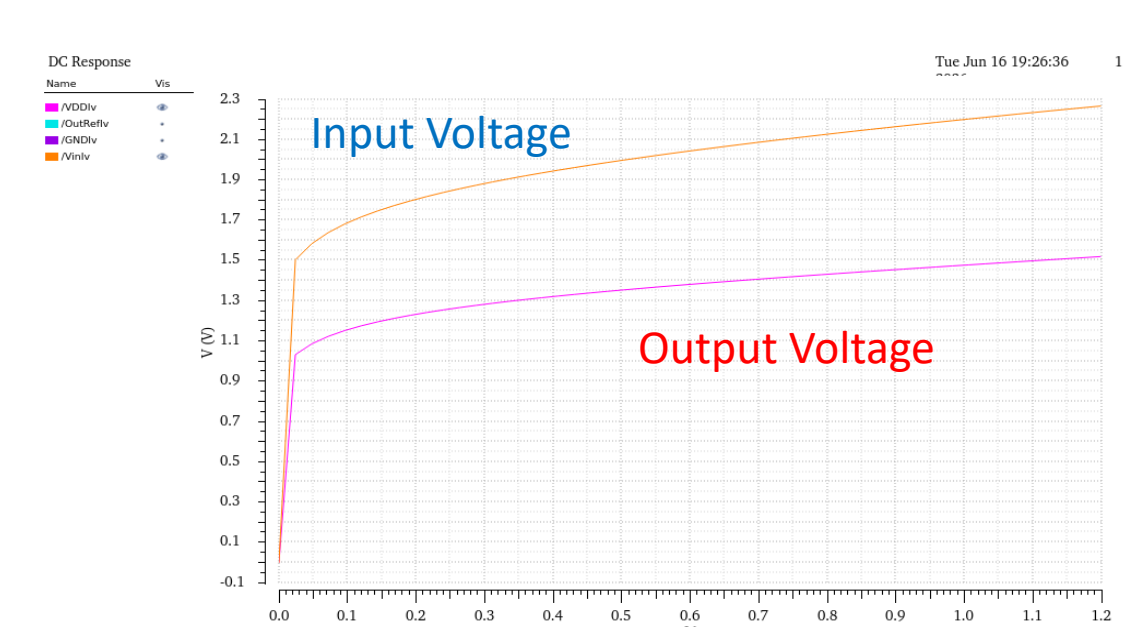
Simulations of both single and four-chip serial configurations.

- Device types and dimensions optimised for both shunt and pass-device.
- Technology limitation: max input voltage = 1.2 V .
- Overvoltage-tolerant design extends capability to 2 V (55 nm process).
- Simulations validated for single SLDO and 4-chip serial chain.



The SLDO block provides separate regulation for VDDA and VDDD.

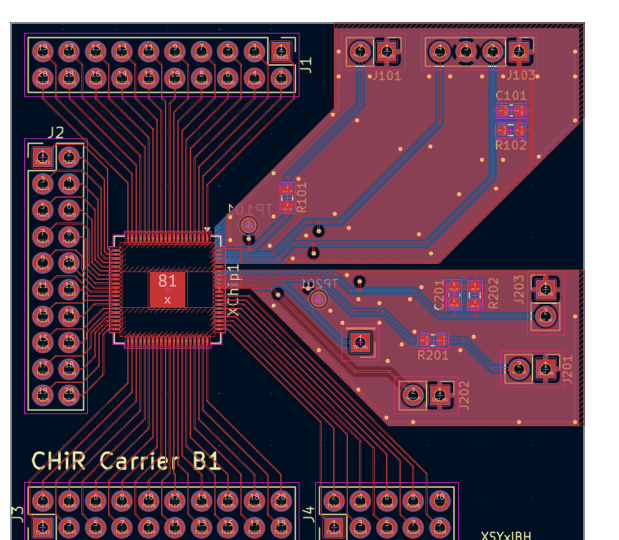
- Separat regulation modules for VDDA and VDDD.
- Enables constant-current operation mode
 - ✓ Loop 1: defines shunt regulation
 - ✓ Loop 2: regulates both VDDA and VDDD outputs
- Simulations performed for single SLDO and 4 chips serial chain



Simulations of both single and four-chip serial configurations.

PCB design and production for CHiR

- A test PCB for CHiR is designed and currently being production
- Full functional test plan prepared: SLDO output characterization, serial-chain regulation, and load transient response will be measured



Ongoing efforts & plans

The ongoing development aims to demonstrate serial powering at module level and establish a practical powering solution for future low-material-budget tracking detectors, while supporting long-term collaboration with the ATLASPix community and the development of serial powering technologies.

- ATLASPix3-based modules
 - ✓ wire-bonding of chips on the 1×4 PCB
 - ✓ full serial-powering functional tests
- CHiR-based tests:
 - ✓ Hardware, firmware and software: ongoing preparation for the module DAQ