# Modeling and Simulation of Pixel Readout Logic for AGORA Vertex Detector

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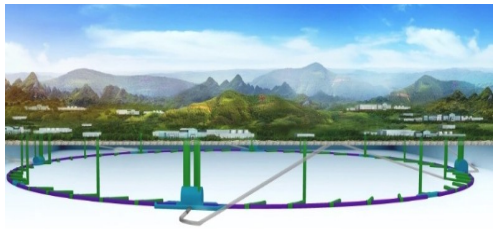
# Outline

- Introduction
  - CEPC & AGORA Detector
- Behavioral Modeling of the PRECIS Pixel Array
  - Column Drain Readout Logic
  - Driver and Load Modeling for Long Interconnects
  - Delay-Parameter Extraction for Logic Gates and Interconnects
  - Timing Design of the Asynchronous Double-Column Readout Logic
- Limitations and Further Optimization
- Summary

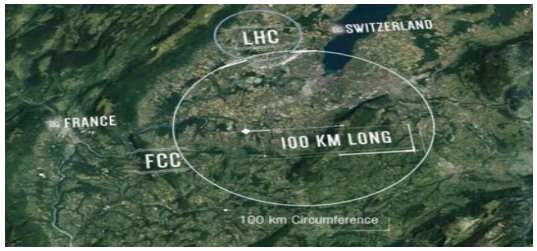


# AGORA: Advanced Glass Optimized Research Apparatus

## CEPC/FCC-ee



CEPC (Circular Electron-Positron Collider)



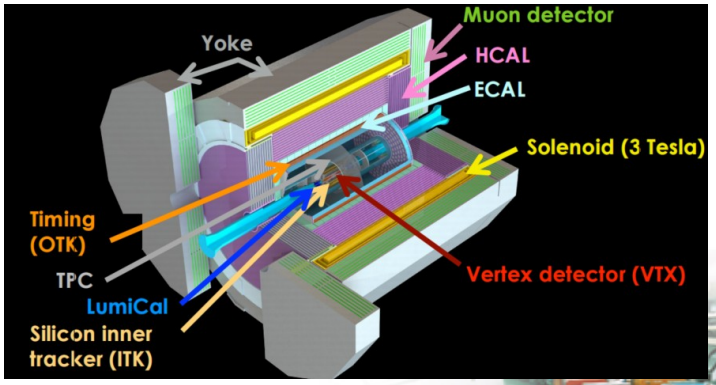

FCC (Future Circular Collider)

## AGORA Detector

| Collision environment challenges | Requirement |
|---|---|
| High luminosity | Readout between 50 MHz (no trigger) and $\gtrsim$ 100 kHz (trigger) |
| Avoid pile-up of Z bosons | Integration time $\lesssim 1\ \mu s$ |
| Beam backgrounds | Hit rate capability up to $\mathcal{O}(200\ \text{MHz cm}^{-2})$ |
| Radiation environment | Few $10^{13}$ 1 MeV$n_{eq}$ cm$^{-2}$ and $\mathcal{O}(100\ \text{kGy})$ per year |

| Baseline Operating Scenario | | | |
|---|---|---|---|
| **Operating Mode** | **Center-of-Mass Energy** | **Instantaneous Luminosity** | **Main Target** |
| **Higgs** | **240 GeV** | **5*10³⁴ cm⁻²s⁻¹** | **Approximately 2.0 × 10⁶ Higgs Bosons** |
| **WW** | **约160 GeV** | **16*10³⁴ cm⁻²s⁻¹** | **Approximately 1.0 × 10⁷ WW Events** |
| **Z** | **91 GeV** | **26*10³⁴ cm⁻²s⁻¹** | **Approximately 5.6 × 10¹¹ Z Bosons** |
| **Under the 50 MW upgrade scenario, the Z-pole luminosity can be increased to approximately 192 × 10³⁴ cm⁻² s⁻¹, which is significantly higher than that of the baseline Z operation, resulting in different readout requirements for low- and high-luminosity Z operation.** | | | |

**Hit Rate up to 200 MHz/cm² under High-Luminosity Z Operation**



# Vertex Specification

- CEPC Reference Detector(AGORA)
  - Spatial resolution < 5 um
  - Time stamp precision < 100 ns
  - Power Consumption < 40 mW/cm$^2$
  - Higgs & high-luminosity Z operation
  - Hit rate expected ~ 200 MHz/cm$^2$ (average)@ $r_{min}$=11 mm

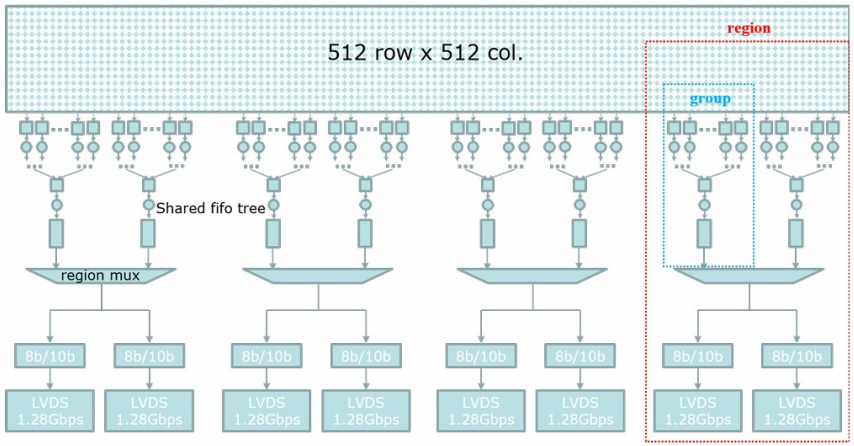
Development of the PRECIS Silicon Pixel Detector Chip

**Table 4.2:** Vertex Detector Design Parameters

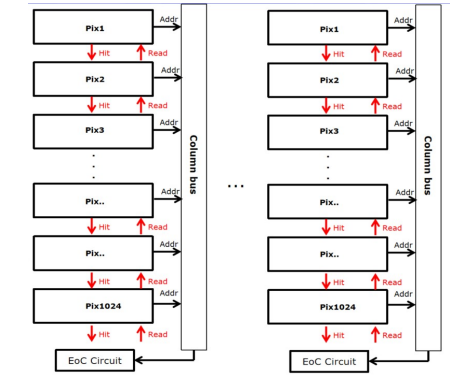
| Parameter | Design |
|---|---|
| Spatial Resolution | ~ 5 μm |
| Detector material budget | ~ 0.8% $X_0$ |
| First layer radius | 11.1 mm |
| Power Consumption | < 40 mW/cm$^2$ (air cooling requirement) |
| Time stamp precision | 100 ns |
| Fluence | ~ $2 \times 10^{14}$ Neq/cm$^2$ |
| Operation temperature | ~ 5 °C to 30 °C |
| Readout electronics | Fast, low-noise, low-power |
| Mechanical Support | Ultralight structures |
| Angular Coverage | $\lvert\cos\theta\rvert < 0.99$ |



# The scheme architecture of PRECIS



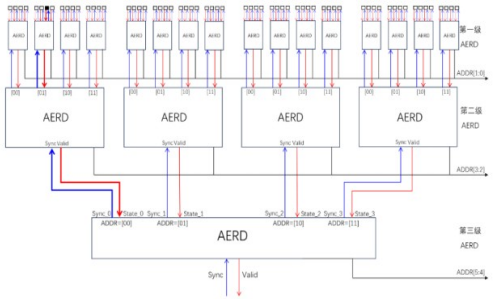

- Architecture Components
  - Analog Front End
  - Pixel-Array Readout Logic
    - **Column Drain VS AERD**
  - Column-Level Readout and Peripheral Data-Readout Path
    - 4 Region
    - Fifo tree in each group
    - 8 channels 8b/10b + LVDS




**Column drain**

**Advantages**
Simple Circuit Structure
Low Routing-Resource Requirement

**Disadvantages**
Its propagation delay increases linearly with the size of the pixel array




**AERD**

**Advantages**
Relatively Uniform Propagation Delay
Shorter Propagation Delay

**Disadvantages**
The structure is relatively complex and requires **more routing resources**

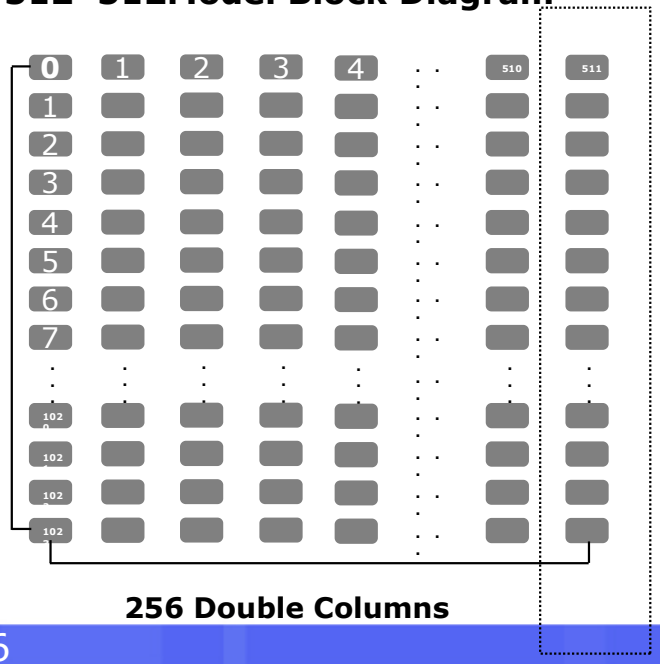
- **Column drain architechture is chosen** due to a strong constraint of only **five metal layers** in the foundry process
- However, it increases the difficulty in optimizing the propagation delay



# Signal Chain in Double Column

- We Need To
  - Predict, understand, and simulate the pixel array
  - Optimize and verify the column-level delay
  - The digital readout path requires a behavioral pixel-array model for joint simulation and debugging
- **Double column Pixel array delay model**
  - **Parameterized Behavioral Delay Model:**

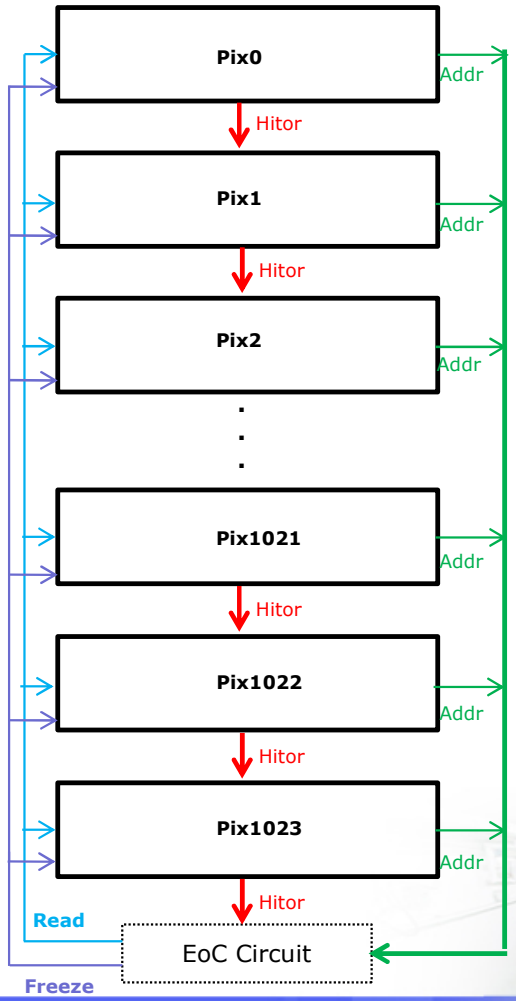
**512*512Model Block Diagram**




**256 Double Columns**

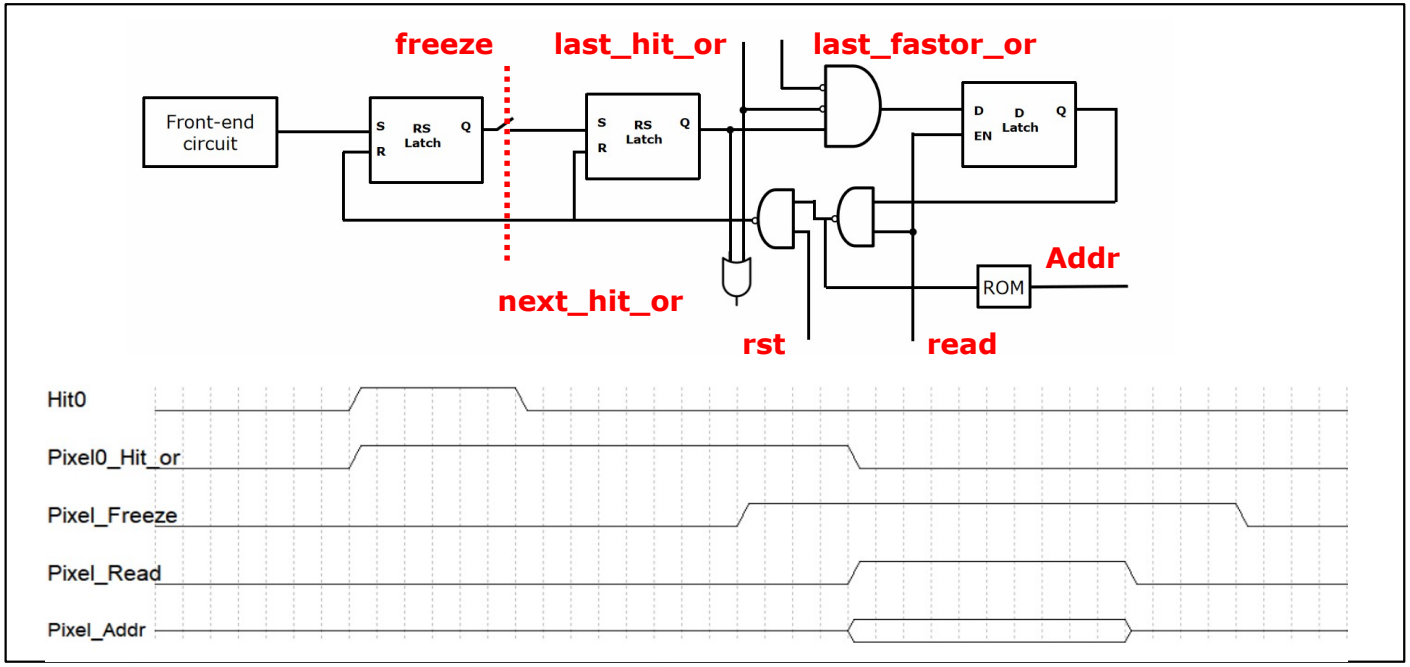
**1,024 Pixel Cells**

**Double-Column Pixel Model**

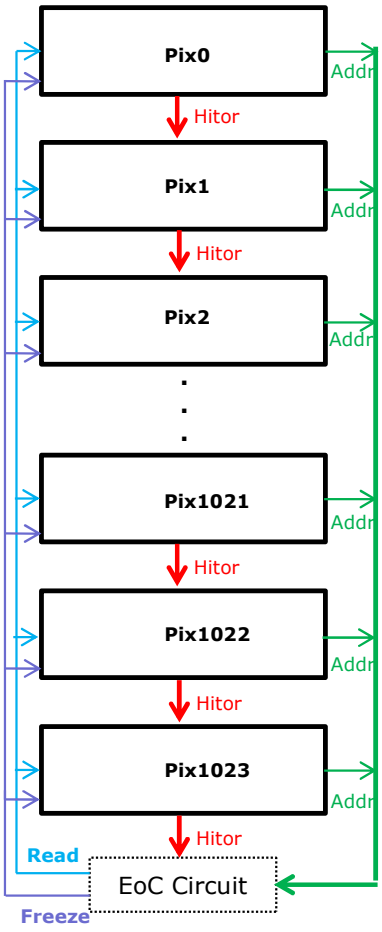


# Pixel Logic and Readout Sequence

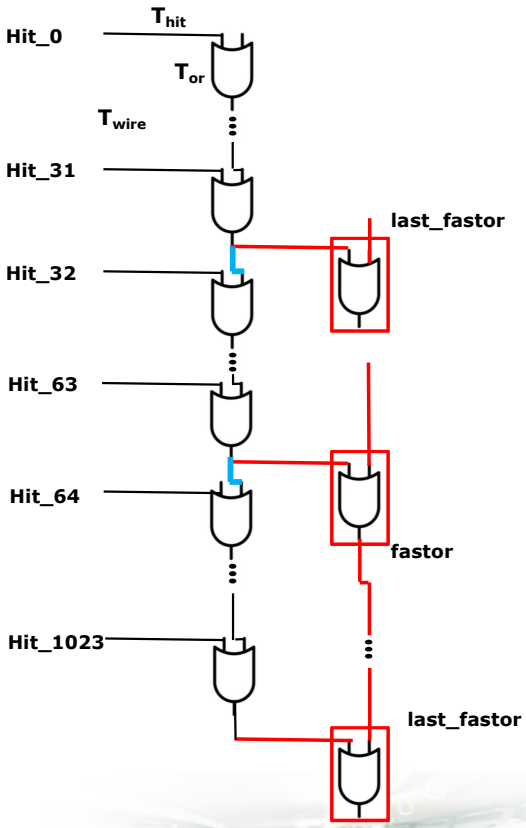
- Components of the Delay of a Single Readout
  - In-Pixel Logic Delay
  - Column-Arbitration Waiting Time (Column-Level Propagation Delay)
  - Propagation Delay of the Read and Freeze Control Signals
  - Address Propagation Time



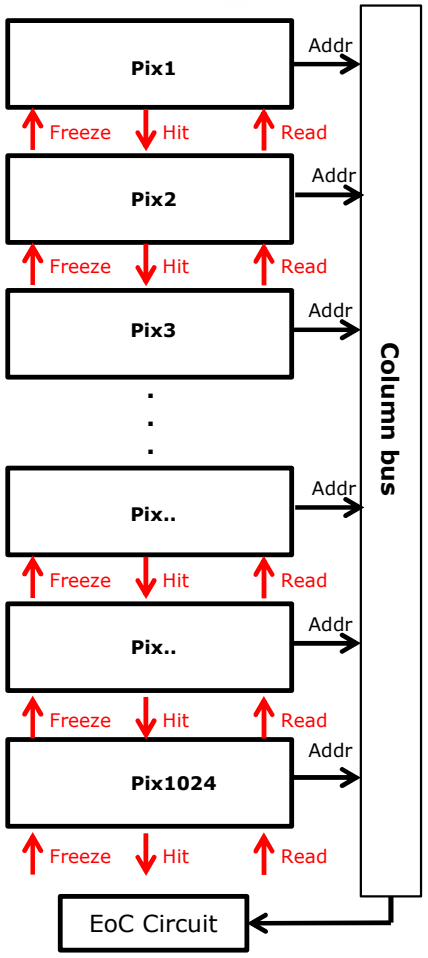
# Critical path delay analysis




- Critical Paths
  - **Hitor**
  - **Read & Freeze**
  - **Addr**
- **Hitor**
  - **0-to-1 Transition**
    - **Create a grouped FastOR chain to accelerate the downward propagation of the hit**
  - **1-to-0 Transition**
    - **Disconnect the intergroup hit-signal chain so that the 1-to-0 transition is also propagated through the FastOR chain.**
- **Hitor & Read & Freeze & Addr**
  - **Buffer Segmentation**
  - **Optimization of Driver Resistance**

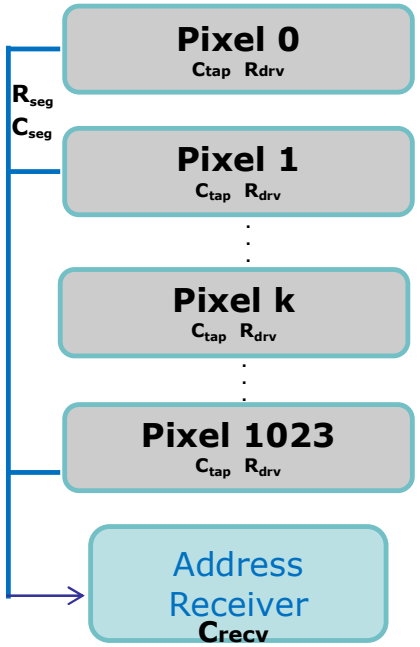


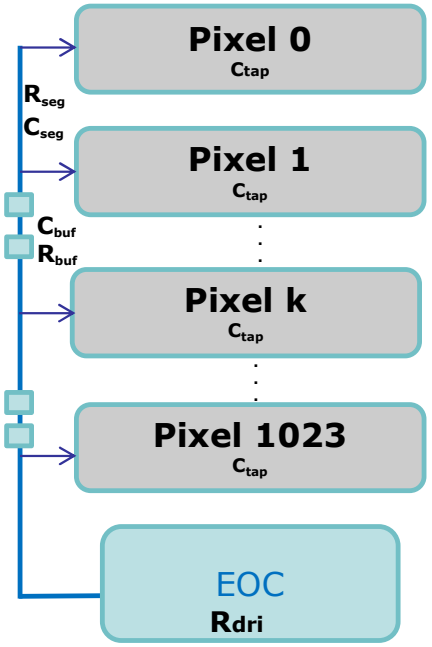
# Double-column pixel delay model

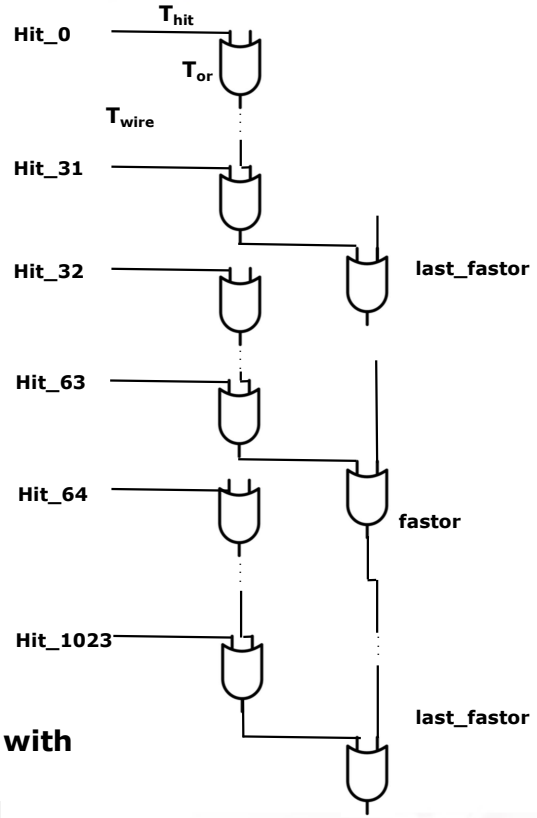



**Column drain R/O**

**Delay Block Diagram**




**The delay is estimated using the Elmore approximation with the specified resistance R and capacitance C**

**For Pixel k**
$T=t_{drv}+t_{wire}$

**For Pixel k**
$T=t_{drv}+t_{drv\text{-}buf}+t_{buf\text{-}recv}$
$t_{drv}$ : Intrinsic Delay of the Driver
$t_{drv\text{-}buf}$ : Delay from the Driver to the Nearest Buffer in the Target Direction
$t_{buf\text{-}tap}$ : Delay from the Buffer to a Pixel Cell

**For Pixel k**
$T=t_{drv}+t_{slow}+t_{fast}$
$t_{drv}$ : Intrinsic Delay of the Driver
$t_{slow}$ : Slow-Chain Propagation Delay
$t_{fast}$ : Fast-Chain Propagation Delay

# Delay of a distributed RC network

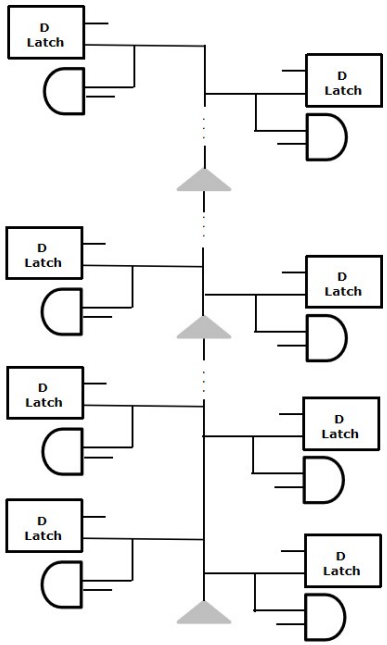
- What is Elmore delay?

$$t_{pd} = \sum_i R_{is} C_i$$

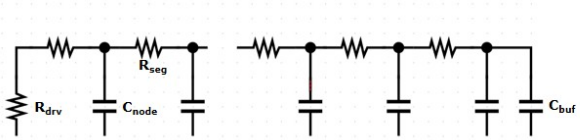
$R_{is}$= *sum of resistance from source to node i*

- How to **apply Elmore** in the delay model?
- Take the "**Freeze**" signal as an example

**Freeze**




**For pixel k**
**d = 1023 - k**
**stage = floor(d/32)**
**offset = d mod 32**
**$C_{base} = 32*C_{TAP} + 31*C_{SEG}$**
**$C_{node} = C_{SEG} + C_{TAP}$**
**$T=t_{drv_input}+t_{drv\text{-}buf}+n*t_{buf\text{-}buf}+t_{buf\text{-}tap}$**




$t_{drv\text{-}buf}(k)$
$= R_{DRV}*(C_{base} + C_{BUF})$
$+ R_{SEG}*[C_{node}*32*31/2 + 32*C_{BUF}]$

$t_{buf\text{-}buf}(k)$
$= R_{BUF}*(C_{base} + C_{BUF})$
$+ R_{SEG}*[C_{node}*32*31/2 + 32*C_{BUF}]$

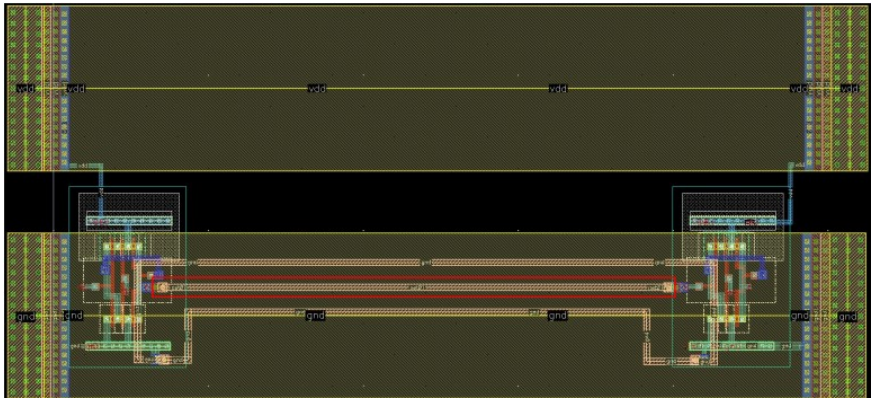
$t_{buf\text{-}tap}(k)$
$= R_{BUF}*(C_{base} + C_{BUF})$
$+ R_{SEG}*[C_{node}*(32*offset-offset*(offset+1)/2) + offset*C_{BUF}]$

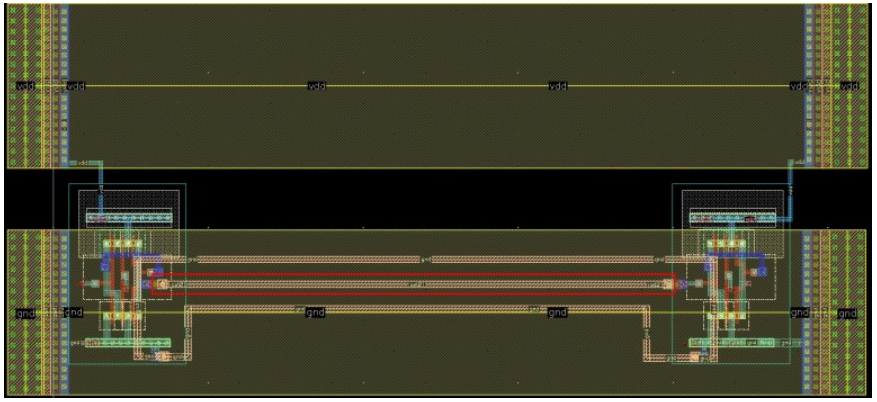
**How** to obtain RC parameters

**RC extraction**

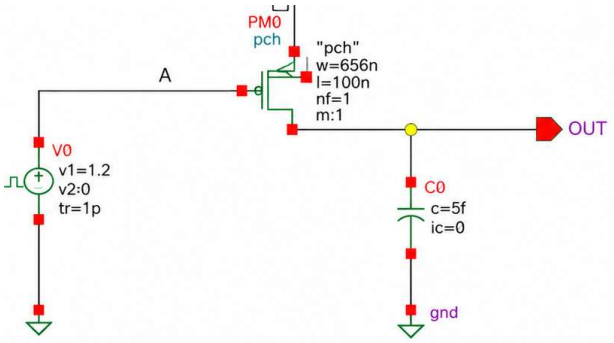


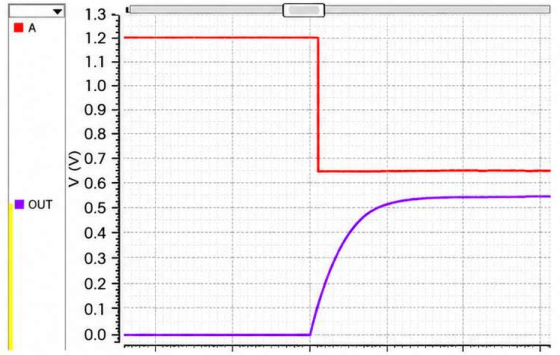
# RC extraction



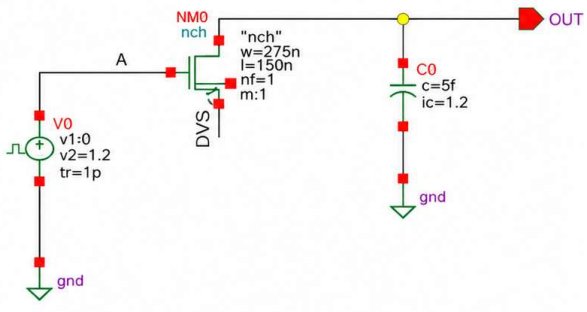


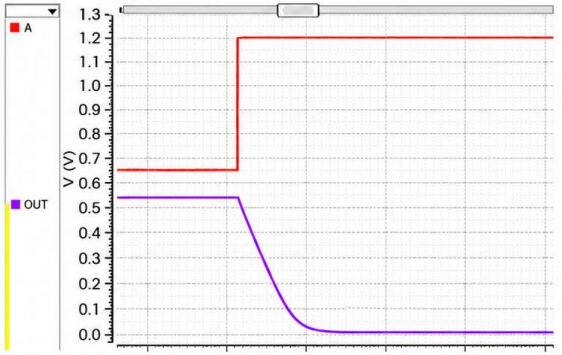
Metal-Interconnect RC Extraction




**PMOS Drive-Resistance Extraction**



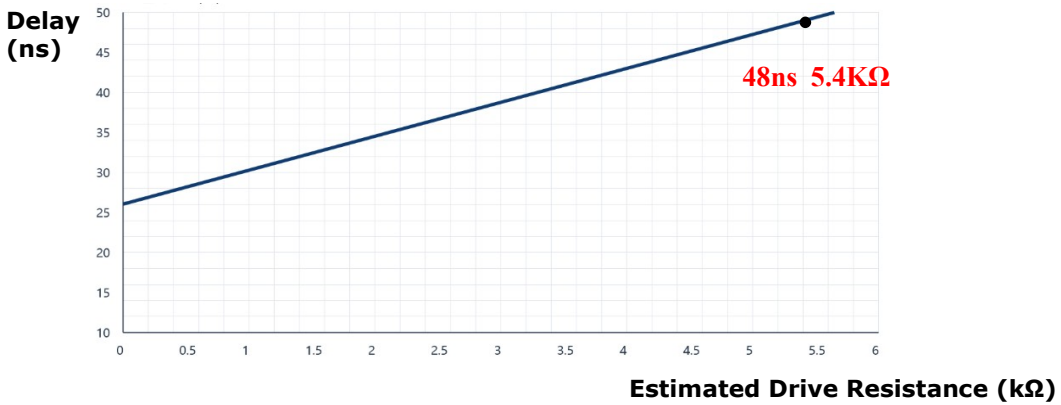




**NMOS Drive-Resistance Extraction**

# Buffer Analysis

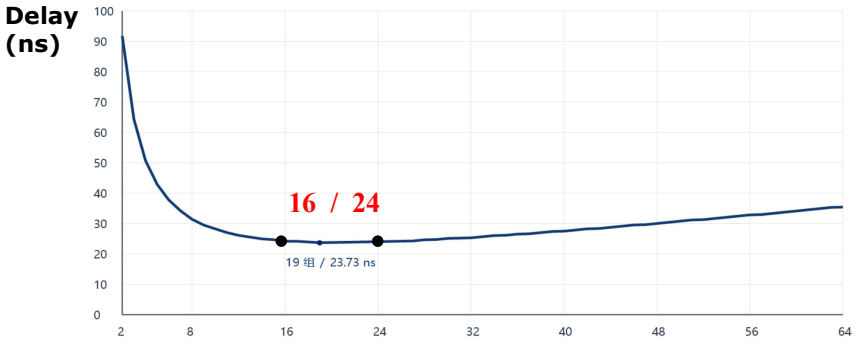
## ADDR & Fast_or

**Addr**

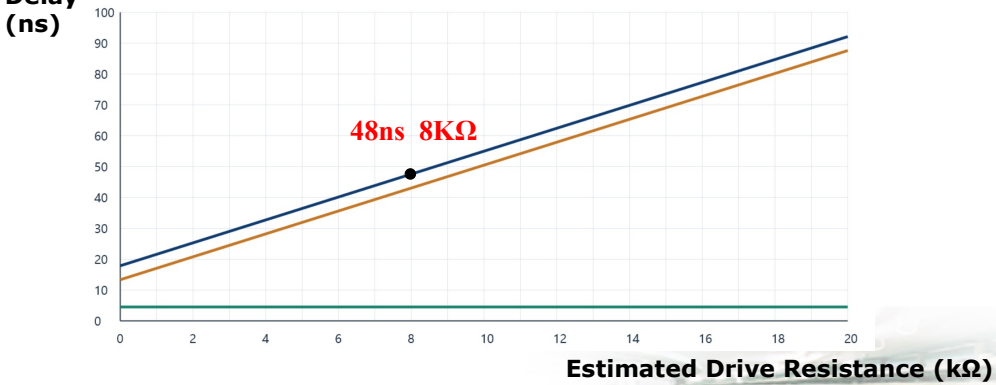



**Relationship between Address Delay and Estimated Drive Resistance**

**Fastor**




**Relationship between FastOR Delay and Estimated Drive Resistance**



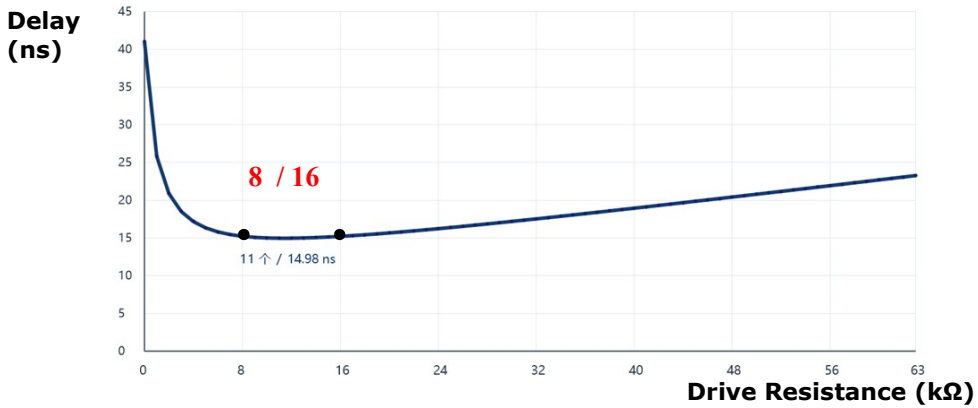

**Relationship between FastOR Delay and the Number of Buffers**

- Address: The signal is driven from the pixel toward the periphery, and buffers cannot be inserted
- Comprehensive Consideration of ROM Area and Timing Margin

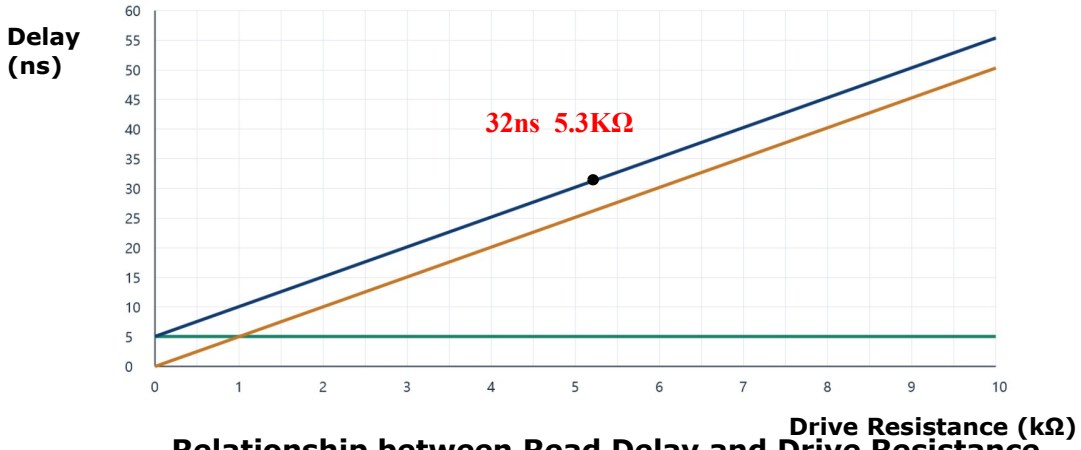
# Buffer Analysis

## Read &Freeze

### Read

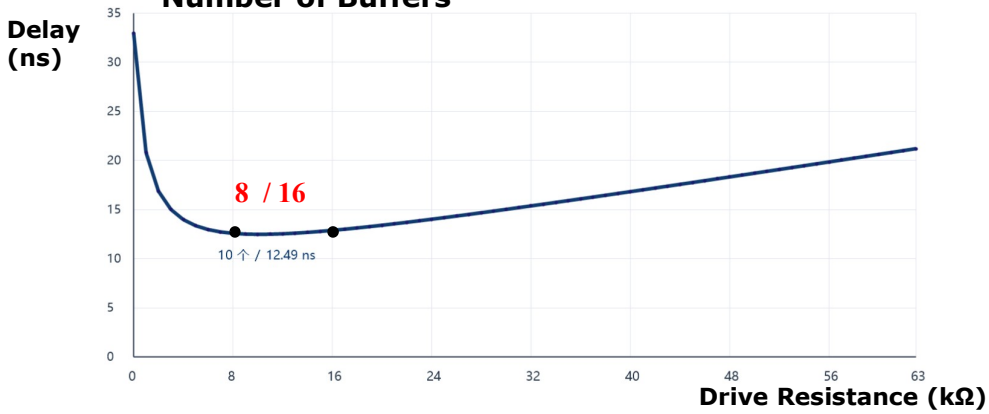



Relationship between Read Delay and the Number of Buffers

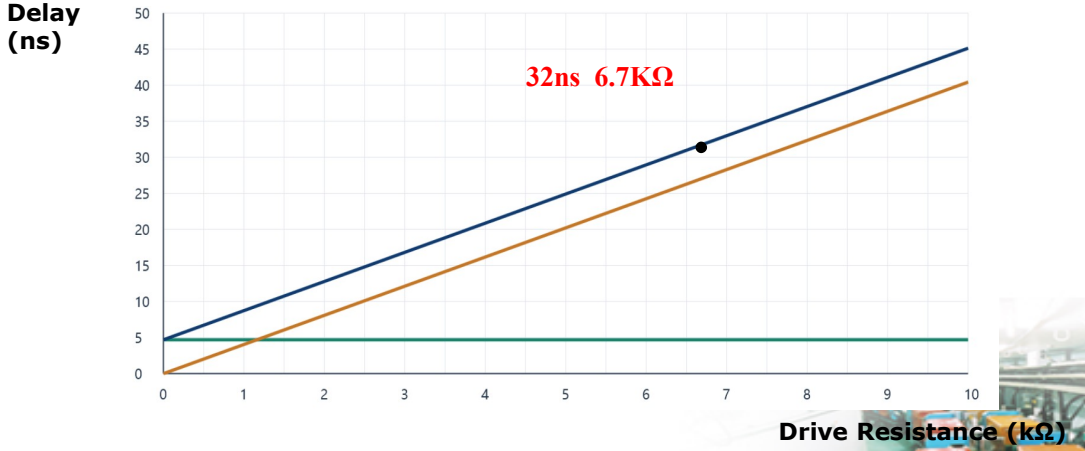



Relationship between Read Delay and Drive Resistance

### Freeze

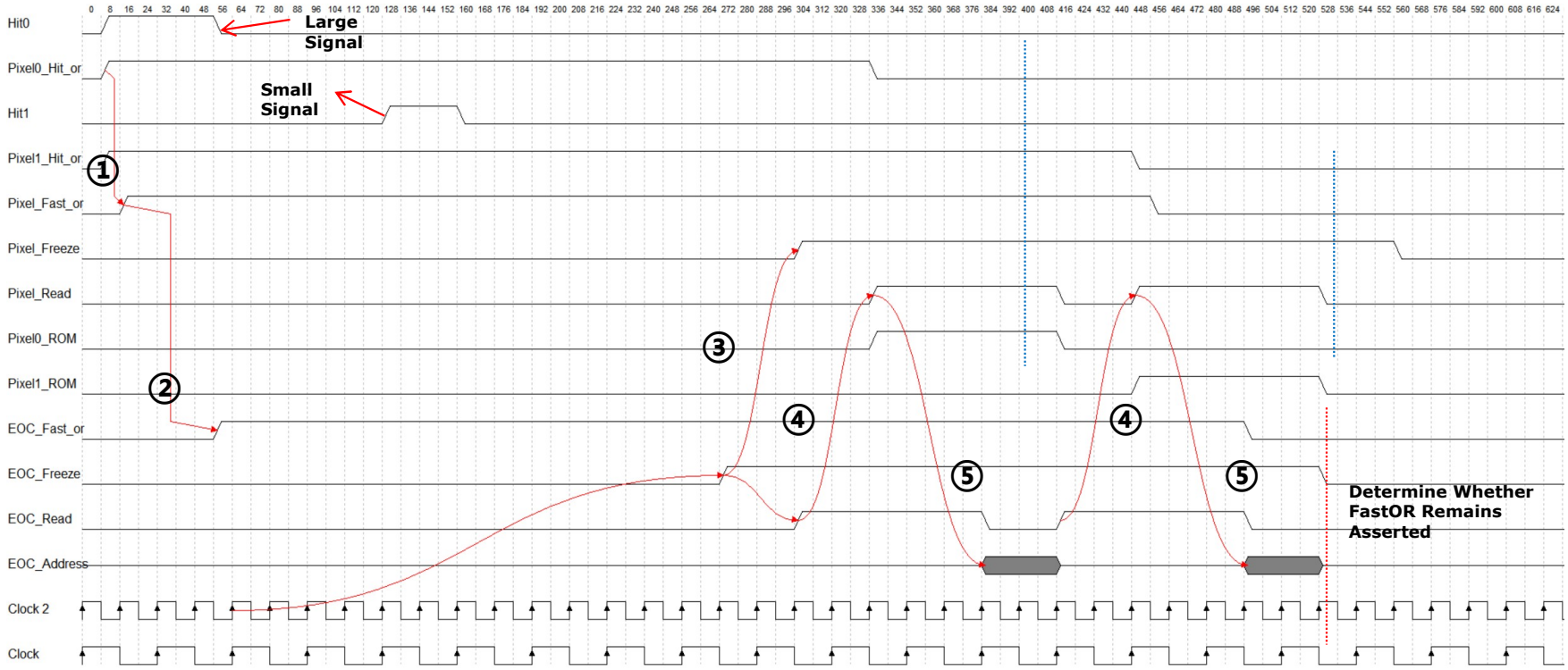



Relationship between Freeze Delay and the Number of Buffers




Relationship between Freeze Delay and Drive Resistance

# Timing Design of the Asynchronous Column-Drain Logic




①Hit_or

②Fast_or

③Freeze

④Read

⑤ADDR

- The timing design of the asynchronous logic has been completed, with one pixel address read out every 112 ns
- The readout time is much shorter than the average double-column hit rate of 0.94 hit/μs
- Almost no hit accumulation occurs in the double column, and the fastor delay is only 48 ns



# Limitations and Optimization

- Limitation
  - The pure resistance model cannot accurately represent the drive characteristics
- Possible Optimizations
  - Calibrate the Delay Model
    - Perform PEX and post-layout simulation using representative layouts
    - Adopt a delay model consisting of a current source and a resistor



# Summary

- Design of the PRECIS Pixel Chip for High-Hit-Rate Operation
  - Adoption of Column-Drain Readout Logic
  - Modeling of Critical Signals Using the Elmore Model
  - Obtaining Interconnect and Logic-Gate Delays through Parameter Extraction and Process Files
  - Completion of the Timing Design of the Asynchronous Double-Column Readout Logic
- Further Optimization of the Delay Model and Validation through Circuit Simulation
  - Adoption of a Two-Stage Model Consisting of a Current Source and a Resistor

Thank you for your time!

