R&D of Silicon Detector System For CEPC OTK

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Institute of High Energy Physics, CAS*

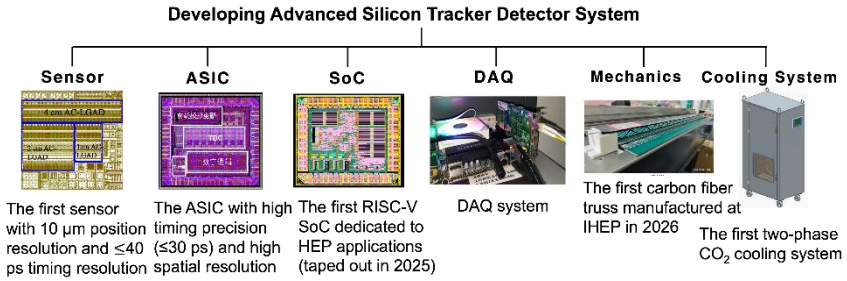
Institute of Physics and Chemistry, CAS

ShanDong University

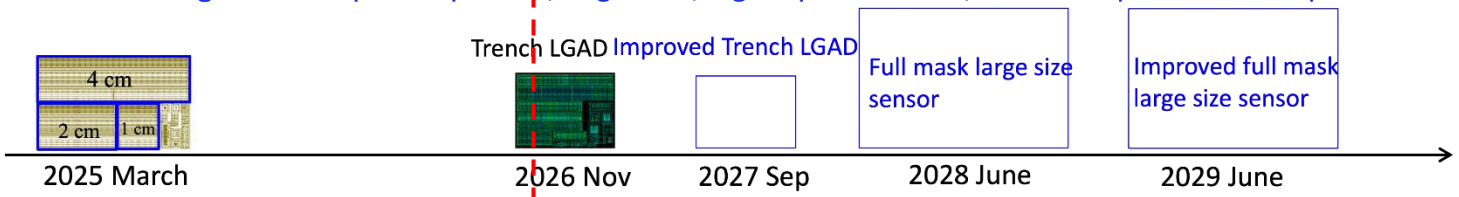
CEPC 2026, Shanghai, 22 Oct 2026

Outer Tracker System R&D Timeline

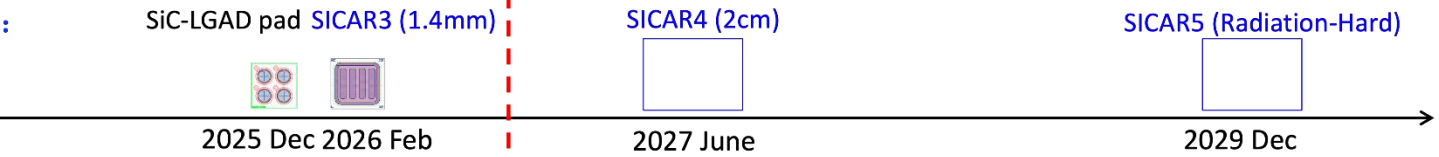
- We are developing semiconductor detector technologies that combine picosecond timing and micron-scale spatial resolution for **CEPC/AGORA OTK.**
- **Goal: build an end-to-end technology chain for high-performance semiconductor tracking detectors.**
- Our R&D program covers:
  - new sensors and dedicated readout electronics
  - DAQ and test platforms
  - mechanical, cooling and system integration



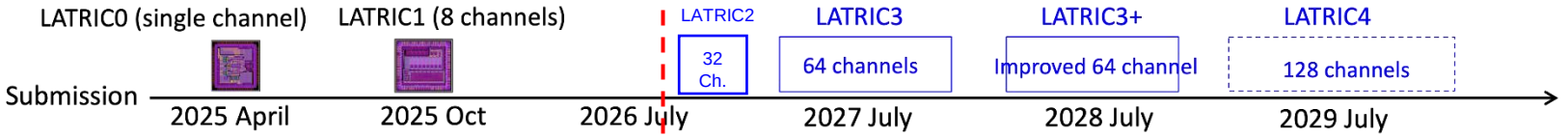
- LGAD sensors are evolving toward improved process, larger size, higher performance, and lower power consumption:



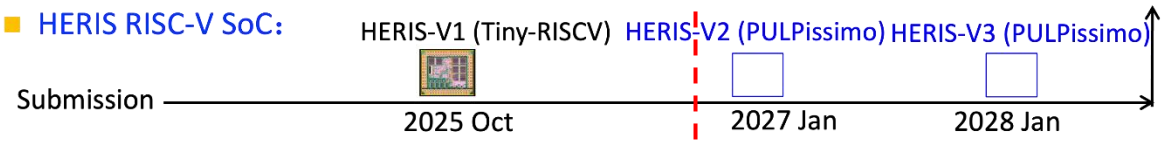
- SiC sensors:



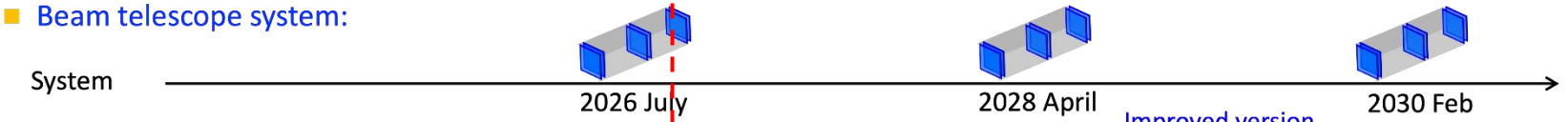
- LGAD readout ASIC, LATRIC, is being developed towards multi-channels:



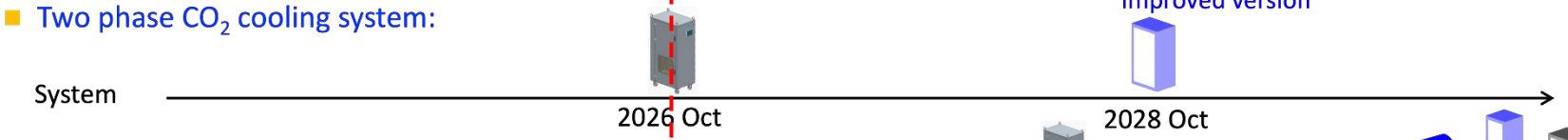
- HERIS RISC-V SoC:



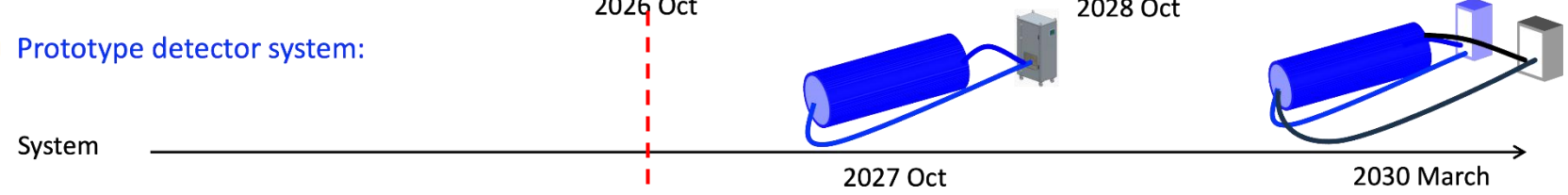
- Beam telescope system:



- Two phase CO_2 cooling system:

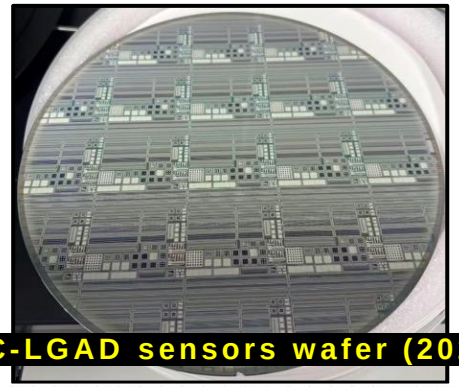


- Prototype detector system:

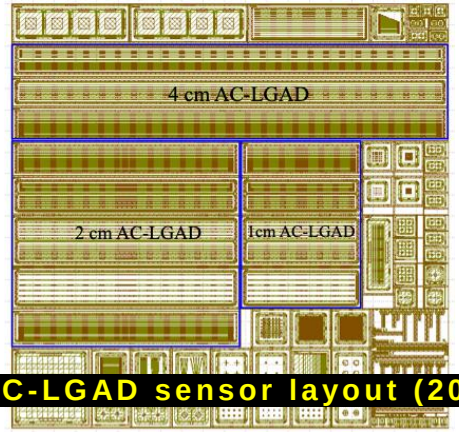


We are here

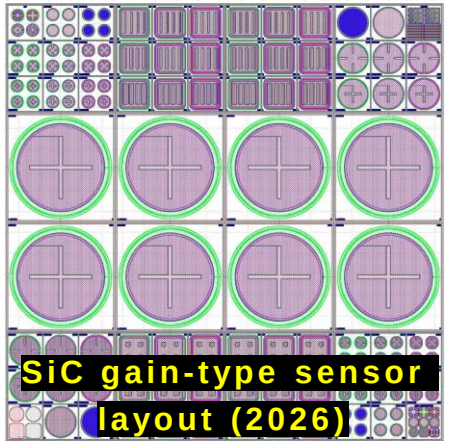
Sensors and Related Chips Development



AC-LGAD sensors wafer (2025)



AC-LGAD sensor layout (2025)



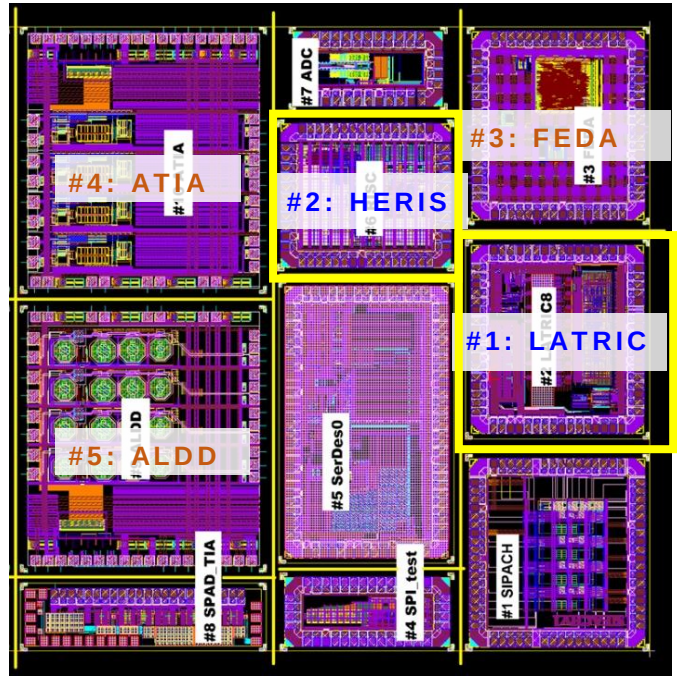
SiC gain-type sensor layout (2026)

Semiconductor detector sensors:

- **Silicon sensors**:
  - Aiming at large-area silicon sensor with time resolution ≤40ps and a spatial resolution ~10 μm→AC-LGAD
- **Silicon Carbide (SiC) sensors**:
  - Aiming at process-stable, engineering-ready 4H-SiC sensor with time resolution ~30ps; suitable for high-temperature and high-radiation environments.

Dedicated readout ASICs:

- **LATRIC series**: low power, highly integrated readout ASICs with excellent timing (≤30 ps) and spatial resolution (matched to 10 μm measurement precision).
- **HERIS series**: a radiation-tolerant RISC-V system-on-chip (SoC) for particle physics



Other dedicated high-speed data-transfer ICs:

- FEDA:10.24Gb/s data concentrator
- FEDI: data-interface chip
- ATIA: optical data receiver
- ALDD: laser-diode driver

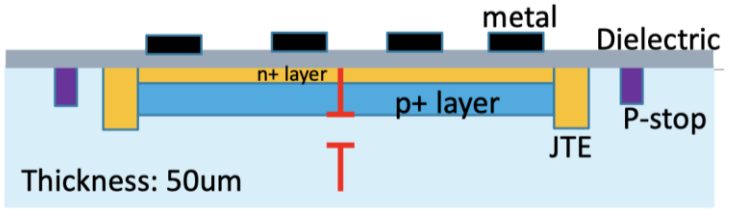
AC-LGAD Silicon Sensor R&D

◘ Target: large-area silicon sensor with ~10 μm spatial resolution and ≤40ps timing resolution.

⇨ The latest AC-LGAD design was submitted for fabrication in Apr 2025;

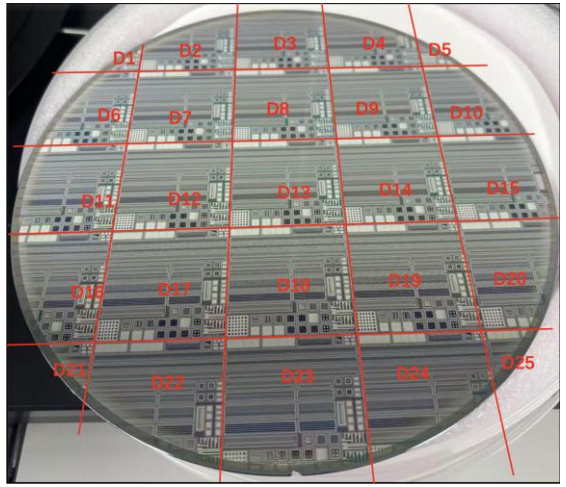
⇨ **7 out of 18 wafers** have completed processing and performance iteration.

- **Pixel sensors**:
  - pixel sizes of 55 μm, 100 μm, 150 μm, 200 μm
- **Strip sensors**:
  - lengths of 1 cm, 2 cm, 4 cm
  - **strip pitch** options 100 μm, 200 μm, 500 μm
- Adjust the **doping concentration** to improve timing and spatial resolution.
- Optimize device structures, including epitaxial-layer thickness, to reduce parasitic capacitance and readout power.

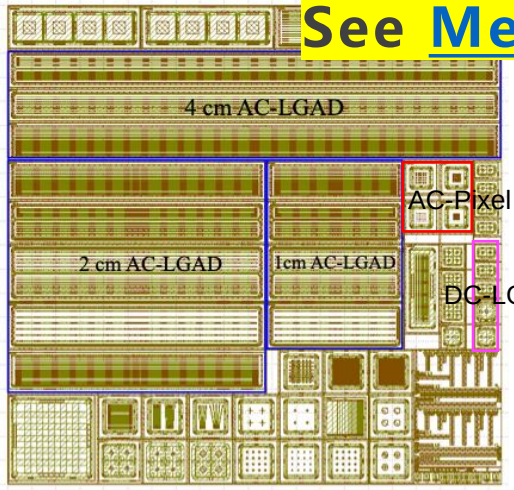


Wafer	EPI thickness	n+ dose
1	50μm	10p
2	50μm	10p
3	50μm	0.01p
7	80μm	10p
8	80μm	0.01p
4	50μm	1p, 0.1p
5	80μm	1p, 0.1p

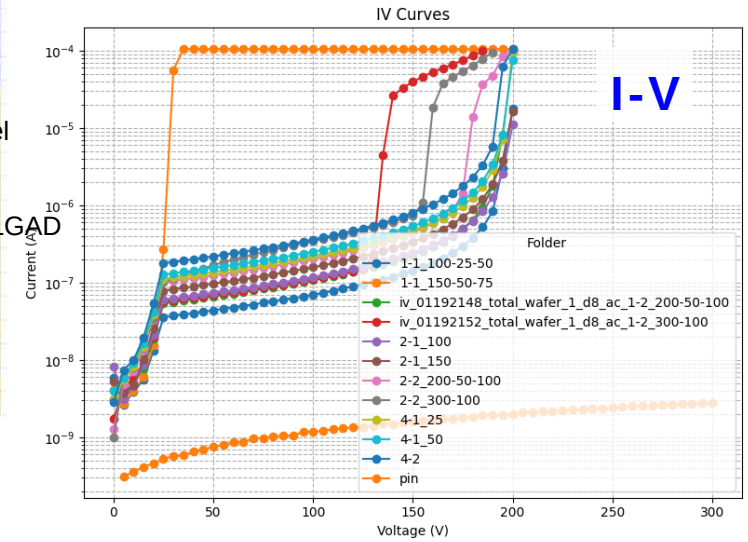
See Mei Zhao's report for details

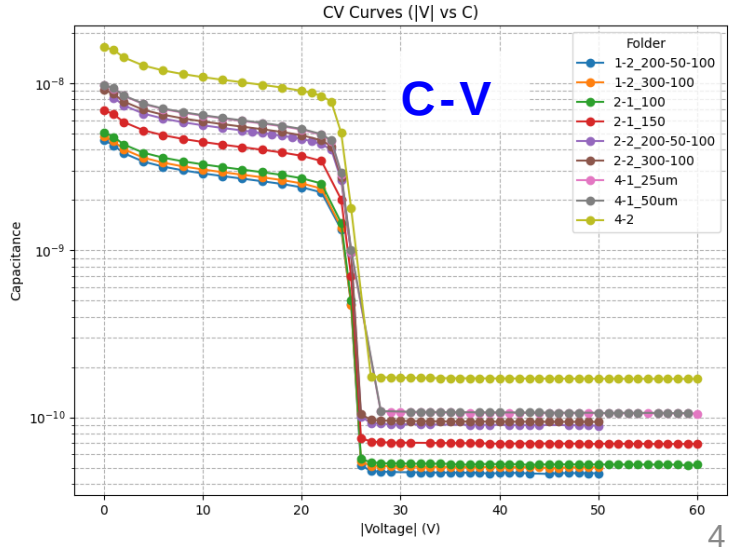


Latest AC-LGAD Wafer



Sensor layout

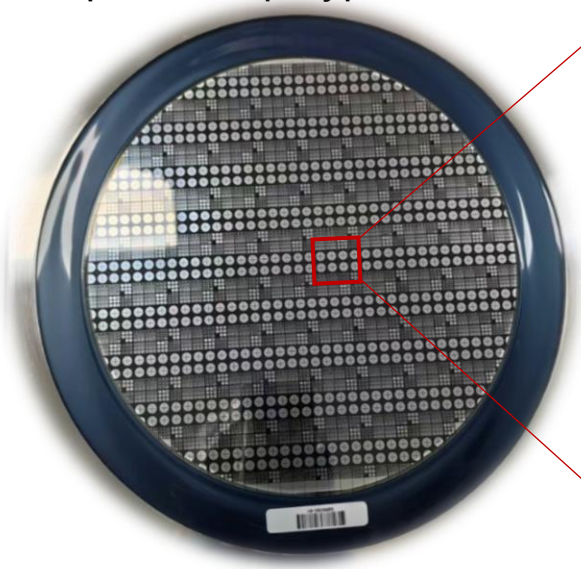




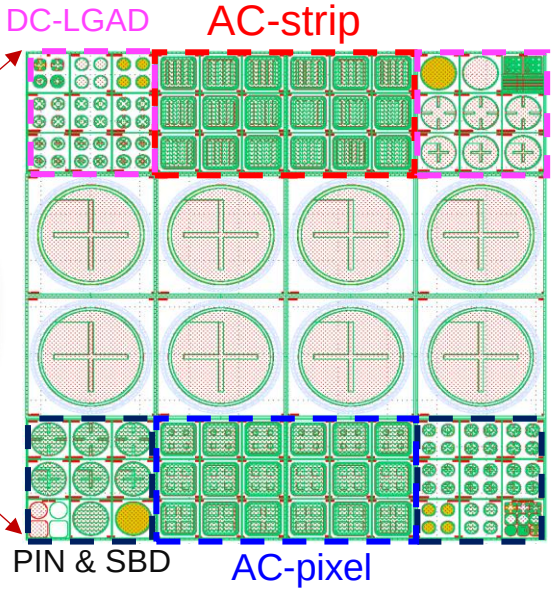
Silicon Carbide (SiC) Sensor R&D

See Xiyuan Zhang & Congcong Wang's report for details

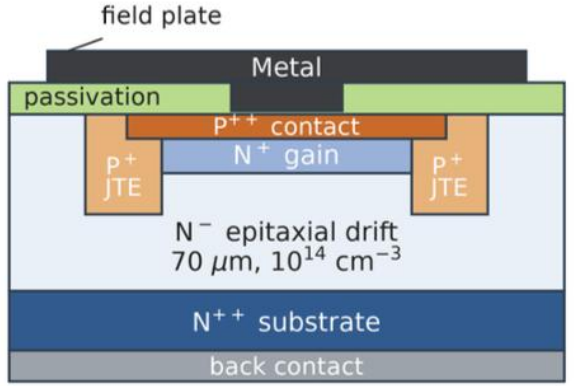
- SiC is a **wide-bandgap material**, offering a high breakdown field, high thermal conductivity & stability, low noise, and excellent radiation tolerance, making it **suitable for high-temperature and high-radiation applications**.
- We have **completed three iterations** of SiC device structures and processes.
- In **2026 we fabricated implanted SiC sensors**, including:
  - PIN diode with active areas: 1.4 mm / 0.5 mm
  - Schottky barrier diode (SBD) with active area: 0.5 mm
  - LGAD with active areas: 1.4 mm / 0.5 mm
  - pixel / strip type AC-LGAD



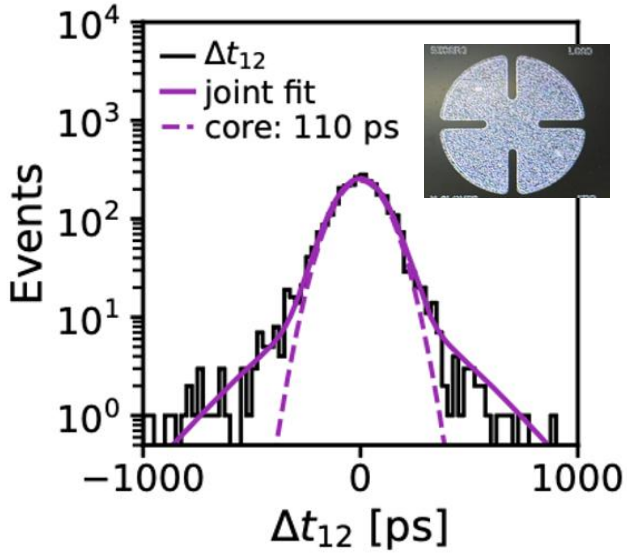
Latest SiC sensor wafer (3rd iteration)
8-inch/MOSFET process line



SiC sensor layout



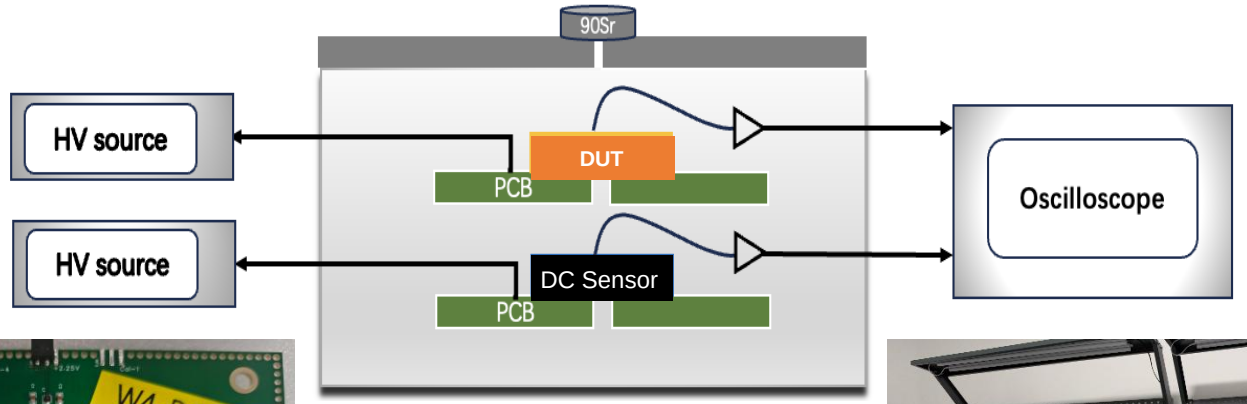
Implanted gain-type SiC (DC-gain) structure

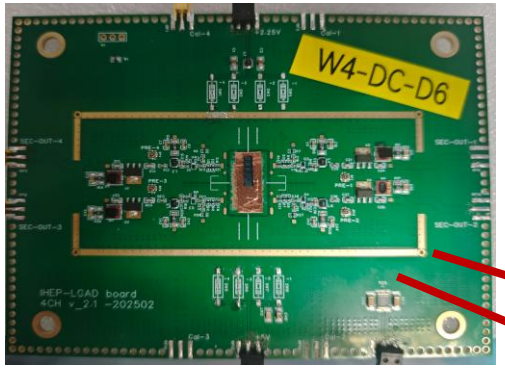


Test with ^{90}Sr β source timing resolution 77ps

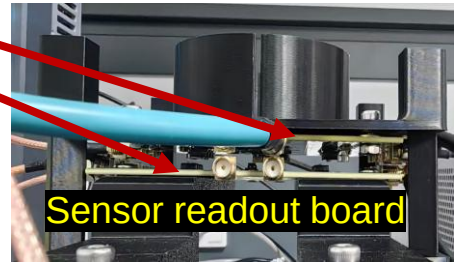
- Next, we will optimize key processes, including
  - substrate and epitaxial-layer, surface preparation, graded termination implantation, high-temperature implantation, dopant-profile control, and anneal activation.
- **Aim to develop stable, engineering-ready large-area high timing and spatial resolution SiC sensors**

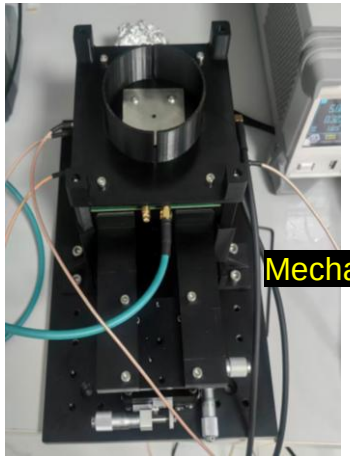
^{90}Sr β Test Setup

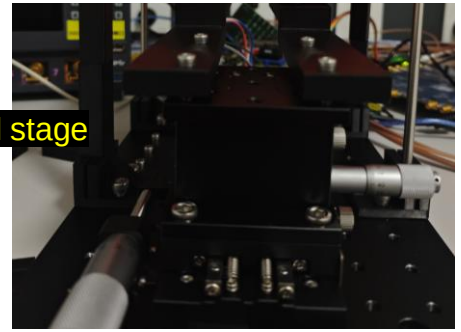


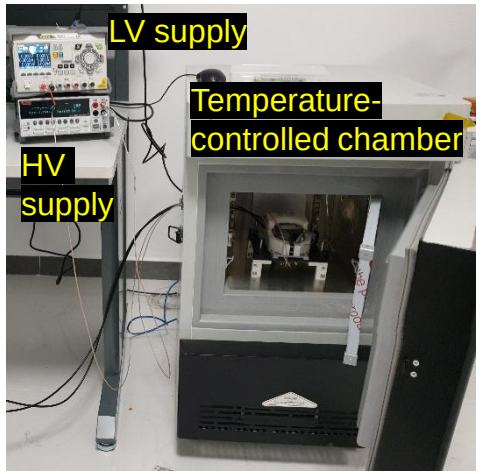


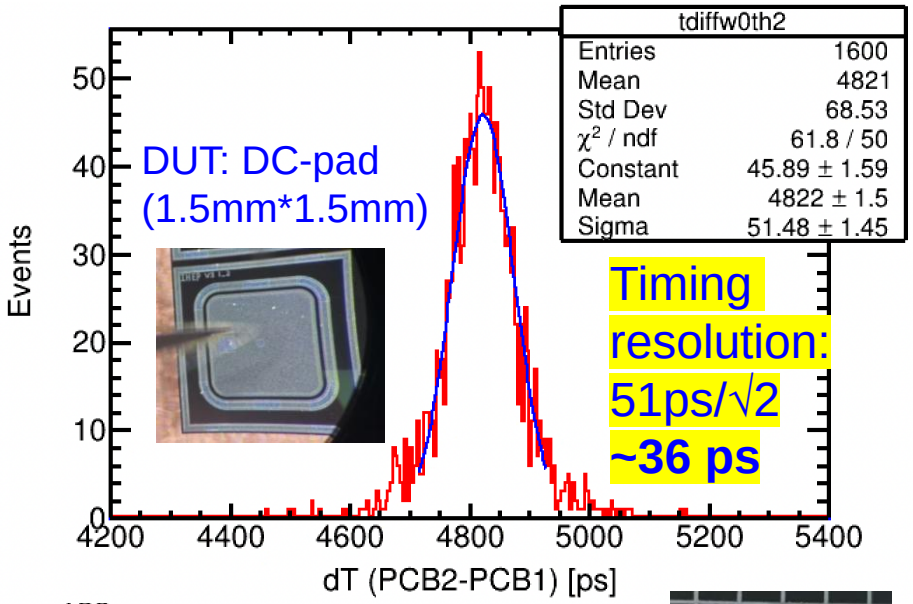


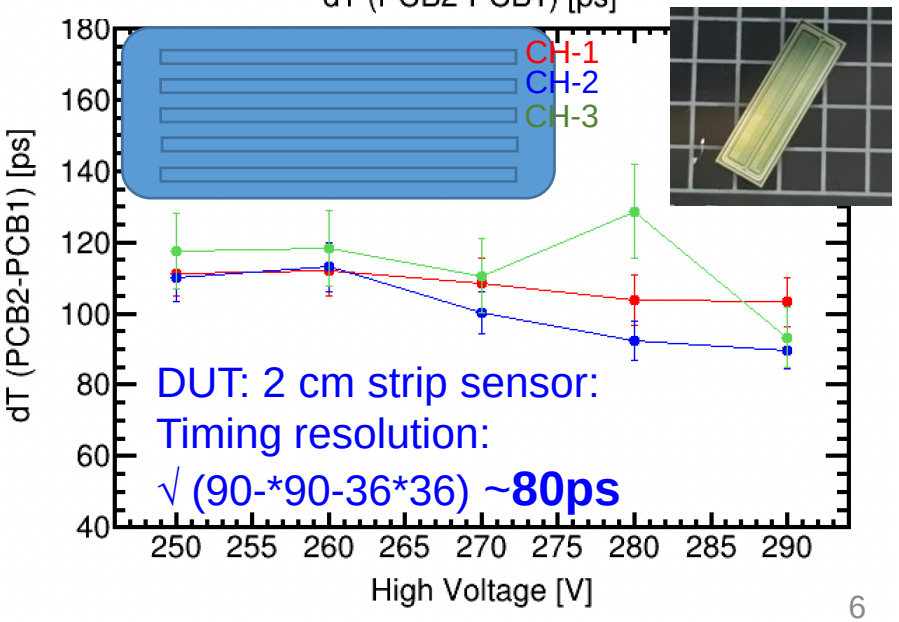












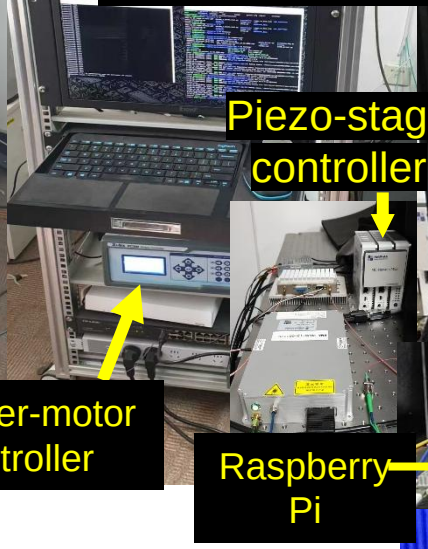
Target: a large-area sensor with timing resolution of ~40ps, spatial resolution ~10 μm.

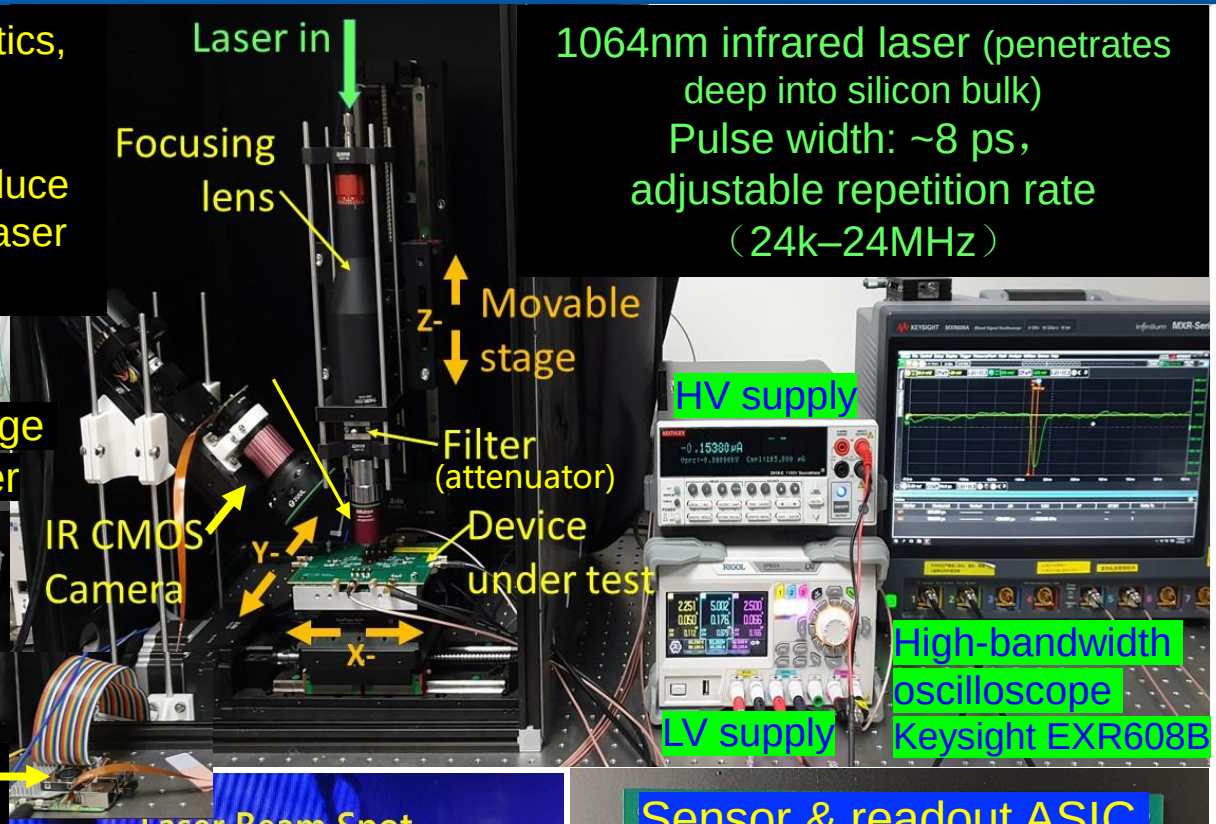
Precision Laser Test System

A precision 3D translation stage combines programmable three-axis motors with a high-precision piezo stage（step size 10nm, repeatability 100nm）, enabling precise scans across large sensor arrays.

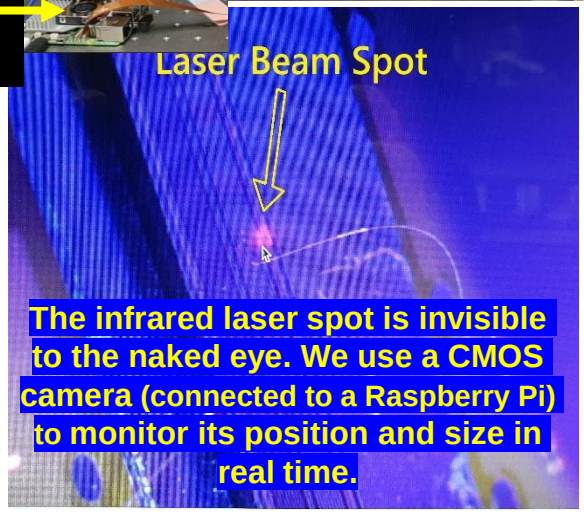


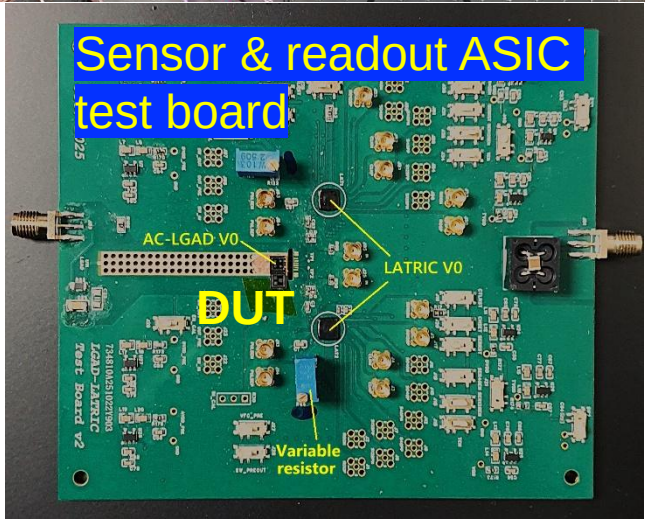
The focusing optics, combined with precise z-axis positioning, produce a micron scale laser spot size

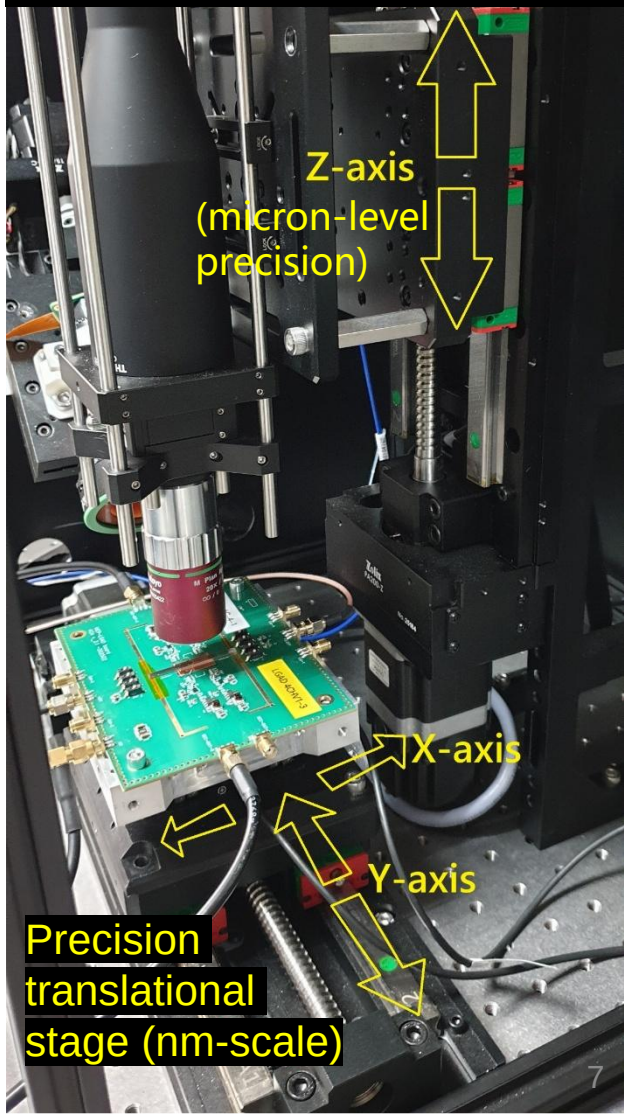




1064nm infrared laser (penetrates deep into silicon bulk)
Pulse width: ~8 ps，adjustable repetition rate（24k–24MHz）

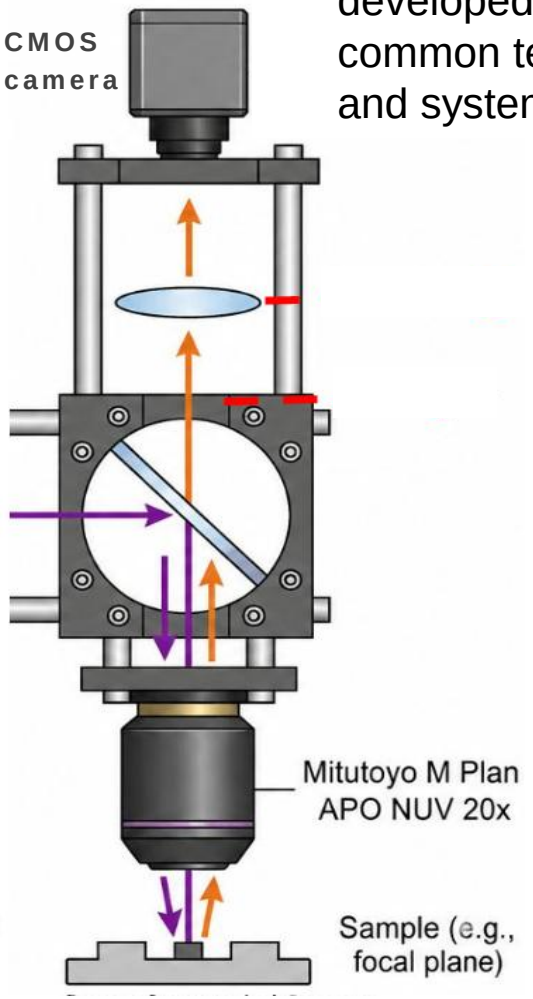


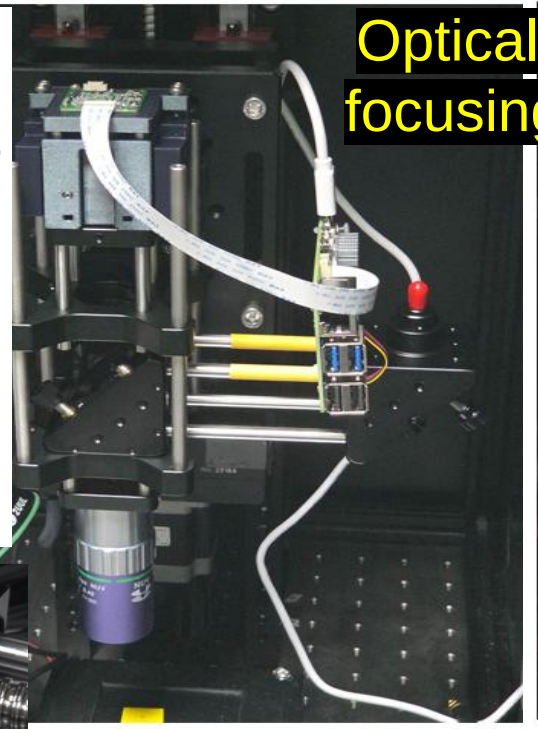


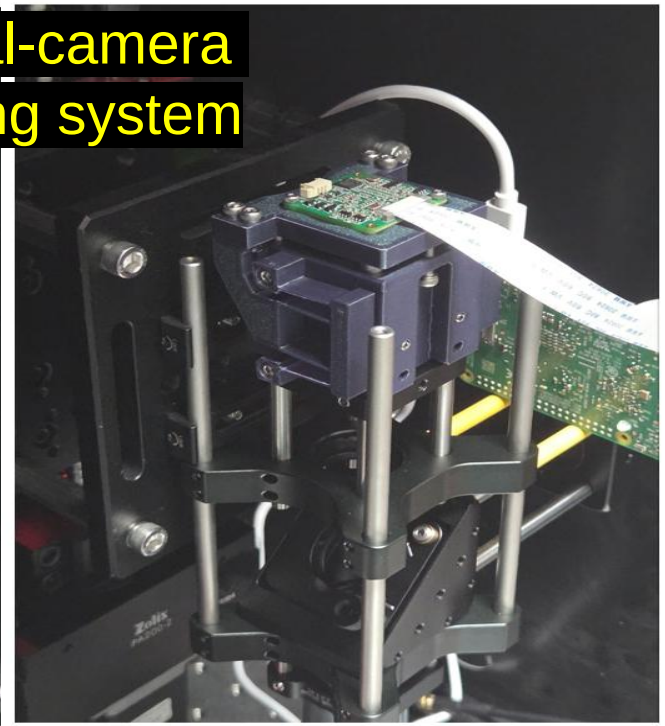


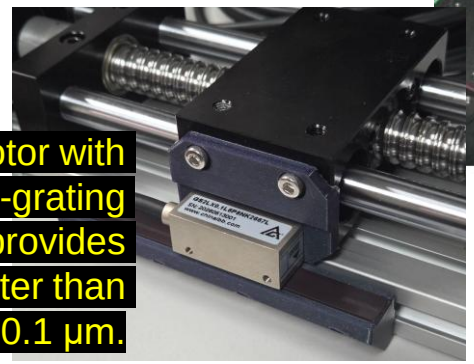
A precision picosecond infrared laser TCT system is used to characterize the latest sensors and readout chips.

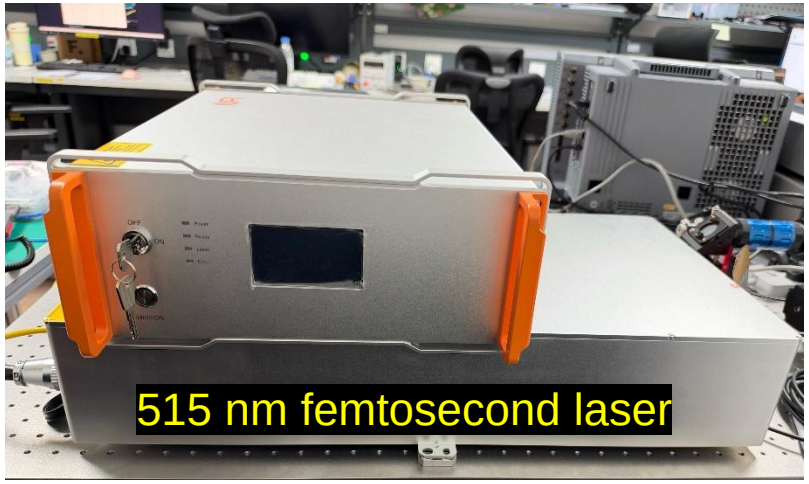
- Developing a **515 nm (<200 fs) laser** test platform for wide-band gap semiconductor sensor characterization using **two-photon absorption** (TPA).
  - penetration depth up to 60 μm
  - emulate MIP ionization response in SiC
- Silicon and silicon-carbide sensors share a jointly developed automated hardware/software framework, common test platforms, front-end readout electronics, and system integration.

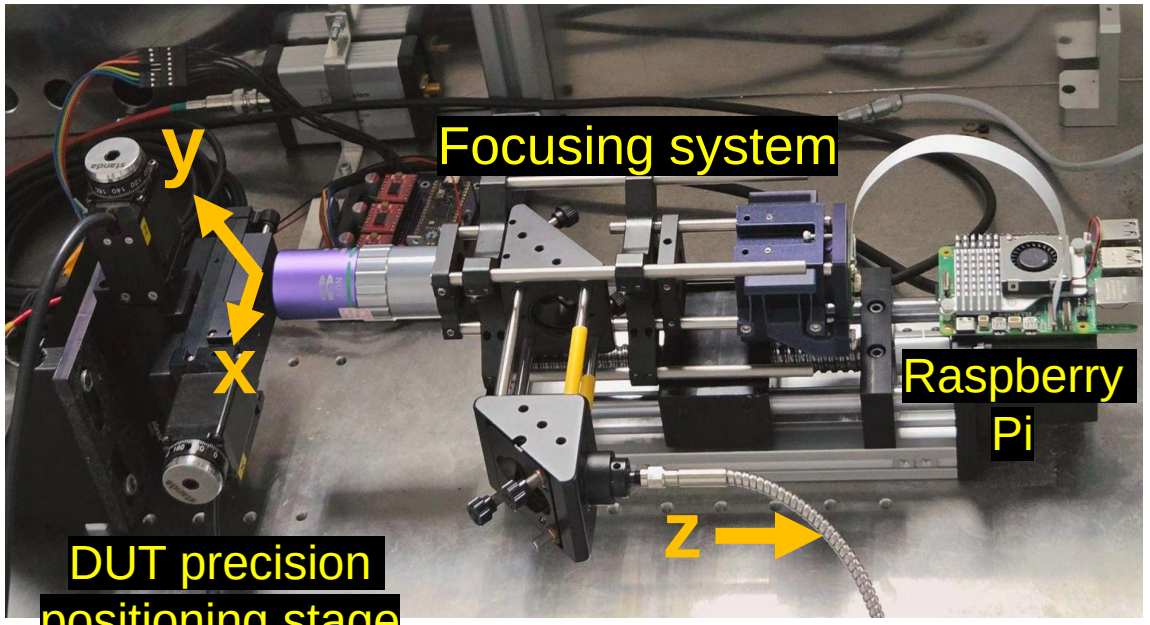




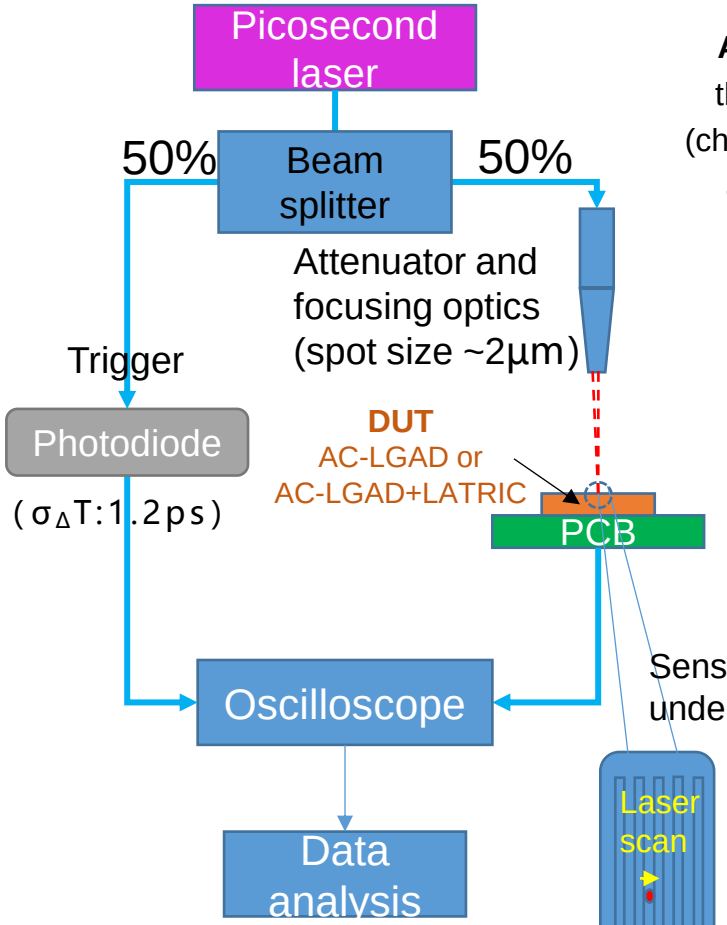




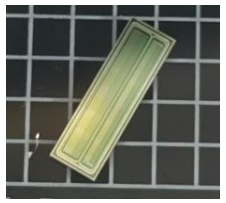




Results at MIP-Equivalent Laser Intensity: Strip Sensor

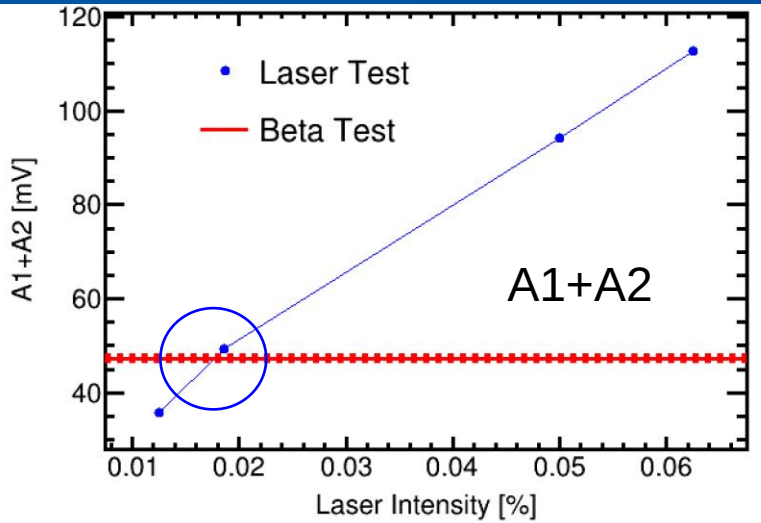


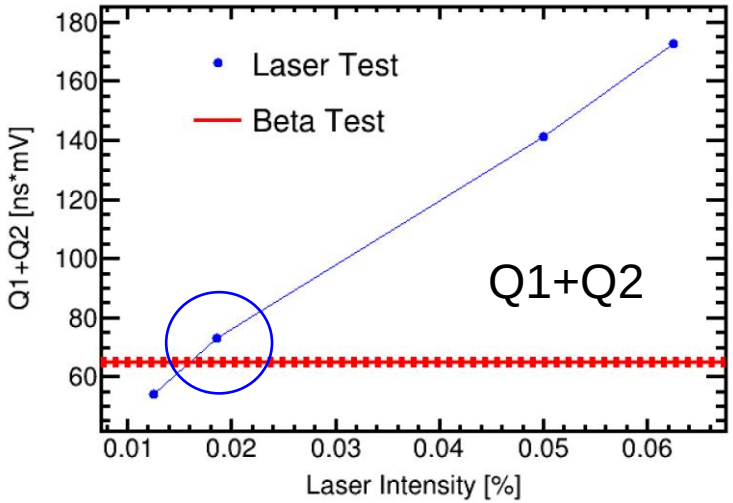




2cm strip sensor

A1 & A2 (Q1 & Q2): the signal amplitudes (charge) of the highest- and second-highest-amplitude strips, respectively.

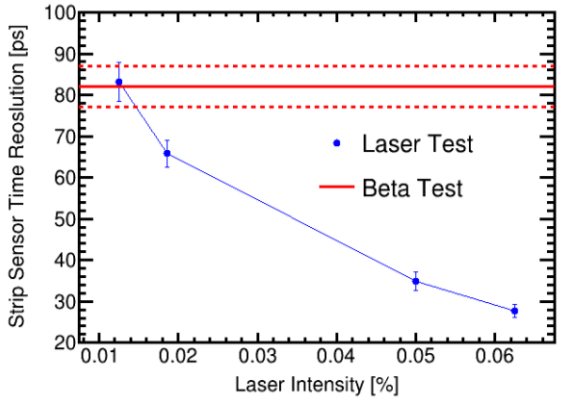




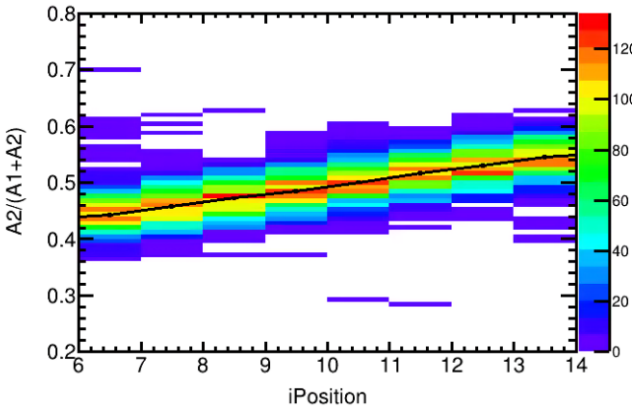
Target: Time resolution ~40ps, spatial resolution 10μm

At MIP MIP-equivalent laser intensity (0.02%), timing resolution is ~60ps, with a spatial resolution is 8μm.

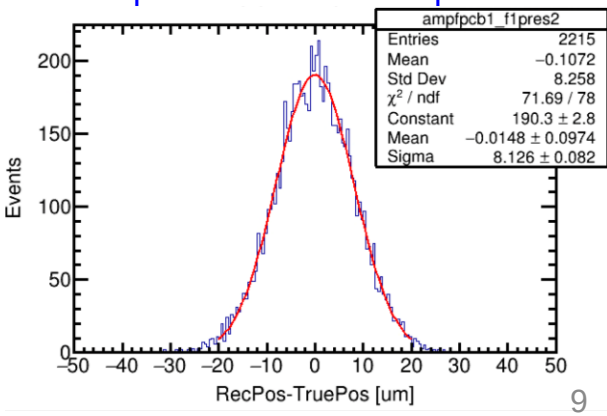
Timing resolution ~60 ps



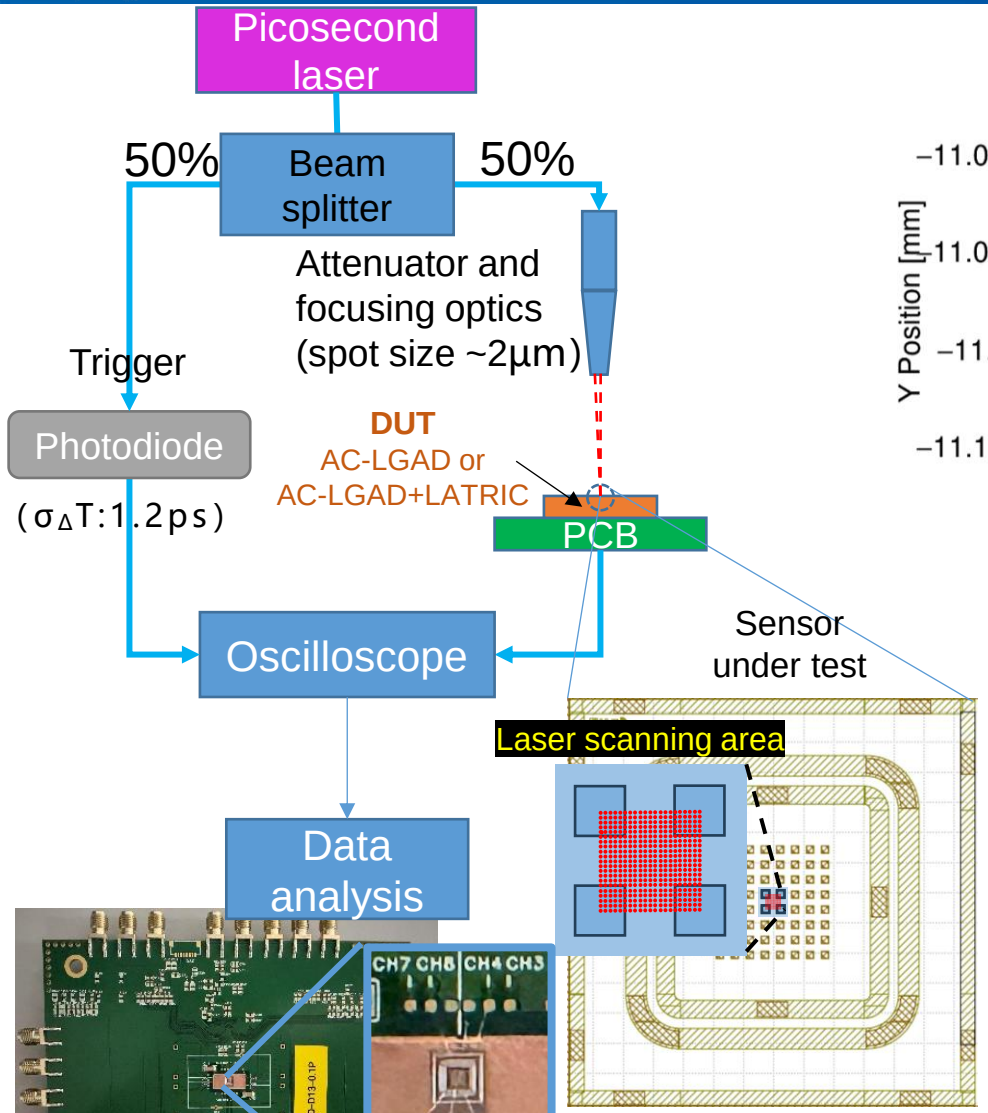
A1/(A2+A2) at eight scan positions



Spatial resolution 8.1μm

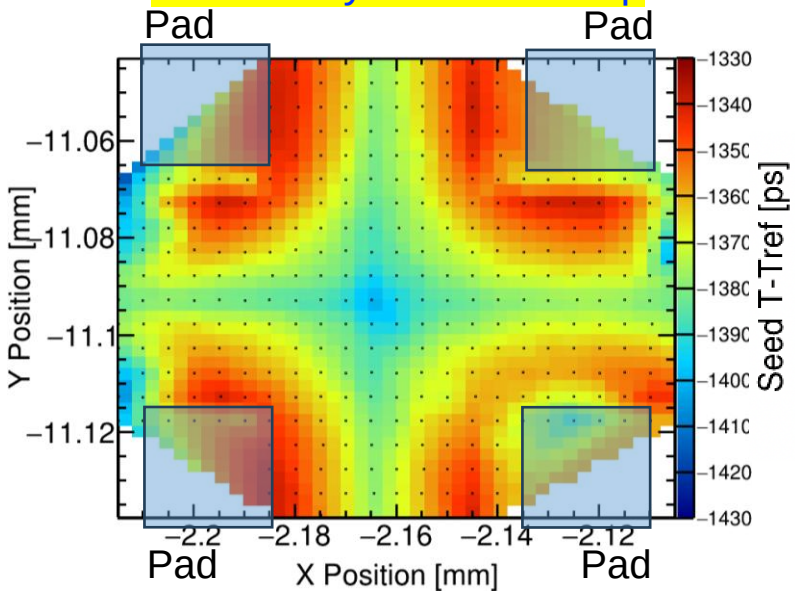


Results at MIP-Equivalent Laser Intensity: Pixel Sensor

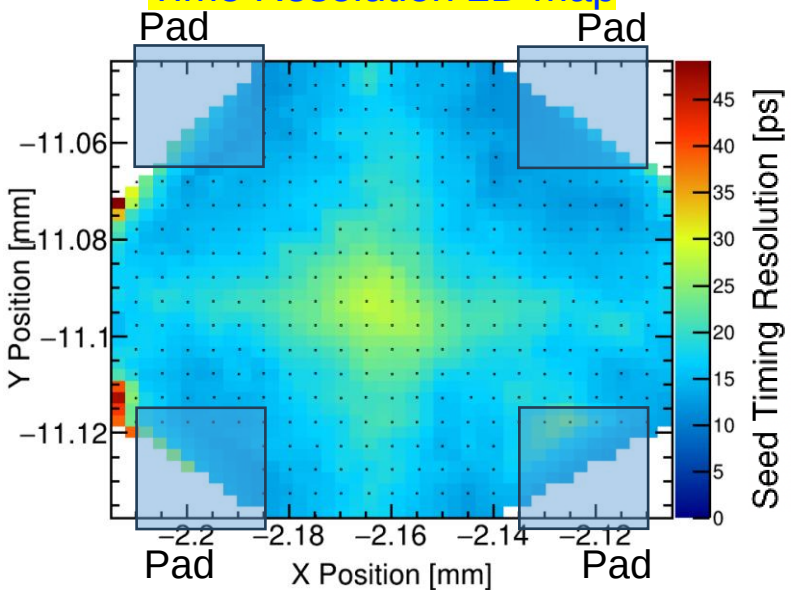


Pixel sensor (100μm pixel)

Time Delay Mean 2D Map



Time Resolution 2D map

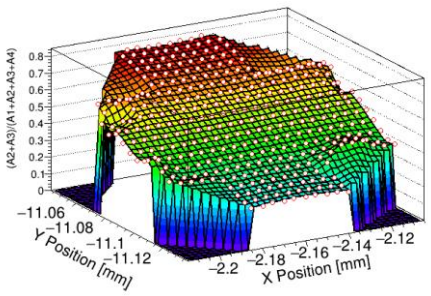


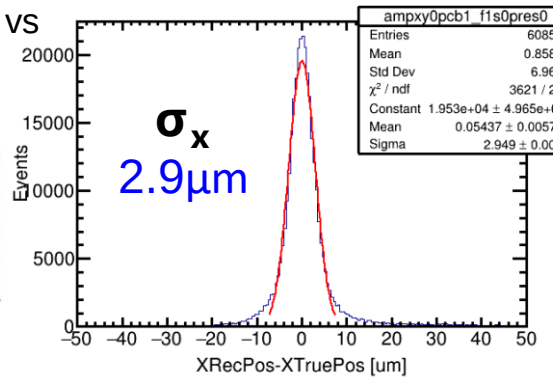
Latest silicon LGAD sensor: 100μm pixels (50μm readout pad)

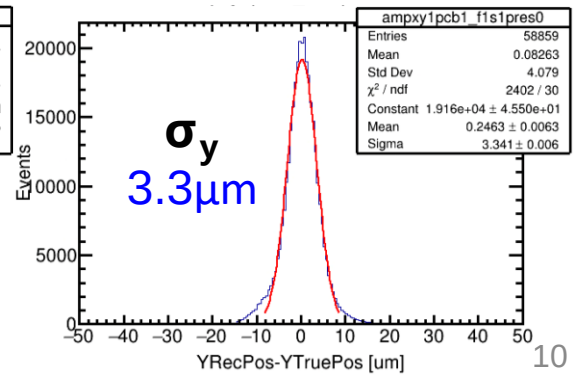
At MIP-equivalent laser intensity (0.02%), spatial resolution is ~3μm, with timing resolution of ~20 ps

See Mei Zhao's report for details

(A2+A3)/(A1+A2+A3+A3) vs Laser Position

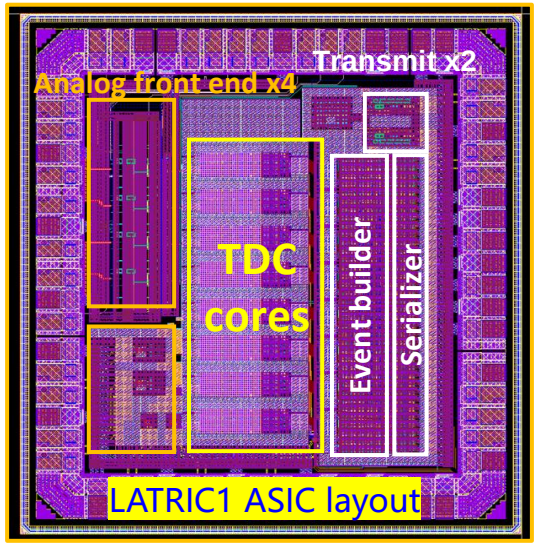




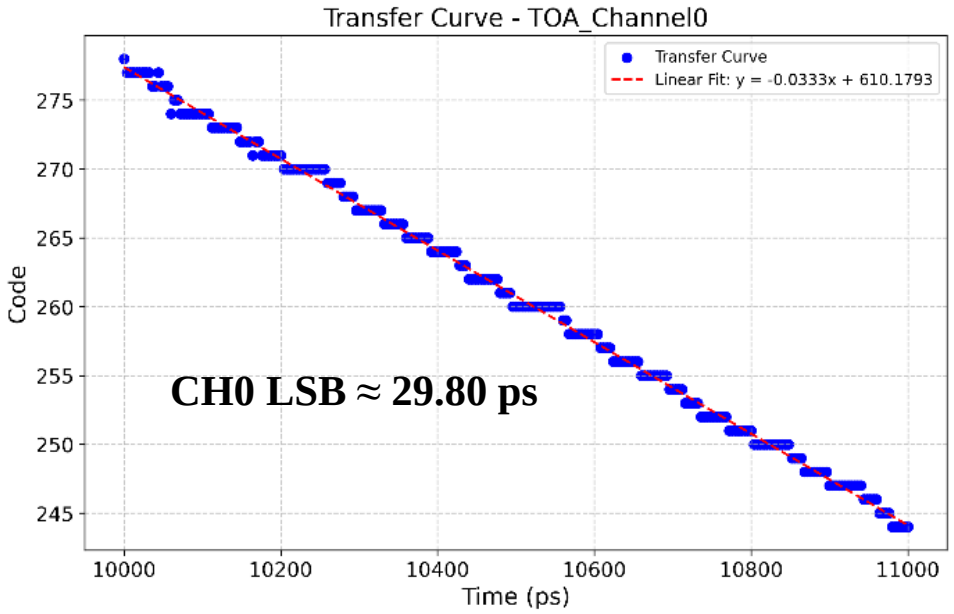


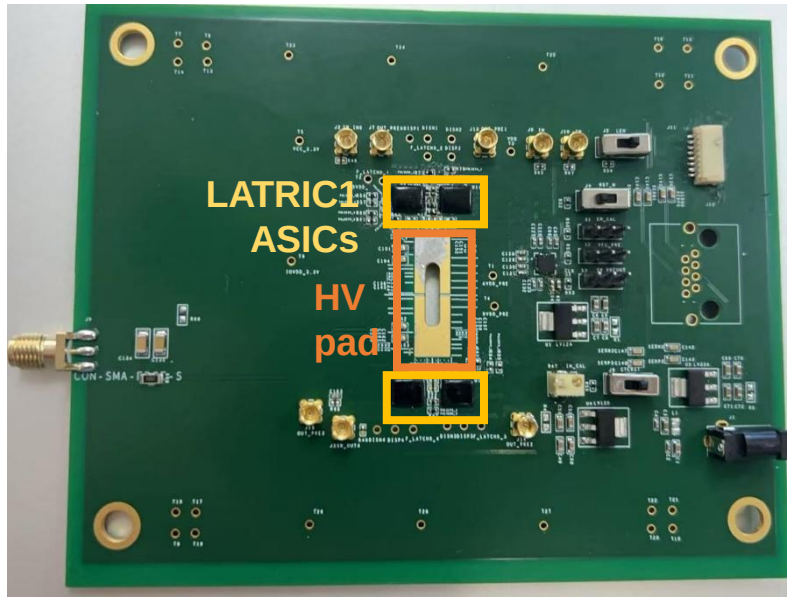
Readout ASIC LATRIC: Latest Development

- **Requirements: timing (≤30 ps), spatial resolution (matched to 10 μm measurement precision), low power, and high integration (100μm channel pitch, and ≥64channel).**
- The first single-channel prototype, LATRIC0 was designed & fabricated in Apr 2025
  - DOI 10.1088/1748-0221/21/04/C04028
- **The 2nd-generation 8-channel LATRIC1 was submitted for fabrication in Oct 2025**
  - 4 channels integrate the analog front end and TDC; while TDC of the other 4 channel connect to differential-pulse receivers. Channel pitch is 100 μm.
  - Enhancements include: a strengthened analog front end with higher preamplifier gain for improved SNR, refined encoder logic, and an event builder with timestamping.



- LATRIC1 returned from fabricationin in Mar 2026.
- Latest measured time-conversion least significant bit **(LSB) ~ 30 ps, meeting the requirement**





LATRIC1 & sensor test board

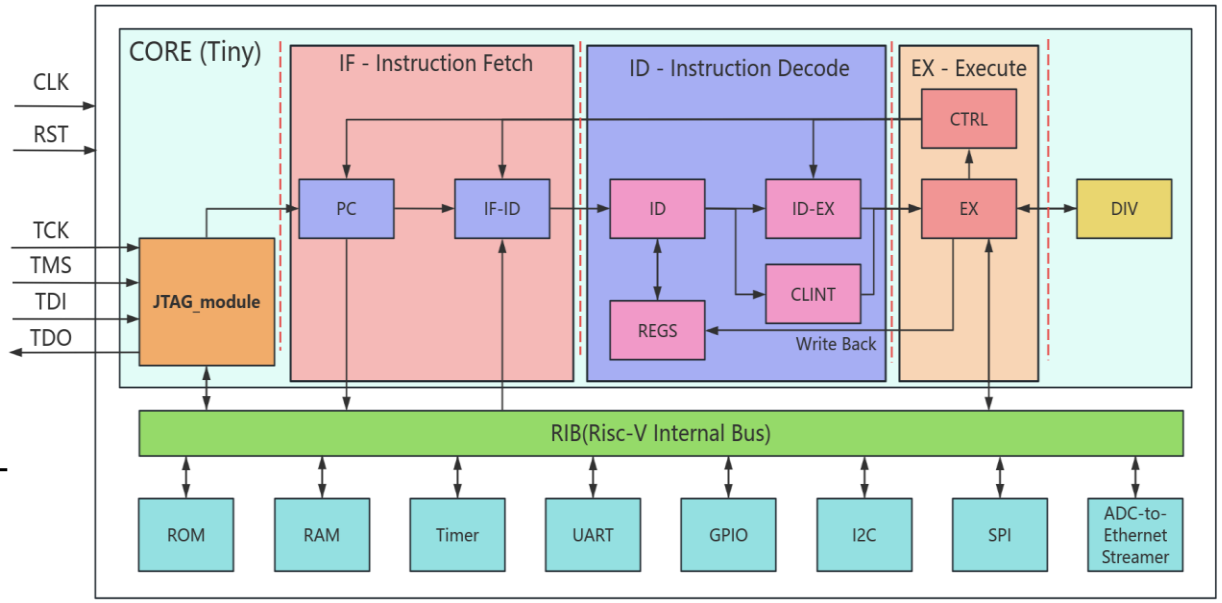
System-on-chip (SoC) development

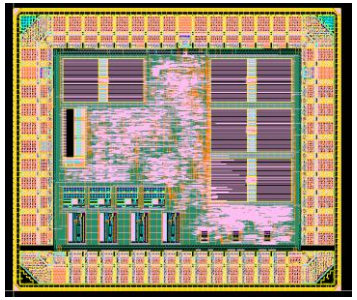
Submitted and accepted for NIMA

High Energy RISC-V SoC, HERIS

- Conventional ASICs use fixed hardware logic, making it difficult to meet the flexibility, configurability, and intelligence required by next-generation detectors.
- Front-end intelligence is a key direction for detector readout electronics, based on programmable SoC architecture (integrating CPU, memory, buses, peripherals, etc.) and shifts the system from passive readout to active sensing and adaptive control.
- Development of the **HERIS-V1 prototype (based on Tiny RiscV architecture)** began in 2025;
  - Our team completed the full workflow, from RTL code development and FPGA prototyping through digital back-end integration
- **Fabricated with 55nm CMOS**;
- **The chip will be integrated with LATRIC to create a coordinated architecture combining precision measurement and on-chip intelligent processing**

- Core (Tiny RiscV)
  - RV32IM instruction set
  - 3-stage pipeline
  - CoreMark/MHz = 2.4
- JTAG interface
  - SupportsOpenOCD
  - SupportsGDBdebug boot
- Peripherals: 4 KB ROM, 32 KB RAM, I2C, UART, SPI, ADC, UDP





- 55 nm process
- Clock frequency 50 MHz
- Die area 1.020 x 1.196 mm
- Supply voltage 1.2 V

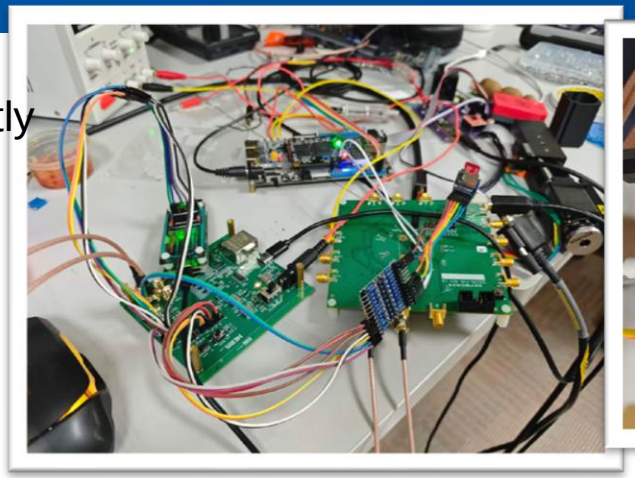
Testing and Performance of HERIS-V1 Prototype

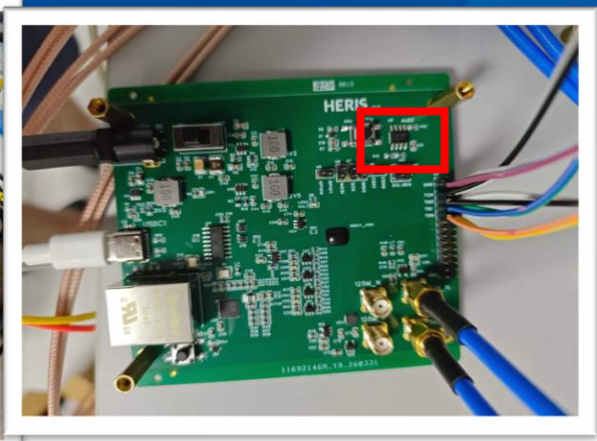
- Functionality tests:
  - Power on，OpenOCD connected & ROM program runs correctly
  - On-board EEPROM and I²C interface operates correctly
  - GPIO functions correctly
  - ROM, SD card and SPI module operates correctly

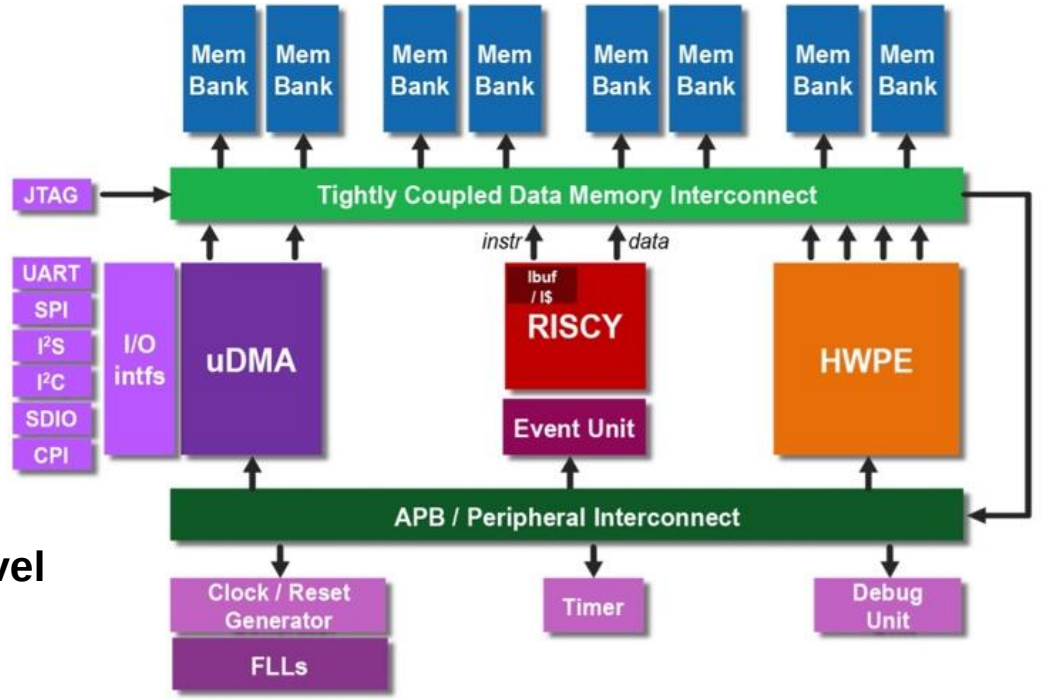
- Rated frequency: 50 MHz,
  maximum operating frequency:150 MHz

- Performance (CoreMark/MHz):
  - ARM Cortex-M0/M0+:approx. 0.9 ~ 1.0
  - PicoRV32 (minimalist RISC-V): approx. 0.5 ~ 0.8
  - HERIS-V1: **1.75** (silicon and FPGA scores agree)
  - VexRiscv / Hummingbird E203: approx. 1.5 ~ 2.2
  - ARM Cortex-M3 / M4:approx. 3.3 ~ 3.4

- **The next-generation HERIS-V2 will use the PULPissimo SoC platform with RISCY/Ibex cores.**
- **Radiation hardening will combine logic layer TMR (triple modular redundancy), memory layer ECC (error-correcting code) & system-level software recovery" in a layered radiation-hardening architecture, alongside software-level self-recovery.**
- **Design completion and fabrication submission are planned for Q1 2027.**





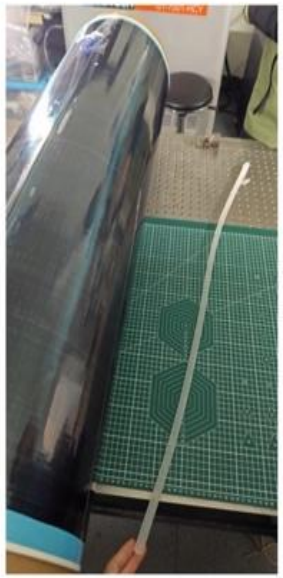


PULPissimo SoC Architecture

Mechanical System for Semiconductor Detectors

See XiaoHui Qian's talk for details

- CEPC Silicon trackers requires
  - minimal material per layer (<1% X_0) to reduce multiple scattering
  - micron-scale deformation and mechanical stability
  - Detector heat must also be removed efficiently.
- This calls for integrated design and fabrication of low-mass, high-strength, thermally conductive carbon-fiber structures and cooling.
- **We have develop in-house carbon-fiber composite structure fabrication techniques & processes.**
- **Several prototypes have been made and tested.**



M40J prepreg



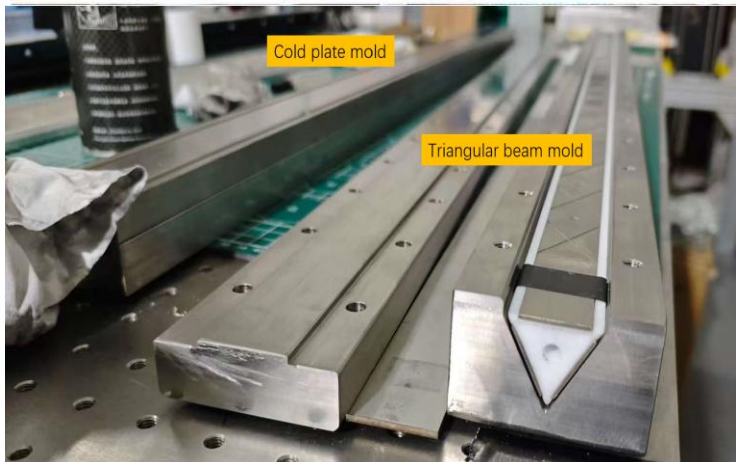
M40J carbon-fiber tow



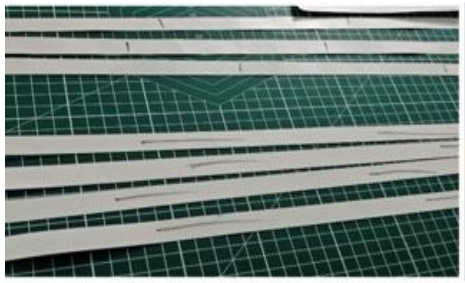
Carbon-fiber resin



Oven



Custom-designed compression mold



Cut carbon-fiber prepreg strips



Laying up carbon-fiber prepreg



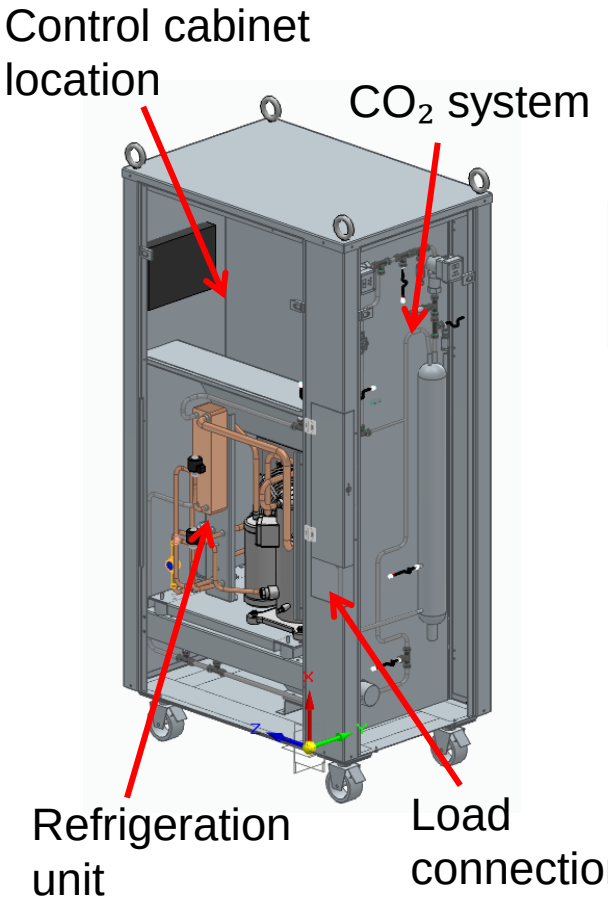
Applying release agent

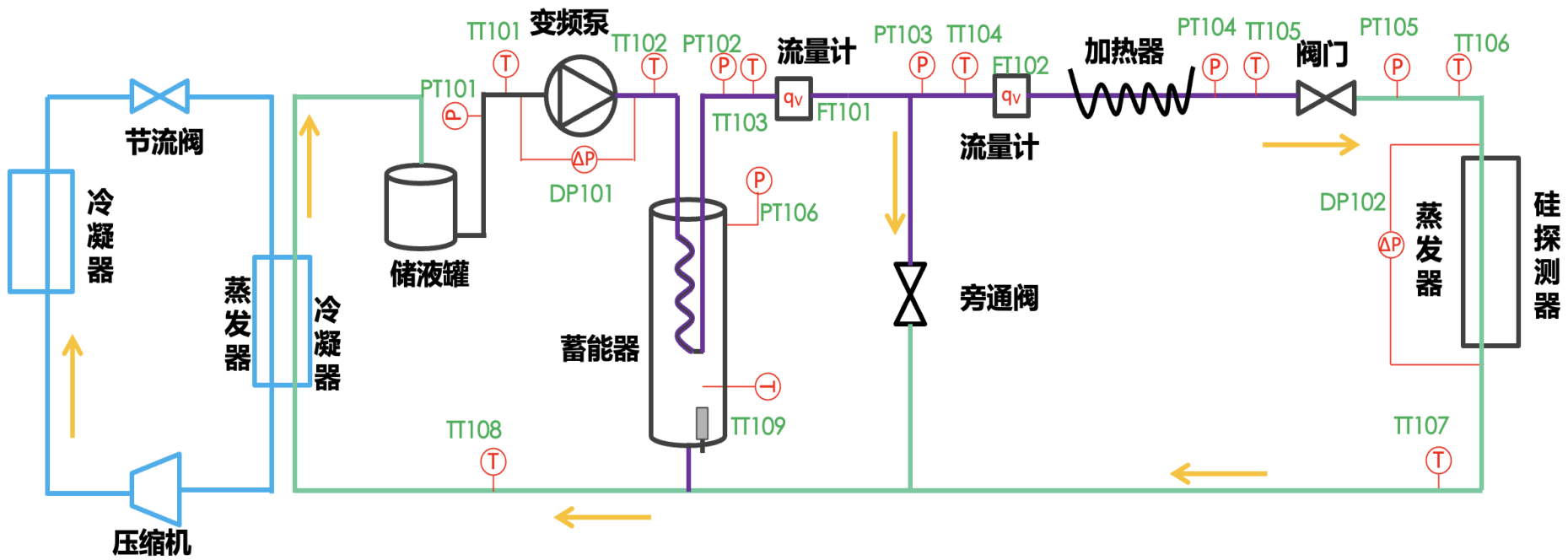


Cured prototype

Two-Phase CO_2 Cooling System Development

- **To meet the low-temperature operating needs of semiconductor detectors, we are working with the Institute of Physics and Chemistry, CAS to develop a two-phase CO_2 cooling prototype.**
- This compact, portable system is rated for heat removal of **~ 1.2 kW** (upgradeable to >2 kW), with operating temperature adjustable from -20°C to 20°C, with temperature stability better than ±1°C



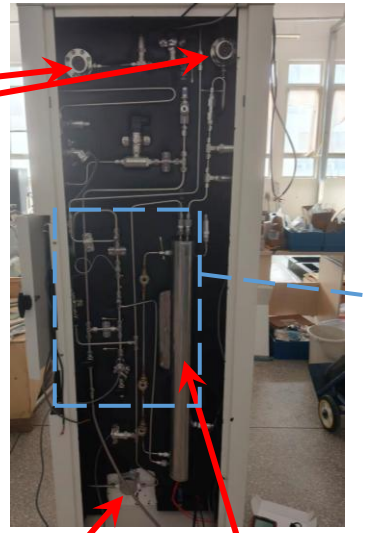


Two-phase CO_2 cooling system schematic

(Instrumentation: 9 temperature sensors, 7 pressure sensors, 2 differential-pressure sensors, 2 flow meters, 2 level sensors)

➢ Latest progress on the two-phase CO_2 cooling system





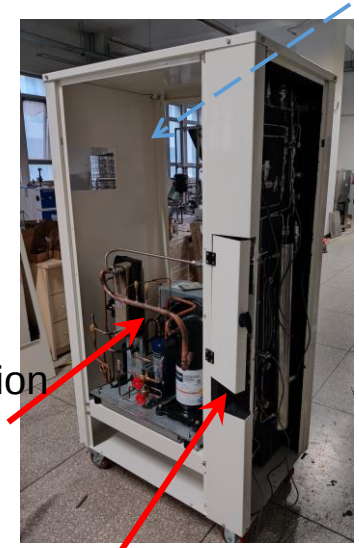




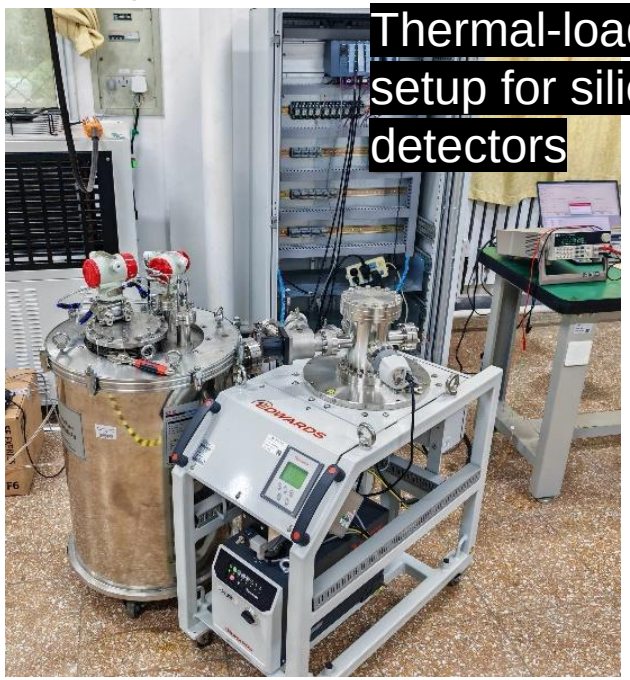
Electrical control cabinet

System integration is under way, commissioning planned in Nov 2026





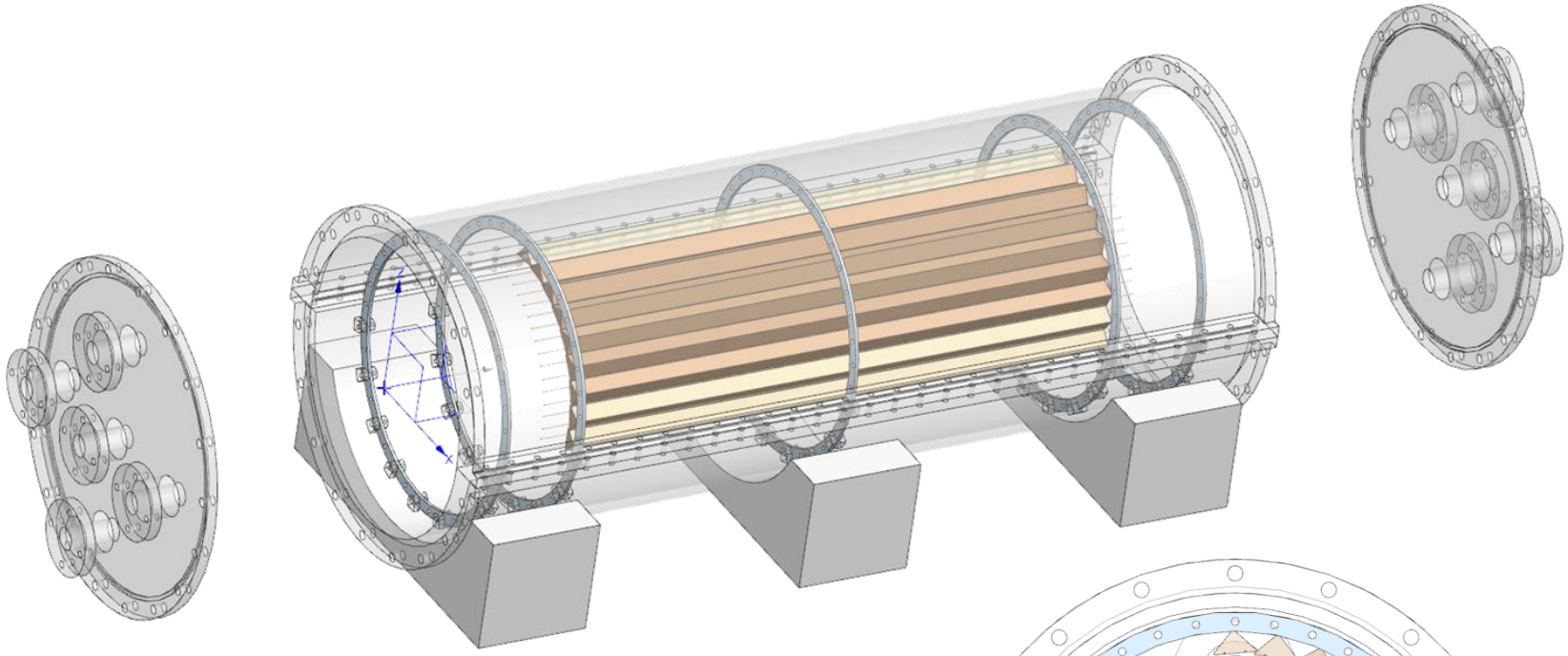
Piping to the evaporator (silicon detector)



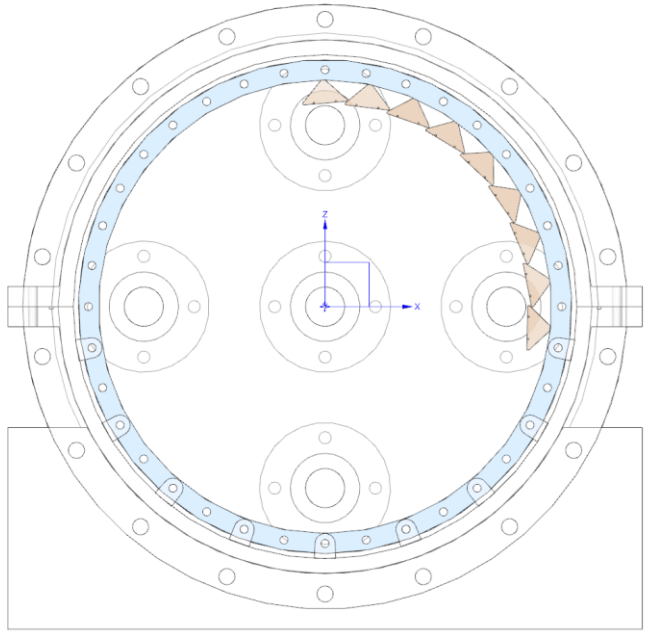
Thermal-load test setup for silicon detectors

Cooling Test Platform Design

- The main body of the apparatus is a vertically split acrylic cylinder. The acrylic cylinder is secured by three arc-shaped support brackets, and 5 sets of aluminum alloy circular discs are used as internal supports.
- The Stave samples are arranged in a 1/4 circumference layout and are secured using outer-ring aluminum alloy circular discs and extension screws.
- The cylinder (excluding end caps) is 1.5 m long (the sample, including connectors, is approximately 1.1 m, leaving a 150 mm margin on each side), with an inner diameter of 0.5 m and a wall thickness of 16 mm.

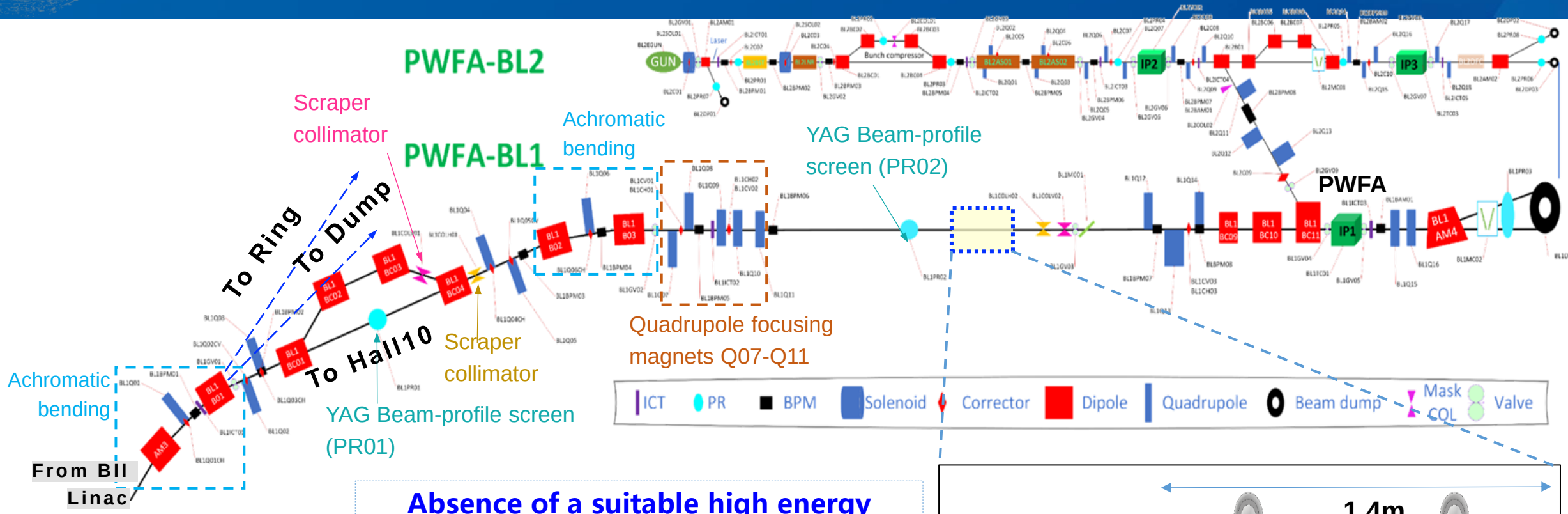


Joint test of stave cooling structures and the CO_2 refrigerator—to validate its performance (incl. temperature distribution, uniformity flow rate, system stability, and etc.)



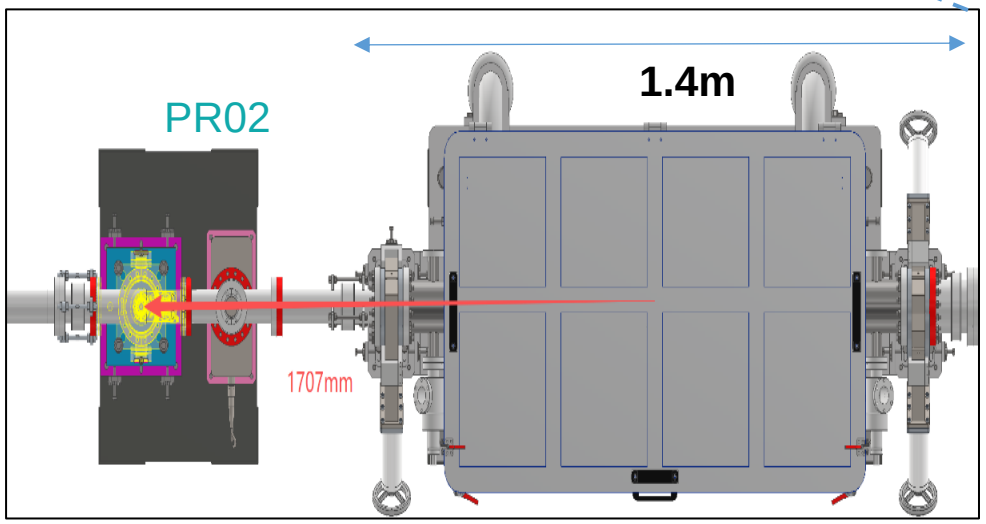
5 sets of aluminum alloy circular discs are used as internal supports

BEPCII-PWFA Beam-test facility (BII-PBTS)



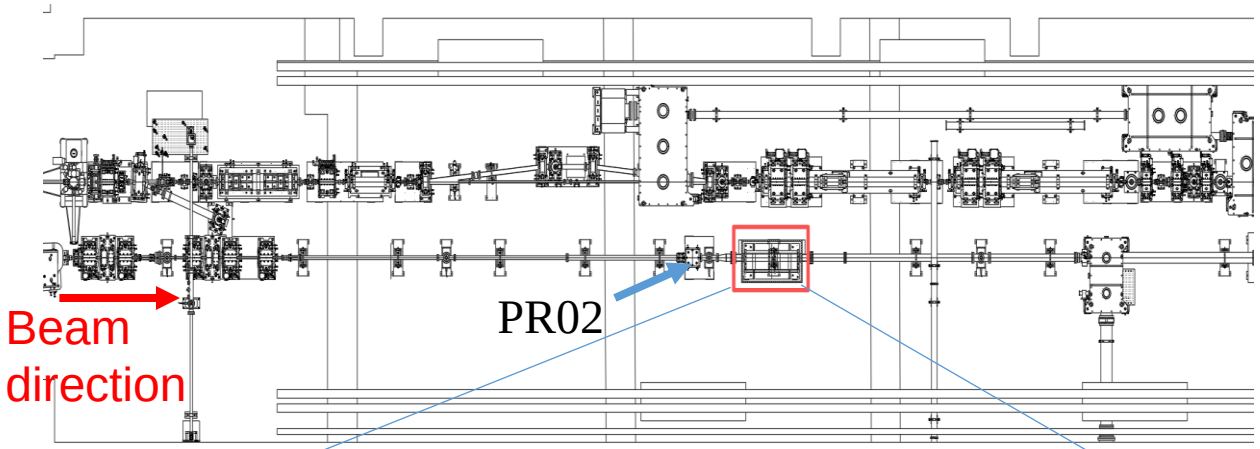
Absence of a suitable high energy beam test facility prompted this effort.

- **Beam energy:** 2 GeV
- **Beam-test chamber:** Expected to be completed and operational in Q1 2027
- **Bunch-density control:**
  - adjust positron/electron gun settings
  - scattering targets (PR01-PR02);
  - scrape the beam;
  - expand the beam using quadrupole magnets Q07-Q11;
  - use particles at the transverse beam edge (adjusted in the chamber)



Beam-test chamber under construction

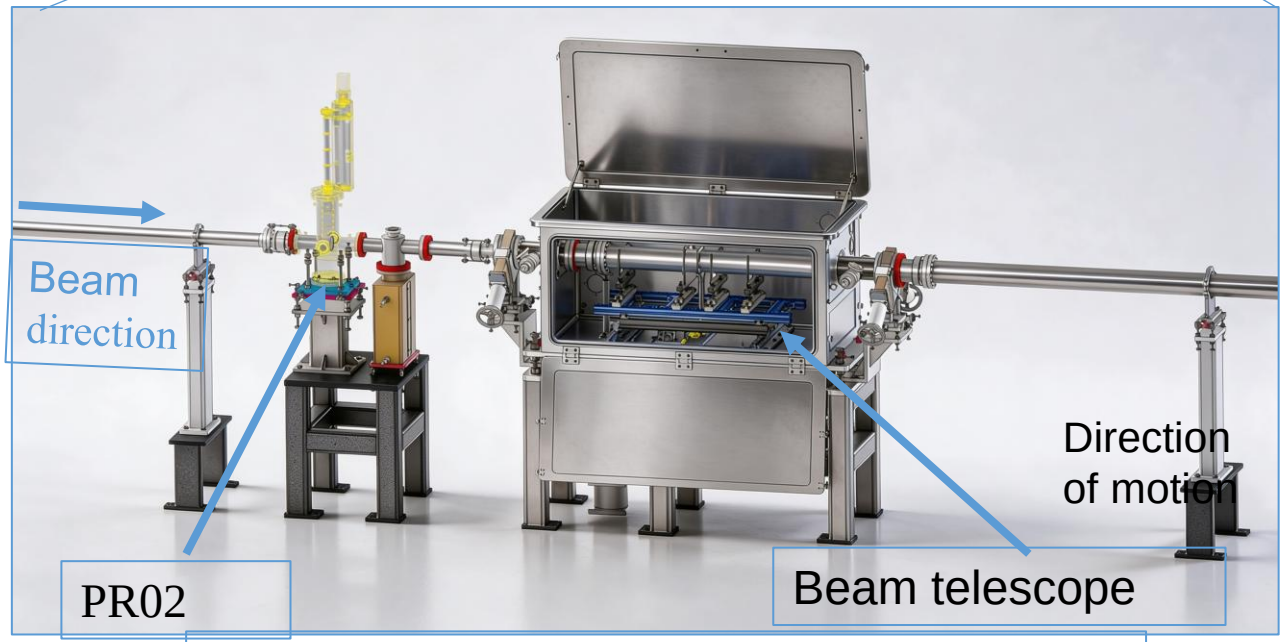
BII-PBTS Beam-test chamber & telescope design





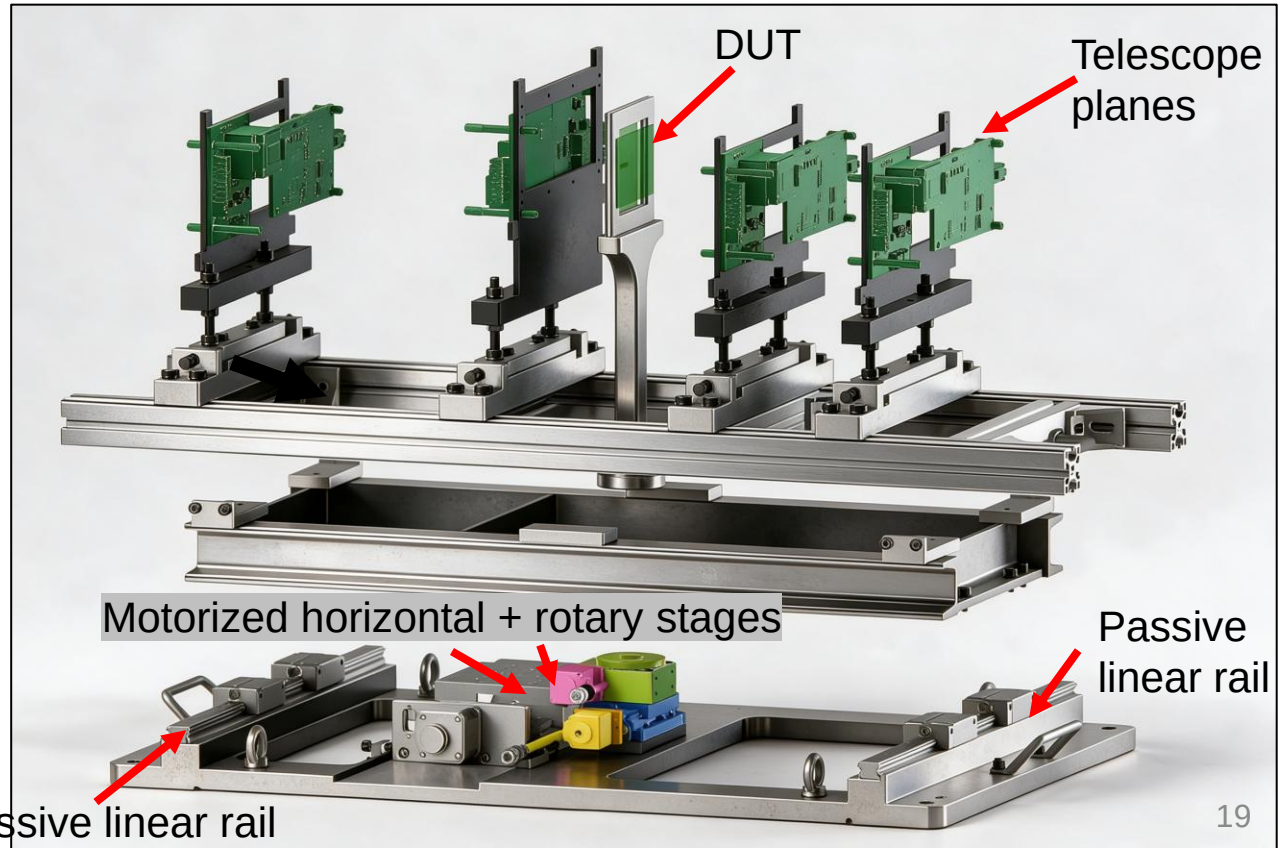
Site before chamber installation

Beam-test chamber



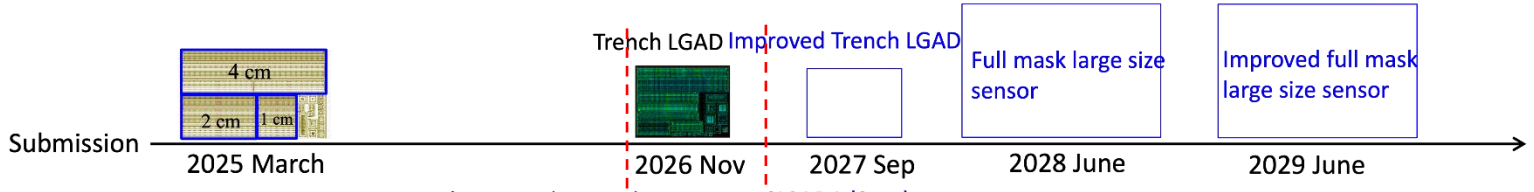
Distance to chamber center PR02 1.7m

Telescope Design

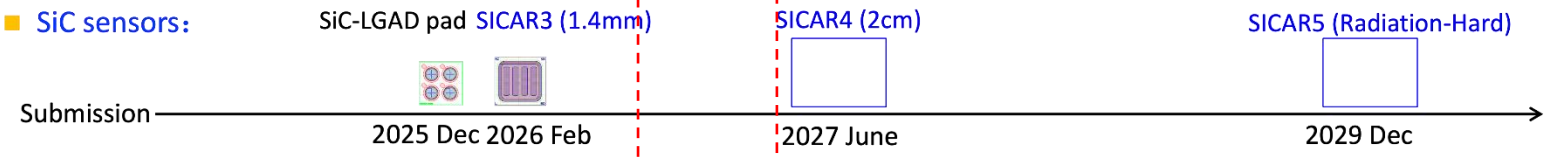


Summary

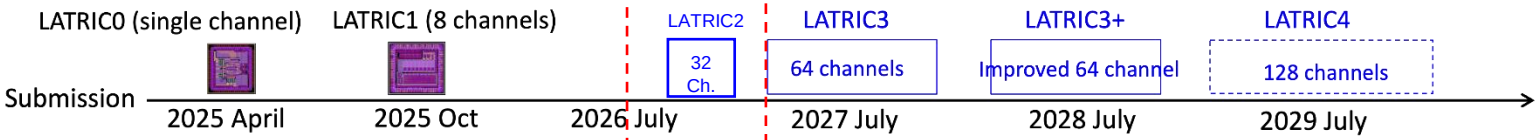
- LGAD sensors are evolving toward improved process, larger size, higher performance, and lower power consumption:



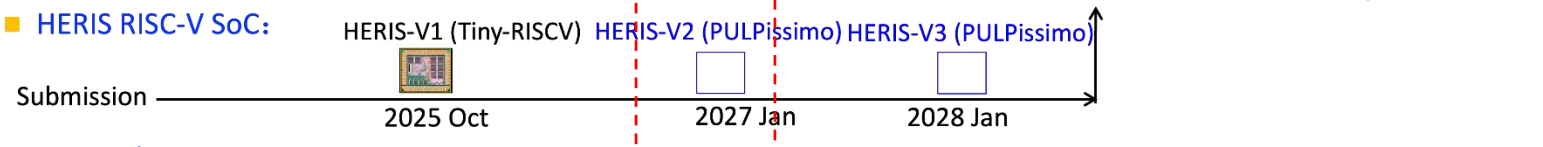
- SiC sensors:



- LGAD readout ASIC, LATRIC, is being developed towards multi-channels:



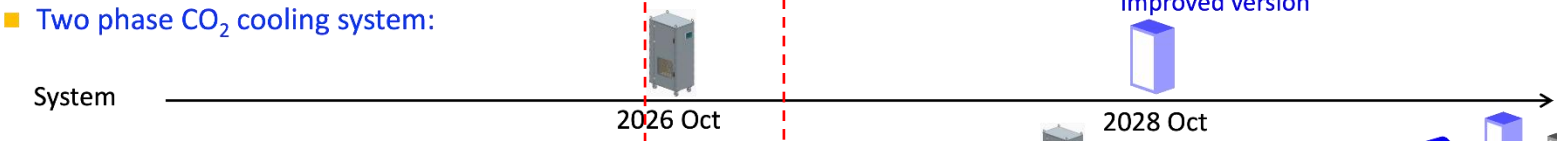
- HERIS RISC-V SoC:



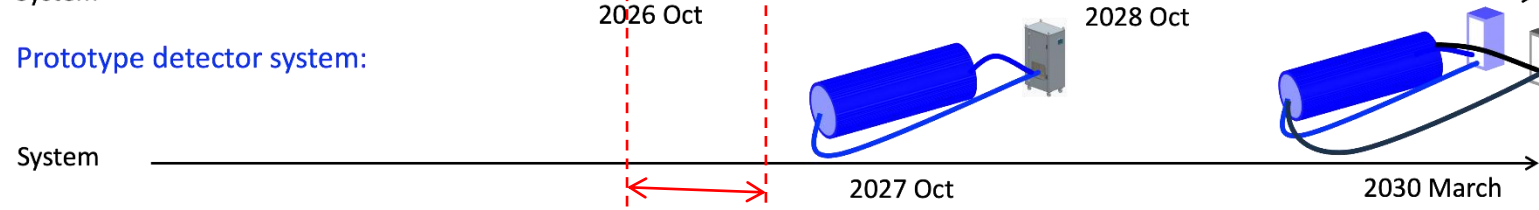
- Beam telescope system:



- Two phase CO_2 cooling system:

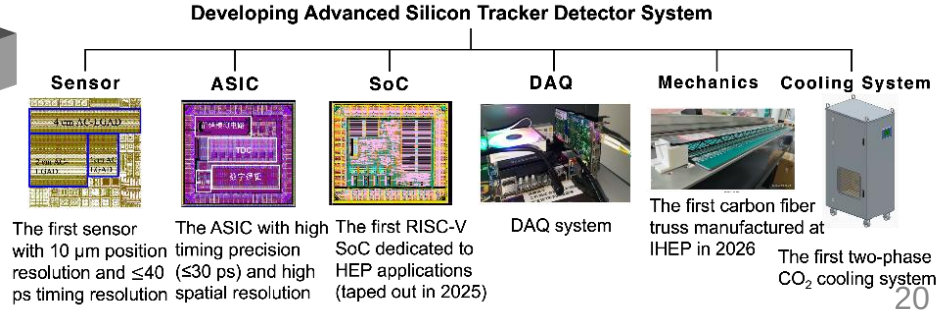


- Prototype detector system:



Q4 2026-Q1 2027

- We are building an integrated research program spanning sensors, dedicated readout electronics, integrated mechanical and cooling system.
  - We have established a complete technology roadmap.
  - Aiming to build core technologies for the next generation of ground- and space-based particle-physics experiments.
- **Plans for Q4 2026–Q1 2027:**
  - **fabricate trench-isolated silicon LGAD;**
  - **test gain-type SiC;**
  - **develop the readout ASIC LATRIC2 (32-channel),**
  - **develop the SoC HERIS-V2;**
  - **build the beam facility and telescope for beam tests;**
  - **develop and commission the two-phase CO_2 cooling prototype; and more.**



Additional Slides

- Semiconductor detectors are technically challenging and have long development cycles. A cross-project research consortium can bring interested institutions together to build an R&D ecosystem, pool resources, collaborate, and share results—turning fragmented efforts into a coordinated program. We welcome domestic partners to work together and advance this detector technology together.
- Alongside our core programs, we will explore semiconductor-detector applications in other fields and welcome cross-disciplinary collaboration.
- We encourage large-scale research facilities to account for beam-test needs and supporting infrastructure，by promoting cross-institutional collaboration, and shared public resources, creating a stronger research ecosystem.
- We welcome you to use BII-PBTS for future beam tests.
- We welcome talented, ambitious students, postdocs, and staff to join the team.

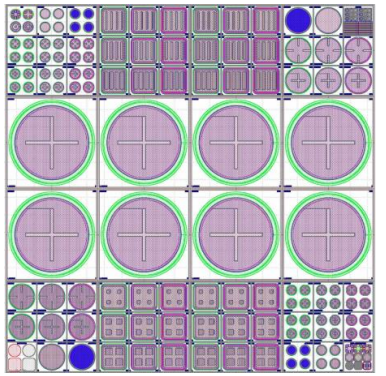
Thank you！

R&D program: Sensors and ASICs

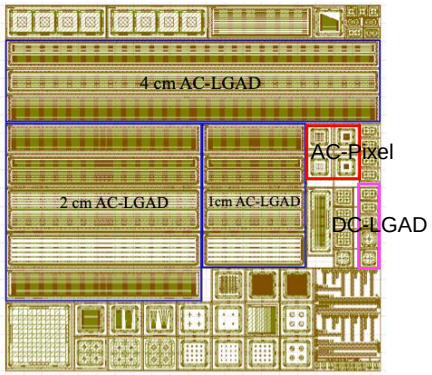
Sensors and ASIC development

- Building a semiconductor-detector R&D program with silicon as the core technology, complemented by coordinated development across materials.
- The end-to-end program covers process development, design, testing, analysis, and system integration.

Gain-type SiC



SiliconLGAD



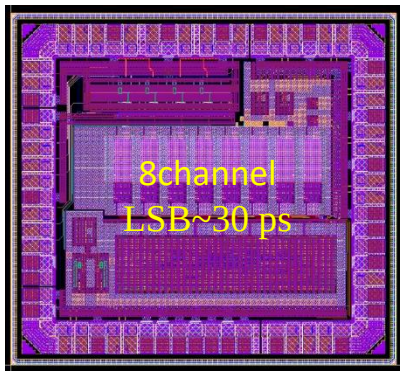
Sensors are moving toward larger formats, higher performance, and lower power.

- The next sensor generation is an important step toward the ultimate performance goals: Reducing capacitance enables larger formats, higher precision, and lower power.

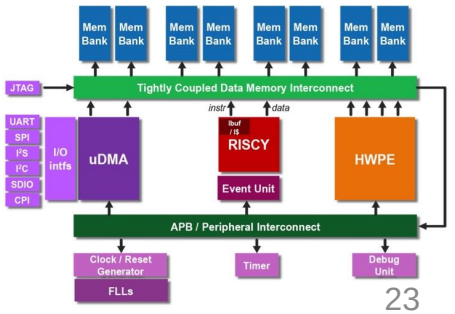
Scaling the high-precision LATRIC readout ASIC to more channels

- The latest32-channel LATRIC2 design is now under way.The next-generation high-performance radiation-tolerantRISC-VSoCHERIS-V2is planned for2027 1: design completion and fabrication submission by January

LATRIC1



HERIS-V2 SoCCore architecture

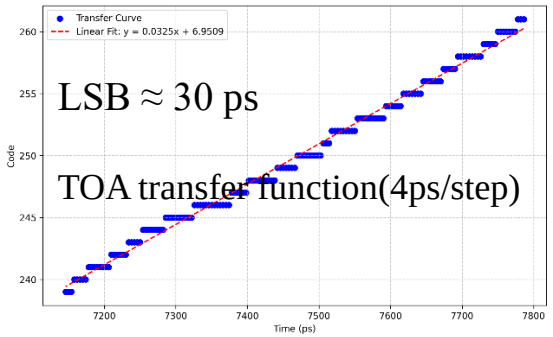


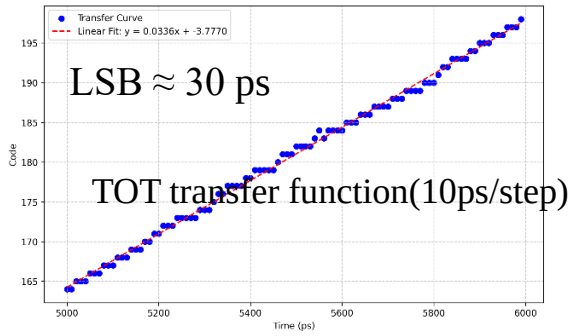
Readout ASICs for semiconductor detectors

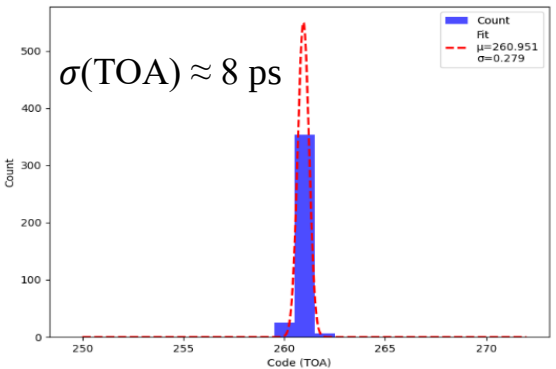
- **Requirements: timing (≤30 ps), spatial resolution (matched to 10 μm μm measurement precision), low power, and high integration (100μm channel pitch, and ≥64channel).**

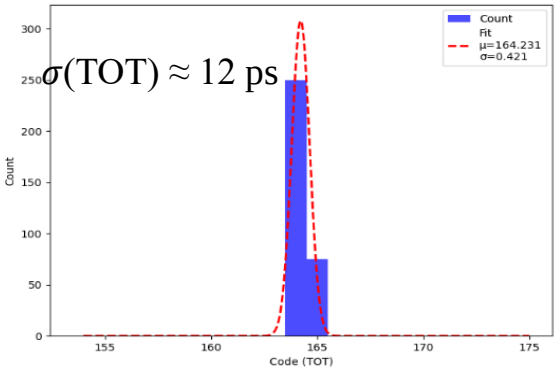
⇨ **The first single-channel prototype, LATRIC0 was designed & fabricated in 2025**

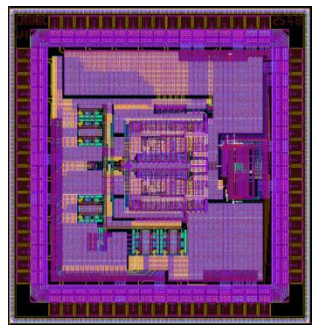
- The ASIC integrates a preamplifier, discriminator, TDC, and serializer for readout.
- The measured time-conversion least significant bit (LSB) is ~30ps. The measured TDC power is 0.1 mA (1.2 V) @ 0.5 MTPS (Mega-Trigger Per Second)，0.3 mA @ 1 MTPS，0.5 mA @ 2 MTPS meeting the design requirements.

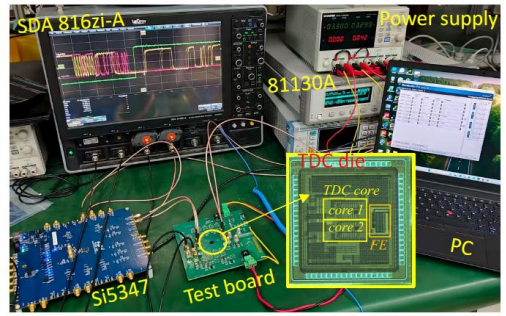






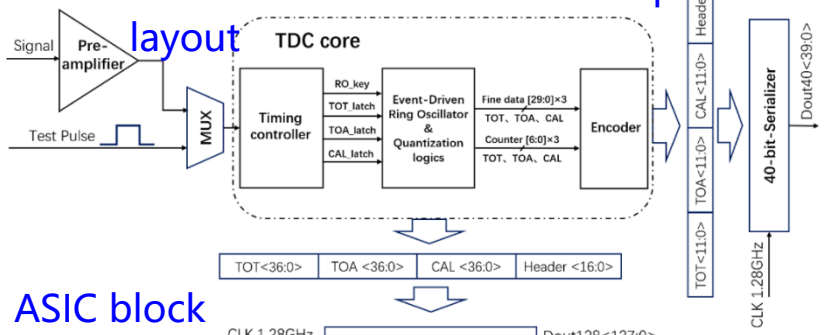






LATRIC0ASIC layout

ASIC test setup

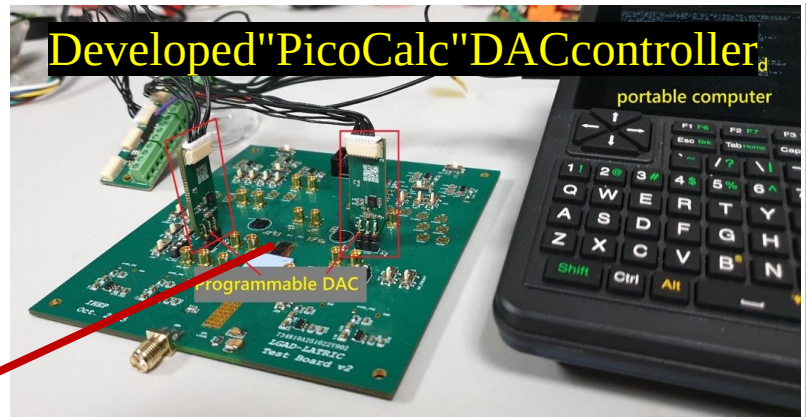


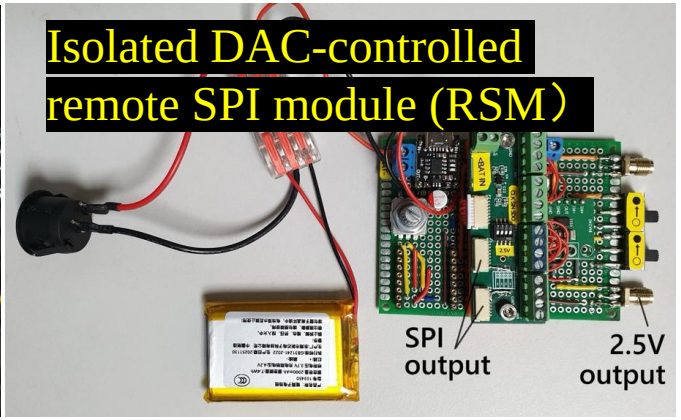
ASIC block diagram

Sensor and readout-ASIC co-testing

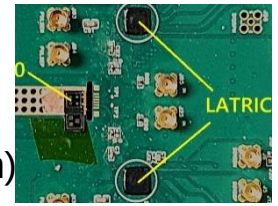
LATRIC readout-ASIC targets:a time resolution better than 30ps, compatible with10 μm spatial resolution, with64 channels or more

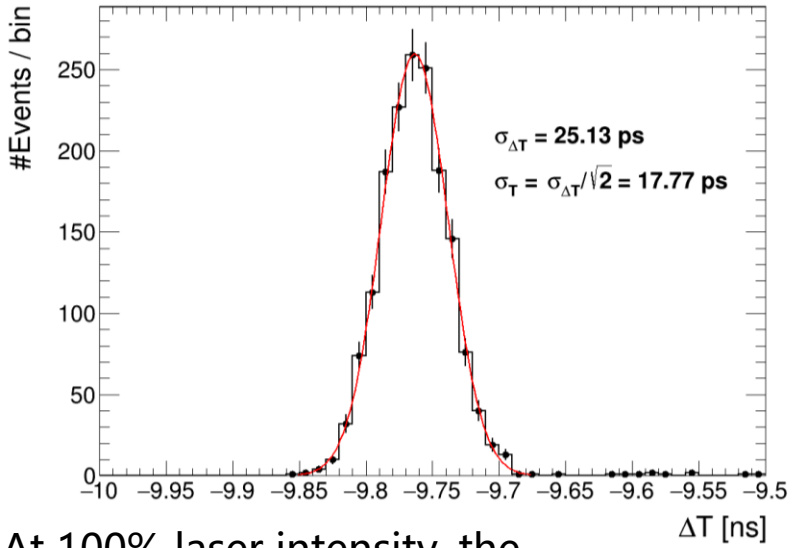
Single-channel LATRIC0 ASIC, designed and submitted for fabrication in 2025, achieved timing resolution better than 30ps, the latest-fabricated 8-channel LATRIC1 is currently under test





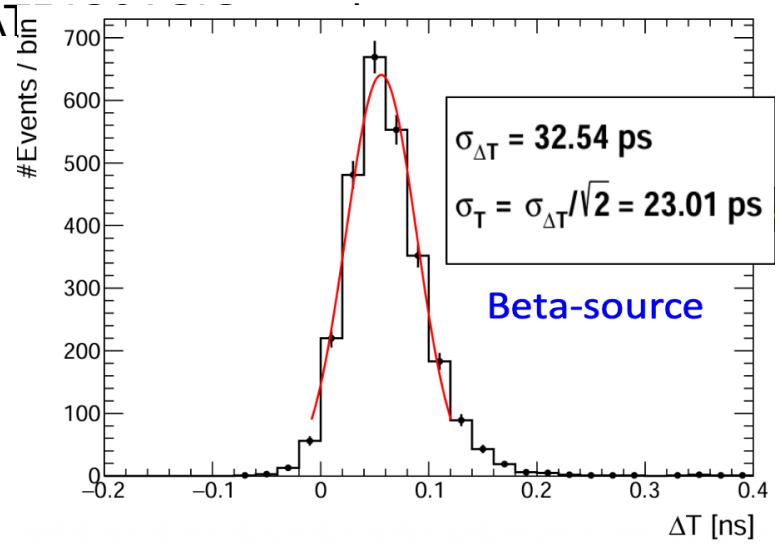
AC-LGAD pixel sensor
(sensor size2.5mm*2.5mm)



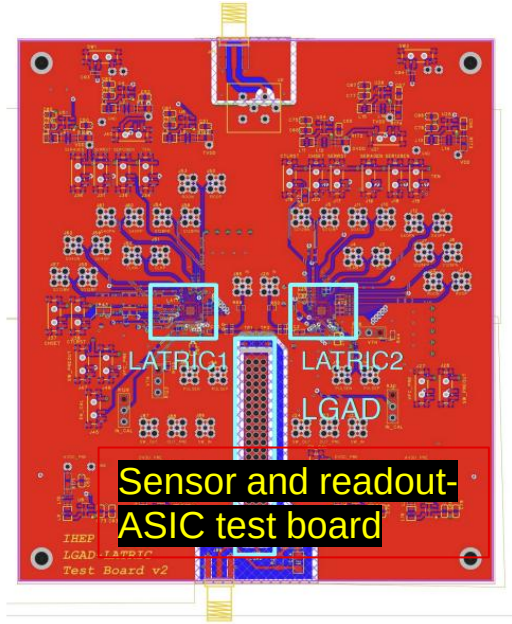


At 100% laser intensity, the measured Ac-LGAD+LATRIC0 achieved a timing resolution of 18ps

Time-difference distribution measured with twoLA



β test: LATRIC0 achieved timing resolution ~23ps



FirstSoC ASIC (HERIS-V1) Successfully tested

- Power on，OpenOCD connected，ROM program running correctly

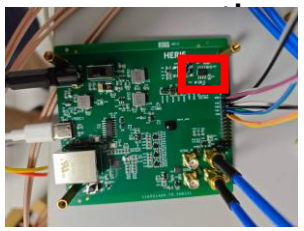
```
PS E:\fpga\Tools\xpack-openocd-0.12.0-6\bin> .\openocd.exe -f .\tinyriscv_JTAG_HS2.cfg
xPack Open On-Chip Debugger 0.12.0+dev-01850-geb6f2745b-dirty (2025-02-07-10:08)
Licensed under GNU GPL v2
For bug reports, read
        http://openocd.org/doc/doxygen/bugs.html
Info : clock speed 1000 kHz
Info : JTAG tap: riscv.cpu tap/device found: 0x1e200a6f (mfg: 0x537 (Wuhan Xun Zhan Electronic Technology), part: 0xe200
, ver: 0x1)
Info : datacount=3 progbufsize=1
Info : Examined RISC-V core; found 2 harts
Info :  hart 0: XLEN=32, misa=0x0
Info : [riscv.cpu] Examination succeed
Info : [riscv.cpu] starting gdb server on 3333
Info : Listening on port 3333 for gdb connections
Info : Listening on port 6666 for tcl connections
```

串口调试助手 + TCP/UDP

端口名：COM5
波特率：115200
数据位：8
校验位：None
停止位：1
RI DSR CTS DTR RTS

```
--- RISC-V Bootloader Started ---
Initializing SD card on SPI channel 1...
SD_INIT: Failed on CMD0
!!! FATAL: SD Card initialization failed. Halting. !!!
Target RAM size: 14336 bytes. Need to read 28 blocks from SD card.
Starting to copy data from SD:@0x0 to RAM:@0x10000000...
```

- On-board EEPROM， I²C interface operating



```
int main() {
    uart_init();
    xprintf("\n=== I2C Master Final Test Program ===\n");
    i2c_init(50000000, 100000);

    uint16_t test_addr = 0x1234;
    uint8_t test_data  = 0xAC;

    eeprom_write_byte(test_addr, test_data);
    uint8_t read_back = eeprom_read_byte(test_addr);
```

UARTOutput

```
== I2C Master Final Test Program ===
[I2C] Write: Addr=0x1234 Data=0xAC
  > Config Check: Slave=0x53, Addr=0x1234, Data=0xAC
[I2C] Read: Addr=0x1234
```

Runs again after power cycling

UARTOutput

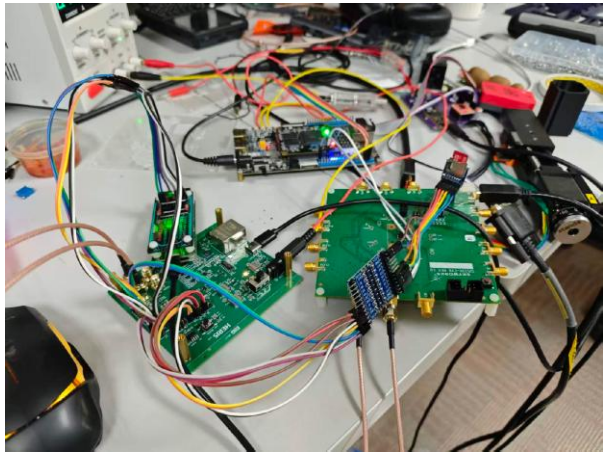
```
int main() {
    uart_init();
    xprintf("\n=== I2C Master Final Test Program ===\n");
    i2c_init(50000000, 100000);

    uint16_t test_addr3 = 0x0123;
    uint8_t read_back3 = eeprom_read_byte(test_addr3);
    uint16_t test_addr2 = 0x1234;
    uint8_t read_back2 = eeprom_read_byte(test_addr2);

    xprintf("[I2C] Verification: Read1 0x%02X, Read2 0x%02X\n", read_back3, read_back2);
```

```
=== I2C Mater Final Test Program ===
[I2C] Read: Addr=0x0123
[I2C] Read: Addr=0x1234
[I2C] Verification: Read1 0xFF, Read2 0xAC
```

- ROM and SD card，SPI module operates correctly

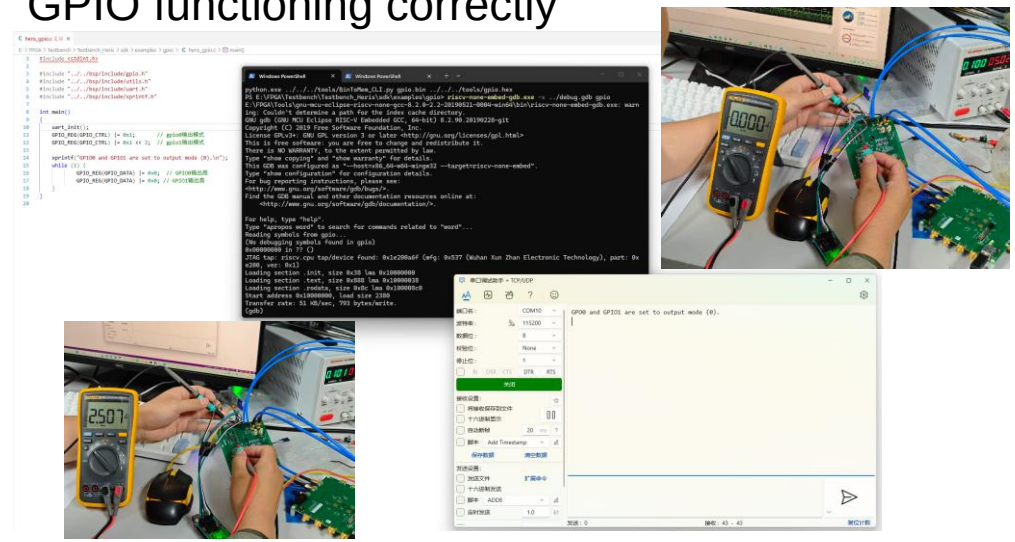


串口调试助手 + TCP/UDP

端口名：COM11
波特率：115200
数据位：8
校验位：None
停止位：1
RI DSR CTS DTR RTS
关闭
接收设置：
将接收保存到文件
十六进制显示
自动断帧 20 ms
脚本 Add Timestamp
保存数据 清空数据

```
--- RISC-V Bootloader Started ---
Initializing SD card on SPI channel 1...
SD Card on SPI CH-1 initialized successfully.
SD Card initialized successfully.
Target RAM size: 14336 bytes. Need to read 28 blocks from SD card.
Starting to copy data from SD:@0x0 to RAM:@0x10000000...
.......
Data copy complete.
Bootloader finished. Jumping to application at 0x10000000...
hello world
```

- GPIO functioning correctly



HERIS-V1Performance

Test conditions

CoreMark Benchmark Statistics

Test Configuration

Item	Value
CPU Architecture	RV32IM Softcore
Benchmark	CoreMark
Iterations	100
Compiler	GCC 8.2.0
Optimization	`-O2 -funroll-loops -finline-functions`
Memory Mode	STATIC
Assumed Timer Clock	50 MHz

Rated frequency: 50 MHz,
maximum operating frequency:150 MHz

Performance (CoreMark/MHz):

- **ARM Cortex-M0/M0+**:approx. 0.9 ~ 1.0
- **PicoRV32 (minimalist RISC-V)**: approx. 0.5 ~ 0.8
- **HERIS-V1:1.75 (silicon and FPGA scores agree)**
- **VexRiscv / Hummingbird E203**:approx. 1.5 ~ 2.2
- **ARM Cortex-M3 / M4**:approx. 3.3 ~ 3.4

HERIS-V1 benchmark score

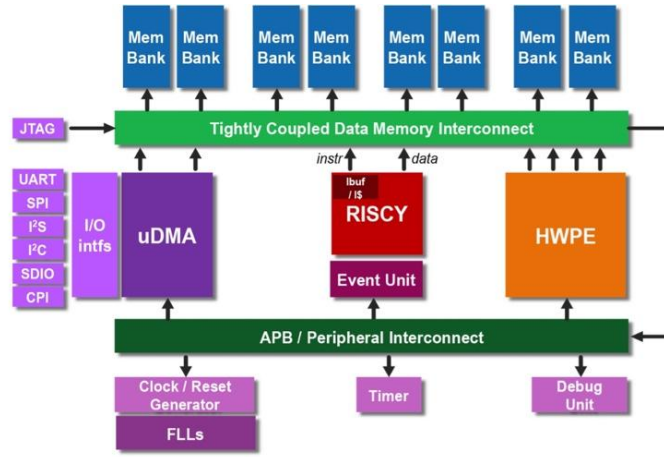
CoreMark Results Summary

Run	Total Ticks	Time (s)	CoreMark	CoreMark/MHz
1	47,140,681	0.943	106.07	2.121
2	57,254,527	1.145	87.33	1.747
3	57,254,216	1.145	87.33	1.747
4	57,254,809	1.145	87.32	1.746
5	57,254,522	1.145	87.33	1.747
6	57,254,148	1.145	87.33	1.747
7	57,255,302	1.145	87.31	1.746
8	57,256,313	1.145	87.30	1.746
9	57,253,503	1.145	87.33	1.747
10	36,131,525	0.723	138.38	2.768
11	57,254,188	1.145	87.33	1.747
12	57,254,522	1.145	87.33	1.747
13	57,254,203	1.145	87.33	1.747

FPGAbenchmark score

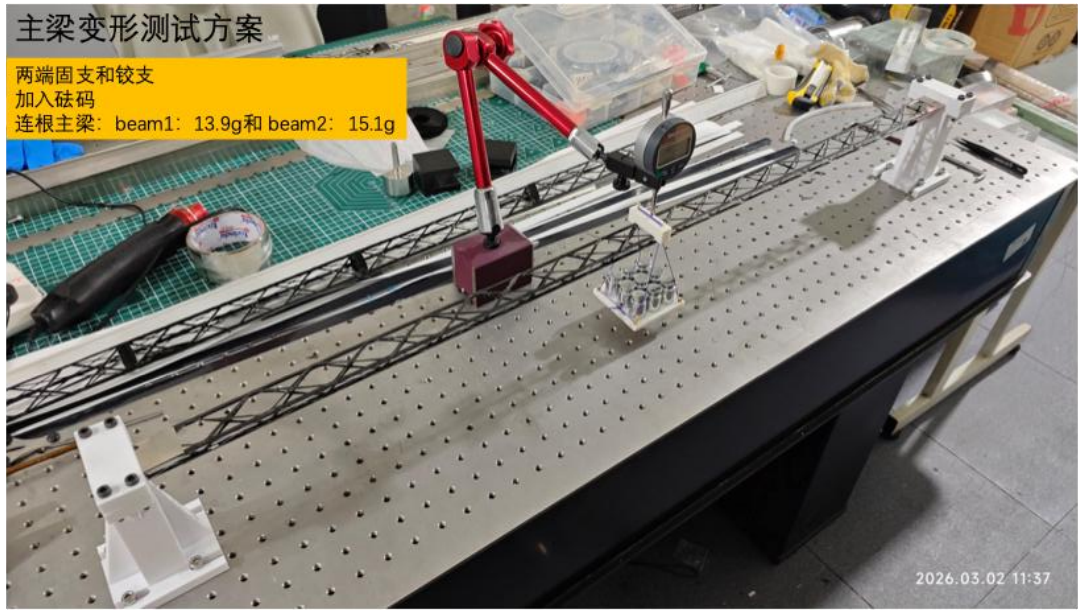
#	Total Ticks	CoreMark	CoreMark/MHz
1	264,551,913	18.90	0.378
2	25,685,150	194.66	3.893
3	55,131,135	90.69	1.814
4	29,876,551	167.35	3.347
5	57,253,579	87.33	1.747
6	57,243,713	87.35	1.747
7	29,906,285	167.19	3.344
8	57,254,426	87.33	1.747
9	41,493,461	120.50	2.410
10	46,612,237	107.27	2.145
11	54,497,797	91.75	1.835
12	48,237,510	103.65	2.073
13	28,275,053	176.83	3.537
14	57,253,726	87.35	1.747
15	13,635,777	366.68	7.334
16	25,475,668	196.27	3.925
17	57,253,893	87.35	1.747
18	57,253,672	87.36	1.747
19	57,253,673	87.36	1.747
20	26,854,754	186.19	3.724
21	57,250,967	87.40	1.748

⇨ **The next-generationHERIS-V2 will use the PULPissimo SoC platform for its core architecture, with RISCY/Ibex cores. Radiation hardening will combinelogic layerTMR (triple modular redundancy)+memory layer ECC (error-correcting code)+system-level software recovery" in a layered radiation-hardening architecture, alongside software-level self-recovery. Design completion and fabrication submission are planned for 20271 design completion and fabrication submission in January**

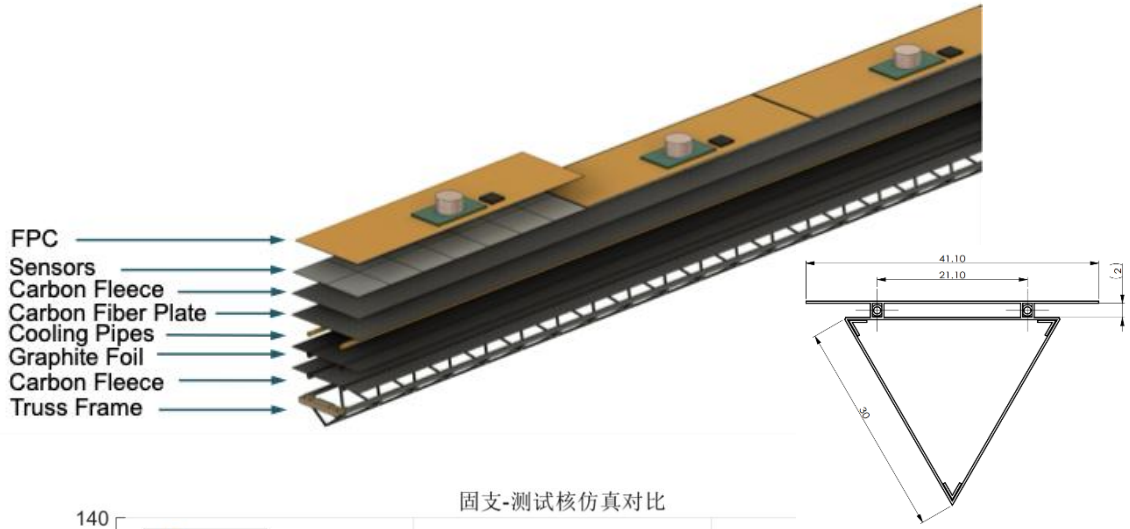


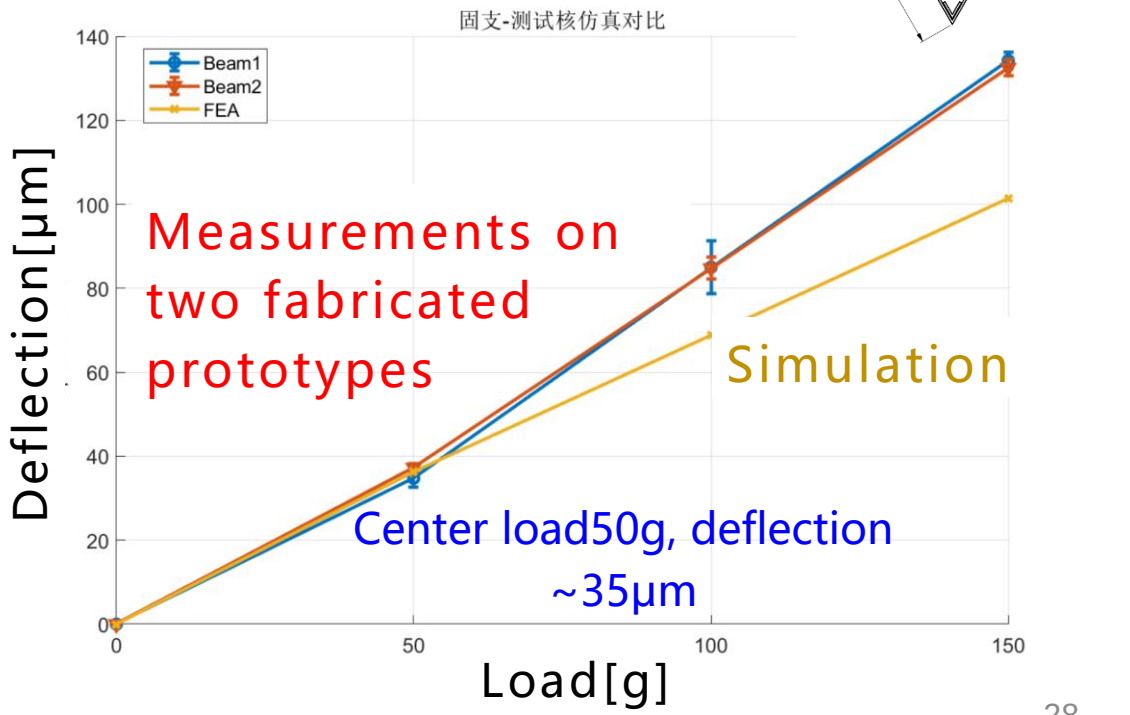
Carbon-fiber composite design and manufacturing

- **Topology optimization is guided by modeling and simulation. In parallel with mold and process development, we are advancing high-strength carbon-fiber prepreg layup, tow winding, and integrated hot-press curing.**
- Key challenges include high modulus, matching thermal expansion across materials, structural flatness, and demolding. Mechanical and optical measurements provide systematic characterization, **building end-to-end expertise in design, process development, and performance validation.**

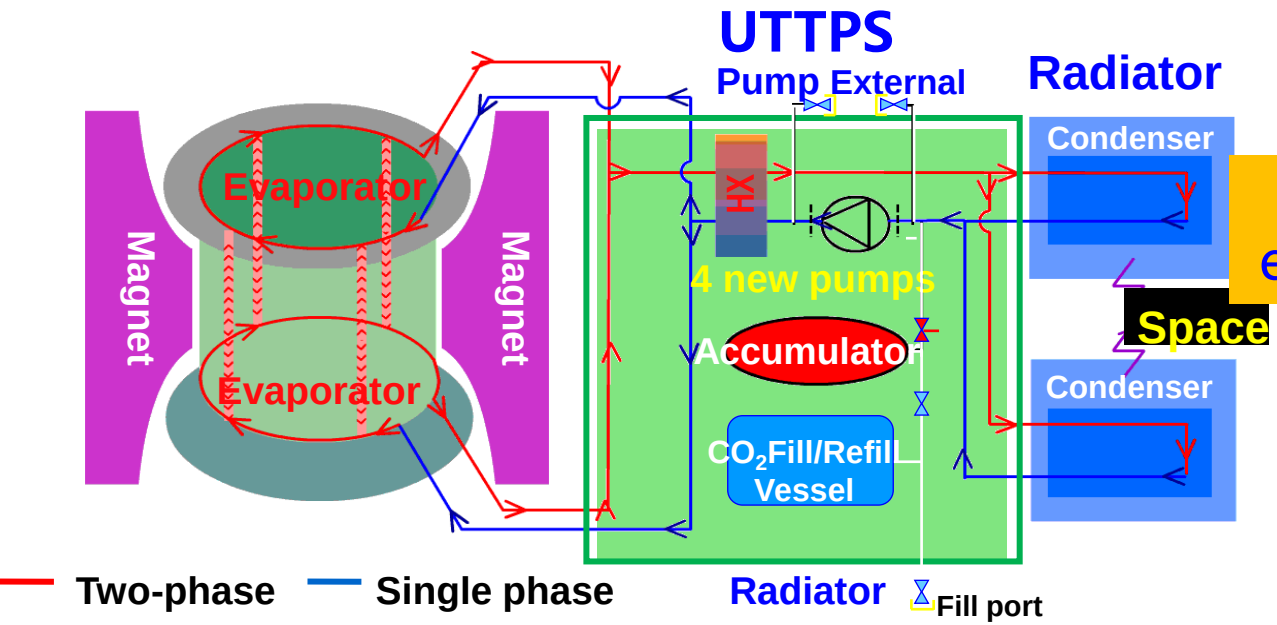


In-house1m carbon-fiber structural prototype (mass:15g): deformation under load

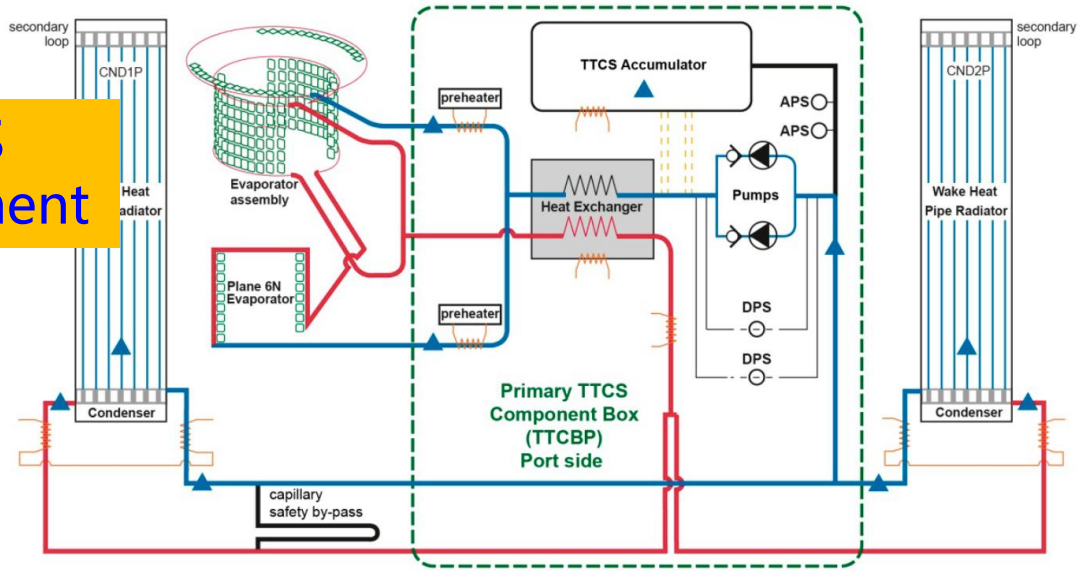




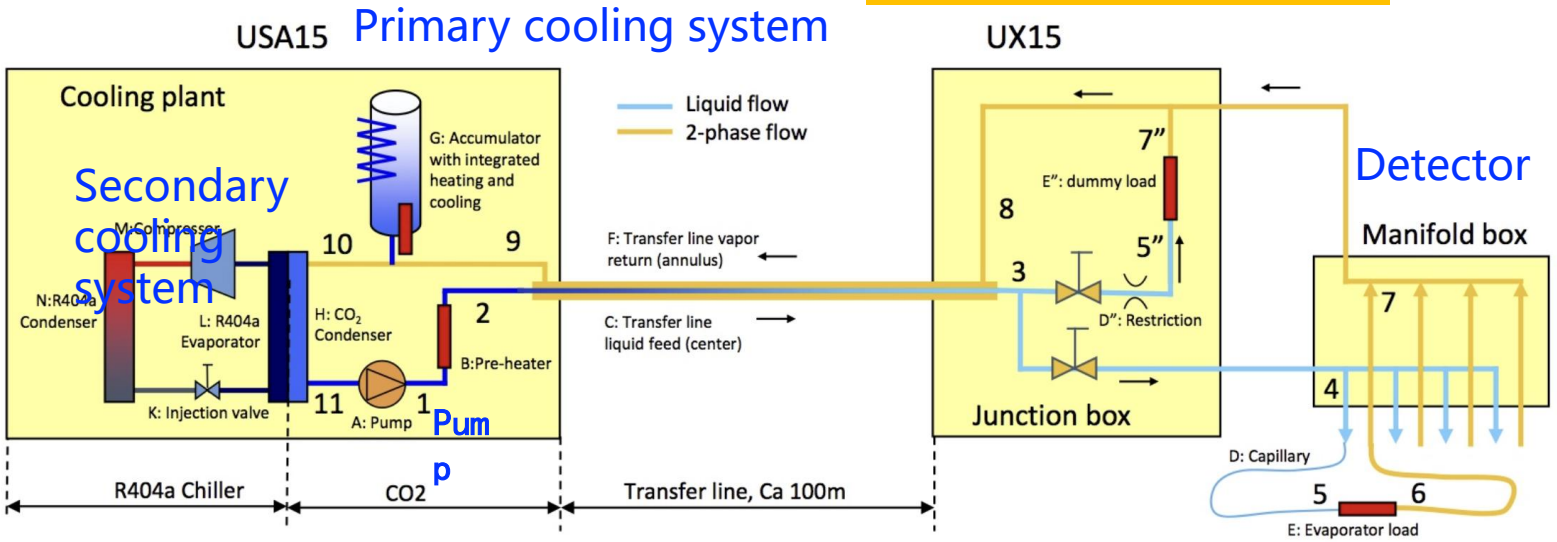
Cooling technologies for semiconductor detectors



AMS experiment



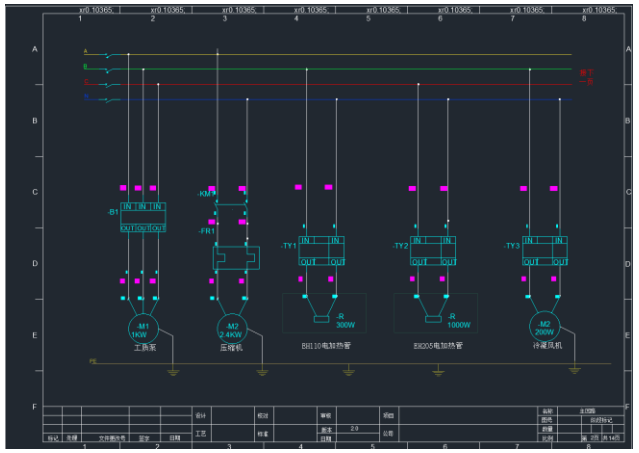
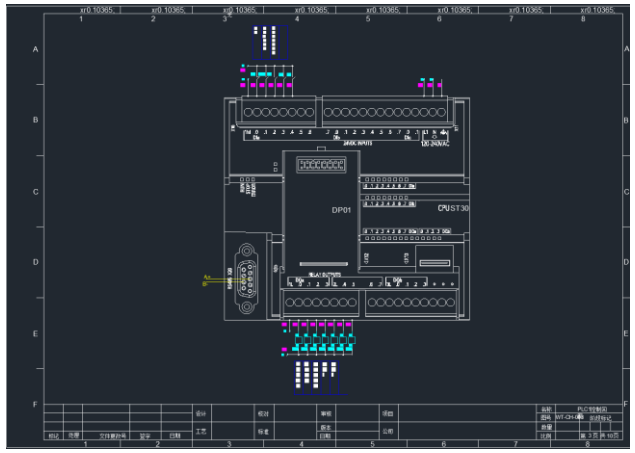
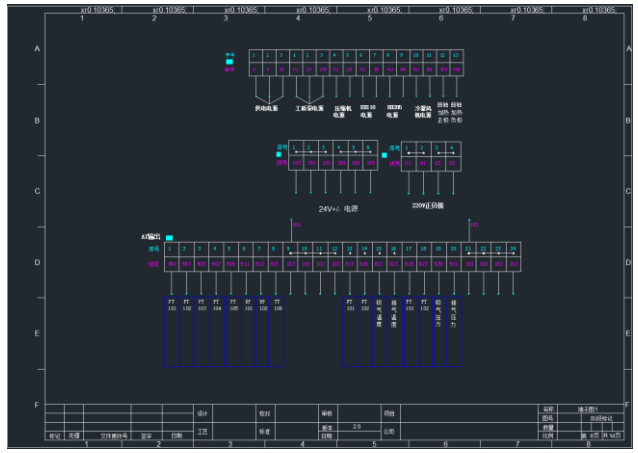
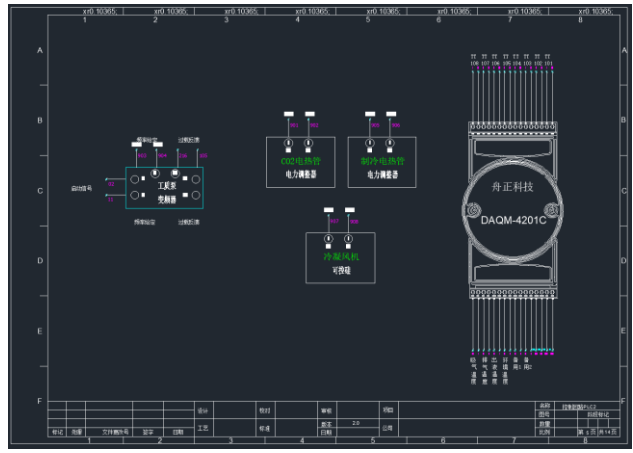
LHC experiment



Two-phase CO_2 cooling is key technology for semiconductor trackers in both future space-and ground-based experiments.

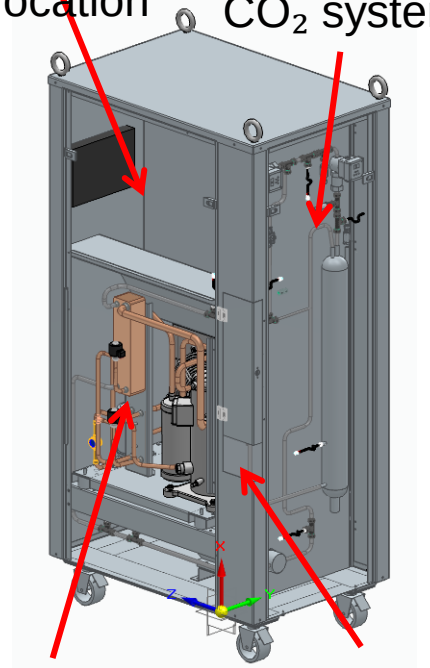
Beyond particle physics, this technology can cool space payloads, electronic equipment, and other high-power-density devices.

➢ System electrical

Control cabinet location

CO_2 system



Refrigeration unit

Load connection

➢ System components



Compres



Plate heat



Expansion-



Filter-R404A



Sight glass-R404A



Oil separator



Vapor-injection



Temperature sensor



Heater



Pressure sensor



Filter-CO2



Differential-pressure sensor



Flow meter

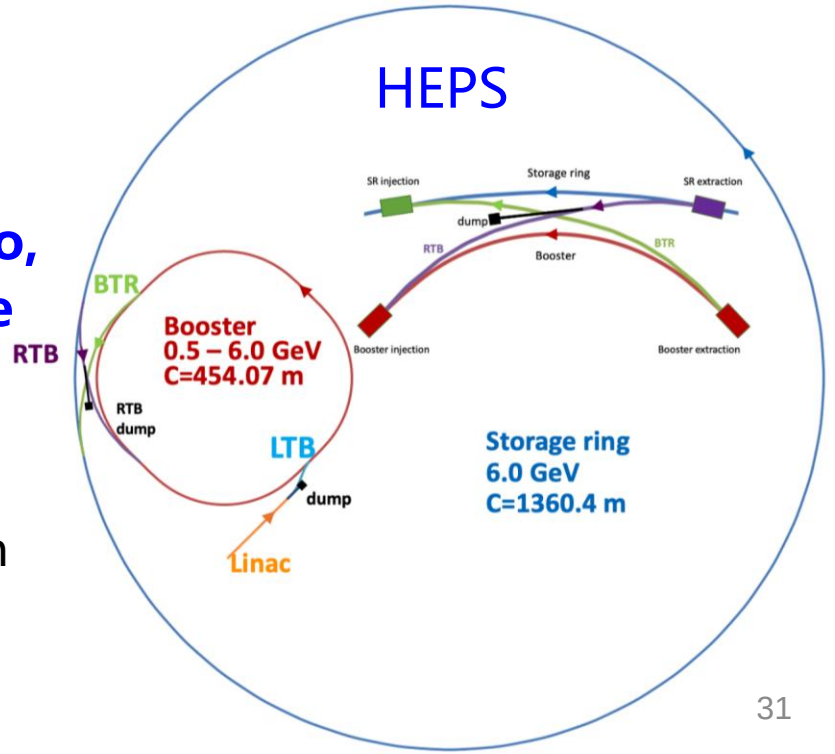


Sight glass-CO2

Developing a beam-test facility

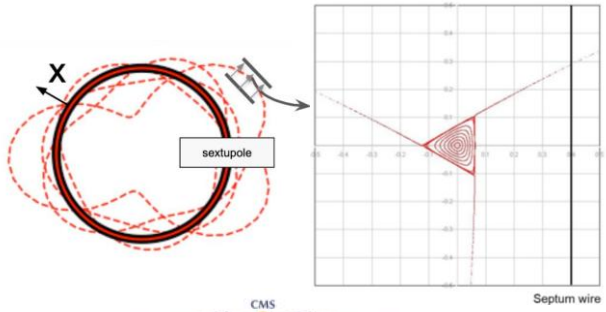
- **Sensors andASIC are ready for beam tests. Requirements include:**
  - **High momentum**(>1 GeV/c) to limit multiple-scattering effects on spatial resolution. For MIP-equivalent dE/dx characterization, proton beams require higher momentum than electron beams (β ~ 1), with proton momentum above>2 GeV/c （ β>0.9 ）
  - **Small momentum spread:** Δp/p<10%
  - **Slow-extracted beam or low-density pulsed beam:**<100 particles/cm^2/bunch
  - **Beam spot size:**>1 mm^2

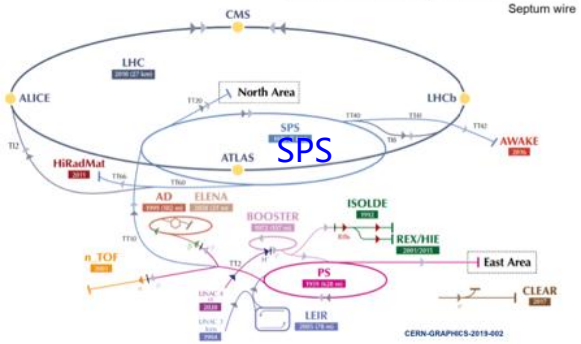
- **In the absence of a suitable high-energy beam-test facility in China, the team began planning a beam-test platform a year ago, focusing on feasibility studies at the High Energy Photon Source (HEPS) and the Beijing Electron–Positron Collider (BEPCII):**
  - **HEPS Linac:**from the linac 500MeV/c electron beam
  - **HEPS RTB Dump:**from the storage-ring booster 6GeV/c electron beam
  - **BEPCII-PWFA:** using the linac beamline to the PWFA station 2 GeV/c electron beam



Design considerations for the beam-test facility

- **A key challenge in using existing accelerators for beam tests is reducing particle density per bunch. Dedicated beam-test facilities such as SPS, PS, ELSA facilities typically use slow extraction:**
  - **In-ring storage and resonant-extraction optics:** configure and tune quadrupole and sex-tupole magnets, increasing transverse amplitude so particles gradually cross the boundary into the extraction channel.
  - **Dedicated extraction channel and beam control:** Configure thin electrostatic and magnetic septa, external transport line and beam diagnostics and control systems
  - **Additional considerations for electron rings:** Assess the impact of synchrotron-radiation damping, quantum excitation, and RF bunch structure on extraction.



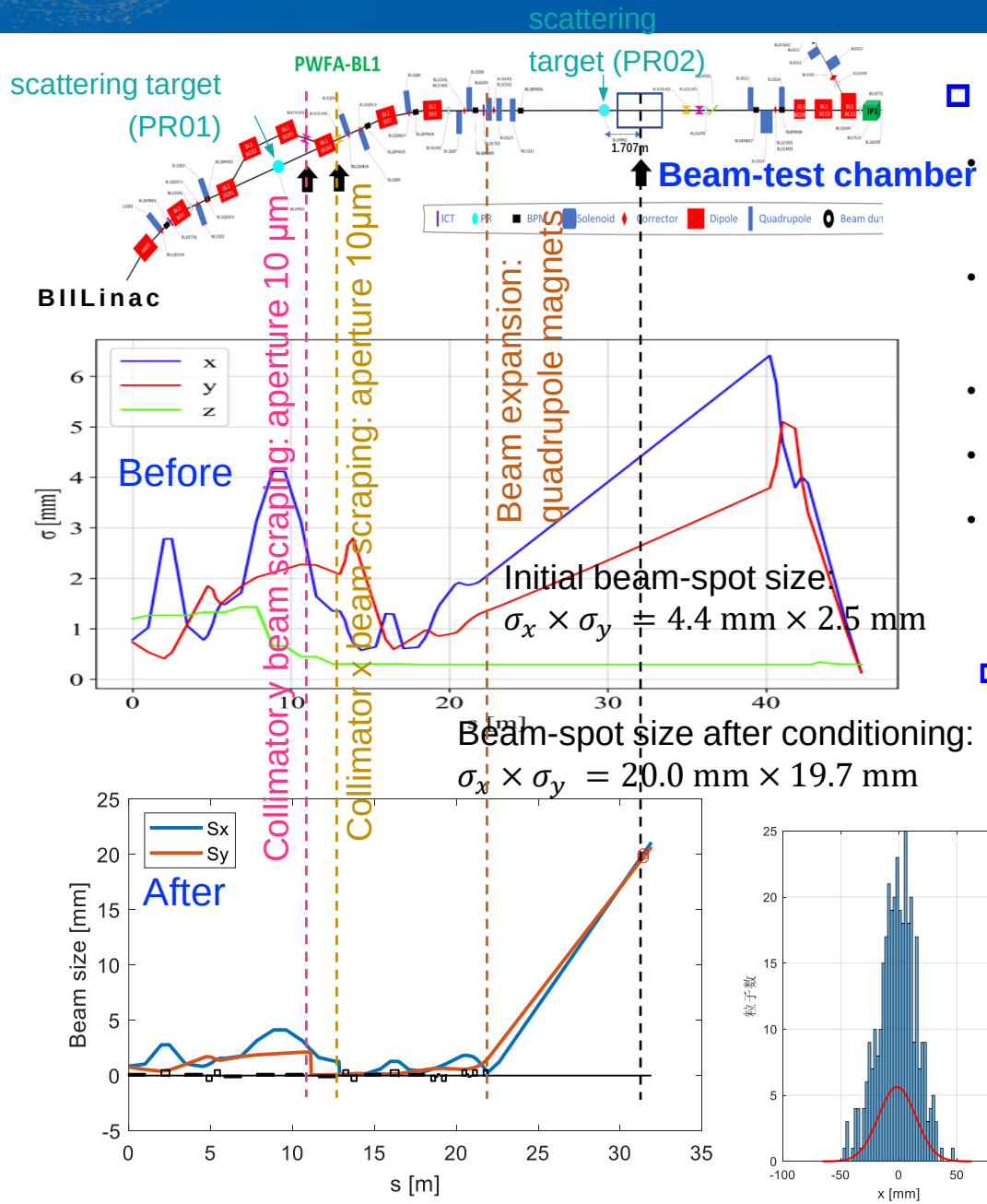


SPS

	Comparison of existing pulsed-beam facilities (without a slow-extraction configuration)		
Beam parameter	**HEPSLinac**	**HEPS RTBDump**	**BEPCIILinac**
Beam energy	0.5GeV	6GeV	2GeV
Energy spread	<0.5%		
Bunch charge	7nC(4.4×10^{10}) e-	5-7nC ($3.1\text{-}4.4\times10^{10}$)e-/Current 14.4nC ($9\times10^{10}$) e-/Design target	2nC (1.3×10^{10}) e- 0.05nC (3×10^{8}) e+
Bunch repetition rate	50Hz	0.5Hz	50Hz
Bunch length	5 ps	80-400 ps	10ps
Facility constraints	Low energy, extensive site modifications required	Very limited space, limited beam-conditioning capability	**Can leverage existing PWFA beamline infrastructure**

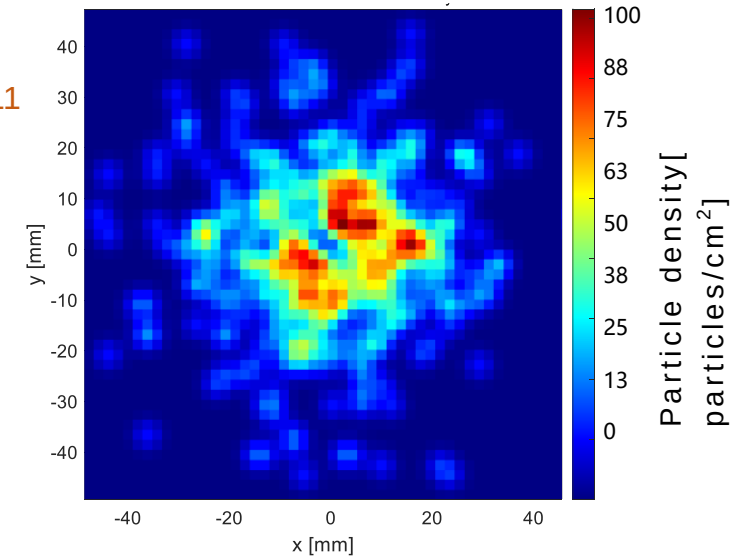

HEPSRTBDump

BII-Linac into PWFA front end Beam-conditioning feasibility study



Existing beam-conditioning equipment:

- Beam scraping: BL1COLV01 minimum aperture ~10μm (y)
  BL1COLH01minimum aperture ~10 μm (x)
- Beam expansion with quadrupoles: Q07-Q11
  Maximum magnet strength K=3.43 m^{-2}
- Scattering targets: PR01-PR02
- Positron beam: particle density is ~1/40
- Reduce particle count by adjusting the electron gun

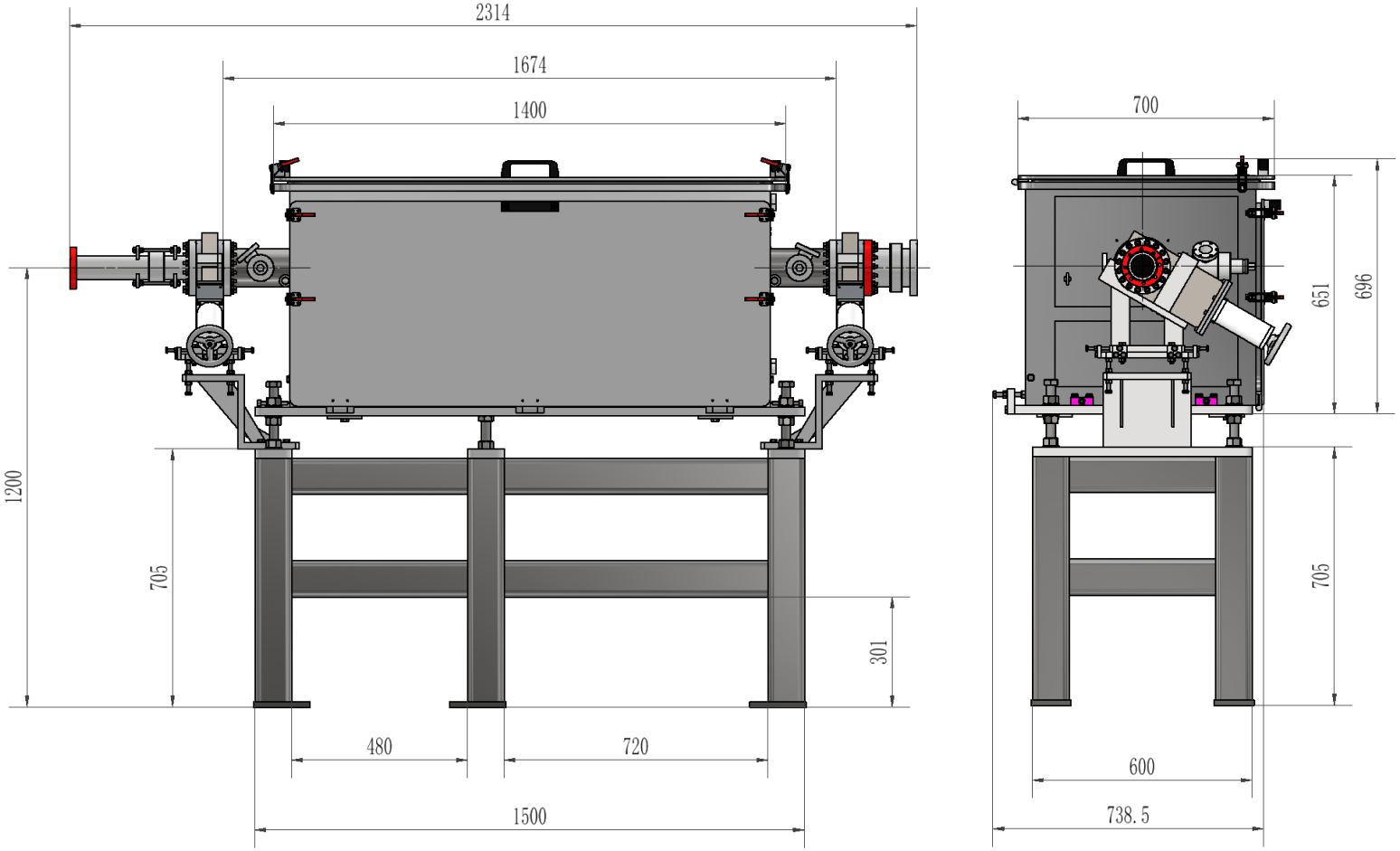


Beam-physics simulation:

Scraping with a collimator (aperture 10μm)+ quadrupole beam expansion		
	Before	**After**
Bunch charge	0.05nC (3×10^8 particles) e+	0.18fC(1×10^3 particles) e+
Beam spot size ($\sigma_x \times \sigma_y$)	4.4mm×2.5mm	20.0mm×19.7mm
Beam-center Particle density	~10^9 particles/cm^2	~100 particles/cm^2
Additional adjustment options: e-gun tuning, scattering targets, and use particles at the transverse beam edge (adjusted in the chamber)		

Beam-test enclosure:

- Dimensions:1.4m×0.7m×0.65m
- Houses the detector mounting stages and provides power and communications, electromagnetic and optical shielding, and cooling.



Mechanical design of the beam-test chamber

Top cover of telescope enclosure







Beam test telescope design

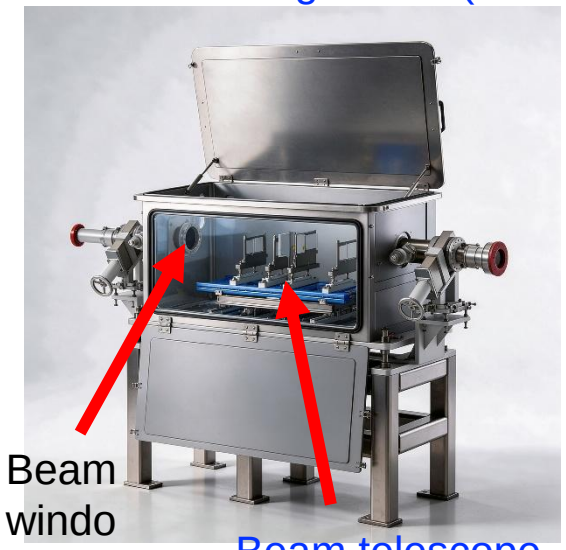
Beam-off configuration (vacuum chamber connected inside the enclosure)



Vacuum-chamber support

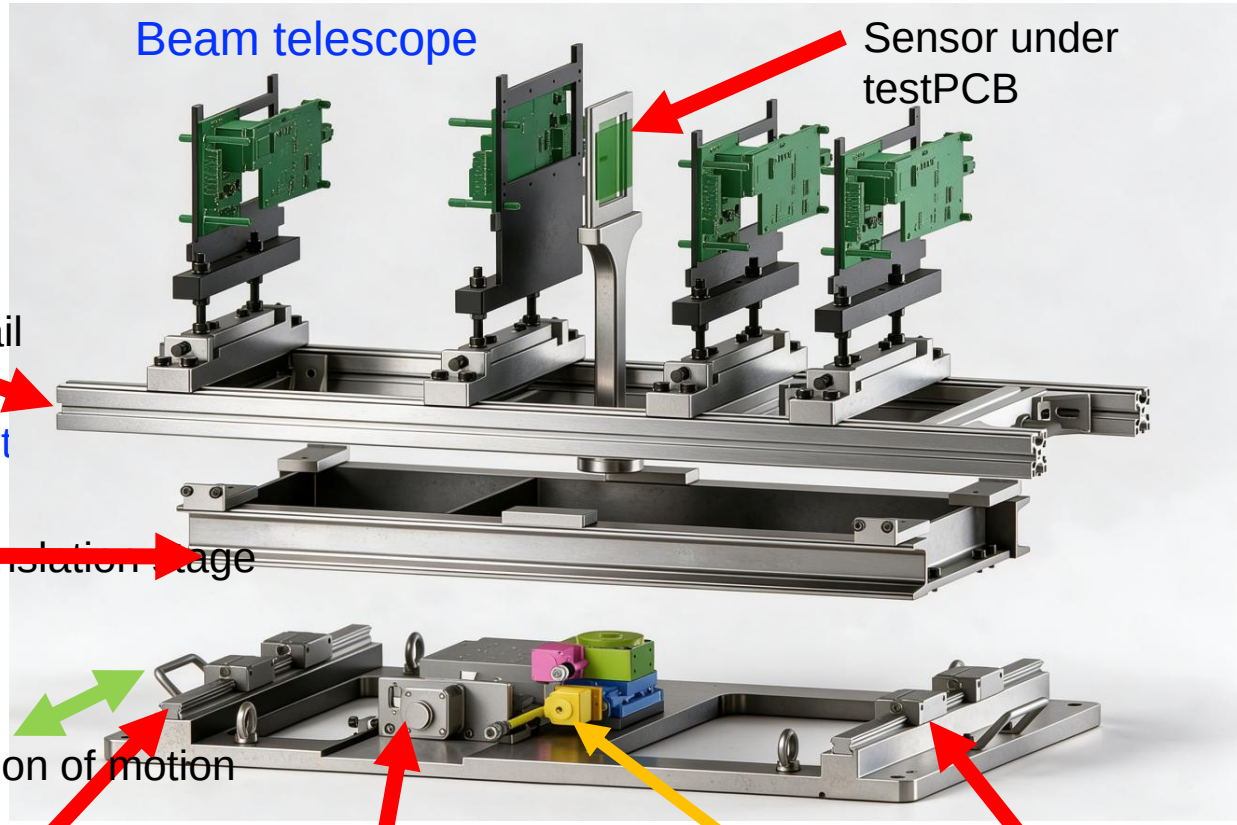
Bellow Vacuum-chambers

Beam-test configuration (vacuum chamber disconnect

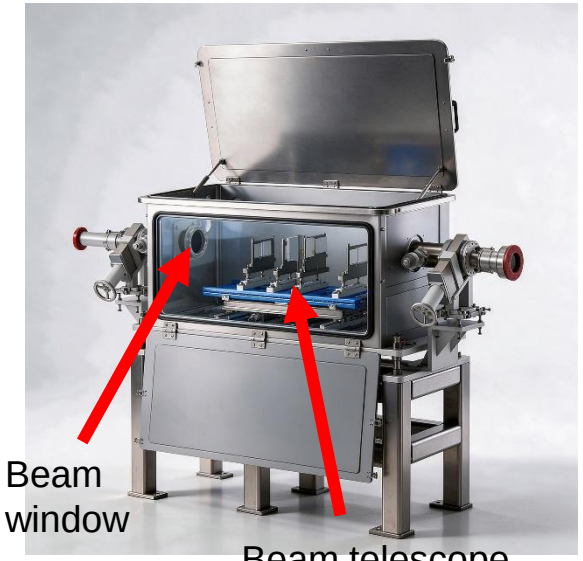


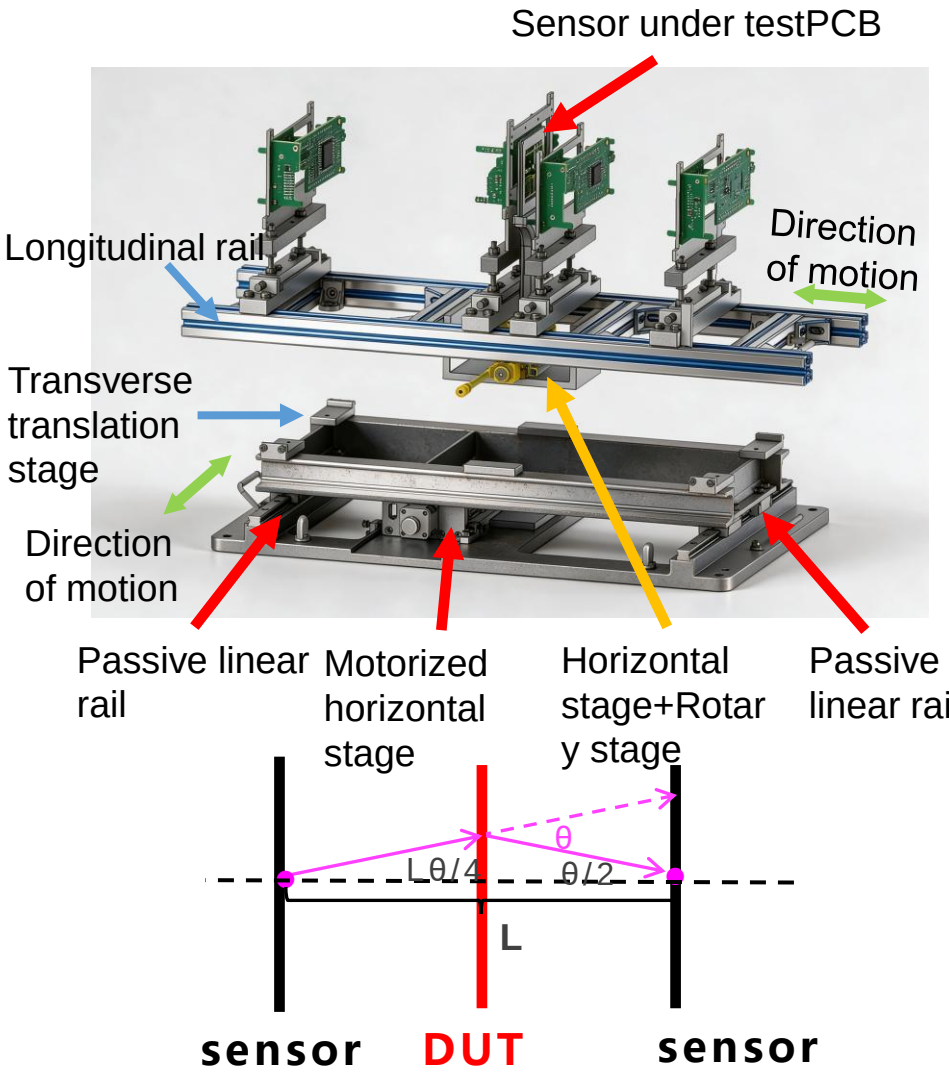
Beam window

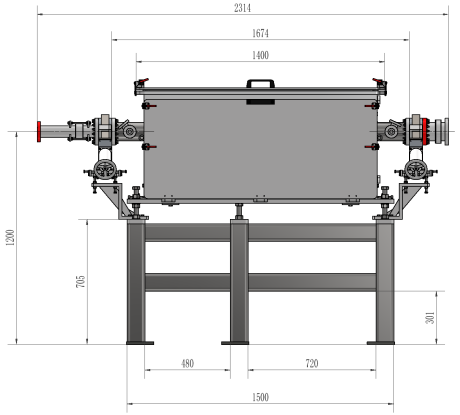
Beam telescope



PEPCII-PWFA Beam-test facility (BII-PBTS) platform







Central sensor spacing: 2 GeV electron beam traversing 750 μm of silicon, with a scattering angle of Θ~0.5mrad, the spread after 1cm is approximately 5 μm. The total spacing between the three central sensors, L must satisfy ΔS=LΘ/4<5μm, i.e.L<4cm

□ BII-PBTSThe BII-PBTS facility makes full use of existing infrastructure. Its modular chamber and beam-telescope systems provide a reusable platform for future beam tests.

⇨ **Advantages:**

- Provides 2GeV low-energy-spread electron beam with adjustable particle density, supporting beam tests of many detector types
- Located in IHEP Hall 10, with well-developed infrastructure for convenient experiments
- Can operate in parallel with BESIII collider operations, enabling independent beam tests
- Beam time will be allocated through an application process, and made available to research groups and individuals requiring beam access.

⇨ **Limitations:**

- The beam-energy range is limited, making it less suitable for wide-range calibration (e.g., calorimeters).
- The chamber has been designed to maximize usable space, but site constraints currently limit it primarily to detectors smaller than<1 m detector tests