The IDEA Silicon Tracker

The 2026 International Workshop on the High Energy Circular Electron Positron Collider
Shanghai, 23 October 2026

Attilio Andreazza - Università di Milano and INFN
For the IDEA Study Group

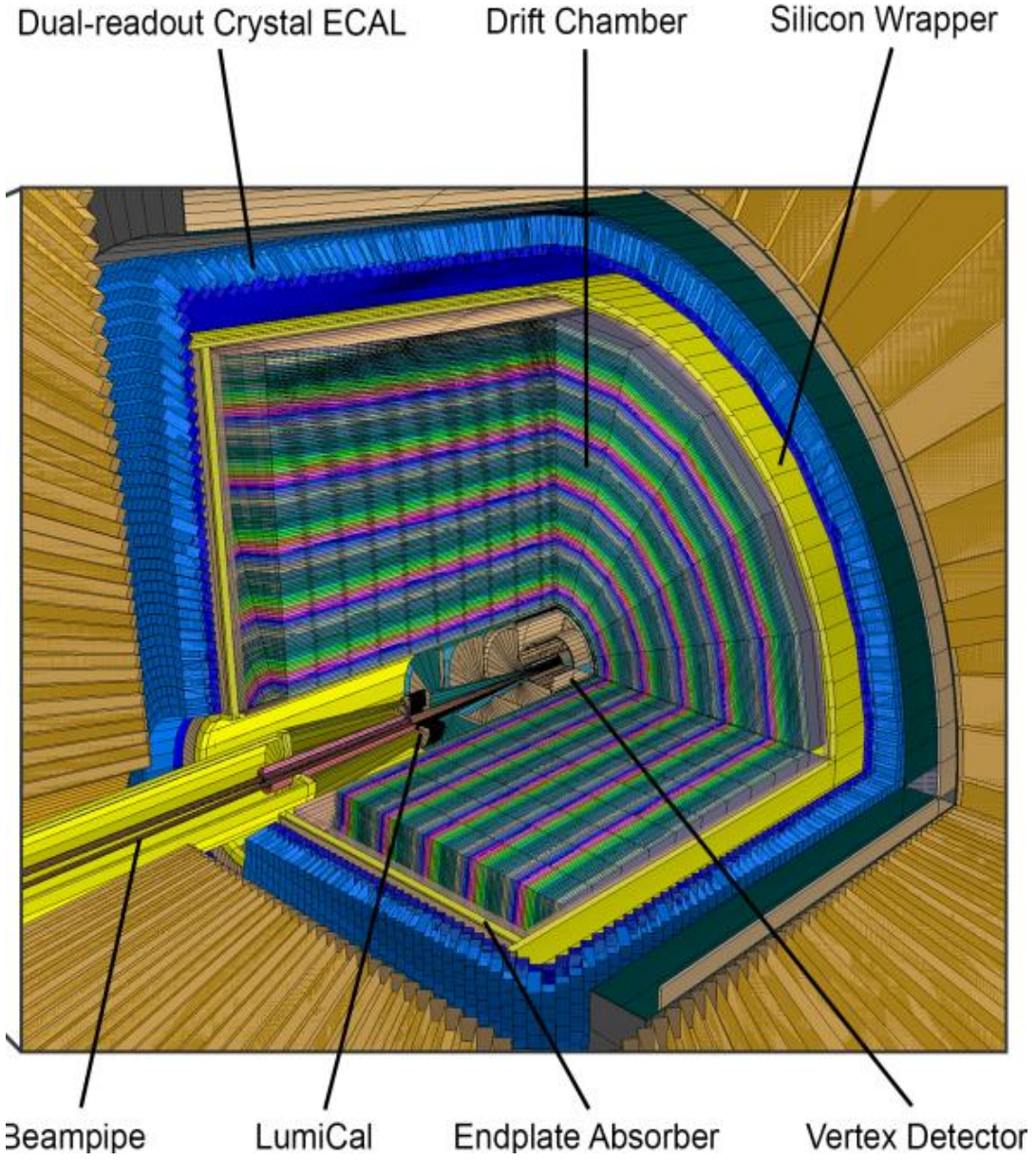




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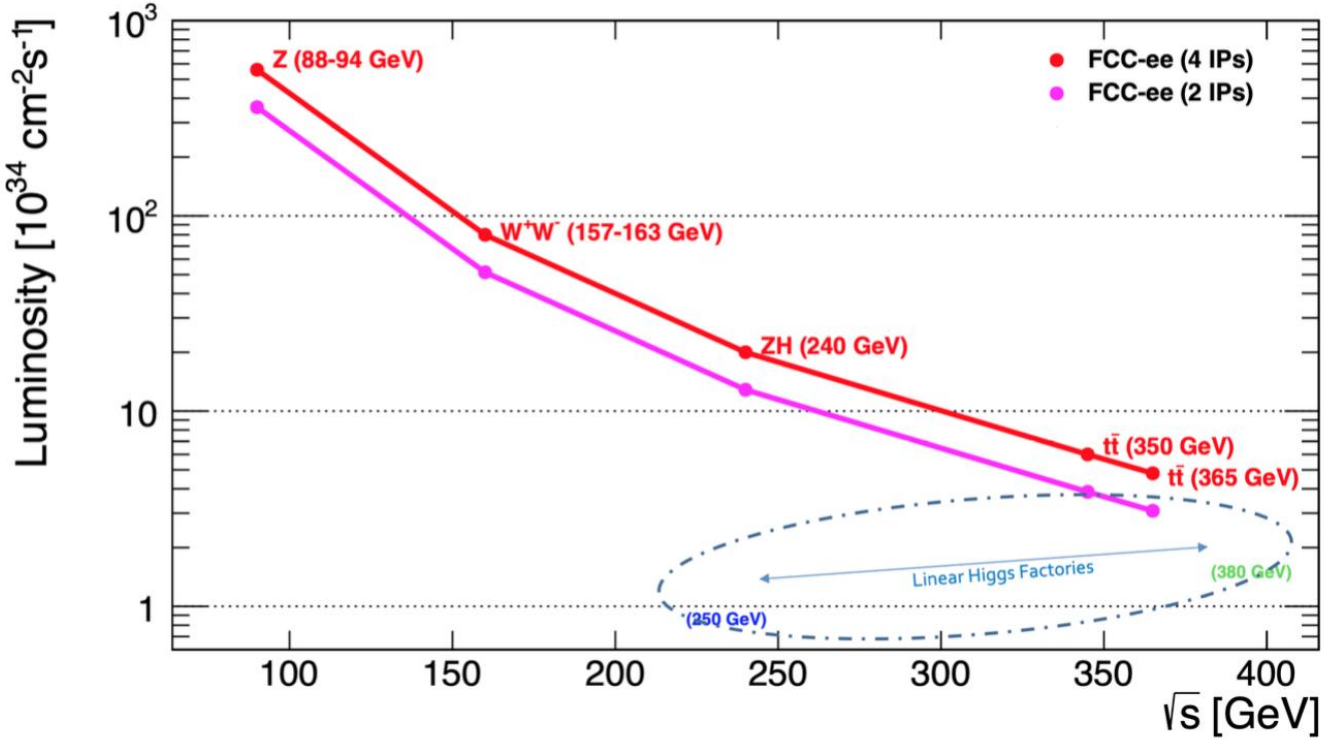
Outline

- Requirements at FCC-ee
- The IDEA detector concept
- Silicon tracking in IDEA:
  - Technologies
  - Inner Vertex Detector
  - Outer Vertex Detector
  - Silicon Wrapper
- Tracker performance
- Conclusions and outlook



Physics requirements at FCC-ee

- Rich physics program at FCC-ee
  - Operation at the Z pole, WW threshold, ZH and tt threshold
- Performance driven by Higgs recoil mass, heavy-flavour and tera-Z physics
- Operating condition (data rate, background)
  from the high-luminosity at the Z pole ($L > 10^{36}\ cm^{-2}s^{-1}$); solenoid field limited to 2 T



- Impact parameter resolution

$$\sigma_d < 3\ \mu m \oplus \frac{15\ \mu m \cdot GeV}{p \sin^{3/2}\theta}$$

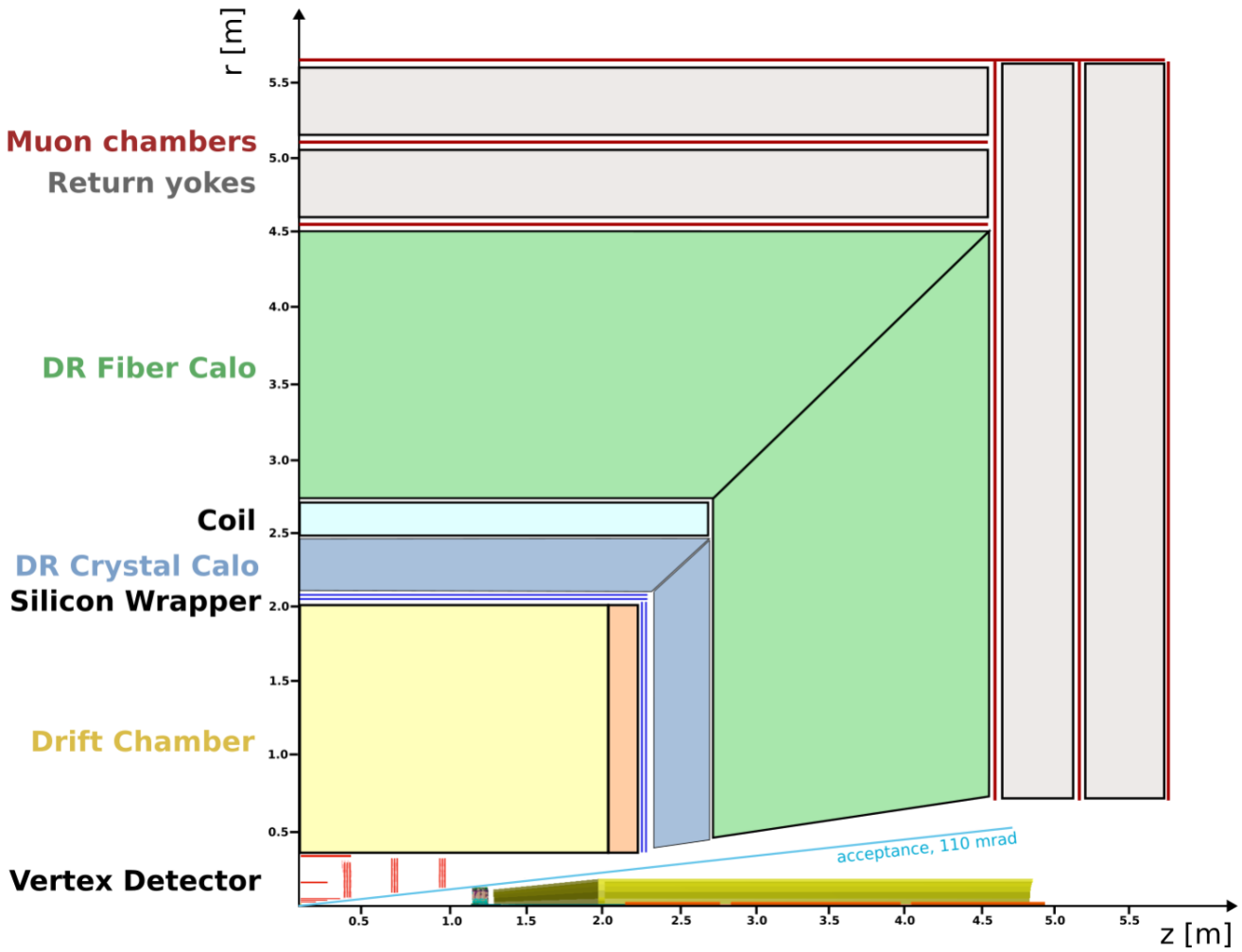
- Momentum resolution

$$\frac{\sigma_p}{p} < 2 \cdot 10^{-5}\ GeV^{-1}\, p \oplus \frac{b}{\sin\theta}$$

- Hit rate near the beam pipe: **200 MHz/cm²** (pair creation, x3 safety)
- Bunch spacing: **20 ns**; physics event rate at Z: **100 kHz**
- Radiation, innermost layer: **tens of kGy/year**

The IDEA Detector Concept

Innovative Detector for e^+e^- Accelerator



Quadrant layout of the IDEA detector

- Low-mass central tracking
  - drift chamber: 112 layers, cluster counting
- **Silicon detectors for precision measurements**
  - **inner vertex detector**
  - **outer vertex detector and disks**
  - **silicon wrapper (+ timing)**
- Dual-readout calorimetry
  - $PbWO_4$ crystal ECAL, then fibre HCAL
- HTS solenoid: 2 T (3 T possible) between ECAL and HCAL
- μ-RWELL muon chambers in the return yoke

See F. Bedeschi's talk
in the Future Experiment Proposals session
arxiv:2502.21223

Si Detector Technologies

- Focus on **depleted monolithic CMOS detectors** (DMAPS)
  - High-voltage/high-resistivity CMOS processes commercially available; large volumes at convenient price
  - Depleted region provides fast rising and "high-amplitude" signals
  - No need of the complex and costly interconnection technique used in hybrid detectors
- **Two baseline technologies:**
  - **ARCADIA** – INFN/LFoundry driven development, collaboration with PSI and IPHC
    - fully depleted, high granularity (25 µm pixels), 30 mW/cm^2 measured at 100 MHz/cm^2: **Inner Vertex Detector**
  - **HV-CMOS** – KIT, China, INFN, Germany, UK collaboration
    - full-reticle sensors, 150 × 50 µm^2 pixels: **Outer Vertex Detector and Si Wrapper**
- **Options under consideration**
  - **Curved ultra-light layout** (ALICE ITS3 inspired, stitched sensors) for the Inner Vertex Detector
  - **LGAD** layer (or a LYSO crystal layer in front of the ECAL) for **time-of-flight** with the Silicon Wrapper

INNER VERTEX DETECTOR

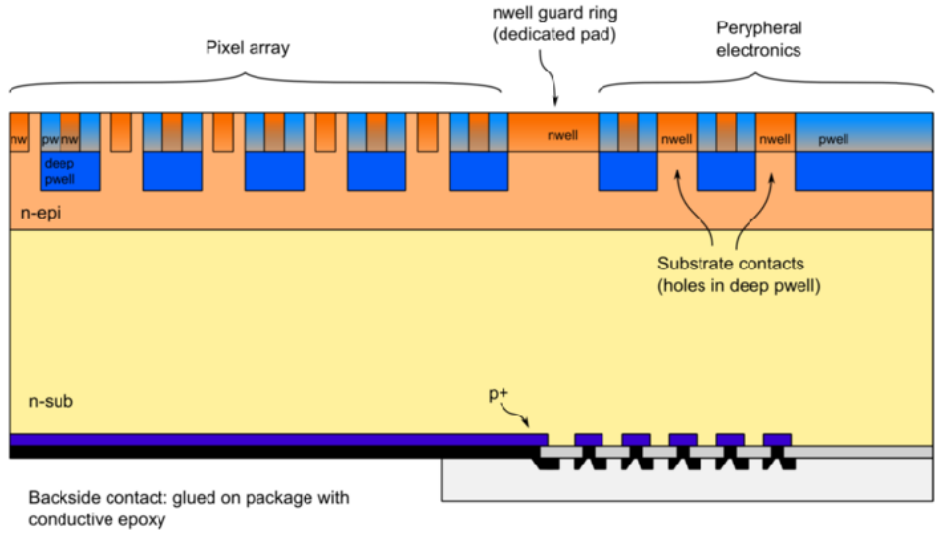
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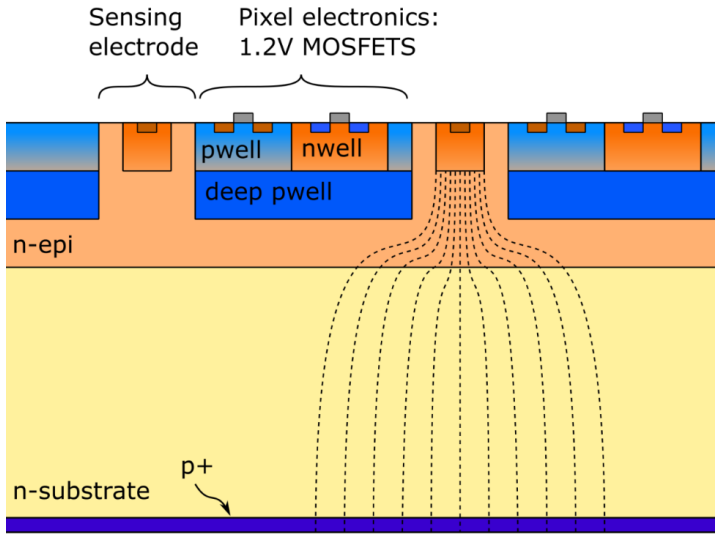
ARCADIA

Advanced **R**eadout **C**MOS **A**rchitectures with **D**epleted **I**ntegrated sensor **A**rrays

Fully Depleted Monolithic Active Pixel CMOS sensor technology platform allowing for:

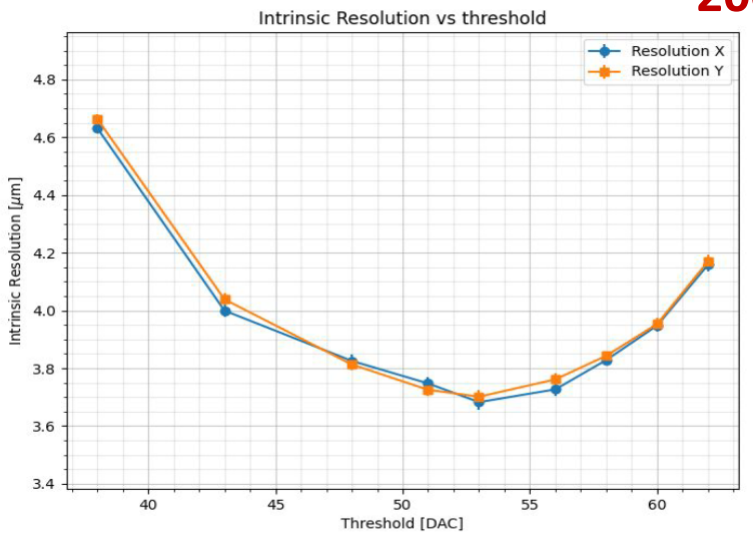
- Active sensor thickness in the range 50 µm to 500 µm;
- Operation in **full depletion** with fast charge collection by drift
- **Small collecting electrode** for optimal signal-to-noise ratio;
- Scalable readout architecture with ultra-low power capability O(**10 mW/cm²**);
- Compatibility with standard CMOS fabrication processes: concept study with small-scale test structure (SEED), technology demonstration with large area sensors (ARCADIA)
- Technology: **LF11is** 110nm CMOS node (quad-well, both PMOS and NMOS), high-resistivity bulk
- Custom patterned backside, patented process developed in collaboration with LFoundry

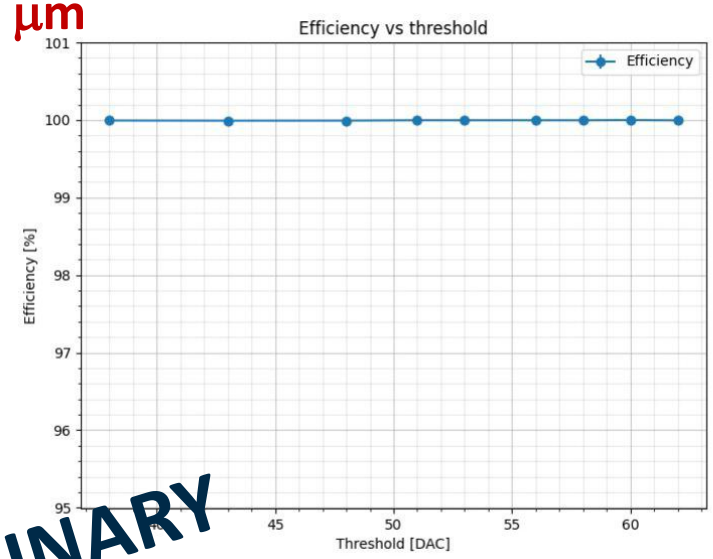




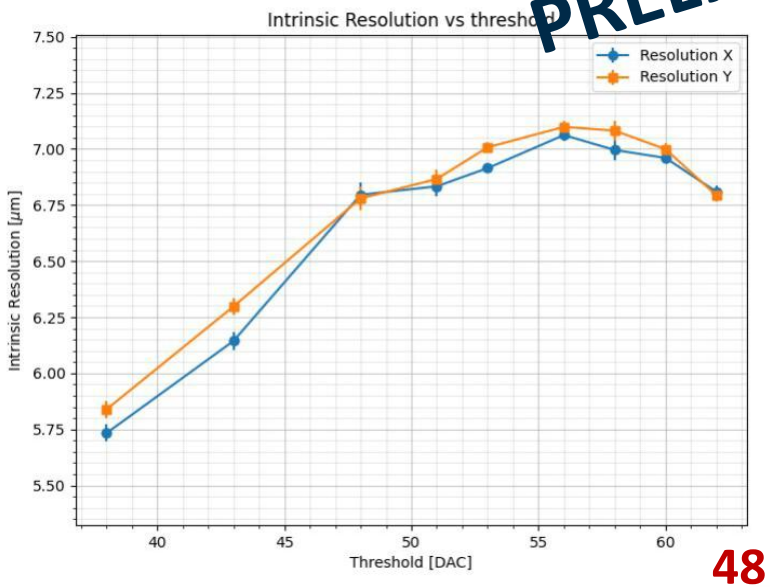
ARCADIA: MD3 Testbeam Results

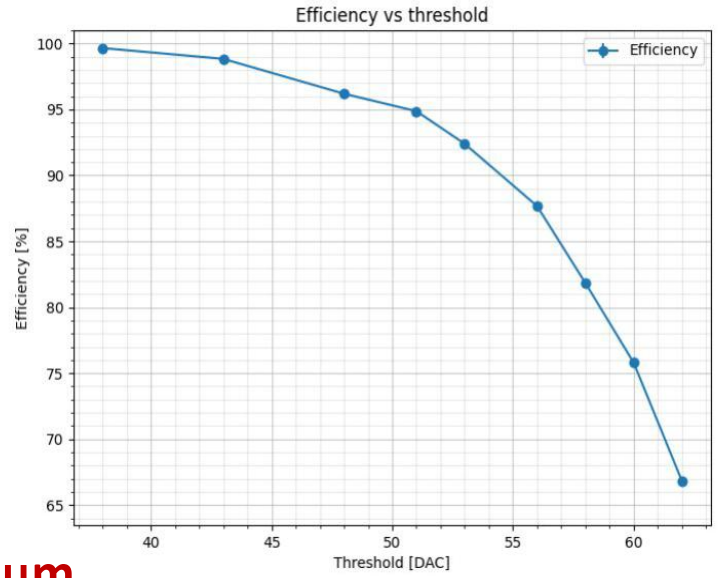
200 μm





PRELIMINARY





48 μm

MD3 demonstrator:

- 512x512 pixels
- 25x25 μm^2 pixels
- Clockless
- Event rate up to 100 MHz/cm^2
- High-rate operation (16 Tx): 30 mW/cm^2

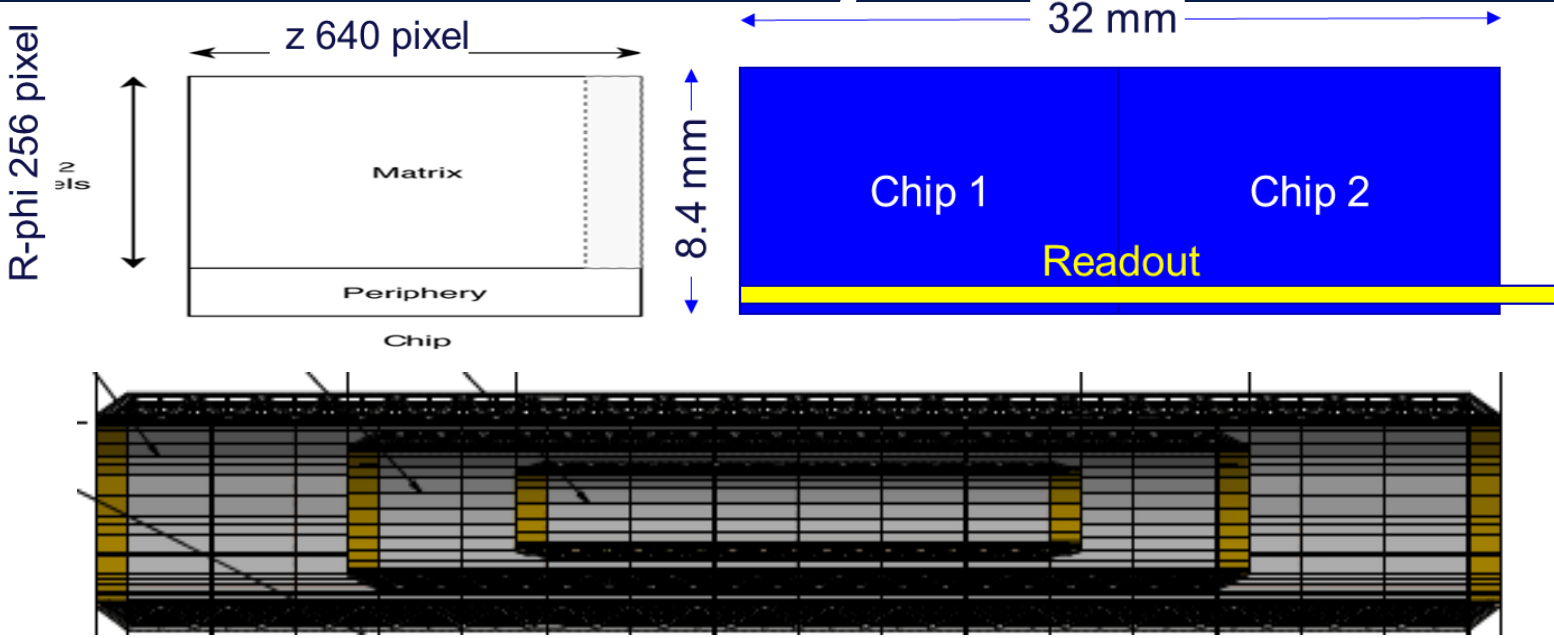
Testbeams at Fermilab (2024) and DESY (2026)

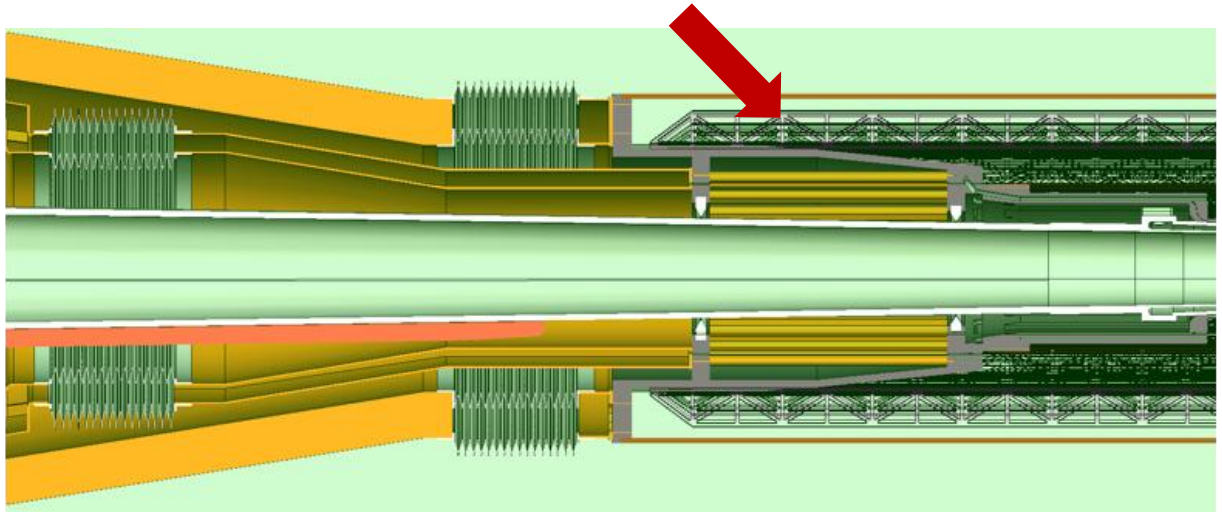
arxiv 2606.25655

- 200 μm and 48 μm active sensor thicknesses tested
- Resolution and efficiency dependence on threshold
- Digital readout: resolution dependent on cluster multiplicity
- Important information for detector layout optimization

Inner vertex layout

- Module: two ARCADIA-inspired chips abutted in z
- 3 barrel layers
  - 13.7, 23.7, 34/35.6 mm radii
  - 15, 24, 36 staves of 6, 10, 16 modules
- Sensors on thin carbon-fibre/Rohacell ladders with data and power buses
  - pinwheel layout, opposite orientation in layer 2





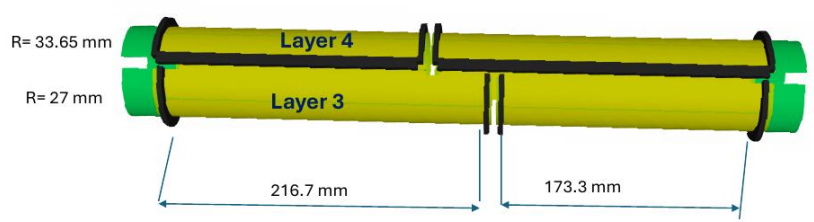
- Power: 12 + 32 + 77 = **121 W** (50 mW/cm^2 assumed, 30 mW/cm^2 measured)
- 0.25% X_0 per layer (+20% from stave overlaps); buses ~0.09% X_0
- **Gas cooling (air or helium)** through carbon-fibre cones
  - CFD: $\Delta T < 15\,^{\circ}$ C along a layer-3 stave; FEA vibration ≈ 1.5 µm at 0.7 g/s
- Total detector weight 285 g
- Mockup construction and testing ongoing (LNF, Pisa, Perugia)

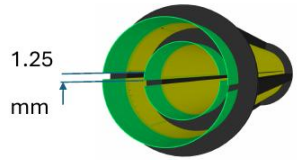
See G. Ammirabile's talk in the MDI session

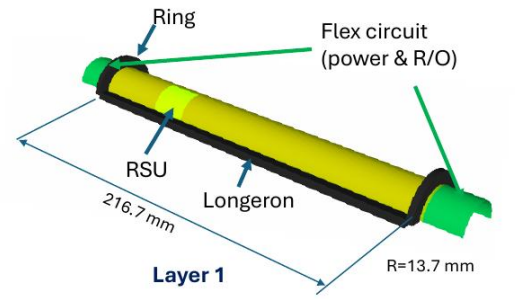
Ultra-light inner vertex

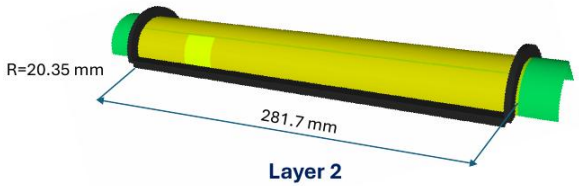
- Curved stitched-sensor layout
  - ALICE ITS3 inspired
  - self-supporting, almost only silicon in the acceptance
- 4 layers of half-cylinders made of repeated sensor units
  - layers 3, 4 split in z (wafer size), staggered for hermeticity
  - 1.25 mm gap between half-shells, partly covered by rotating layer 2
- **0.075% X_0 per layer** vs 0.25% (flat), uniform in ϕ
- Integration studies ongoing

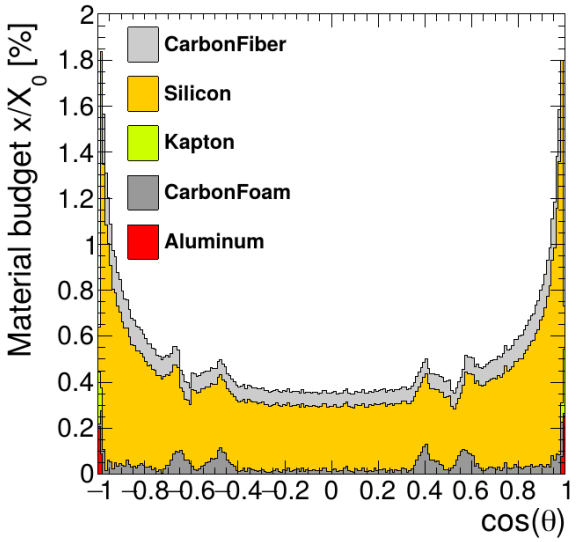
Layer	R [mm]	RSU ϕ × z	|cosθ| <
1	13.7	2 × 10	0.992
2	20.35	3 × 13	0.990
3	27	4 × (8 + 10)	0.990
4	33.65	5 × (10 + 8)	0.986

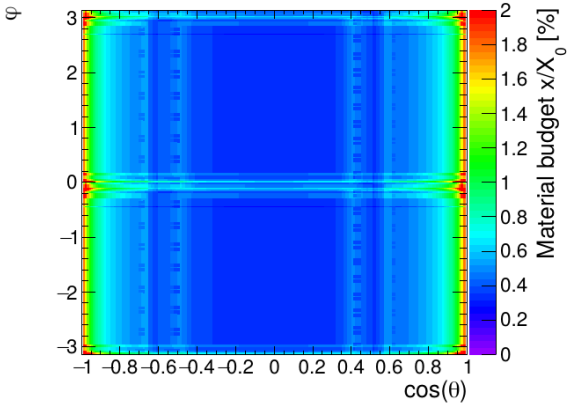










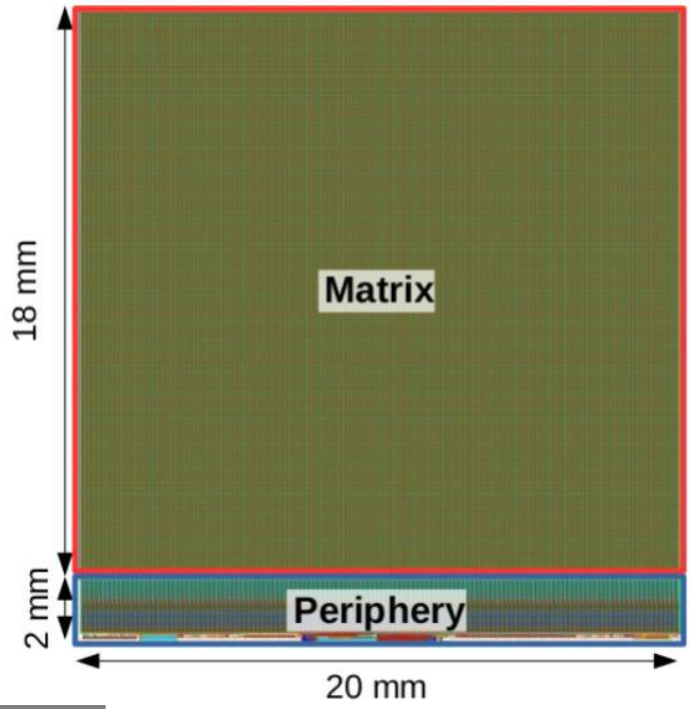


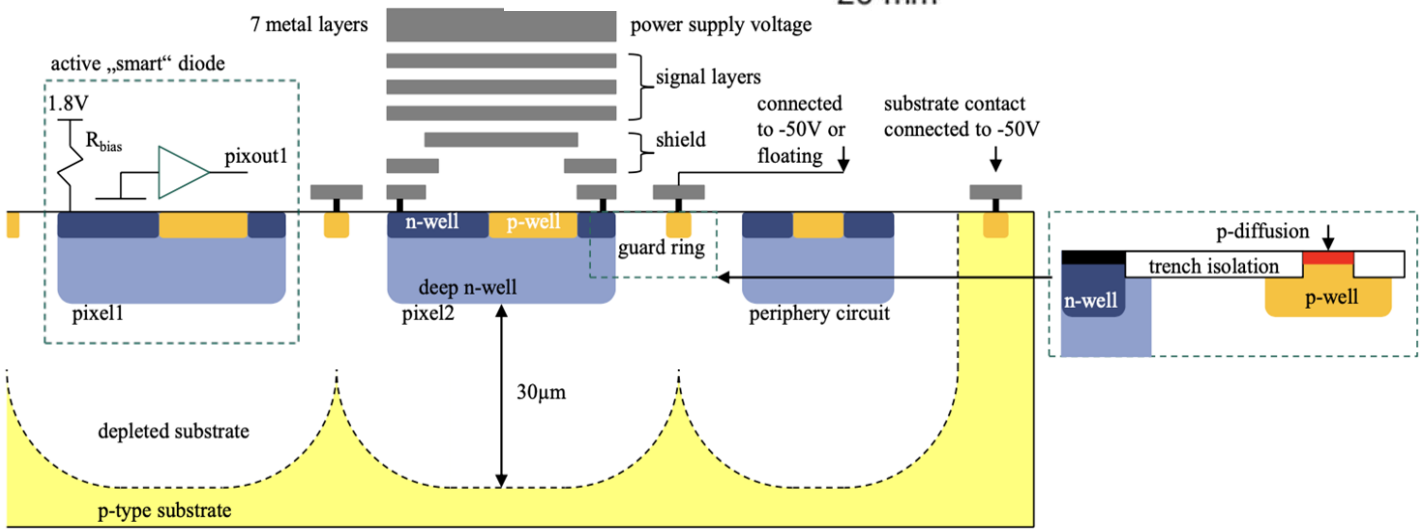
OUTER VERTEX DETECTOR

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ATLASPIX3 Detector

- **ATLASPIX3 general features**
  - **TSI 180 nm HVCMOS** technology
  - full-reticle size **20×21 mm²** monolithic pixel sensor
  - 200 Ωcm substrate (other substrates up to 2 kΩcm also possible)
  - **132 columns of 372 pixels**
  - **pixel size 50×150 µm²** (25×150 µm² on recent prototypes)
  - **breakdown voltage ∼-60 V**
  - up to **1.28 Gbps downlink**
  - **25 ns timestamping**
  - analog pixel matrix, digital processing in periphery
- Both **triggerless** and **triggered** readout modes:
  - two End of Column buffers
  - 372 hit buffers for triggerless readout
  - 80 trigger buffers for triggered readout





Serial Powering Chain

Distribution of power and data signals along the local supports

- **serial powering** to reduce dissipation on the distribution lines
- **minimize** the number of connections

Read-out units are:

- **multi-chip modules** (example 2x2 quad modules)
- (or large stitched detectors)

Minimal I/O connection on chip requires:

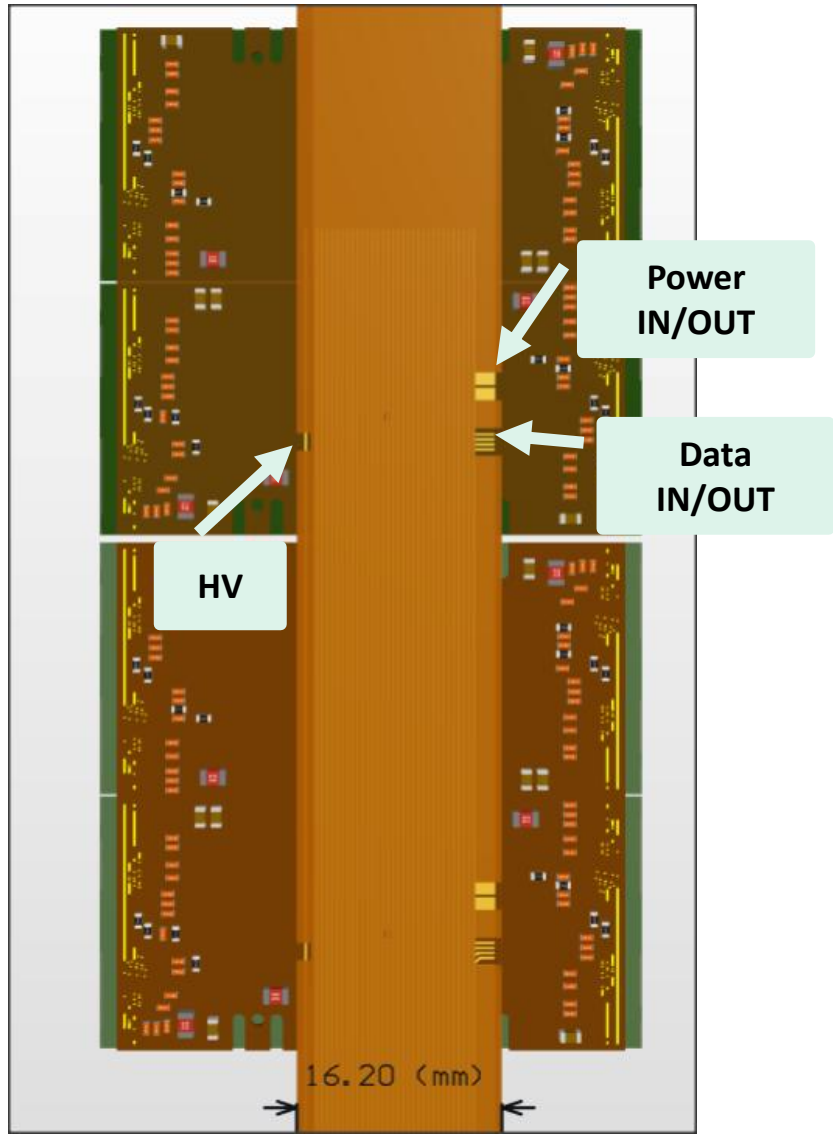
- Serial powering chain: all biases generated internally by shunt-LDO regulators
- chip-to-chip data transmissions: local data aggregation on module
- clock data recovery

not available on ATLASPIX3 modules

Reducing material by developing PCB with Al as conductor

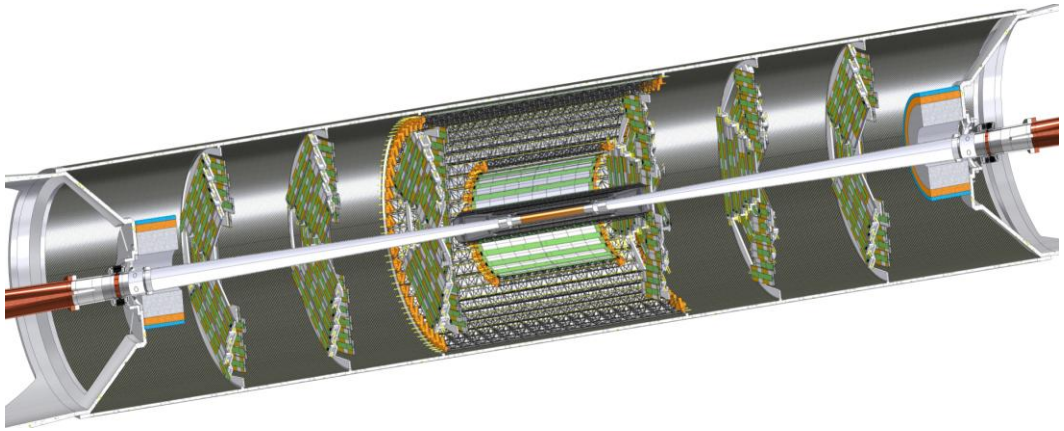
- on going design of PCBs to prototype a serial power chain

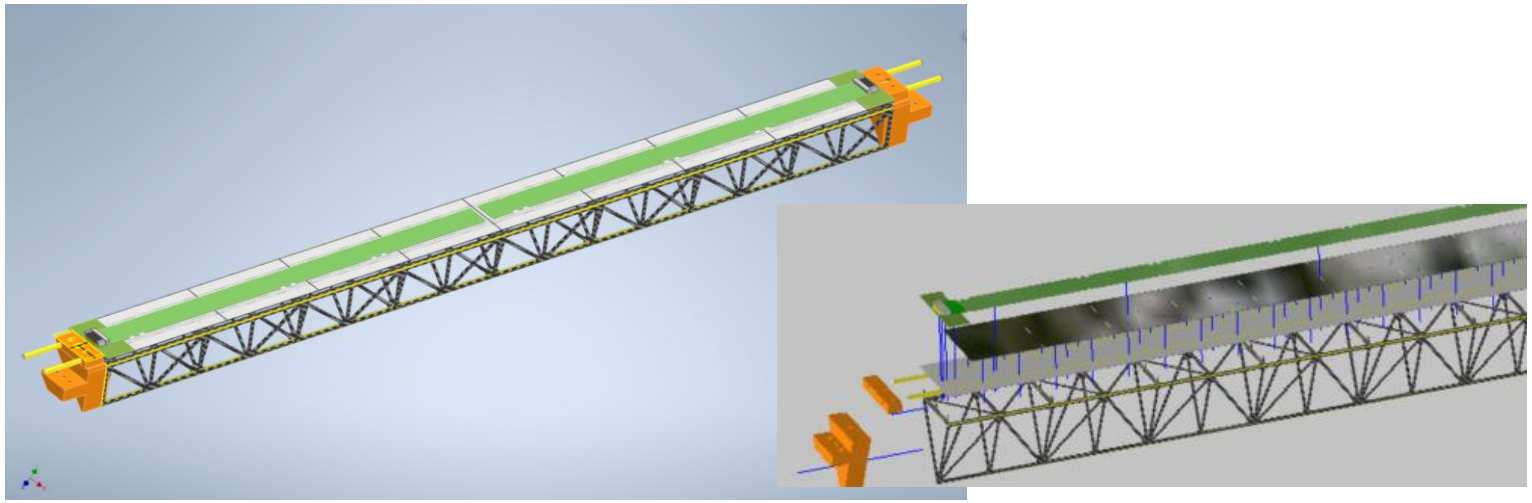
Serial powering tests: JINST 20 (2025) C02036

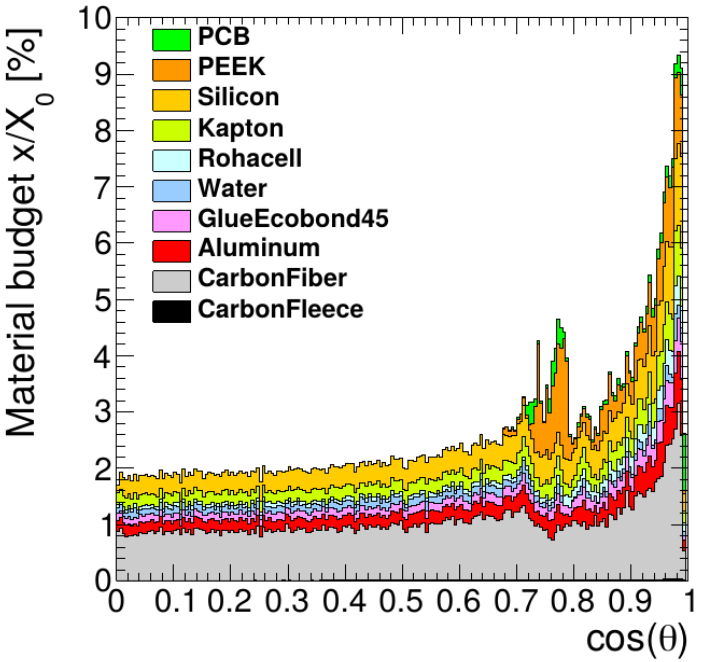


Outer Vertex Layout

- Modules: 4 ATLASPix3-like chips, 40.6 × 42.2 mm², 50 µm thick
- 2 barrel layers, 13 cm (23 ladders × 8 modules) and 31.5 cm (51 × 16)
  - covering $|\cos\theta| < 0.77$
- 2 × 3 disks at $|z| \approx 0.3, 0.62, 0.93$ m
  - $0.77 < |\cos\theta| < 0.99$
- Light triangular carbon-fibre truss, water-cooled
- Power at 100 mW/cm²: 0.3 kW (middle barrel), 1.4 kW (outer barrel), ~0.9 kW (disks)



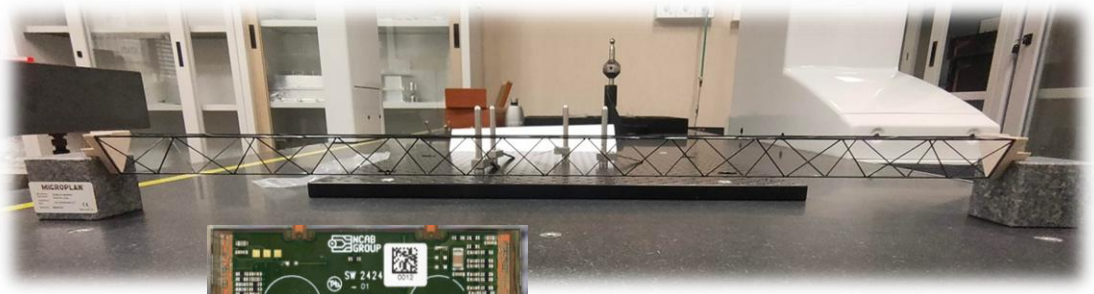




Material budget of the complete flat vertex detector

Feasibility studies

- Demonstrating the detector concept with realistic components:
  - light mass stave and cooling plate available
  - assembled multi-chip HV-CMOS modules
  - operated a serial power chain
  - Al power bus just delivered from CERN Micropattern Fabrication Lab







- Planning more advanced development for the FCC reference design studies:
  - joint effort between DRD3 and LHCb
  - new sensors with full periphery and daisy chaining of data submitted in LFoundry 150 nm process
  - development of thin Al flexes with FBK

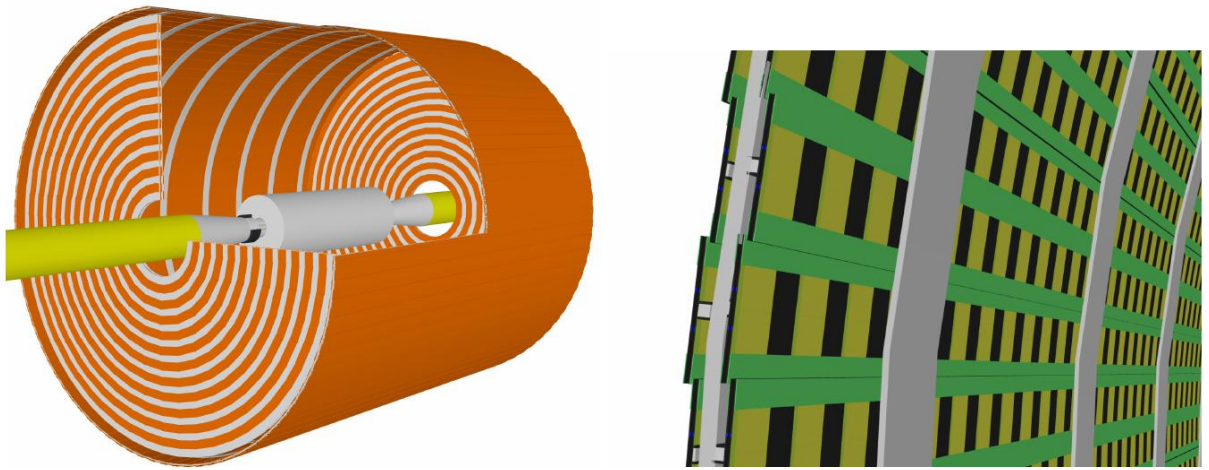
More details in Y. Gao's talk

SILICON WRAPPER

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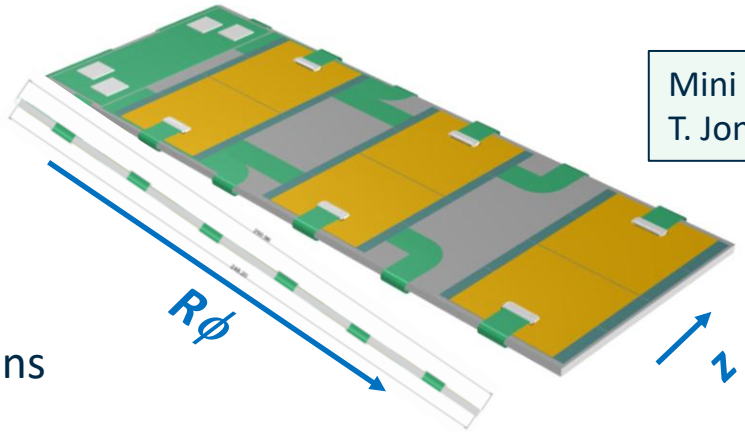
The IDEA Concept: Si Wrapper

- **Precision silicon layer around the drift chamber**
  - **improve momentum resolution**: $\sigma(p_t)/p_t \simeq 0.3\%$ at 10 worse without it
  - **extend tracking coverage** in the forward/backward re drift chamber has few hits
  - precise and stable ruler for acceptance definition (< O
  - *may provide TOF measurement*
- Double layer: 2 barrel layers (r = 2.04, 2.08 m) + 2 disks per side
  - hermetic down to $\cos\theta \lesssim 0.989$
  - O(10 μm) resolution, 2–5% X_0
- Covered area ~87 m^2: 209 m^2 of silicon, 124 520 sensors
  - important impact on services



Silicon Wrapper in DD4hep: global layout and overlapping barrel staves

- Mini stave concept:
  - Staves with two sensor rows on both sides, flex on top, 1.4 mm carbon-fibre support and cooling pipes in the middle
  - Barrel: staves overlap in ϕ; disks: overlapping rings at two z positions



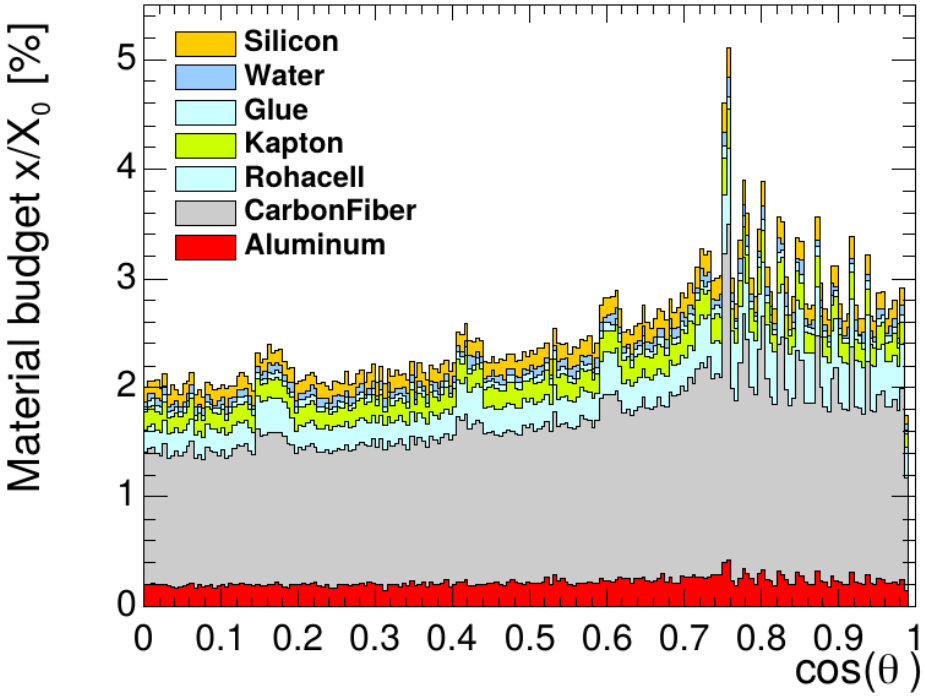
Mini stave concept
T. Jones - Liverpool

Si Wrapper: layout and challenges

Layer	R [m]	|z| [m]	Sensors	Si [m²]	|cosθ|
Barrel 1	2.04	< 2.4	43 492	≈ 73	< 0.762
Barrel 2	2.08	< 2.4	43 492	≈ 73	< 0.756
Disk 1	0.35–2.04	2.30	9 384 × 2	≈ 15.8 × 2	0.748–0.989
Disk 2	0.35–2.04	2.32	9 384 × 2	≈ 15.8 × 2	0.751–0.989
Total			**124 520**	**≈ 209.4**	

ATLASPix3-sized sensors (42.2 × 40.2 cm²); disk numbers are per side

- **Challenges** to be addressed over the next years
  - very large area: signal aggregation, powering and cooling must be addressed early
  - barrel: longerons attached to support rings around the drift chamber
  - endcaps in two D-shaped halves, installed after the beam-pipe/vertex support tube
  - drift-chamber services must exit without acceptance gaps in the wrapper



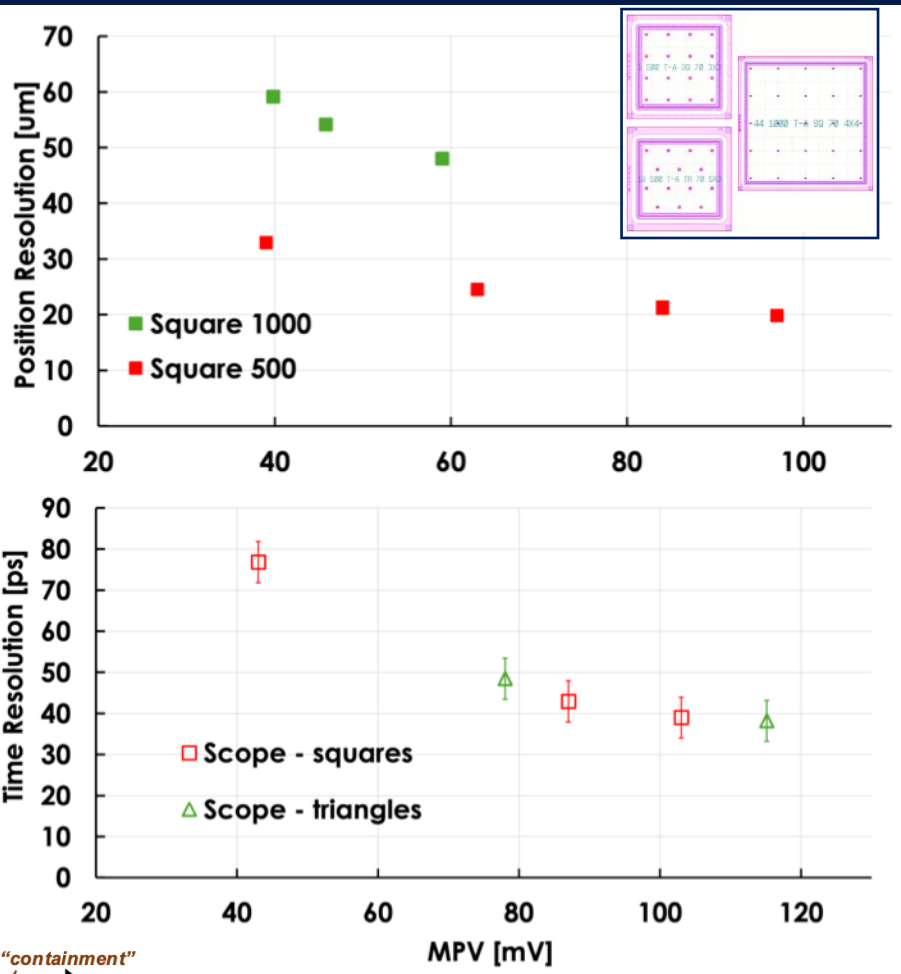
Material budget: 2–5% X_0

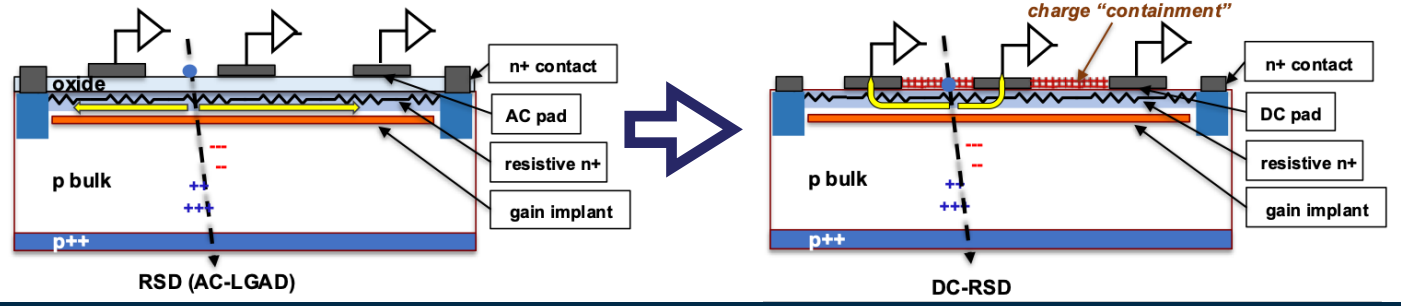
- **Open sensor options:**
  - HV-CMOS (like the outer vertex)
  - RSD and CMOS RSD
  - silicon strips

RSD: Structures

- RSD sensors have been produced with different geometries of pads and collecting electrodes
  - Several methods for the reconstruction of the hit position and time have been developed: from simple linear interpolation, to look-up tables, to ML algorithms using sampled signals
  - In all cases, position resolution in the range 3-5% of the electrode pitch, and timing resolution comparable to those of standard LGADS (few tens of ps) have been achieved
- A different readout concept is being explored
  - overcome a few non-ideal features of the RSD architecture (extended signal sharing, bipolar signals, baseline fluctuations)
  - restoring a DC readout while keeping the resistive sharing of signals

  ⟹ **DC-RSD**





NIM A 1080 (2025) 170796

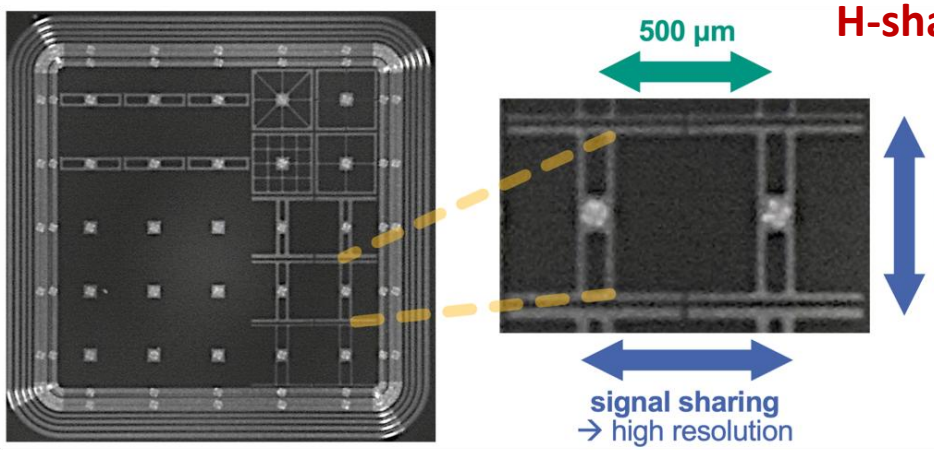
JINST 20 (2025) 06, C06016

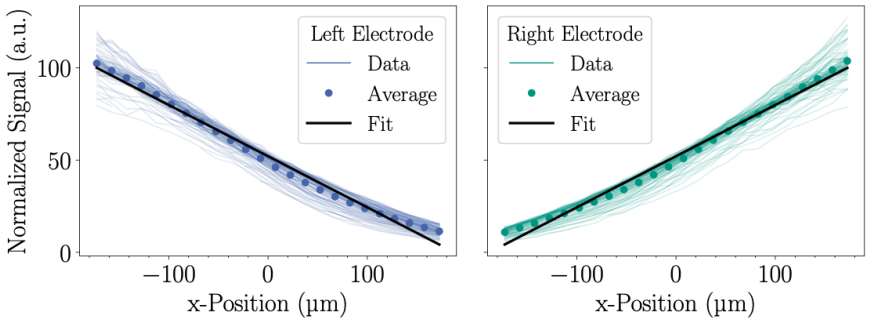
Resistive Silicon Detectors: strips

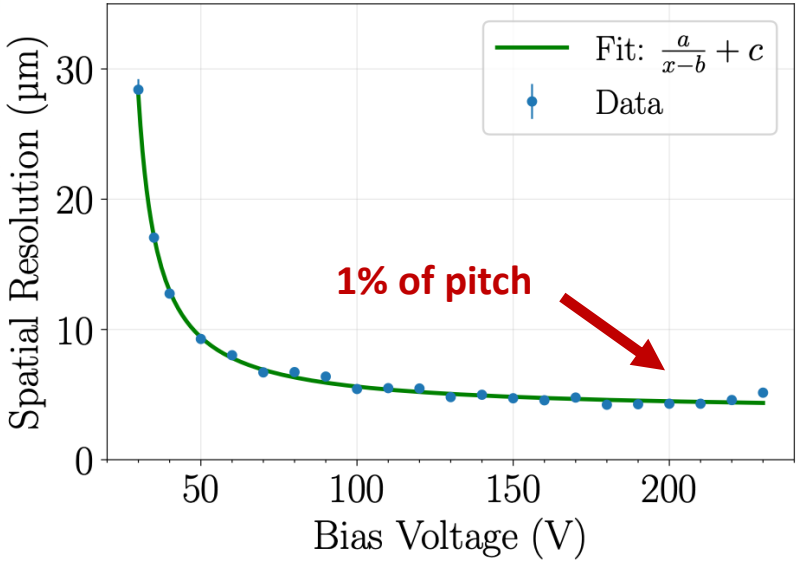
- Strip geometries are being developed for various future applications
  - Precision measurement of one coordinate via charge sharing
  - Very good performance achieved even with simple linear interpolation
  - Other coordinate measured from cell pitch, alternate-side readout, or special geometries
  - **Timing performance preserved**

H-shaped electrodes

JINST 21 (2026) 07, C07023

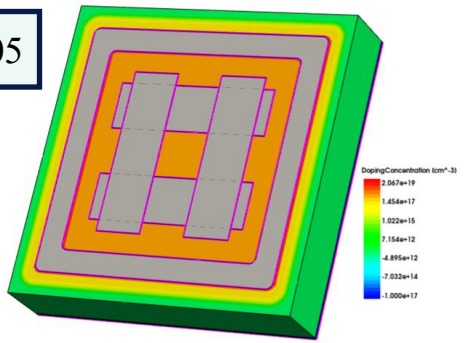


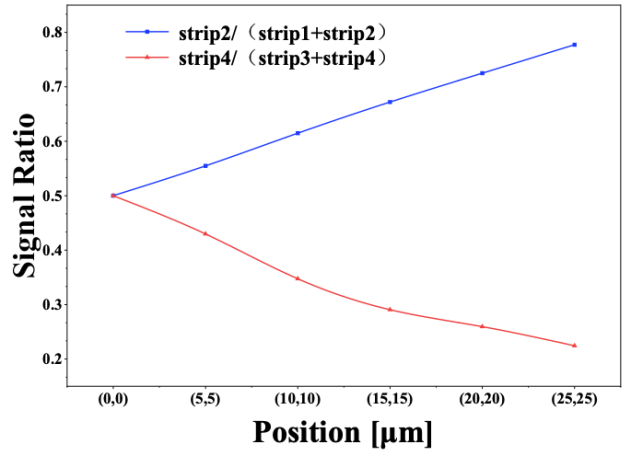




Crossed-strip design (CS-RSD)

arXiv:2609.06105

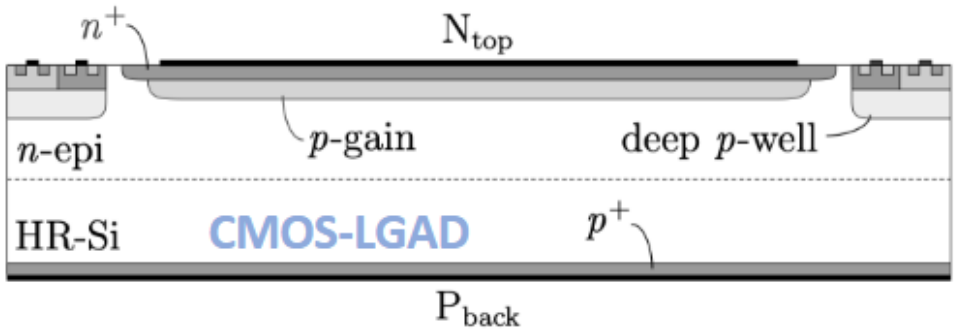




CMOS-RSD

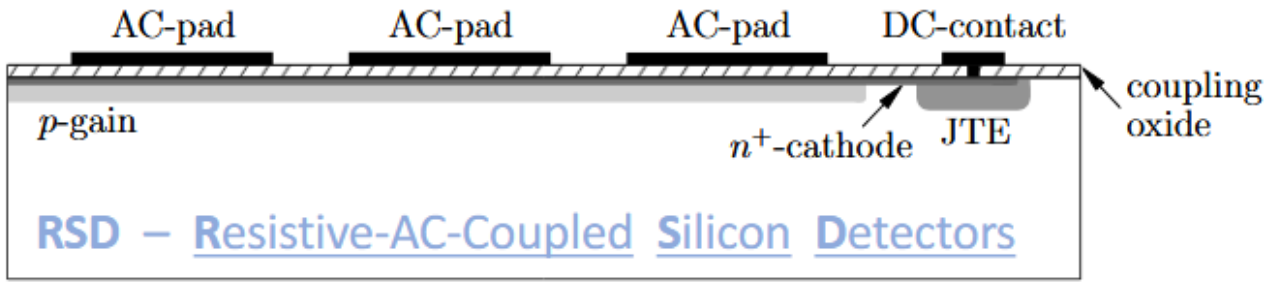
Full details in M. Mandurrino's talk

CMOS integration of the **LGAD technology** already demonstrated (in LF11is)



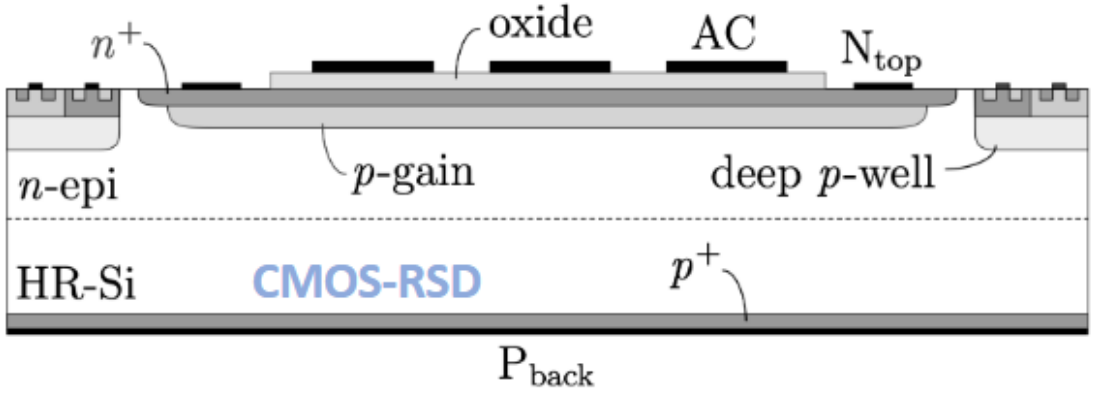
Spatial resolution **~3% of sensor pitch** (allowing to relax the channel density)

Time resolution similar to standard LGADs: **30-40 ps**



Plausible concurrent targets:

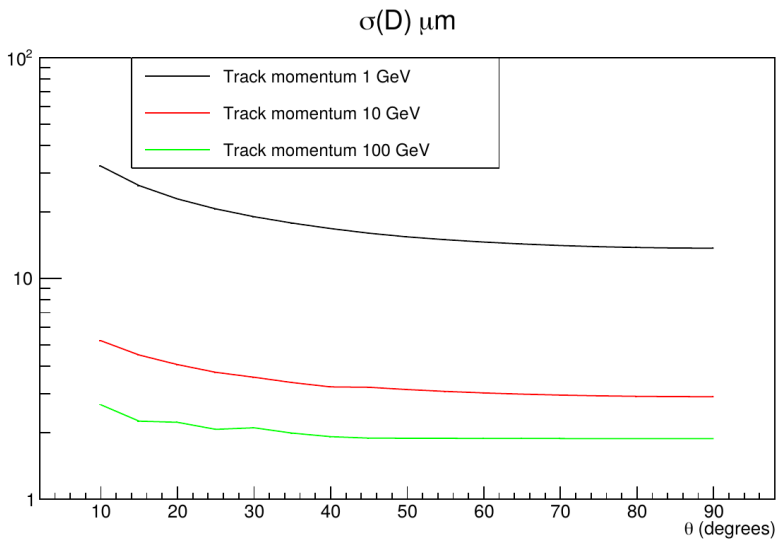
- **σ_t = 10-20 ps**
- **µm-level σ_x**
- **100% FF**



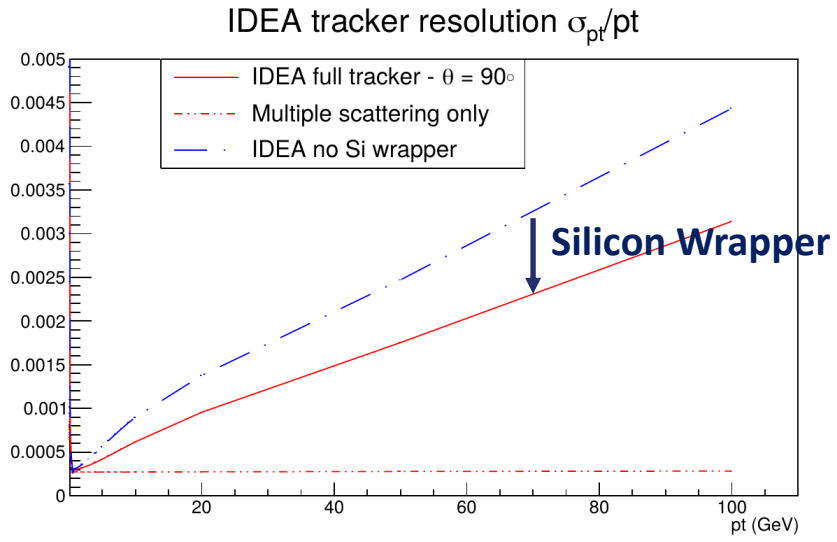
Detector layout and process flow design activities are ongoing

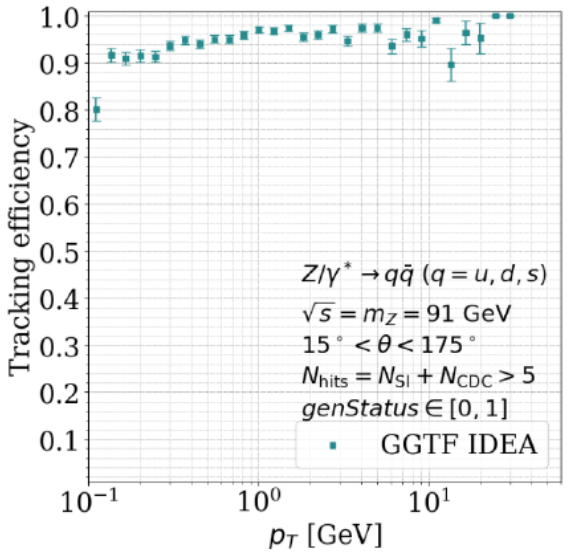
First prototypes in next silicon production runs (std. CMOS process)

Tracker performance



Delphes fast simulation with full covariance matrix; muons





Full simulation, GGTF track finder

Impact parameter

- σ(d) ≈ 2 μm asymptotically at high momentum over most of the acceptance
- ~13 μm at 1 GeV/c, ~3 μm at 10 GeV/c at 90°

Momentum resolution

- $\sigma(p_t)/p_t \simeq 0.3\%$ at $p_t = 100$ GeV/c
- clearly degraded without the Silicon Wrapper
- multiple-scattering term very small

Track finding

- GNN-based track finder (GGTF) on full simulation
- Z/γ* → qq̄ (u, d, s) at √s = 91 GeV: efficiency ≳ 90% above ~0.2 GeV/c
- preliminary

Summary and outlook

- The IDEA silicon tracker poses different challenges for its three subsystems:
  - Vertex detectors: extremely high resolution and low mass (0.25% X_0 per layer, 0.075% in the curved option)
  - Large-area detectors: system issues (Si Wrapper: 209 m^2, 124 520 sensors)
  - Depleted monolithic CMOS pixels are a cost-effective, high-performance solution
- **Detector concept developed using existing prototypes:**
  - **ARCADIA** (LF 110 nm): fine granularity and low power for the inner vertex
    - 3 layers at 13.7–35.6 mm, 121 W, gas cooling; ultra-light stitched layout under study
  - **ATLASPIX3** (TSI 180 nm): full-size sensor for the outer vertex and the Si Wrapper
    - Outer vertex: 2 barrels + 3 disks per side, water cooling, serial powering
  - **Si Wrapper** presents many interesting options: DMAPS, timing via LGAD (~100 ps) or LYSO layer

Plenty of opportunities to join and **contribute new ideas** and innovative solution

- **Electronic design and sensor development** still needed within the time scale of future e^+e^- factories, especially for the LF 110 nm design
- **System aspects** can already be addressed with existing detectors
- Silicon Wrapper **mechanical structure and services are** particularly challenging

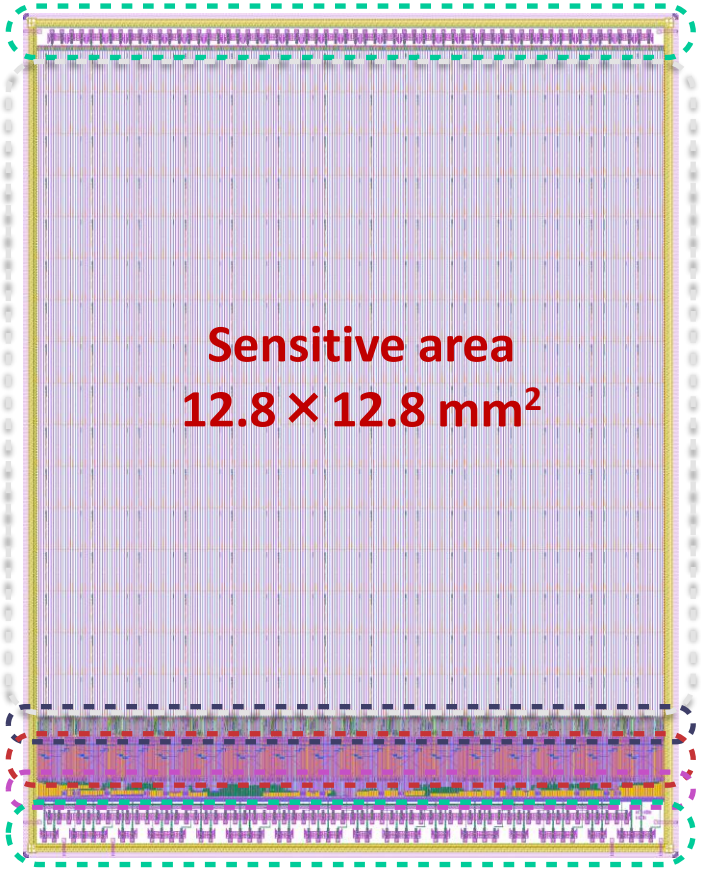
BACKUP

INFN MILANO
UNIVERSITÀ DEGLI STUDI DI MILANO
DIPARTIMENTO DI FISICA

ARCADIA: MD3 demonstrator

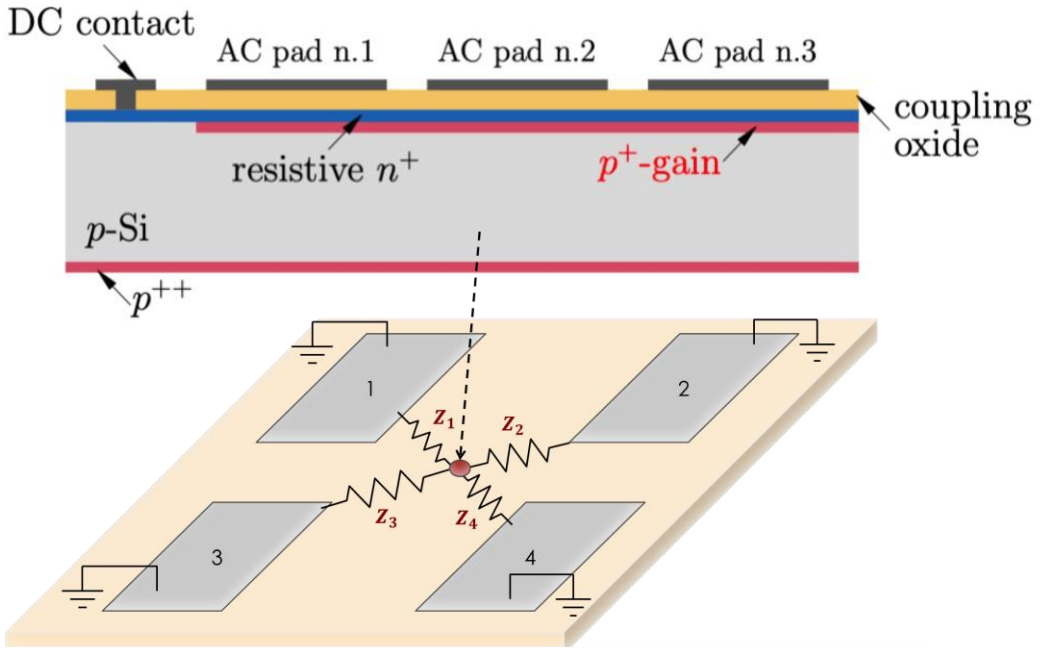
- Demonstrator layout:
  - **Top Padframe** Auxiliary supply, IR Drop Measure
  - **Matrix**
    - 512x512 pixels, Double Column arrangement
    - 25x25 μm^2 pixels
    - Clockless
  - **End of Sector (x16)** Reads and Configures 512x32 pixels
  - **Sector Biasing (x16)** Generates I/V biases for 512x32 pixels
  - **Periphery**
    - SPI, Configuration, 8b10b enc, Serializers
    - Triggerless data-driven readout
    - Event rate up to 100 MHz/cm^2
    - High-rate operation (16 Tx): 17-30 mW/cm^2
    - **Low-power operation (1 Tx): 10 mW/cm^2**
  - **Bottom Padframe** Stacked Power and Signal pads

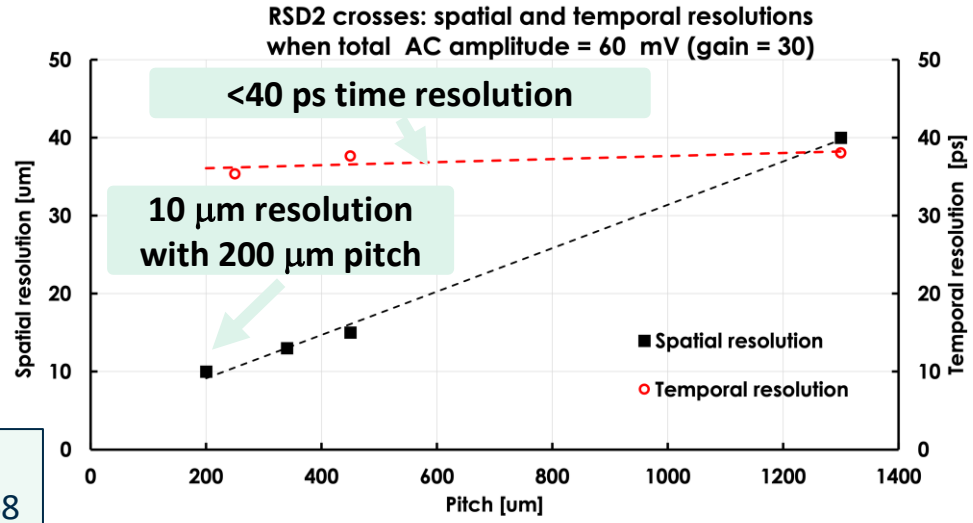




Si-Wrapper: alternative RSD option

- LGAD detector with **continuous gain layer**
- Charge collection through **resistive n-layer**
- Readout by induction on **AC coupled pads**
- Fully active detector
  - avoids inefficient regions due to the insulation between pixels needed in LGAD sensors
- Charge sharing defined by the relative impedance of the path between the charge deposition and readout electrodes
  - Sharing is deterministic (in low pitch pixel detectors sharing is dominated by Landau fluctutations)
  - Timing resolution approximatively independent from pixel pitch
  - Position resolution ~5% of the readout pitch: more space in readout pixel cell to implement precision TDC

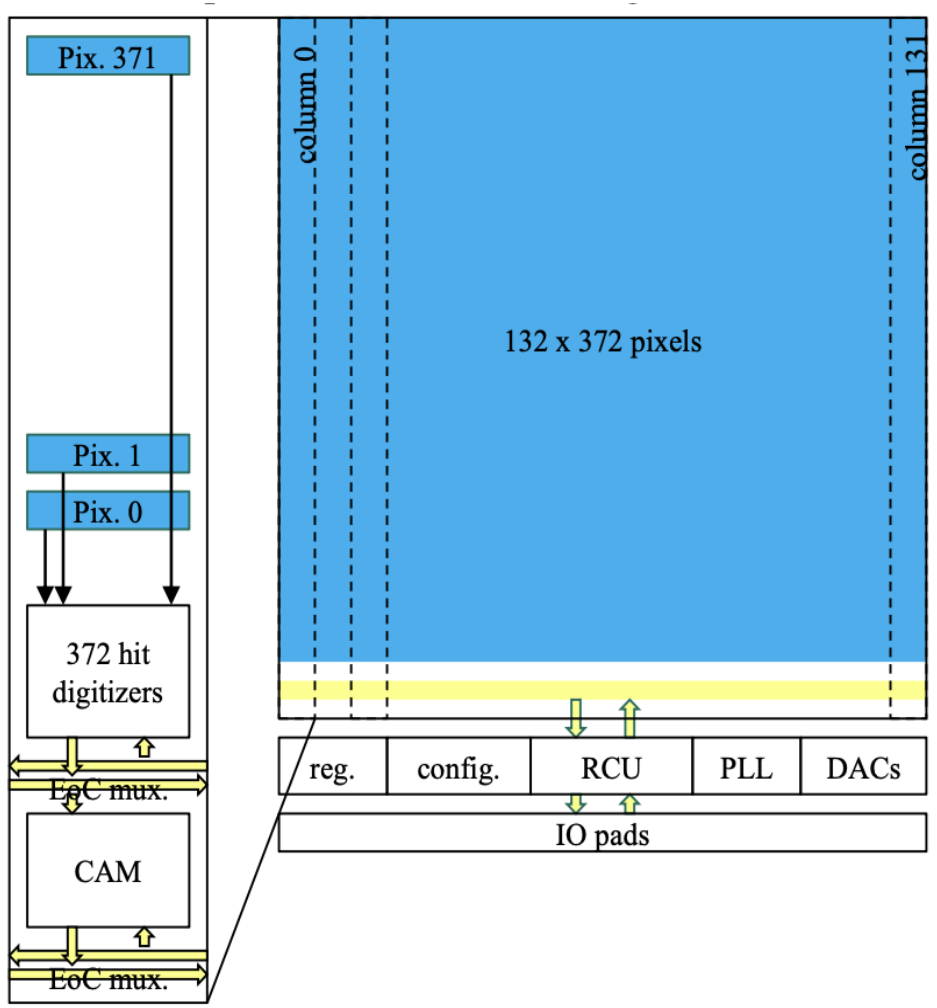




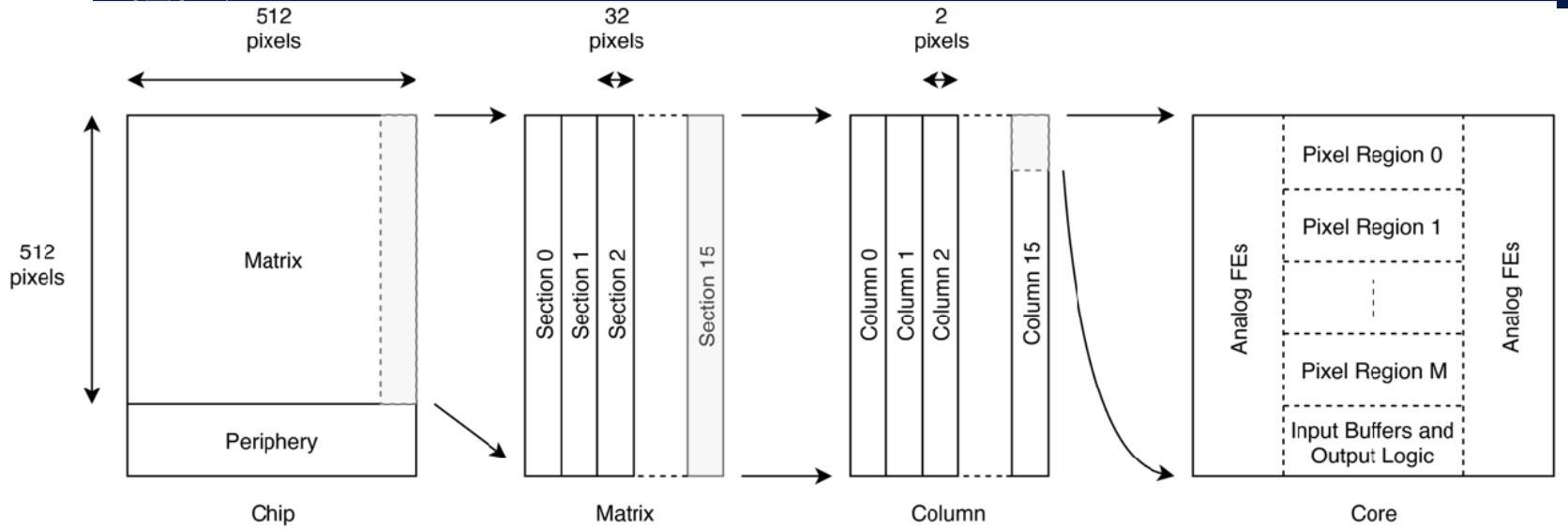
N. Cartiglia et al.
arXiv:2301.02968

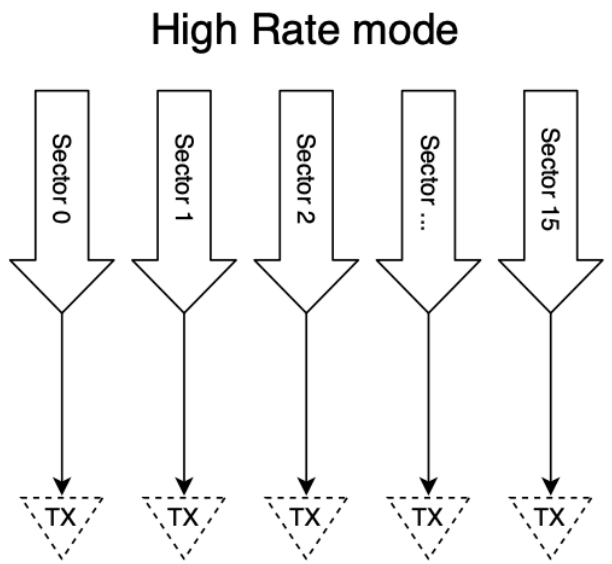
ATLASPIX3 Readout Architecture

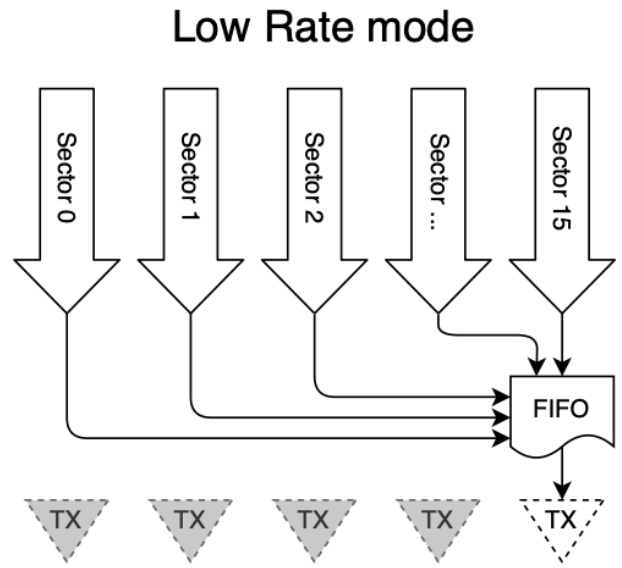
- **Chip architecture**
  - organized in 132 columns, each with:
    - 372 pixels
    - **372 hit digitizers** (HDs)
    - **80 content addressable memory cells** (CAM)
    - **two end-of-column multiplexers** (EoC mux)
  - **digital part** (HDs, CAM, EoCs) in **chip periphery**, separated from analog pixels electronic (CSA and comparator)
  - chip periphery also contains the readout control unit (RCU), the clock generator, configuration registers, DACs, linear regulators and IO pads
  - **triggerless** and **triggered** readout
    - two EoCs
    - 372 hit buffers for triggerless RO
    - 80 trigger buffers for triggered RO



ARCADIA: MD3 Architecture



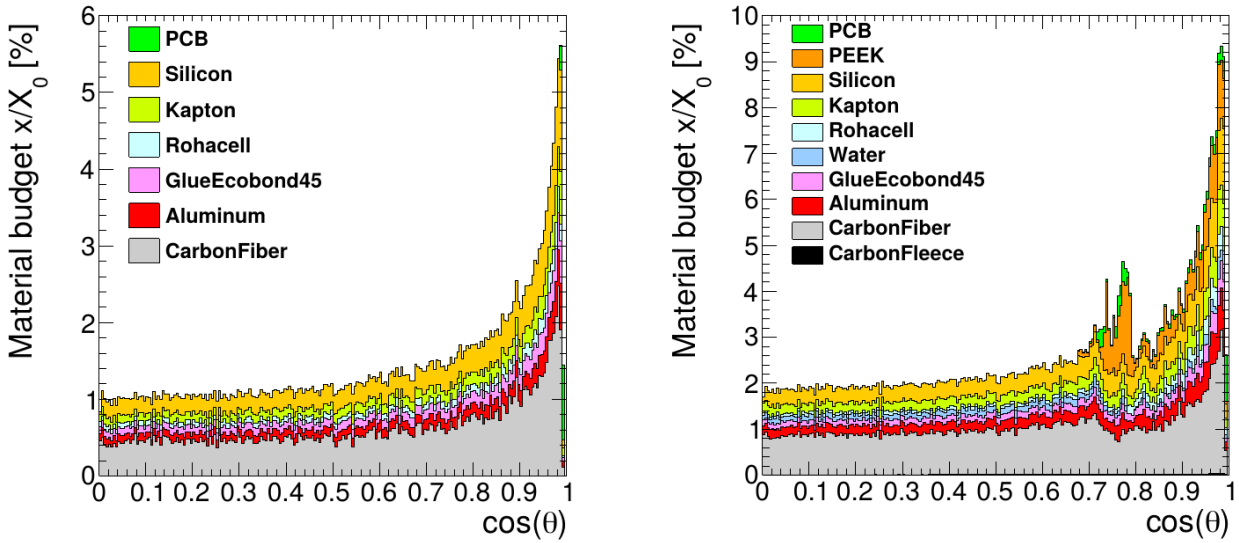




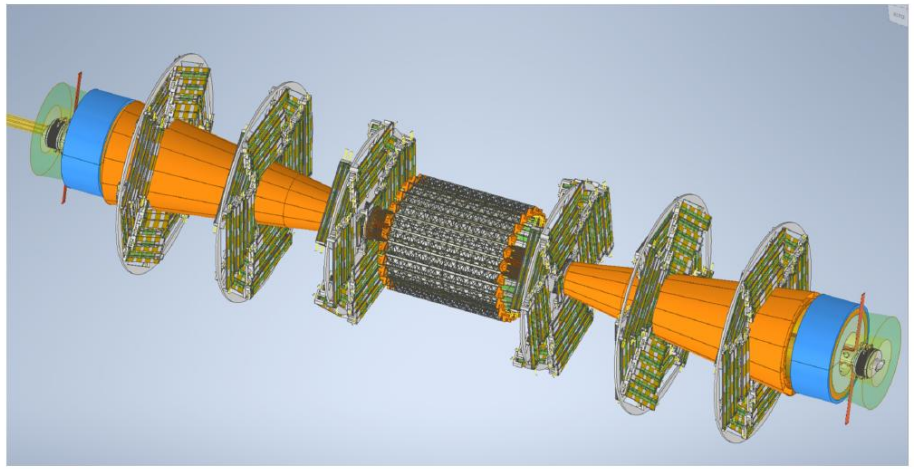
- Pixel size 25 µm x 25 µm, Matrix core 512 x 512, 1.28 x 1.28 cm silicon active area, “side-abuttable”
- Triggerless data-driven readout and low-power asynchronous architecture with clockless pixel matrix
- Event rate up to 100 MHz/cm^2 (post-layout simulations, to be demonstrated: test-beam in late 2023)
- Each sector has an independent readout and output link when operating in High Rate Mode
- Sector data is sent out (8b10b encoded) via dedicated 320MHz DDR Serialisers
- In Low Rate Mode, the first serialiser processes data from all the sections. The other serialisers and C-LVDS TXs(*) are powered off in order to reduce power consumption.

Vertex detector: cooling and material

- **Inner vertex:** gas cooling
  - channels in the carbon-fibre structure; carbon-fibre cones force convection
  - air or helium considered
  - CFD: $\Delta T < 15\ ^{\circ}$ C along a layer-3 stave
  - FEA: max. displacement ≈ 1.5 µm at 0.7 g/s
- **Outer vertex and disks:** 100 mW/cm^2
  - too high for air cooling by at least a factor 2
  - demineralised water in 2.2 mm polyamide tubes inside the staves



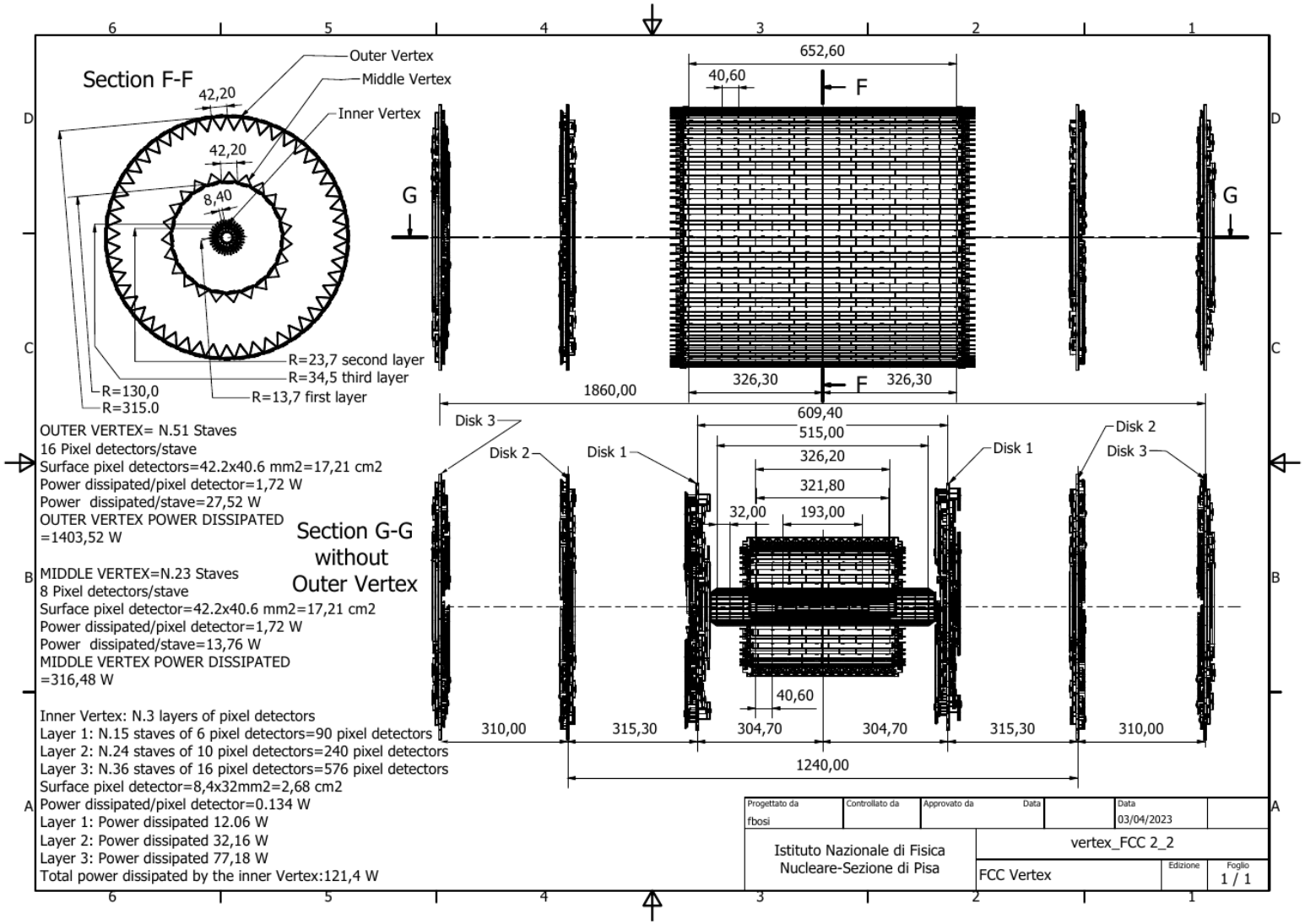
Material budget vs cosϑ: flat inner vertex (left), complete flat vertex detector (right)



Middle barrel, disks and cooling cones; luminosity calorimeters in blue

- Flat inner vertex: 0.25% X_0 per layer at normal incidence
  - overlap between staves adds ~20%
- Ultra-light curved option: 0.075% X_0 per layer
- Complete flat vertex detector reaches ~10% X_0 at the edge of the acceptance (outer layers, disks, PEEK rings)

The IDEA Vertex Detector: layout

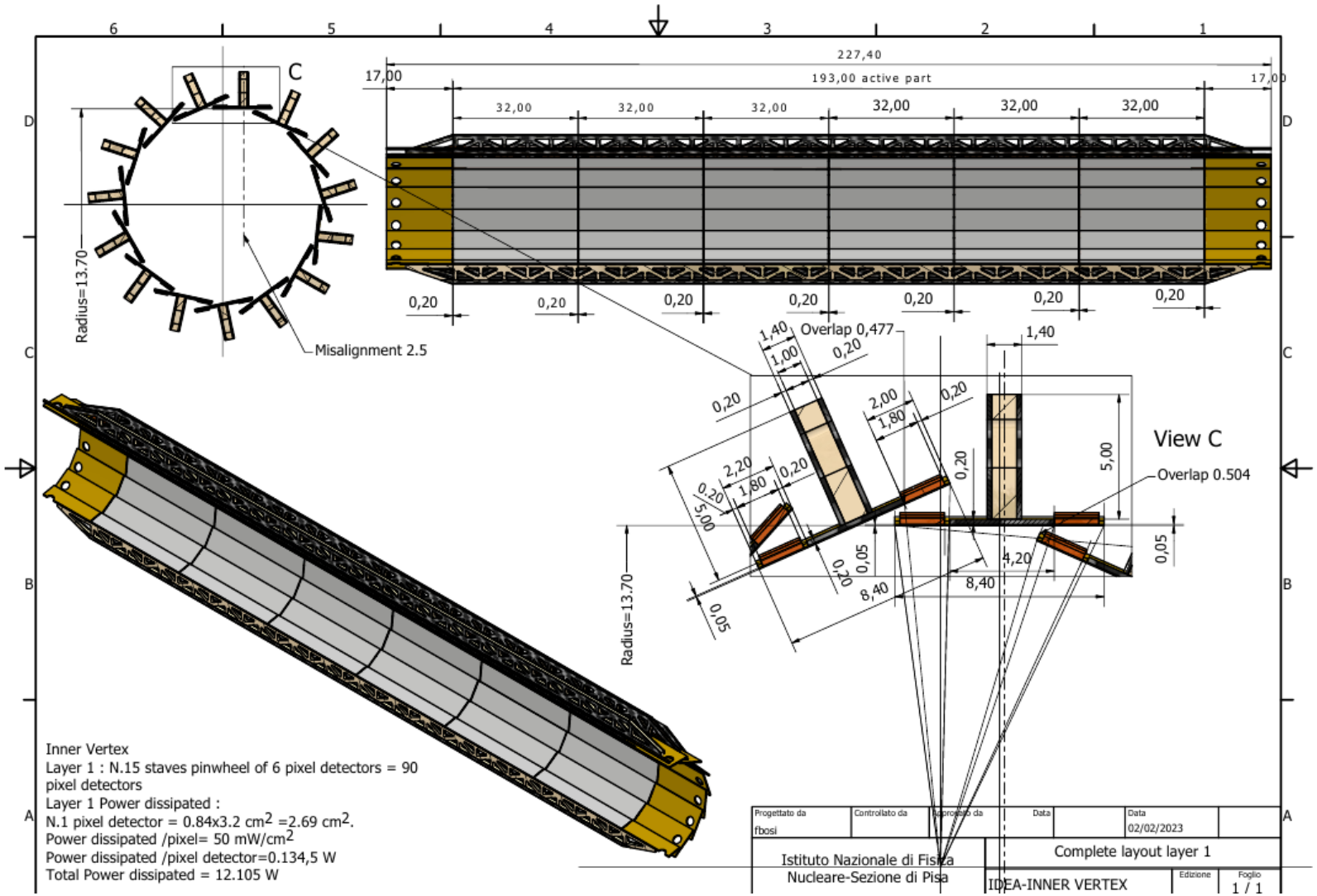


Baseline vertex detector: barrel layers (left), outer barrel and disks (right), inner and middle barrels

Layer	R [mm]	|z| [mm]	Staves × mod.	P [W]
Inner 1	13.7	< 96.5	15 × 6	12
Inner 2	23.7	< 160.9	24 × 10	32
Inner 3	34/35.6	< 257.5	36 × 16	77
Middle	130	< 163.1	23 × 8	316
Outer	315	< 326.3	51 × 16	1400
Disk 1	34.5–275	305	56 × 2–6	135
Disk 2	70–315	620	48 × 3–7	420
Disk 3	105–315	930	40 × 4–7	370

Disk rows: per side

Inner vertex: layer 1

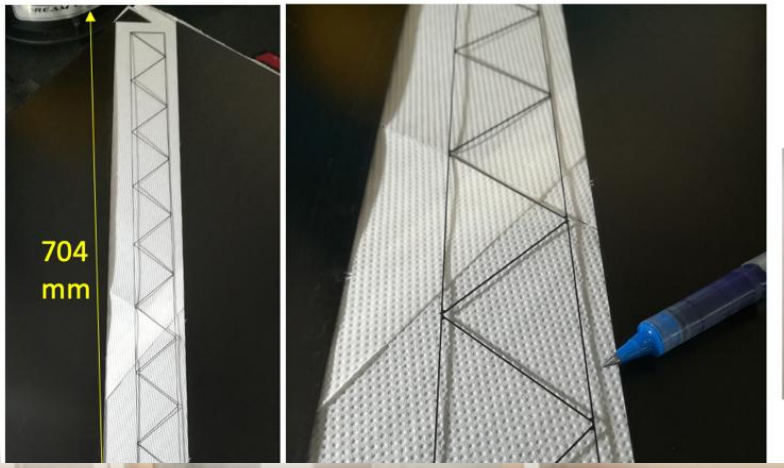


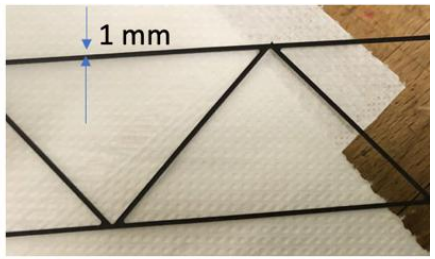
Layer 1: 15 staves of 6 modules in pinwheel geometry; sensors face the beam line, buses on the opposite side

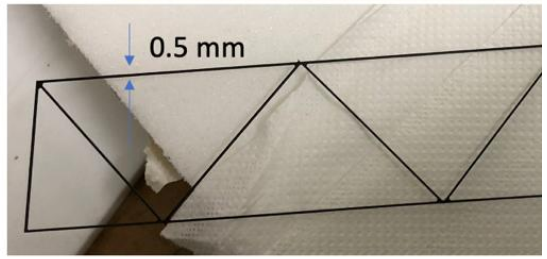
Outer Vertex Stave prototyping

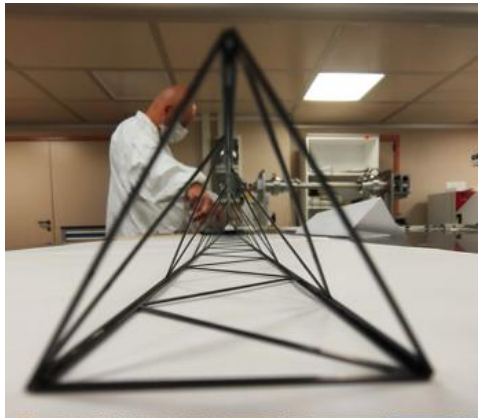
Prototypes built for Belle II upgrade in Pisa

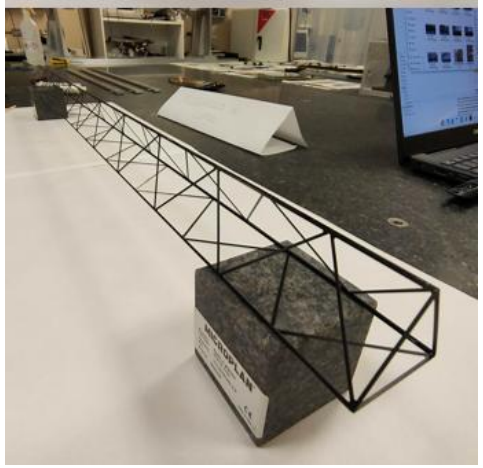
CF water-jet cut (by WatAJet Company)









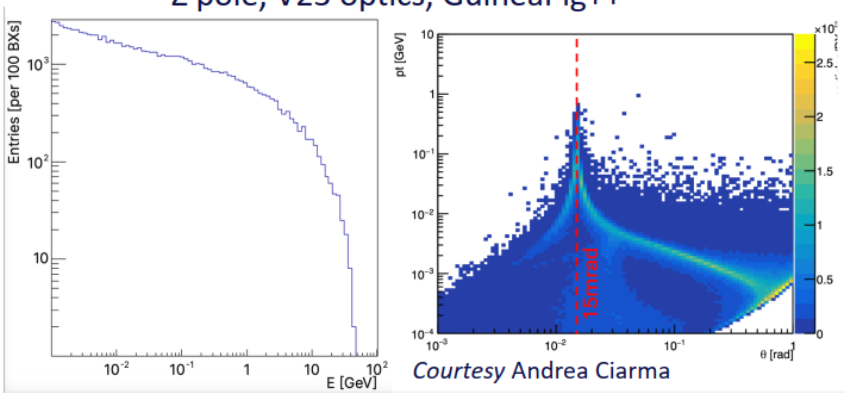




Beam Background

Incoherent Pairs Creation (IPC)

Z pole, V23 optics, GuineaPig++

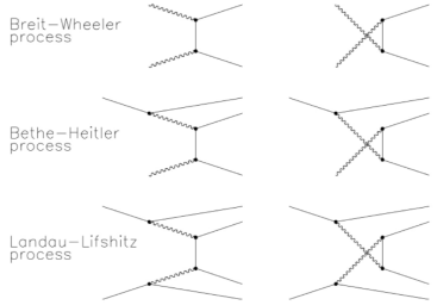


Courtesy Andrea Ciarma

see talk by A. Ilg

- Cluster size of 5, safety factor of 3, 25 μm pitch pixels
- Cut at 1.8 keV of deposited energy (500 e^-)

Secondary e+e- pairs produced during bunch crossing via the interaction of beamstrahlung photons with real or virtual photons.



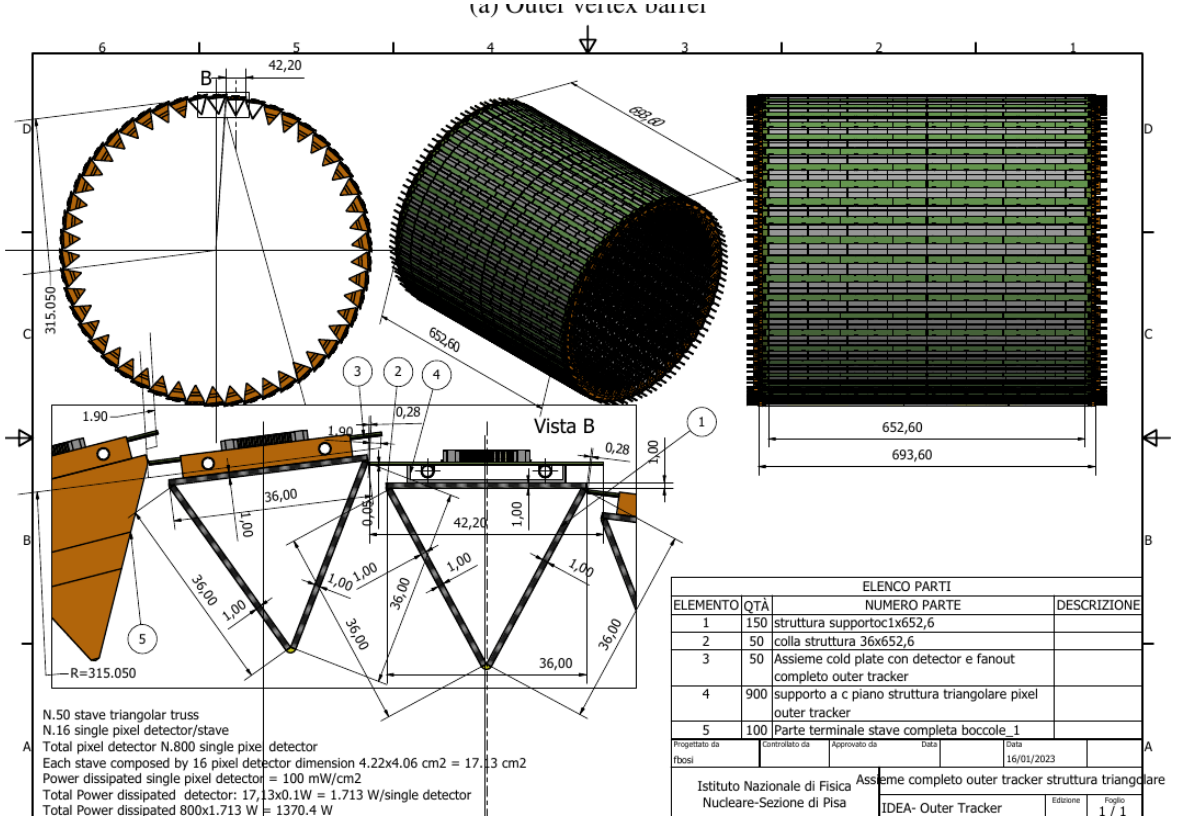
First occupancy and hit rates calculations in the vertex detector

	FCC-ee	ALICE ITS3
Occupancy	$\sim 20\times10^{-6}$	$\sim 30\times10^{-6}$
Hit rate	$170\ MHz/cm^2$	$250\ MHz/cm^2$

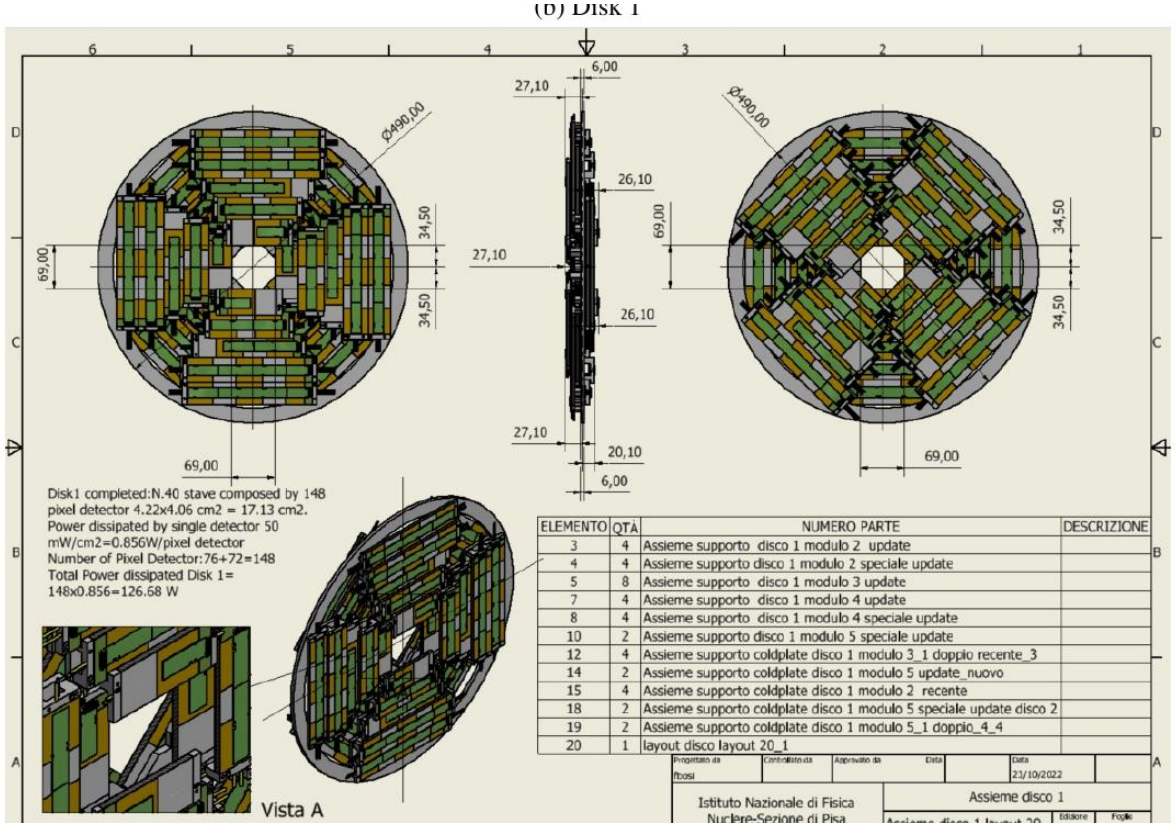
M. Boscolo @ MAPS detector for FCCee Workshop

- **Updated estimates** (IDEA paper)
  - incoherent pair creation is the dominant source
  - innermost vertex layer at the Z pole: **~200 MHz/cm²** (safety factor 3 included)
  - peak annual TID in the inner vertex: a few tens of kGy
  - 1 MeV n_{eq} fluence: a few 10^{13} cm^{-2} (FLUKA)
- Single-beam backgrounds mostly stopped by collimators and absorbers
  - ~1 Gy/year downstream of the IP, ~1 kGy/year at SR absorbers and around the central chamber
- Injection and other incoming-beam backgrounds still to be studied

Outer vertex: engineering layout



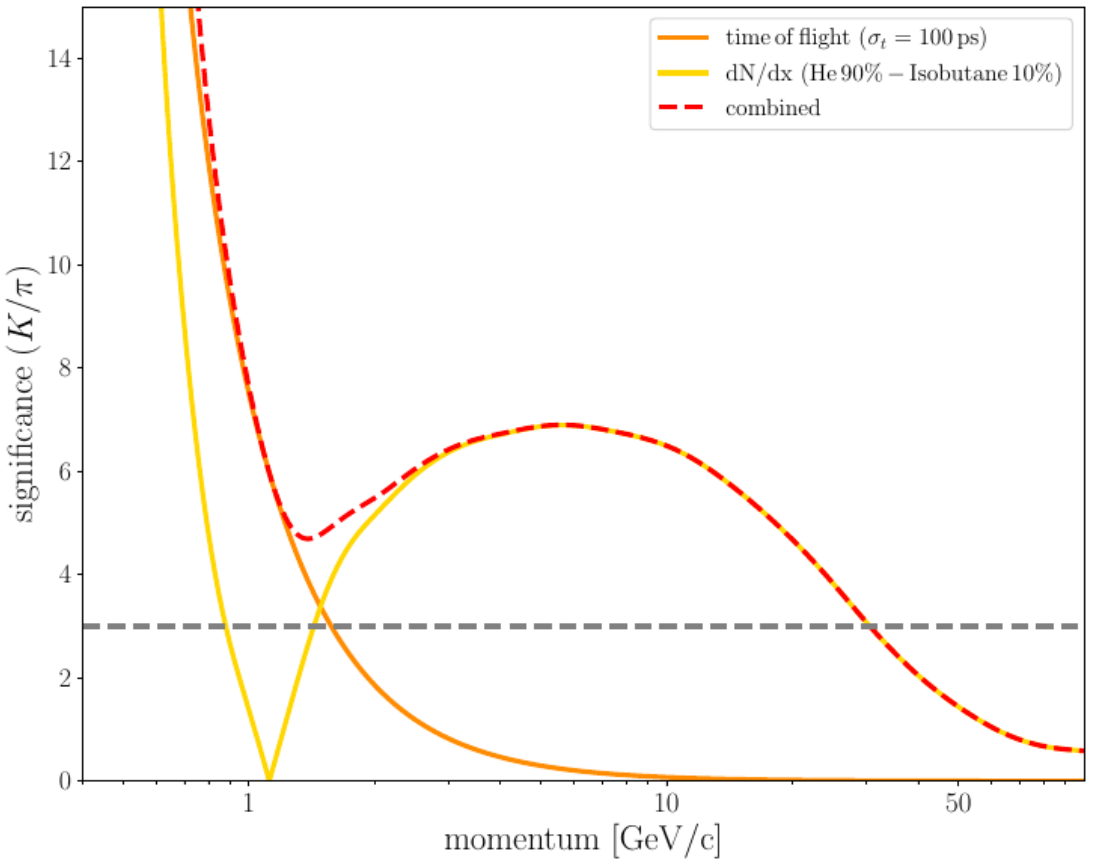
Outer barrel: 51 ladders of 16 modules on triangular carbon-fibre trusses



Disk 1: petals built from the same modules as the barrels

TOF measurement in Si Wrapper

- Particle identification is essential for many physics measurements
  - wide momentum range; K/π separation for flavour tagging and strange tagging
- **dN/dx** (cluster counting) in the drift chamber
  - ≈ 2 times better than truncated-mean dE/dx
  - > 3σ K/π separation up to ~30 GeV/c
  - except 0.9 < p < 1.6 GeV/c, where Bethe–Bloch curves cross
- **TOF** over 2 m covers the gap with O(100) ps
  - LGAD layer in the Si Wrapper: goal ~100 ps per track
  - alternatively a 6 mm LYSO layer in front of the ECAL: ~20 ps for MIPs
  - also crucial for long-lived particle searches



K/π separation: cluster counting, 100 ps TOF over 2 m, combined

Can it be implemented in the Si Wrapper without compromising the spatial resolution?