Development of HVCMOS-based CEPC/AGORA Silicon Inner Tracker

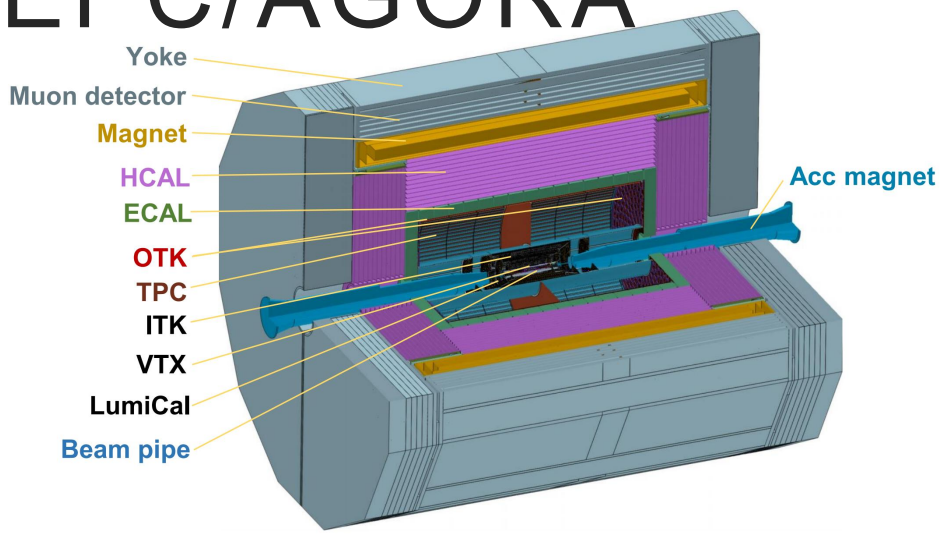
徐子骏 Zijun Xu (IHEP, CAS)

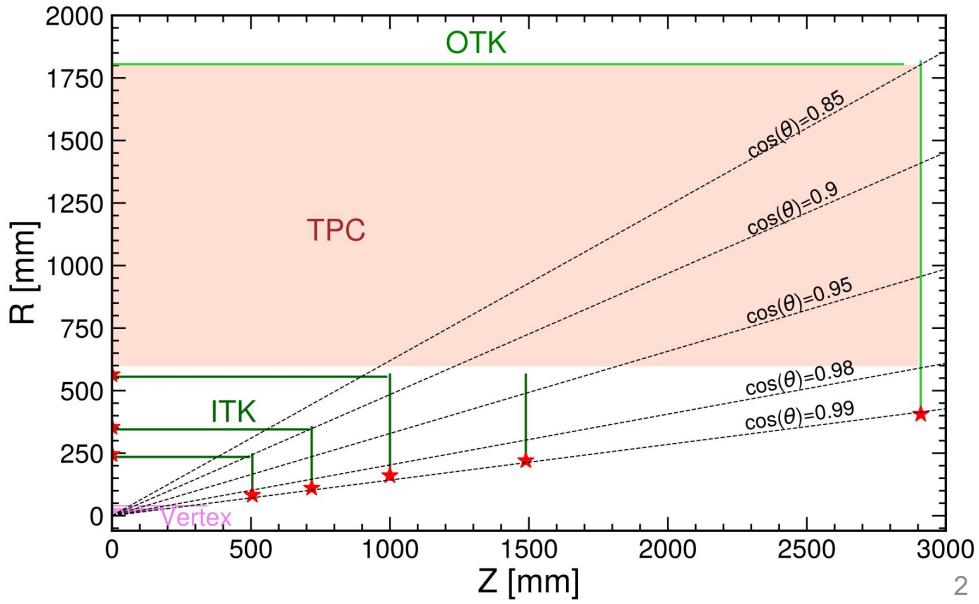
on behalf of CEPC/AGORA-ITk collaboration

CEPC workshop, 2026-Oct-22, Shanghai

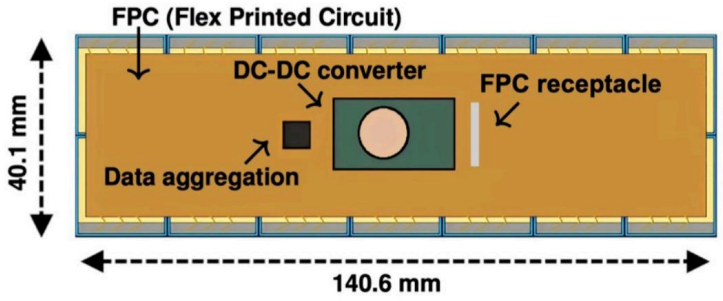
Silicon Inner Tracker for CEPC/AGORA

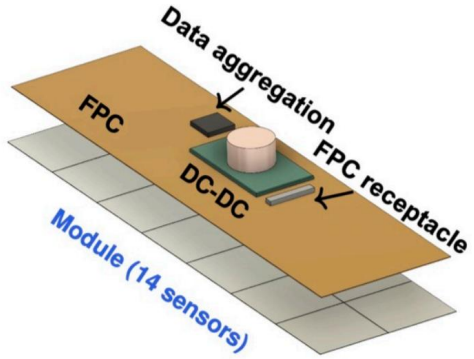
- CEPC TDR for Reference Detector, arXiv:2510.05260
- Large area silicon tracker, ITk ~20 m^2
- spatial resolution of ~8 μm in the bending direction from requirement on momentum resolution
- timing resolution of 3~5 ns to tag bunch-crossings
- low material budget
- moderate power consumption

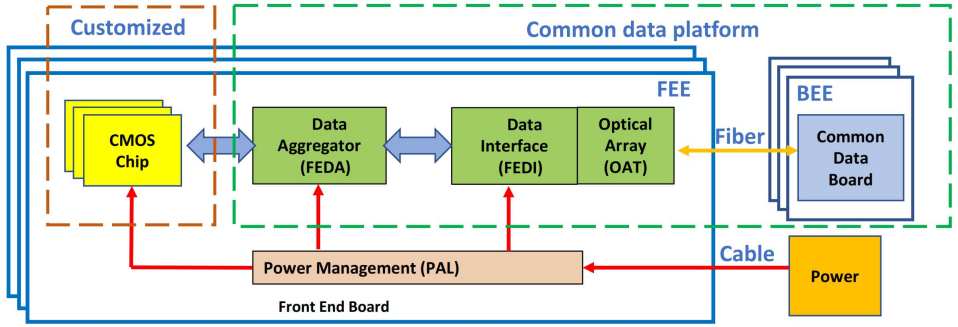


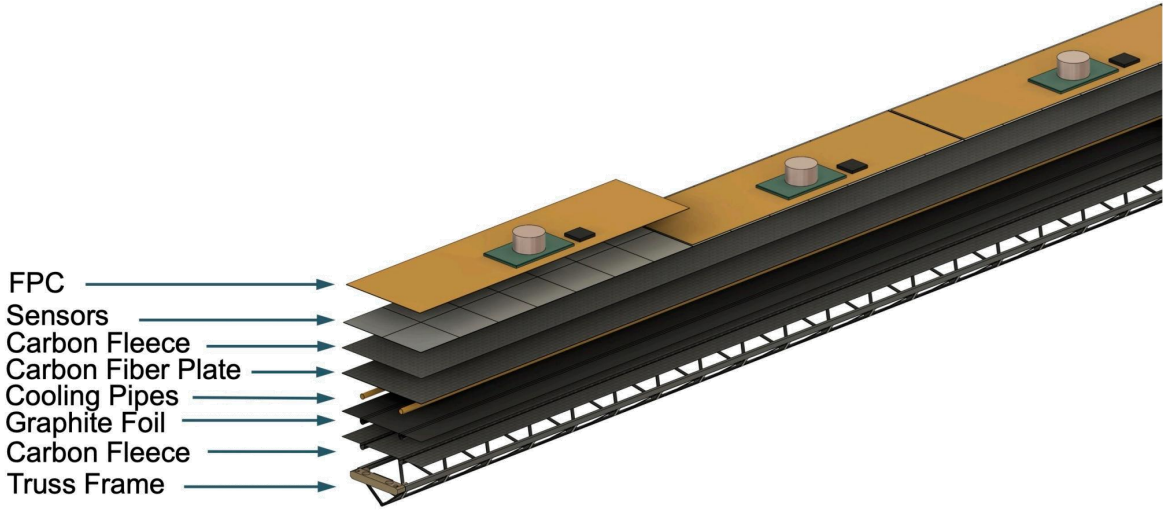


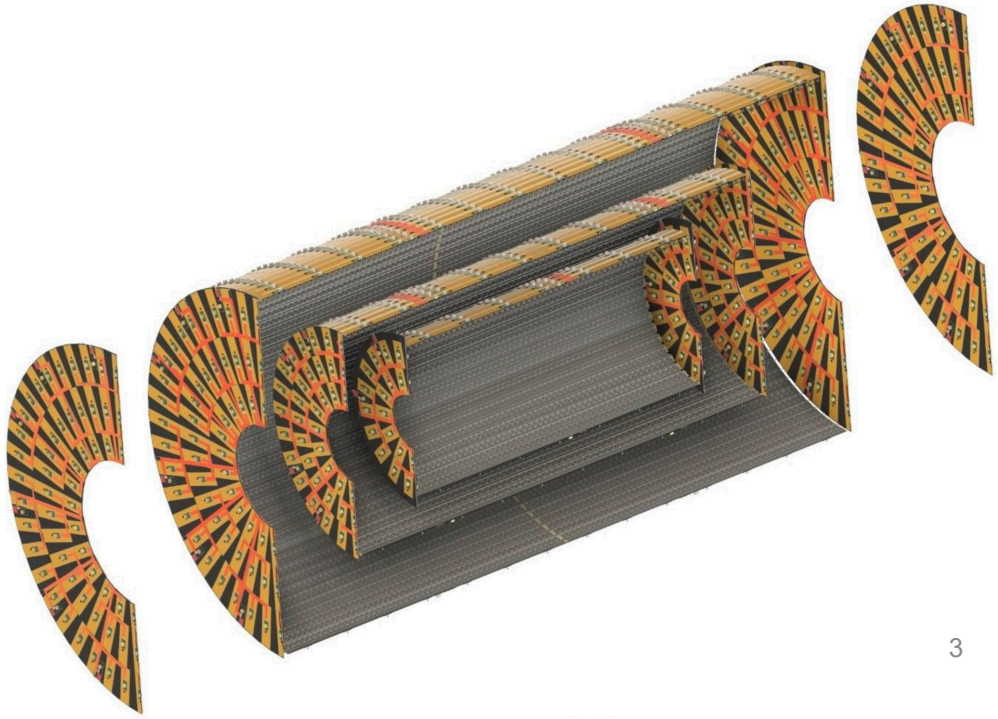
MAPS-based Silicon ITk for CEPC/AGORA





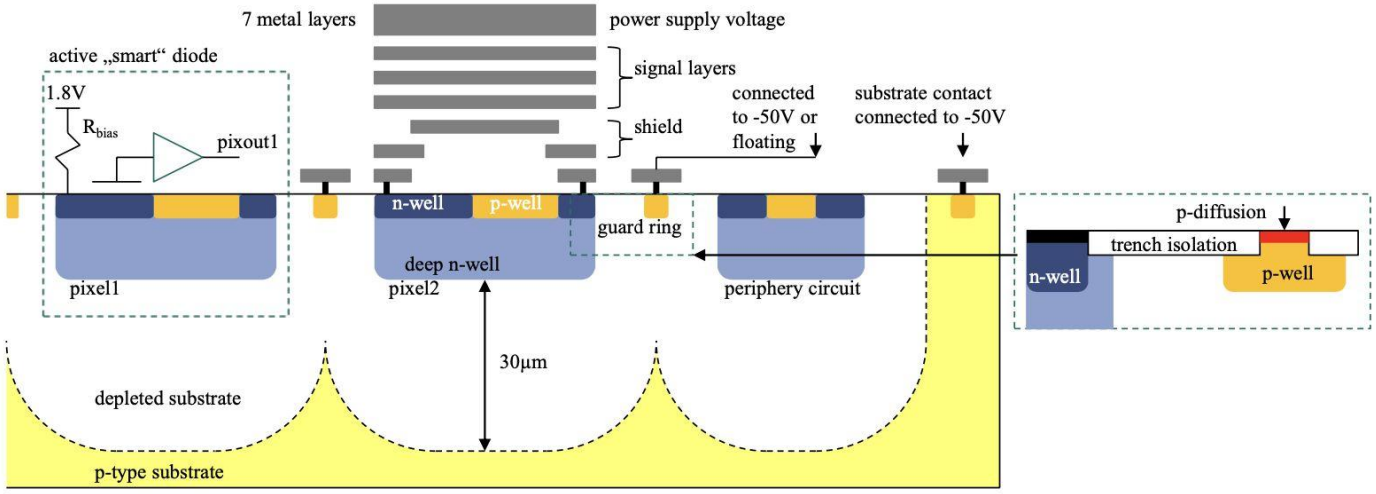






HV-CMOS for Monolithic Active Pixel Sensors

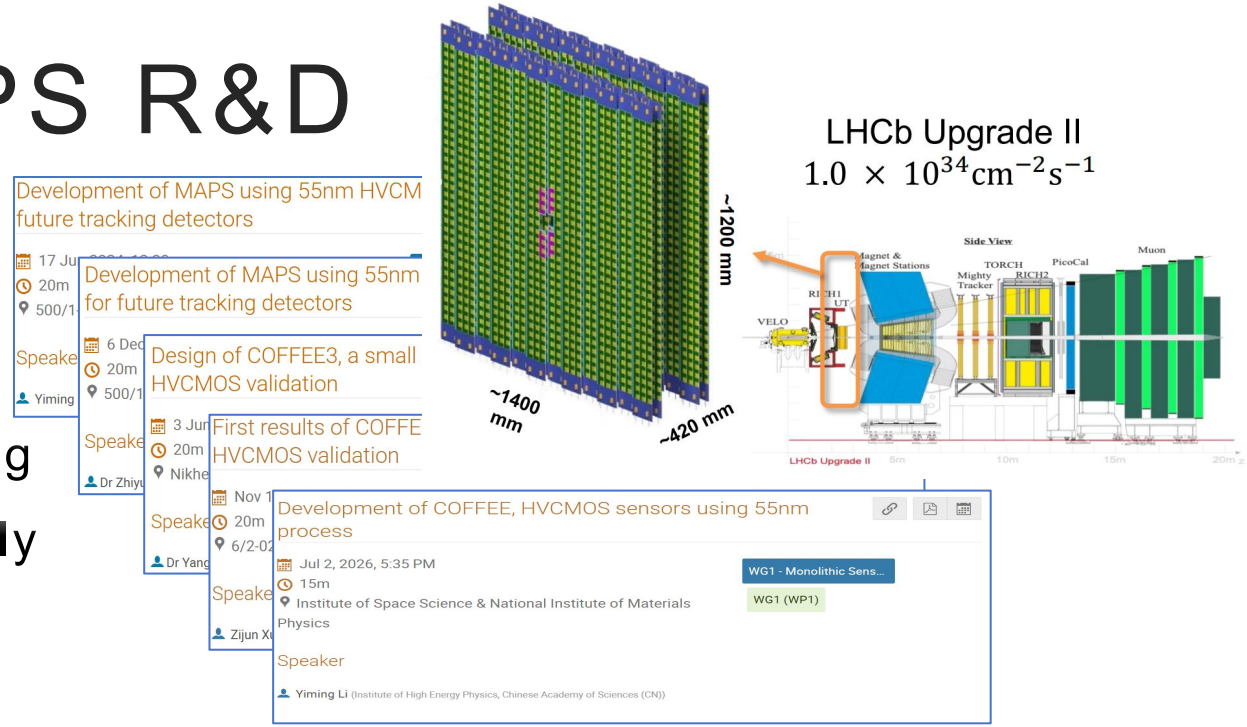
- **full depletion** possible due to large electrode
- intrinsically **radiation hard**
- **fast** charge collection
- **cost-effective**: based on commercially available process
- relatively larger capacitance noise, power



- ATLASPix3 as example, link

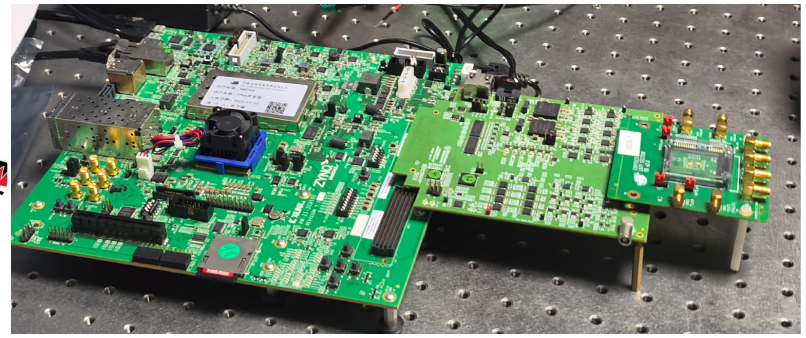
Collaborations for MAPS R&D

- actively involved in CERN activities
  - DRD3, LHCb upgrade, ...
  - test-beam and irradiation facilities sharing
  - joint serial powering R&D with US/UK/Italy
  - joint aluminum flex R&D with Italy/UK
  - ...



- Caribou DAQ for MAPS R&D
  - open source hardware/firmware/softwar
  - FE chip specific carrier board, firmware software IP blocks by ourself
  - as a user, keep reporting bugs and solutions





CMOS sensOr in Fifty-FivE nm procEss (COFFEE)

COFFEE

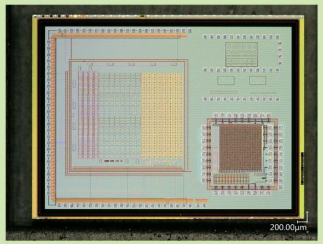
CMOS SENSOR IN FIFTY-FIVE NM PROCESS

NIM A1069 (2024) 169905
JINST 20 (2025) C10011

COFFEE 2

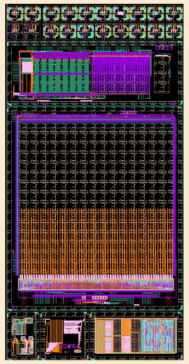
First HVCMOS 55nm prototype chip

- Breakdown at -70V
- Responsive to laser, X-/beta-ray sources



CHiR (COFFEE-HiRes)

- Validation of process modification
- Key design feature

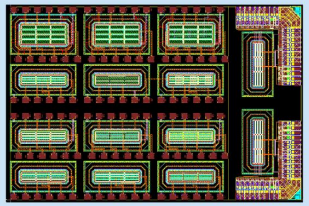


Quarter-size chip submission

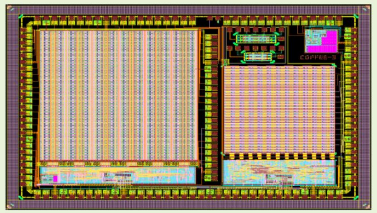
… | 2022 | 2023 | 2024 | 2025 | 2026 | 2027

Submission timeline

COFFEE1
- Prototype in LL process
- Validation of deep N-well structure



COFFEE3
- Two pixel arrays with data-driven readout
- Designed for good timing resolution and moderate power consumption



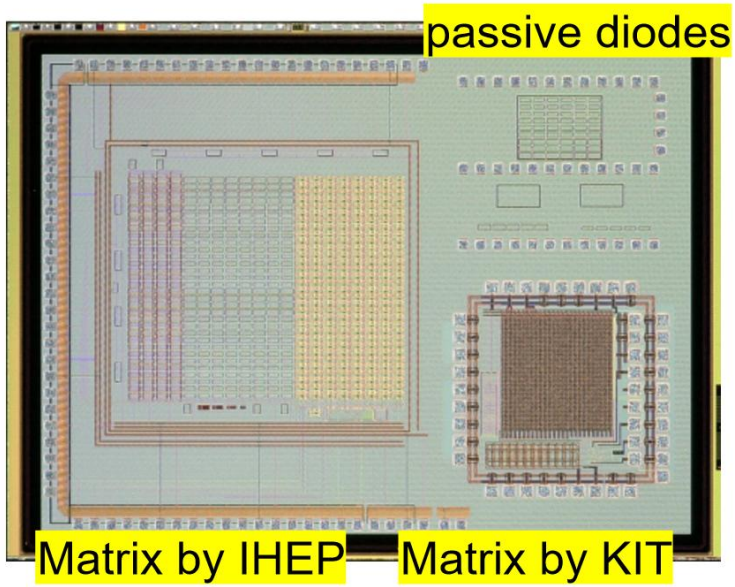
Full size chip with all functionalities implemented planned ~end 2027

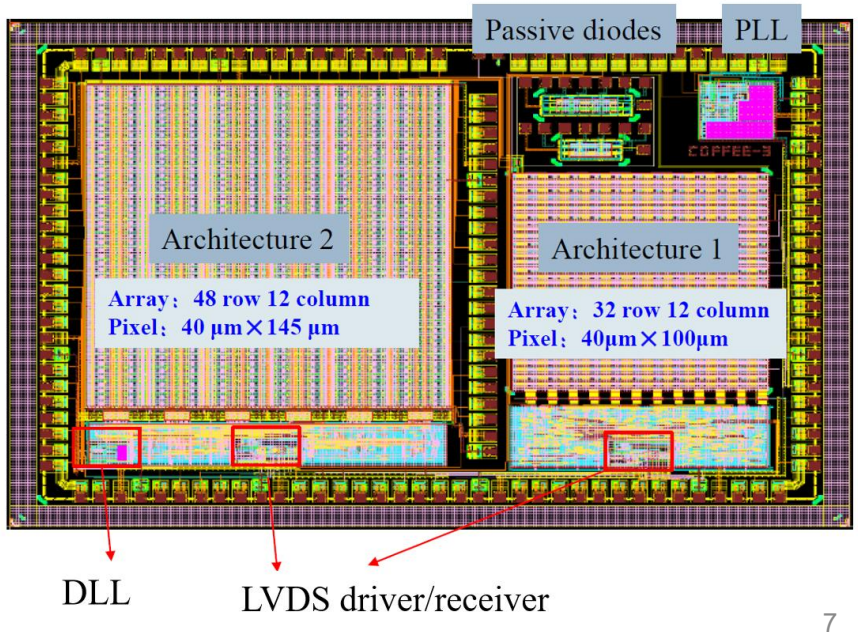
COFFEE chips

- COFFEE2
  - Passive diode for sensor charactizing
  - R&D for pixel electrode structure, in-pixel Amplifier and comparator

JINST, 2024, 19(4): C04059
JINST, 2025, 20(10): C10011
JINST, 2026, 21(4): C04078
JINST, 2026, 21(4): C04075
NIMA, 2024, 1069: 169905
NIMA, 2026, 1092: 171919
NIMA, 2026, 1092: 171886
NIMA, 2026, 1089: 171574
...

- COFFEE3
  - PLL, DLL, LVDS IP accumulation
  - architecture 1:NMOS design in-pixel. Less X-talk between analog and digital circuits
  - architecture 2: CMOS design in-pixel. Advanced readout design, more suitable for high hit density environment



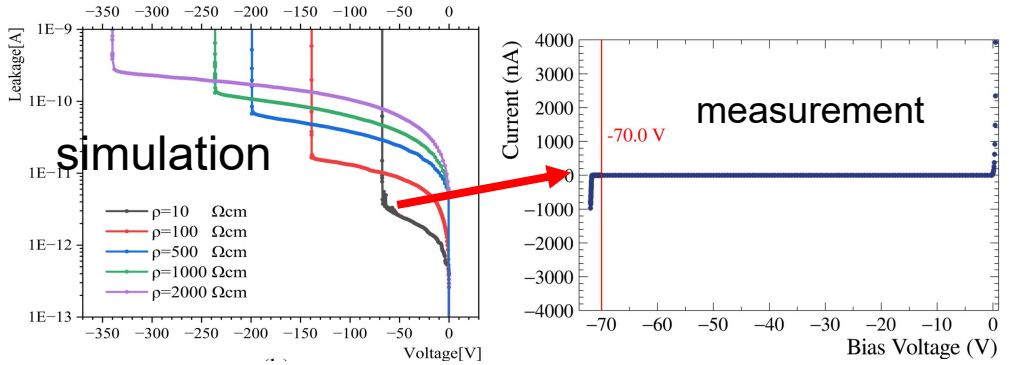


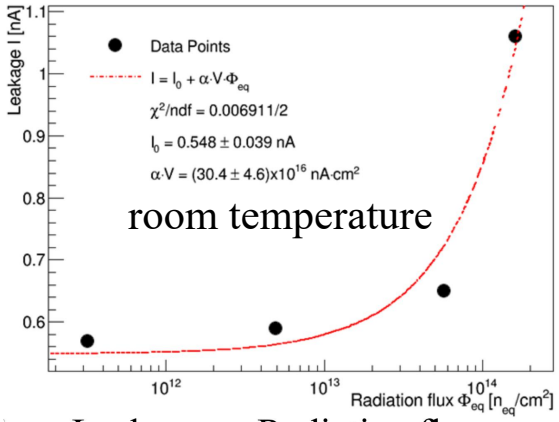
MPW chip size ~ 3×4 mm^2

Sensor (charge sensing diode)

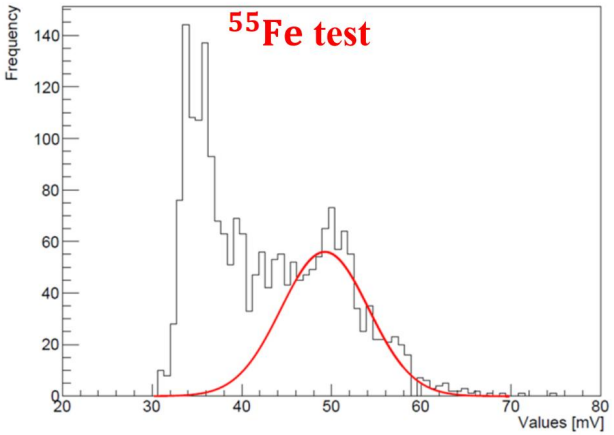
- COFFEE2/3 got consistent sensor IV/CV performance
  - consistent with TCAD simulation
  - V(Breakdown) ~ 70V for 10 Ω·cm resistivity wafer
  - irradiation: 80MeV proton@CSNS/APEP; X-ray @IHEP/Zhejiang Univ.
- sensor depletion depth only ~10 μm from simulation, and inferred from radiation source (^{55}Fe vs ^{90}Sr) study of COFFEE2
  - high resistivity wafer will increase break-down voltage

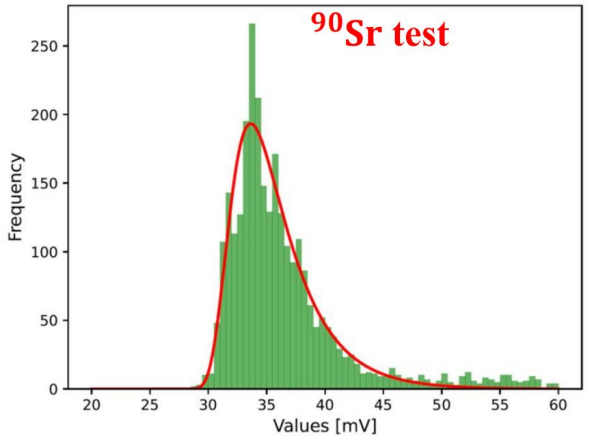
    => increase depletion zone, reducing capacitance noise

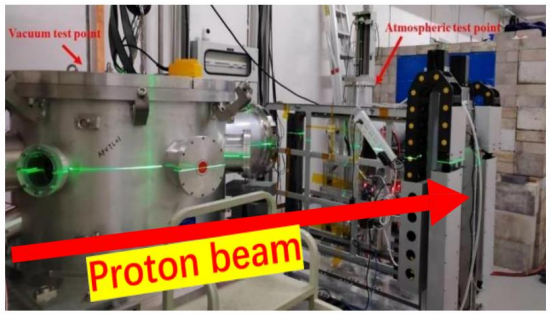




Leakage vs Radiation flux





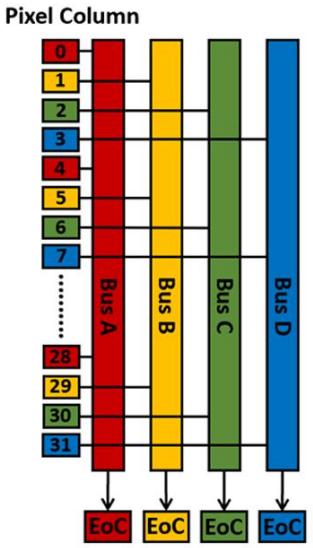


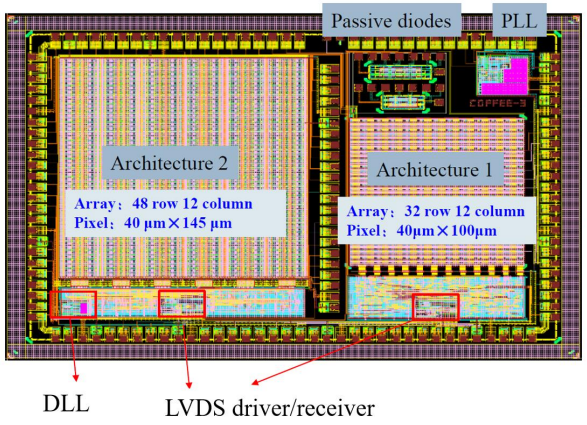


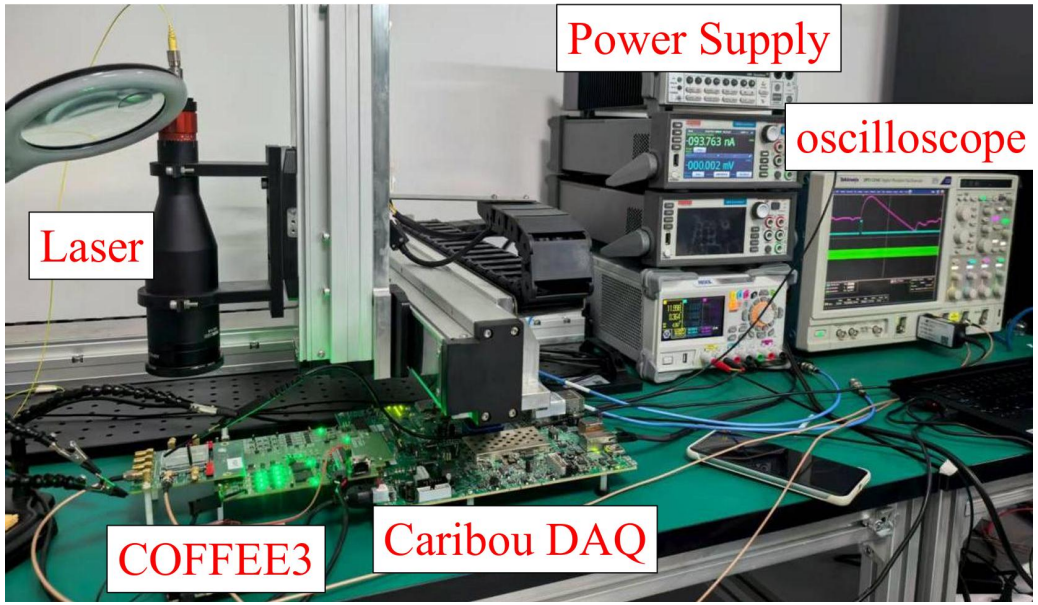
[Fan Hu's](#) poster

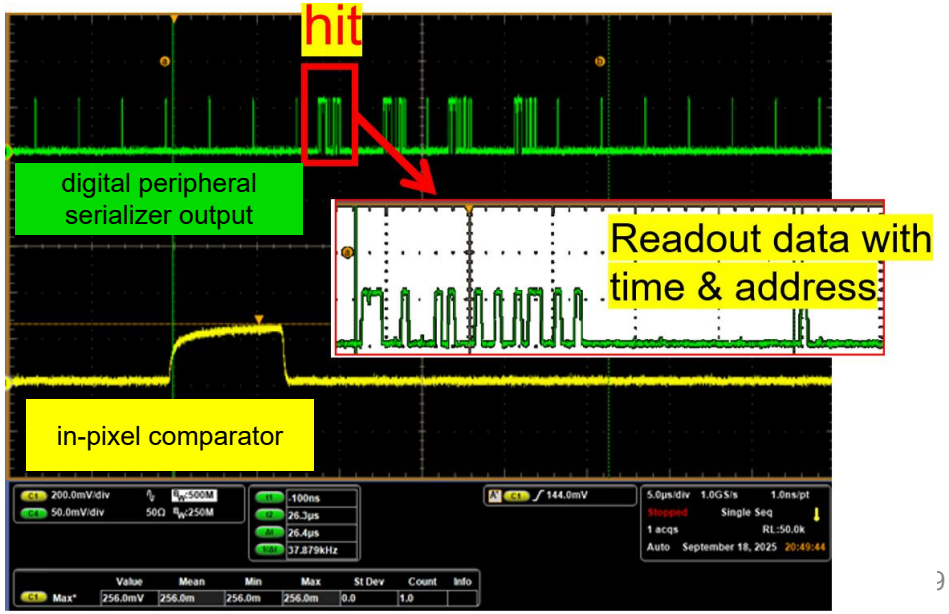
COFFEE3 Pixel-matrix-1

- in-pixel circuit + digital peripheral responsing to global charge injection and laser injection
  - digital readout schemes optimized for high hit density



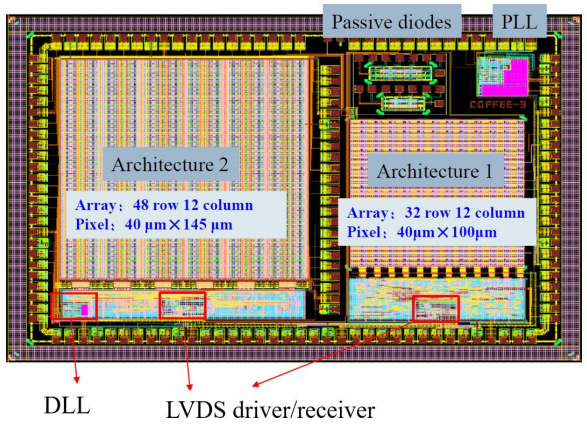


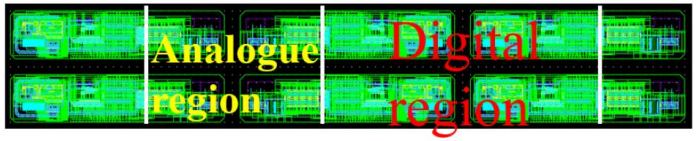




COFFEE3 Pixel-matrix-2

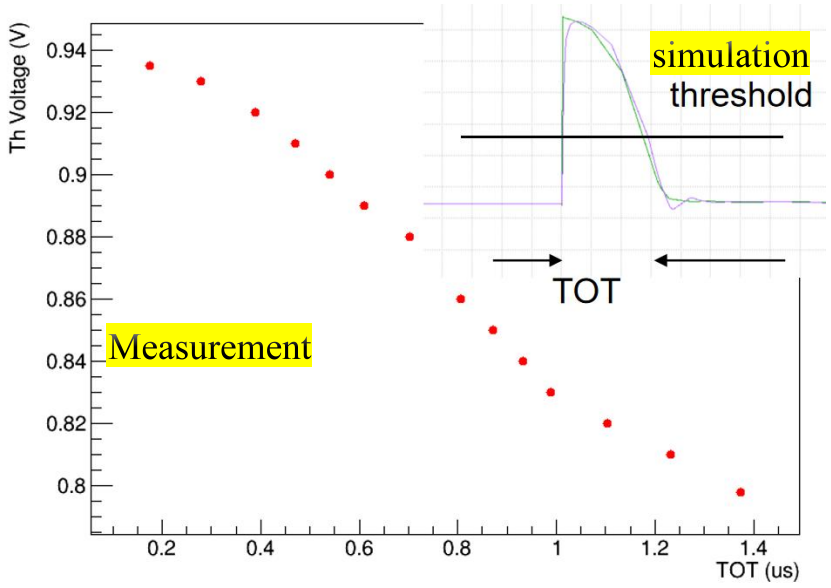
- In-pixel CSA and comparator output for laser signal and ^{55}Fe source (6 keV X-ray)
  - time-over-threshold (TOT) ~ 1 us, agree with simulation

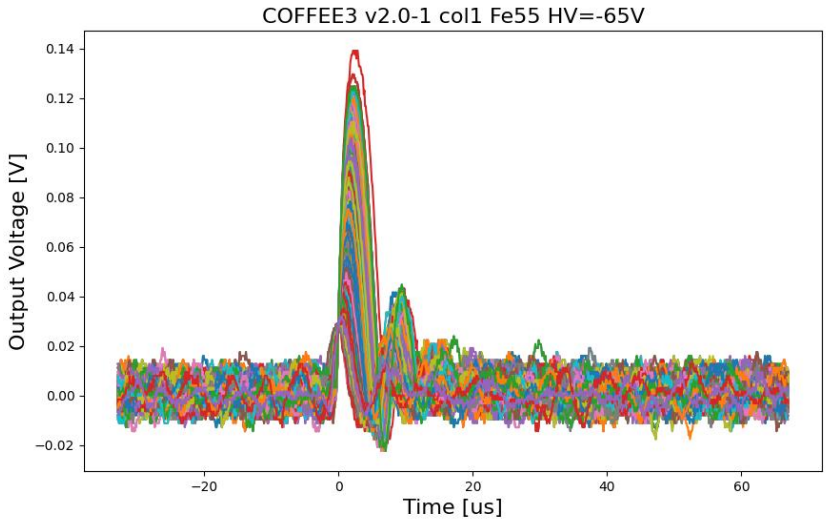




Layout of 2×3 pixels， signal pixel size is 40×145 μm^2

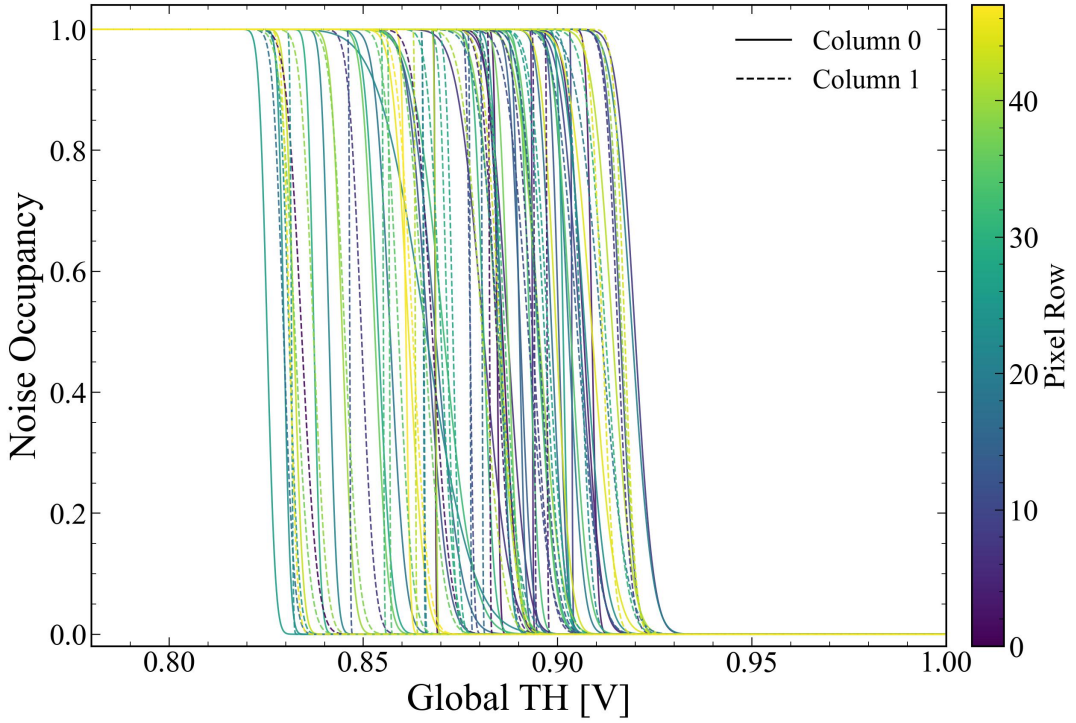
The actual manufacturing size will be scaled down to 0.9 times the layout size.

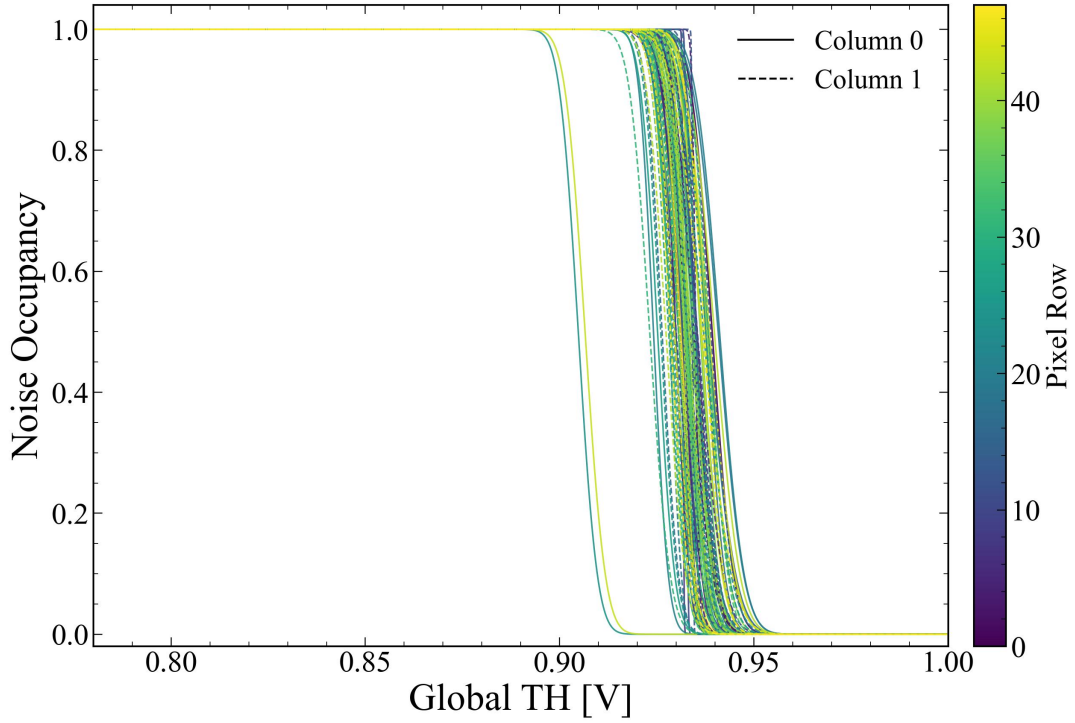




COFFEE3 Pixel-matrix-2

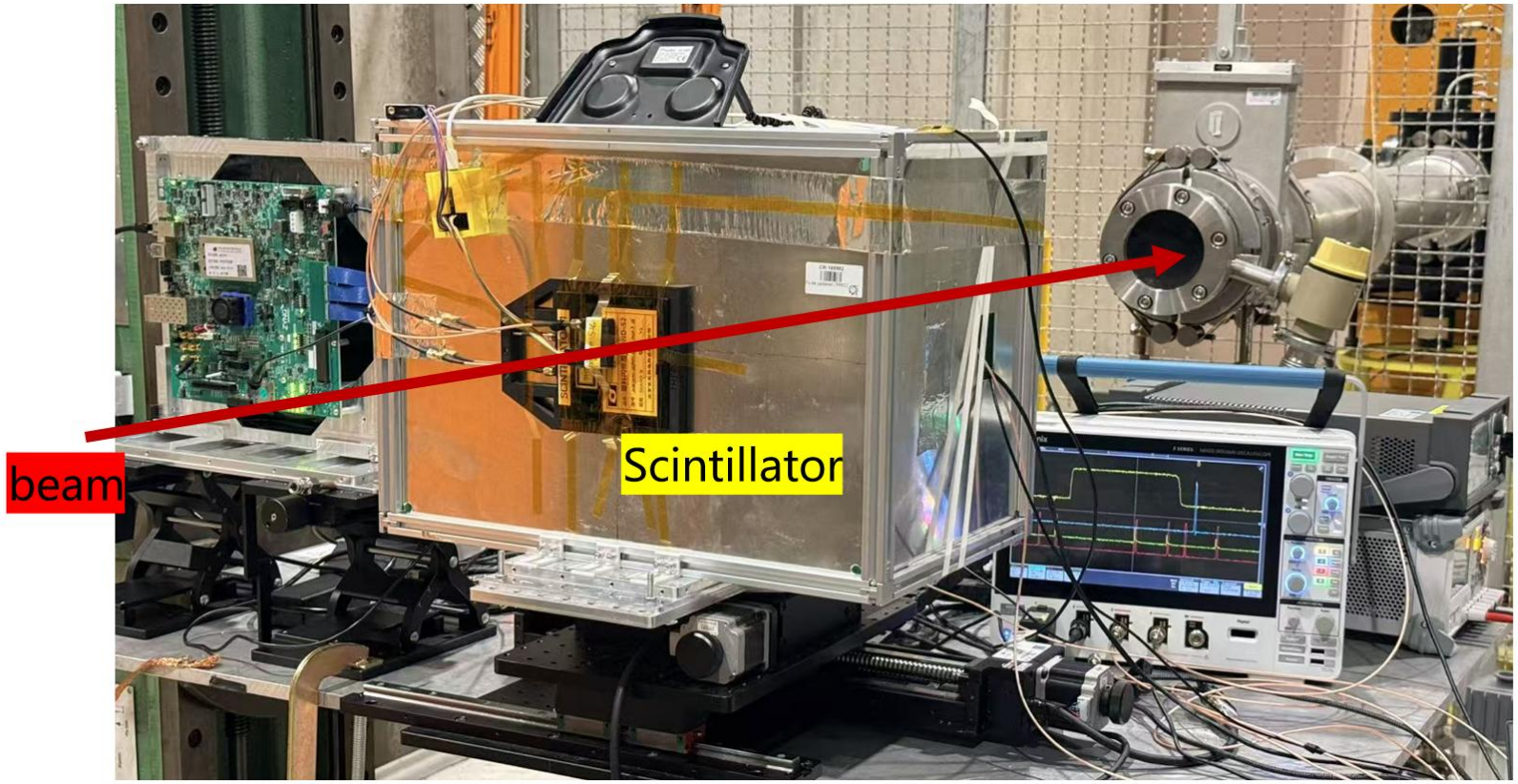
- Global Threshold for all pixels
- in-pixel 4-bit TDAC: tuning local Threshold to compensate individual differences

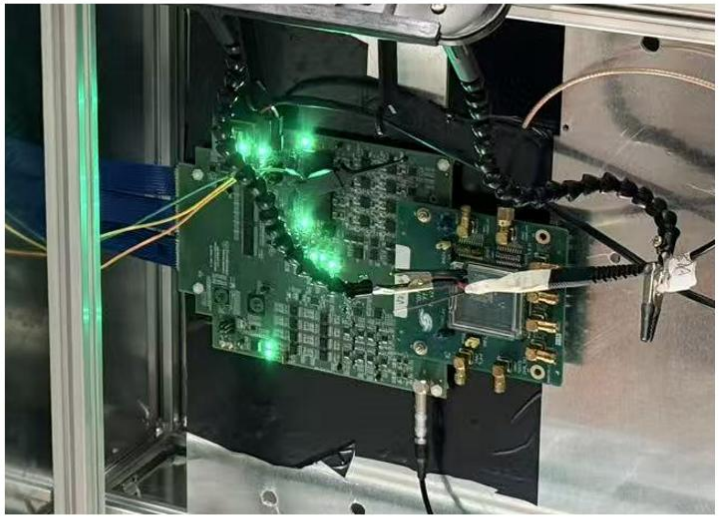




COFFEE3 testbeam

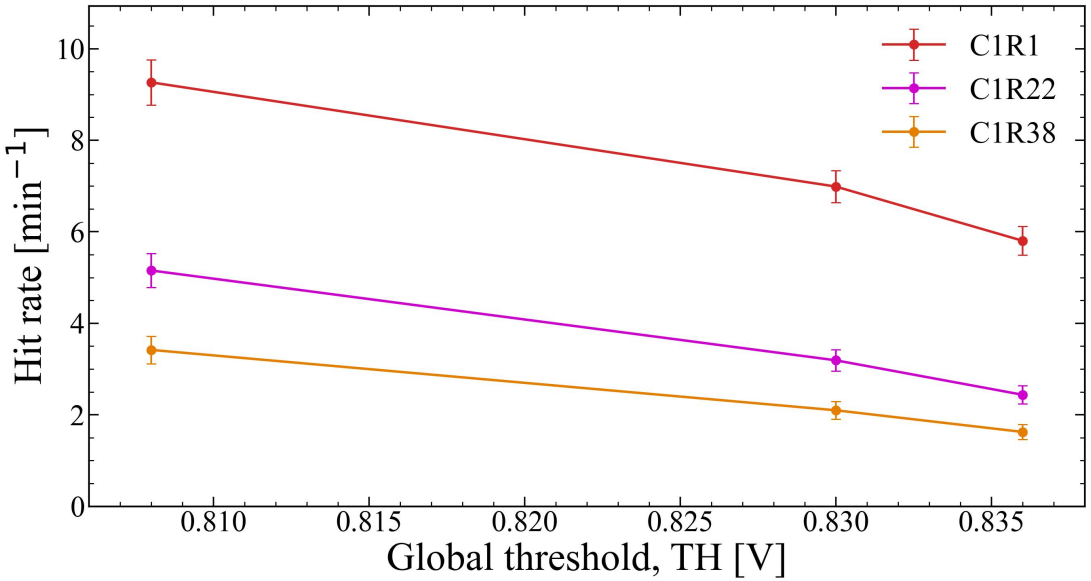
- 2026, CERN SPS, mix hadron, ~180 GeV/c

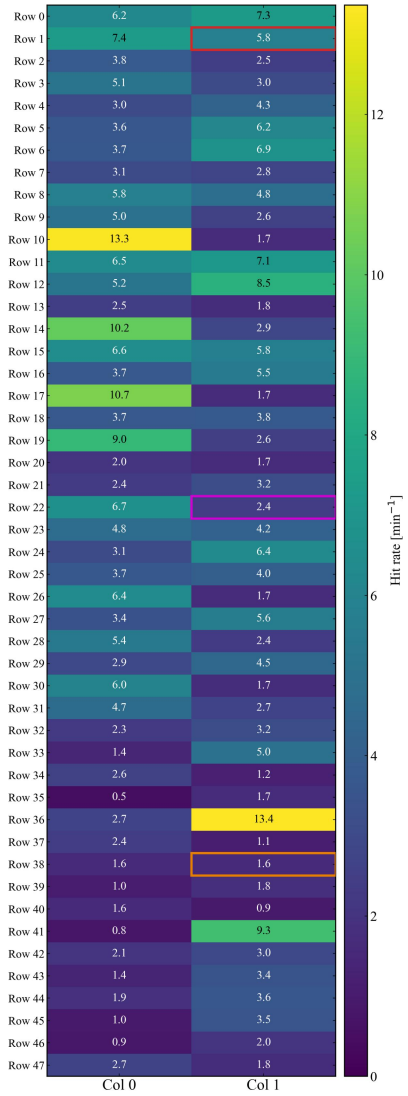




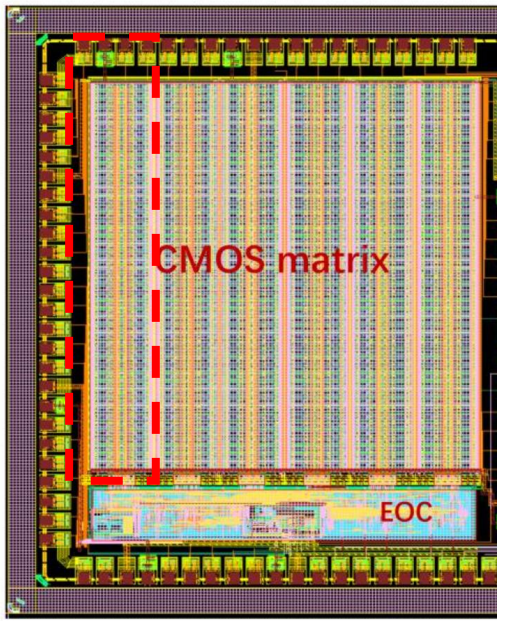
COFFEE3 testbeam: preliminary results

- 2026, CERN SPS, mix hadron, 180GeV/c
- all pixels alive, a few are noisy
- readout architecture is verified
- Global Threshold function is verified
- sensor performance will be improved with high-R wafer





- 2 columns 96 pixels tested



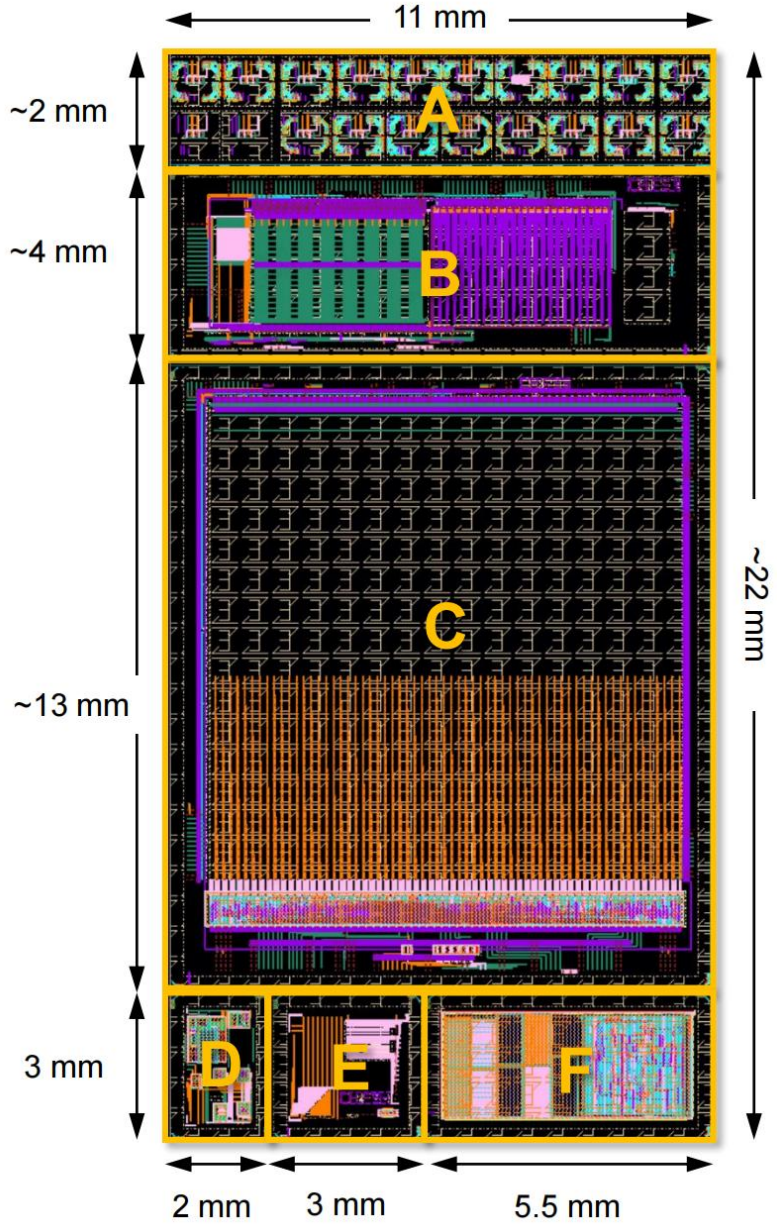
[Yuman Cai's](#) poster

Process improvement: CHiR

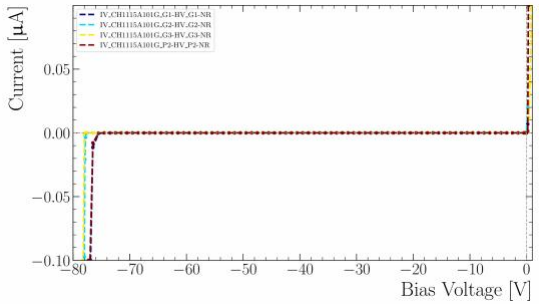
- Encouraging testing results from COFFEE2/3
  - but sensor breakdown voltage and cross-talk are not ideal
- process modification + high-R wafer is needed

- CHiR (COFFEE-HiRes) design goal
  - Priority: to validate the process with high-res wafers
  - 1k/2k/4k Ohm cm wafers available from two manufactures
  - Radiation effects of simple components (eg. MOS) with or w/o radiation hardening
  - Implementation of “Five-well process”: to validate basic IP not affected by process modification

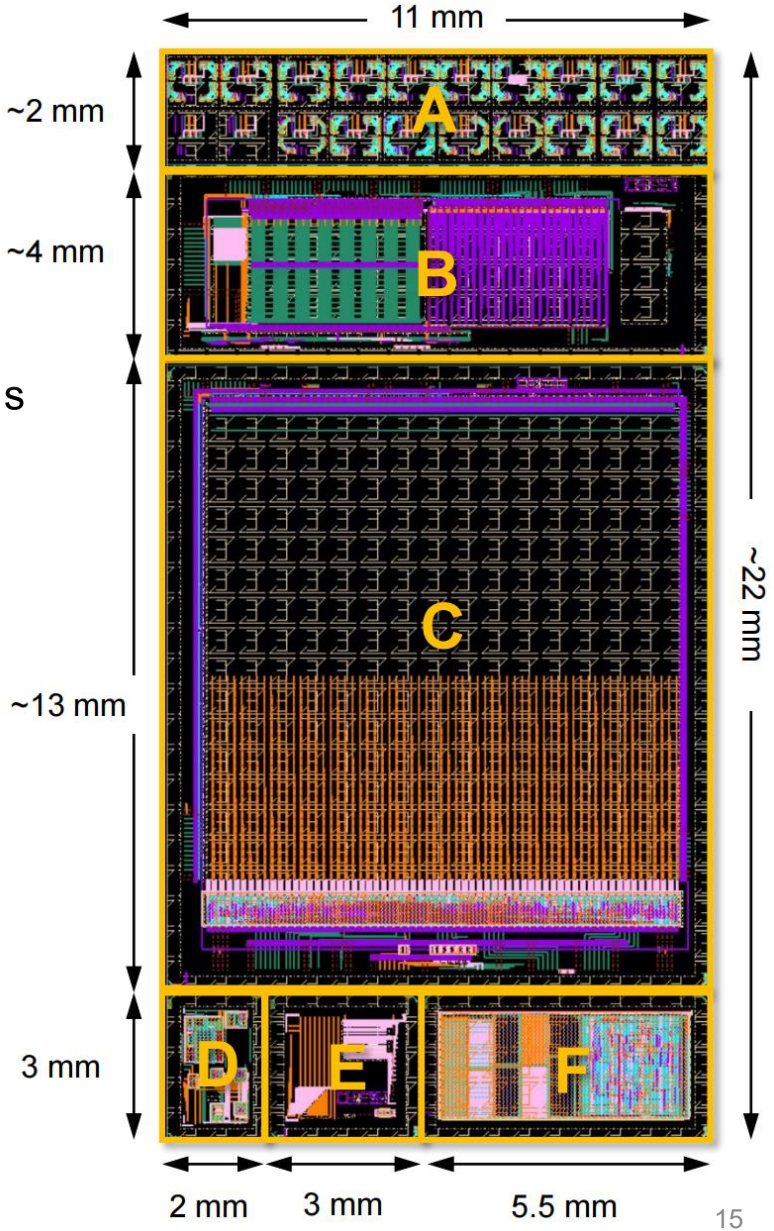
[Bingchen Yan’s](#) poster



CHiR1 chip(s)



- Passive sensor validation:
  - IV from normal wafer is consistent with COFFE2/COFF3
  - A: 20 arrays of 3x4 passive pixels with diff guard ring designs
  - Pixel size: 38 um x 175 um
- Pixel array design
  - B: 9 variations of in-pixel frontend designs
  - C: main pixel array of 256 x 64 pixels;
  - E: alternative small pixel arrays
- IP validations
  - D/E: shuntLDO, PLL, DLL, LVDS, ...
  - F: digital modules and transistors for TID and SEE studies
- Submitted in early 2026, testing results is on-the-way



COFFEE/ChiR Team keep increasing

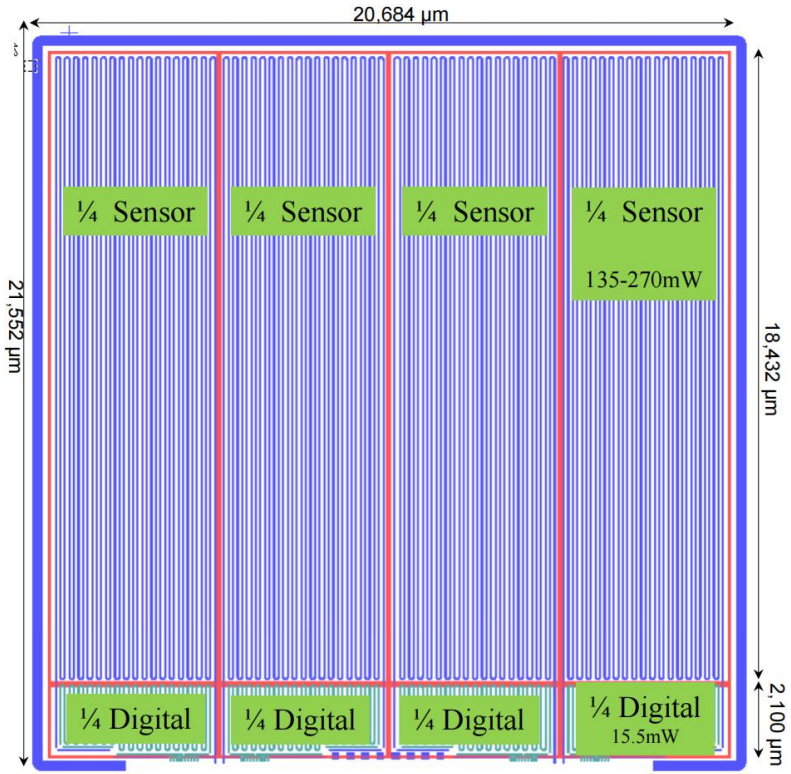
Name list: Random ranking

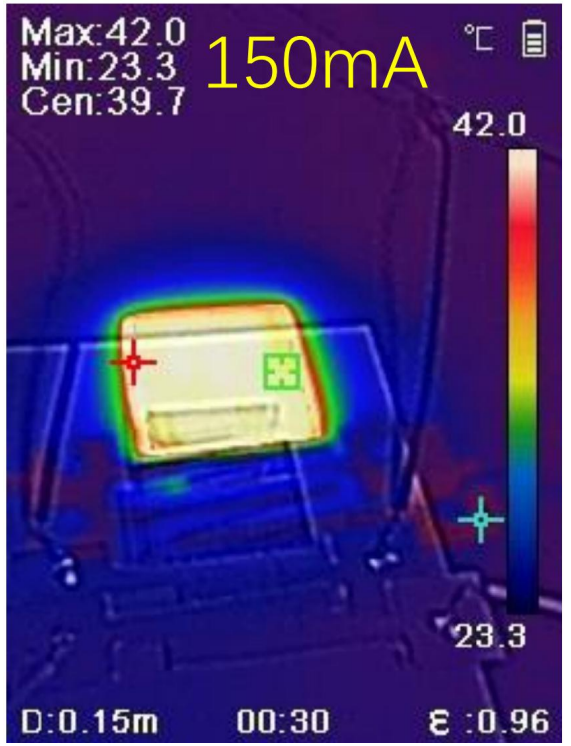
Leyi Li, Xiaoxu ZHANG, XiaoMin WEI, Weiguo LU, Pengxu LI, Mei ZHAO, Bingchen Yan, Anqi WANG, Yuanhong JIAO, Yujie WANG, Huimin Wu, Zexuan ZHAO, Yu ZHAO, Zheng Wei, Jianpeng DENG, Zhan SHI, Kunyu XIE, Xinhao XIE, Xiaolong WANG, Ziying ZHANG, He HUANG, Qinyu Bao, Junyuan YAN, Shenyao TANG, Hui ZHANG, Ruoshi DONG, Yang CHEN, Xuekang LI, Xinyang GUO, Zhuojun CHEN, Zhiyu XIANG, Zijun XU, Zeng CHENG, Kang LIU, Menke CAI, Boxing WANG, Yuman CAI, Mingjie FENG, Xingyu TONG, Tianyu LIANG, Tianyu SHI, Qinze LI, Congcong WANG, Yuan YUAN, Yiyang Pan, Fan Hu, Xiaoming DENG, Yihang GUO, Xiaokong LAI, Kai CHEN, Lei ZHANG, Meng WANG, Hongbo ZHU,Yang ZHOU, Yiming Li, Jianchun WANG ……..

& **Independent KIT design in COFFEE2**: Hui ZHANG, Ruoshi DONG, Ivan PERIC;

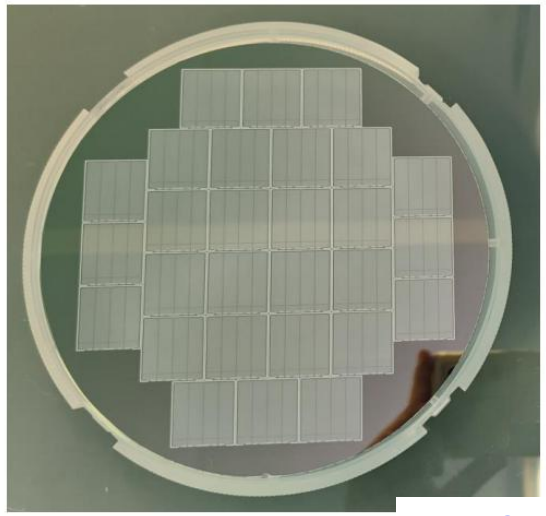
Dummy MAPS

- silicon chip with resistors inside for mechanics/thermal/integration R&D
  - material, chip size, powering/GND pads, and power consumption are consistent with real MAPS

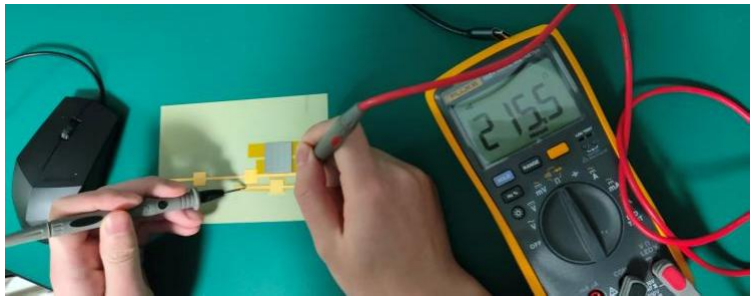




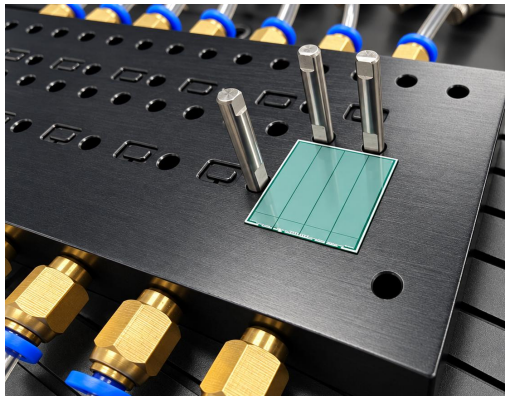
6-inch wafer

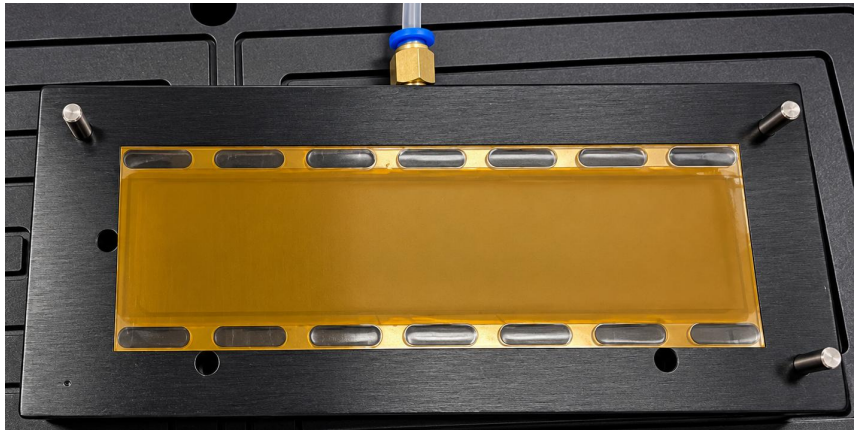


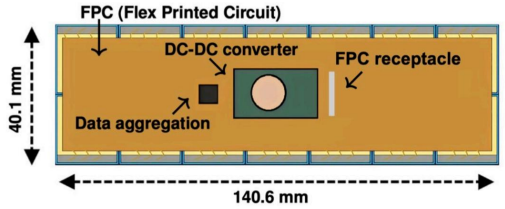
By Congcong Wang

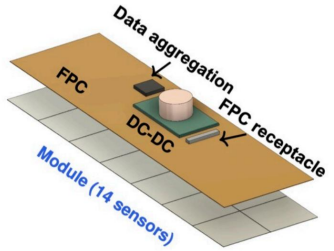


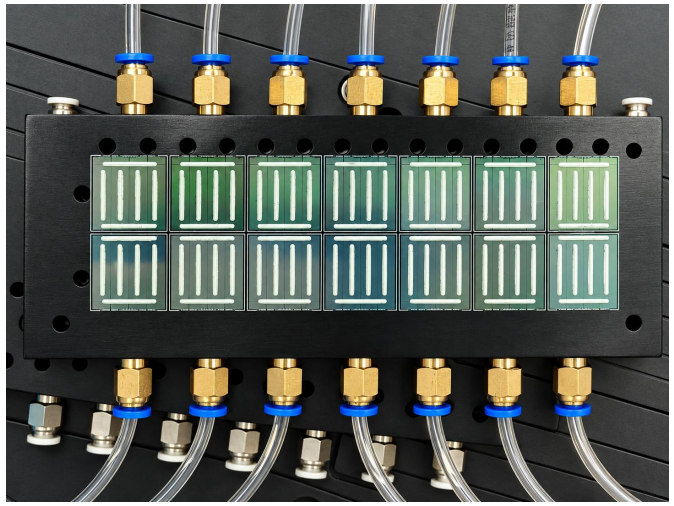
CEPC ITk modules assembly



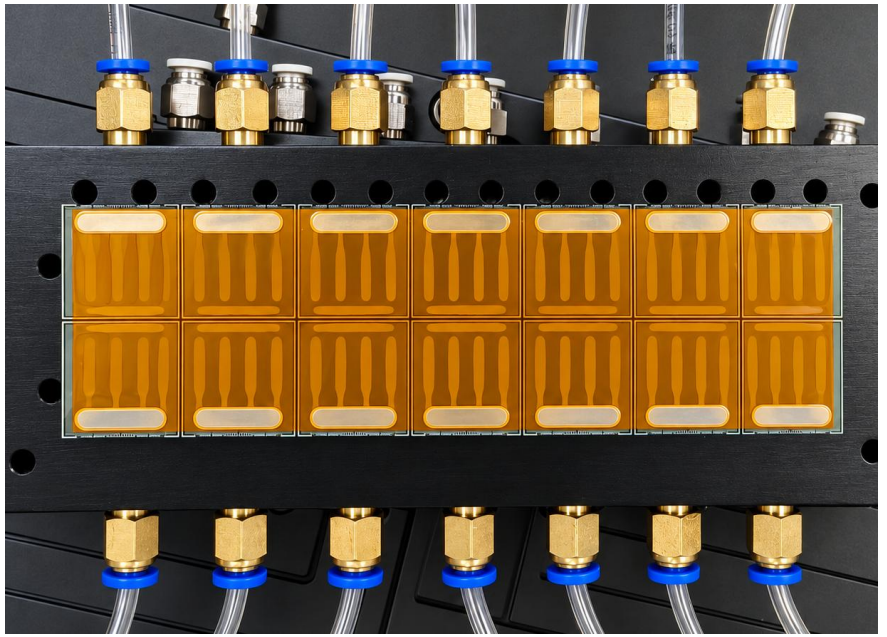






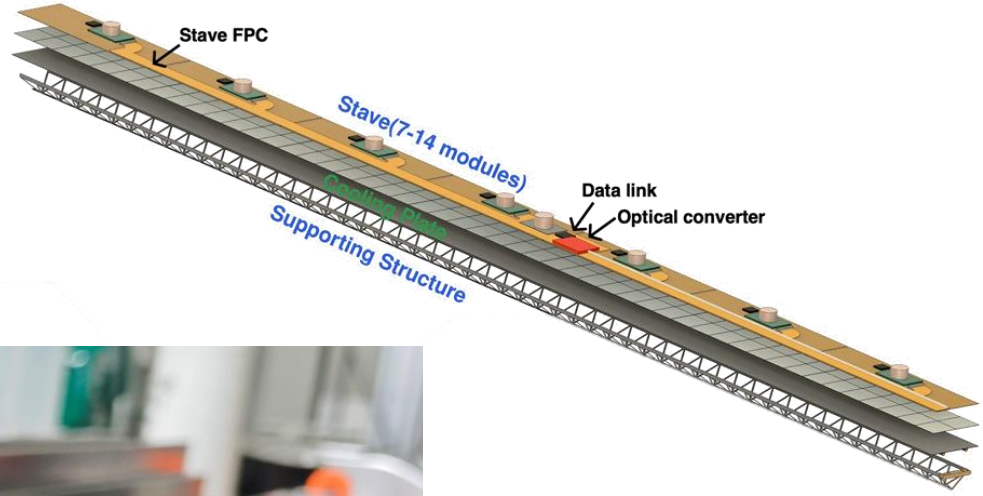


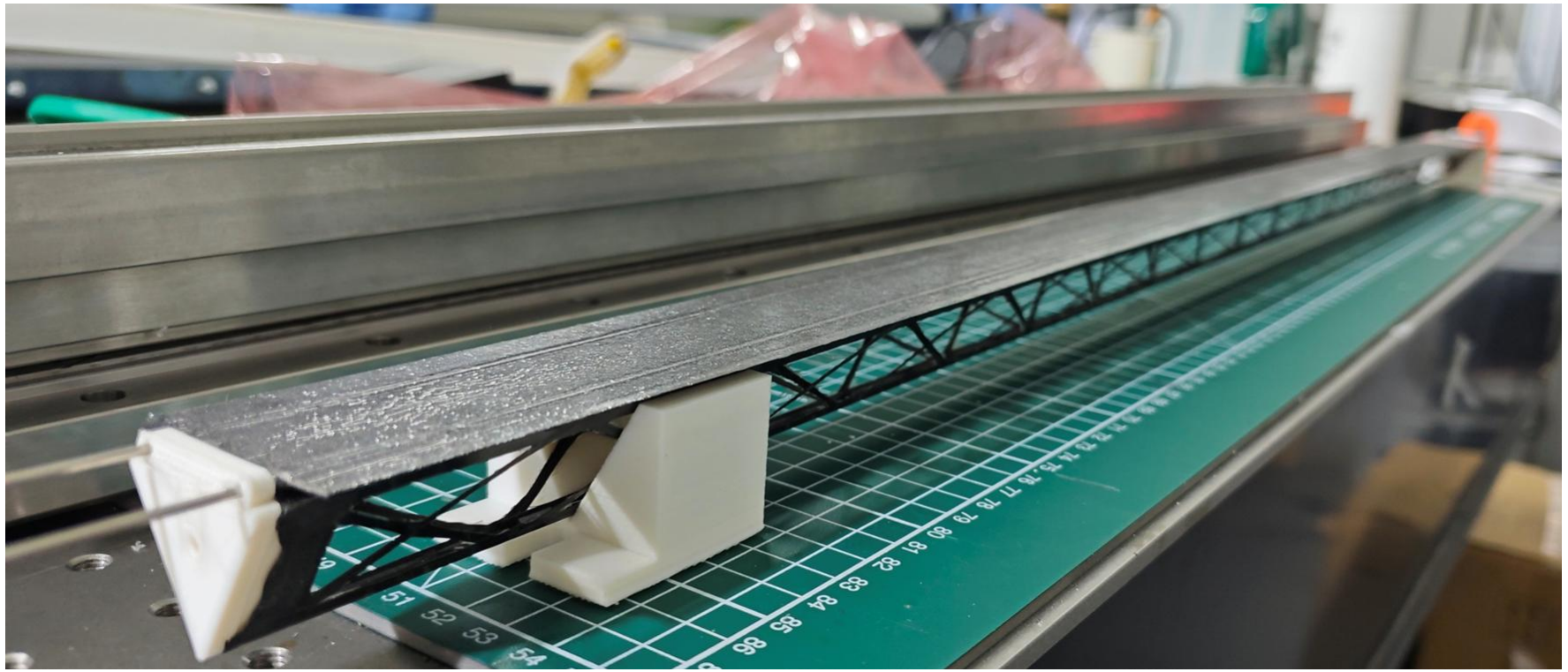




[Xiaoming Deng](#)'s poster

CEPC ITk Stave design

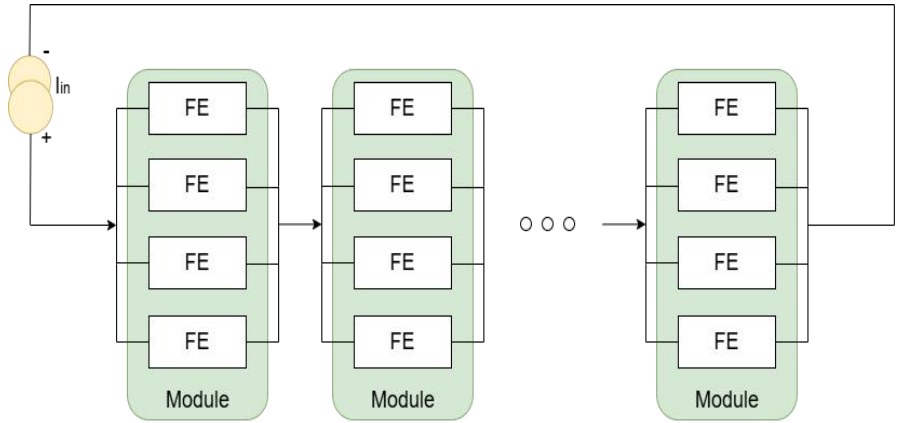


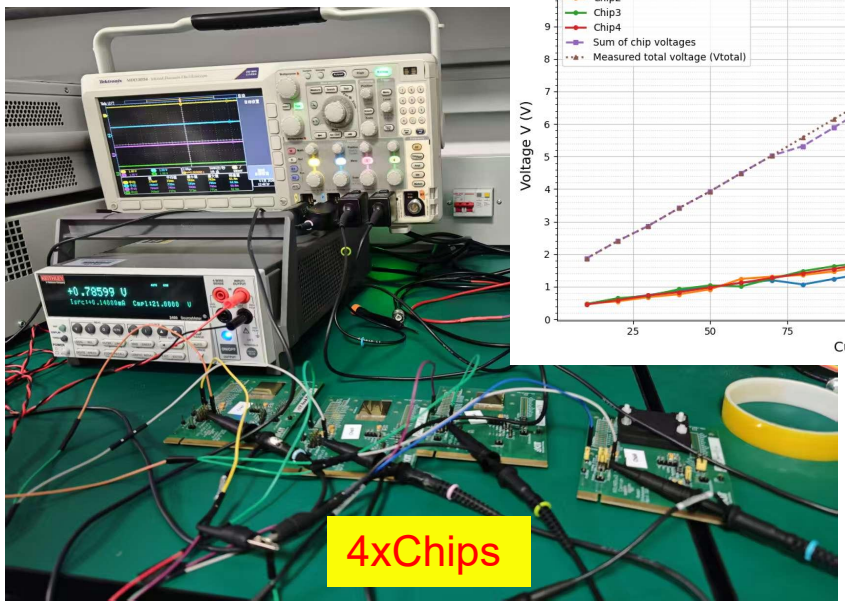


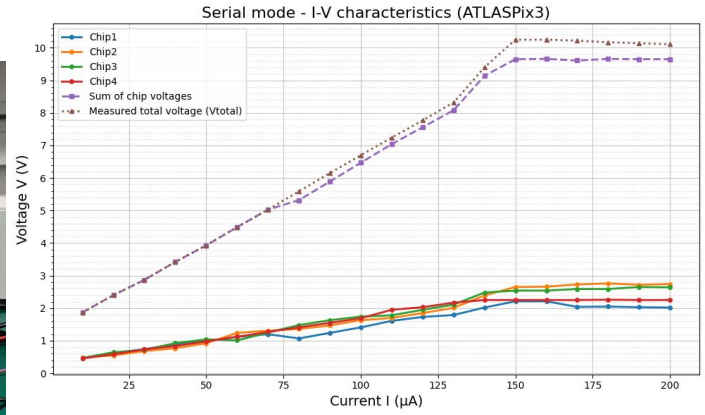
- Successfully fabricated a 1000 mm triangular CF truss beam, mass ~15 g
- see Xiaohui Qian's talk

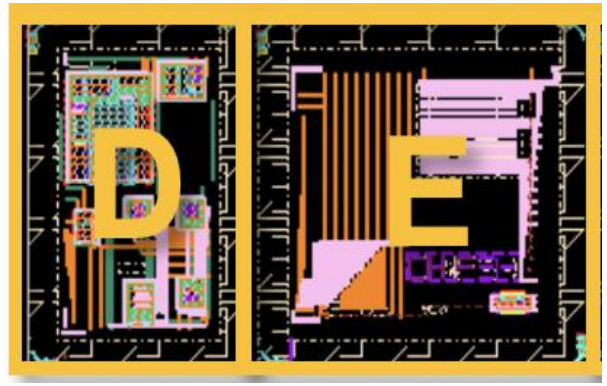
Serial Powering R&D

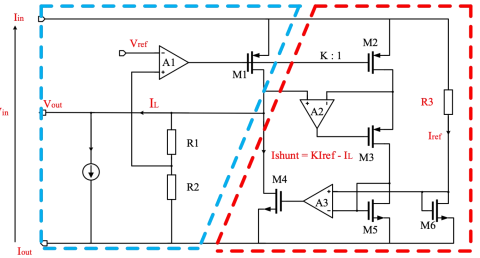
- modules are powered in series by a constant current
  - significantly reduces material budget
  - ATLASPix 3.0 as practice
  - 2x designs of SLDO implemented in CHiR

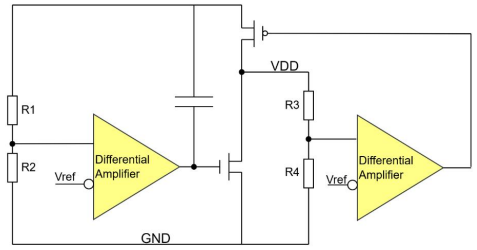








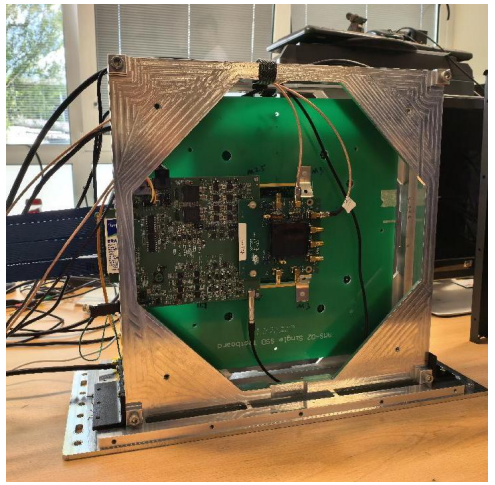


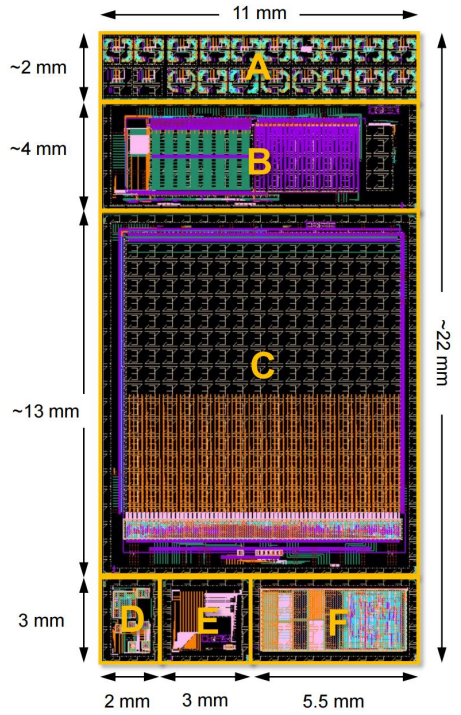


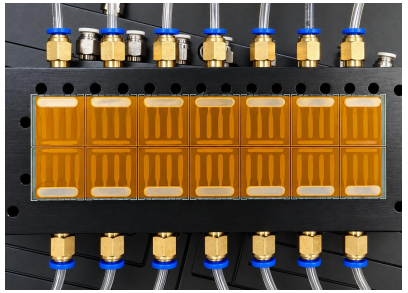
[Tianyu Liang's](#) poster

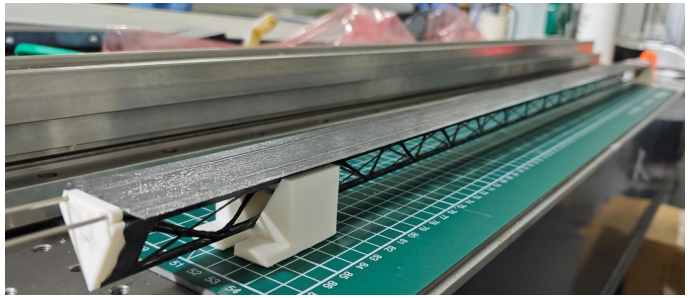
Summary

- Encouraging results from COFFEE2/3
  - most analog/digital, in-pixel/EOC circuits verified
  - irradiation and testbeam on-going
- ChiR: process modif. + high-R wafer
  - chip submitted, results on the way
- ITk module and stave R&D in progress
  - dummy MAPS for mechanics/thermal
  - module assembly procedure
  - carbon fiber truss beam
  - FE/module serial powering









Backup

CEPC Ref-Detector

Table 2.1: Physics objects and key observables used as benchmarks for setting the requirements and the optimization of the CEPC detector.

Physics objects	**Measurands**	**Detector subsystem**	**Performance requirement**
Tracking	Coverage Recon. efficiency Resolution in barrel Resolution in endcap	Tracker	$\lvert\cos\theta\rvert \leq 0.99$ $\geq 99\%$ ($p_{\mathrm{T}} > 1$ GeV/c) $\sigma_{p_{\mathrm{T}}}/p_{\mathrm{T}} < 0.3\%$ ($\lvert\cos\theta\rvert \leq 0.85$) $\sigma_{p_{\mathrm{T}}}/p_{\mathrm{T}} < 3\%$ ($\lvert\cos\theta\rvert > 0.85$)
Leptons (e, μ)	PID efficiency Mis-ID rate	Tracker, ECAL HCAL, Muon	$\geq 99\%$ ($p > 5$ GeV/c, isolated) $\leq 2\%$ ($p > 5$ GeV/c, isolated)
Photons	PID efficiency Mis-ID rate Energy resolution	ECAL, HCAL	$\geq 95\%$ ($E > 3$ GeV, isolated) $\leq 5\%$ ($E > 3$ GeV, isolated) $\sigma_E/E \leq 3\%/\sqrt{E\,(\mathrm{GeV})} \oplus 1\%$
Vertex	Position resolution	Vertex	$\sigma_{r\phi} = 5 \oplus \frac{10}{p(\ \mathrm{GeV}) \times \sin^{3/2}\theta}\,(\mu\mathrm{m})$
Hadronic jets	Energy resolution Mass resolution	Tracker ECAL, HCAL	$\sigma_E/E \sim 30\%/\sqrt{E\,(\mathrm{GeV})} \oplus 4\%$ BMR $\leq 4\%$
Jet flavor tagging	b-tagging efficiency c-tagging efficiency	Full detector	$\sim 80\%$, mis-ID of uds $< 0.3\%$ $\sim 50\%$, mis-ID of uds $< 1\%$
Charged kaon	PID efficiency, purity	Tracker, TOF	$\geq 90\%$ (inclusive Z sample)

CEPC Ref-Detector

Table 2.3: Parameters and layout of the CEPC tracker including VTX, ITK, TPC, and OTK. The column labeled $\pm z$ shows the half-length of the barrel layers, and the z position of the endcap disks. The column labeled σ_ϕ and σ_t represent the spatial resolution in the bending direction and time resolution, respectively.

Components		**Radius** R [mm]		$\pm z$ [mm]	**Material** [X_0]	σ_ϕ [μm]	σ_t [ns]
Beam pipe		10.55		85.0	0.454%	—	—
VTX	Layer 1	11.1		80.7	0.067%	5	100
	Layer 2	16.6		121.1	0.059%	5	100
	Layer 3	22.1		161.5	0.058%	5	100
	Layer 4	27.6		201.9	0.061%	5	100
	Layer 5	39.5		341.0	0.280%	5	100
	Layer 6	47.9		341.0	0.280%	5	100
Beam pipe protective cylinder		66.3		462.0	0.19%	—	—
ITK Barrel	Layer 1 (ITKB1)	235.0		493.3	0.68%	8	3–5
	Layer 2 (ITKB2)	345.0		704.8	0.68%	8	3–5
	Layer 3 (ITKB3)	555.6		986.6	0.68%	8	3–5
OTK Barrel	Layer 4 (OTKB)	1,800.0		2,840.0	1.58%	10	0.05
TPC	Inner wall	600.0		2,900.0	0.45%	—	—
	Gas	605.4–1,779.6		2,750.0	1.00%	110–144	—
	Outer wall	1,800.0		2,900.0	0.69%	—	—
		R_{in}	R_{out}				
ITK Endcap	Disk 1 (ITKE1)	82.5	244.7	505.0	0.76%	8	3–5
	Disk 2 (ITKE2)	110.5	353.7	718.5	0.76%	8	3–5
	Disk 3 (ITKE3)	160.5	564.0	1,000.0	0.76%	8	3–5
	Disk 4 (ITKE4)	220.3	564.0	1,489.0	0.76%	8	3–5
OTK Endcap	Disk 5 (OTKE)	406.0	1,816.0	2,910.0	1.37%	10	0.05

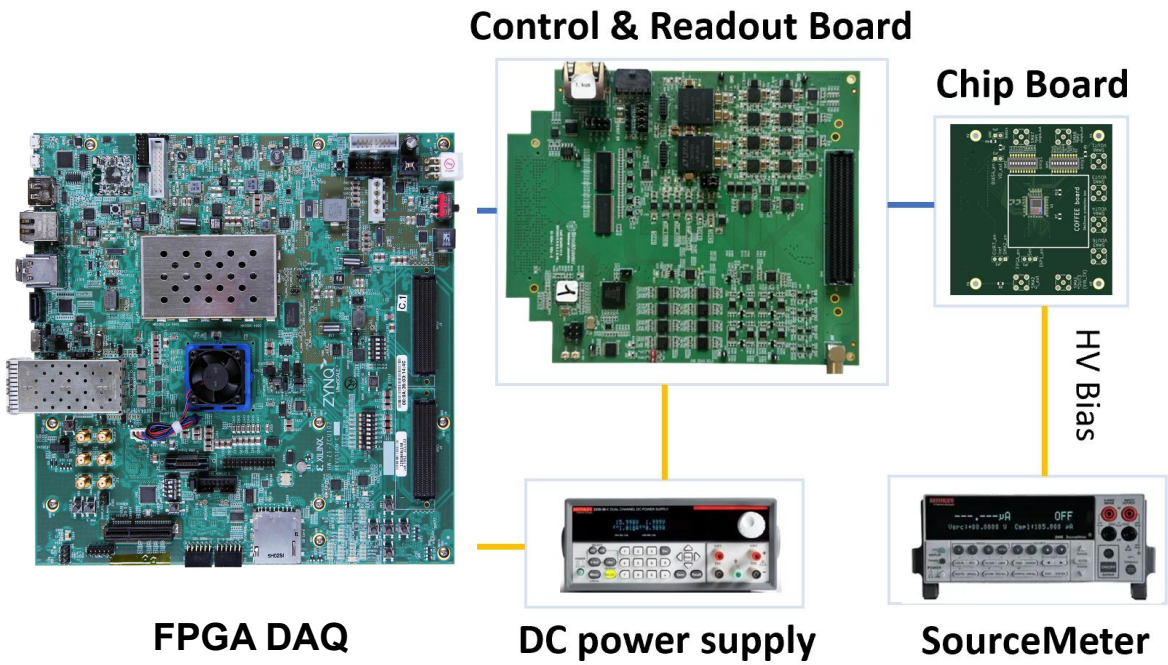
Bench-top DAQ Setup

- Caribou DAQ from DRD3: power, clk, DAC, slow-ctrl, fast readout, …
- FE chip specific carrier board, firmware IP, and software by ourself

Control and Readout (CaR) board

Feature	Description
Adjustable Power Supplies	8 units, 0.8 – 3.6 V, 3 A
Adjustable Voltage References	32 units, 0 – 4 V
Adjustable Current References	8 units, 0 – 1 mA
Voltage Inputs to Slow ADC	8 channels, 50 kSPS, 12-bit, 0 – 4 V
Analog Inputs to Fast ADC	16 channels, 65 MSPS, 14-bit, 0 – 1 V
Programmable Injection Pulsers	4 units
Full-Duplex High-Speed GTx Links	8 links, <12 Gbps
LVDS Links	17 bidirectional links
Input/Output Links	10 output links, 14 input links, 0.8 – 3.6 V
Programmable Clock Generator	Included
External TLU Clock Reference	Included
External High-Voltage (HV) Input	Included
FEAST Module Compatibility	Supported
FMC Interface to FPGA	Included
SEARAY Interface to Detector Chip	320-pin connector

Resources for various target applications

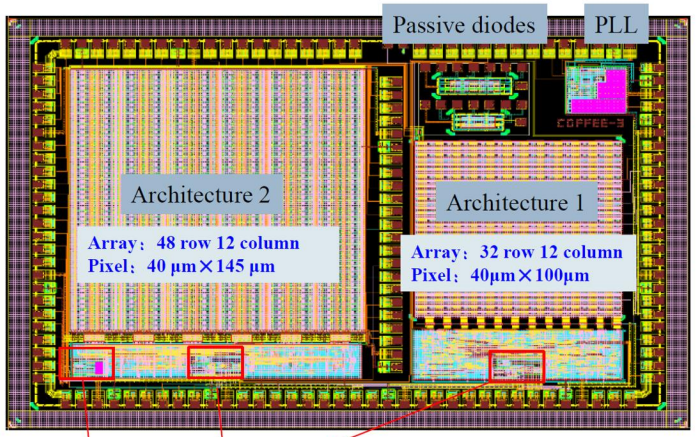


HV-CMOS

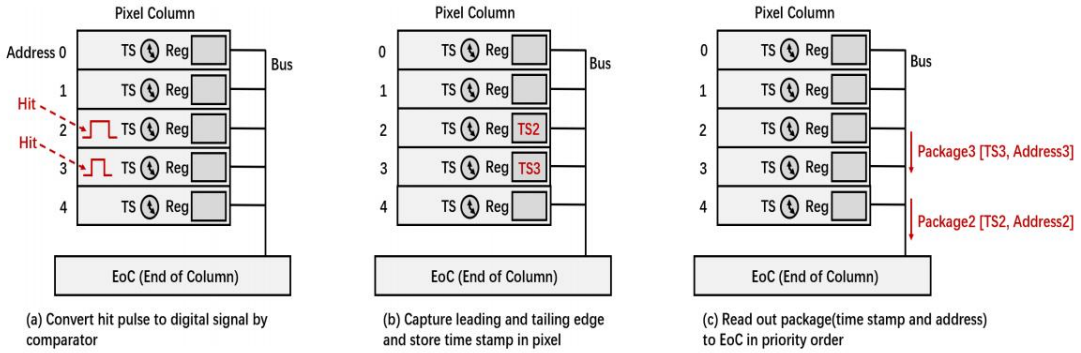
Table 5.3: The HV-CMOS sensor key parameters

Parameter	Value
Sensor size	2 cm × 2 cm (active area: 1.74 cm × 1.92 cm)
Sensor thickness	150 μm
Array size	512 × 128
Pixel size	34 μm × 150 μm
Spatial resolution	8 μm × 40 μm
Time resolution	3–5 ns
Power consumption	200 mW/cm^2
Technology node	55 nm

COFFEE3 Readout Architectures



Architecture 2： employs a TDC within each pixel. Particle hit information (arrival time, end time) is recorded locally in each pixel and then read out to the bottom of the array in priority order.



(a) Convert hit pulse to digital signal by comparator

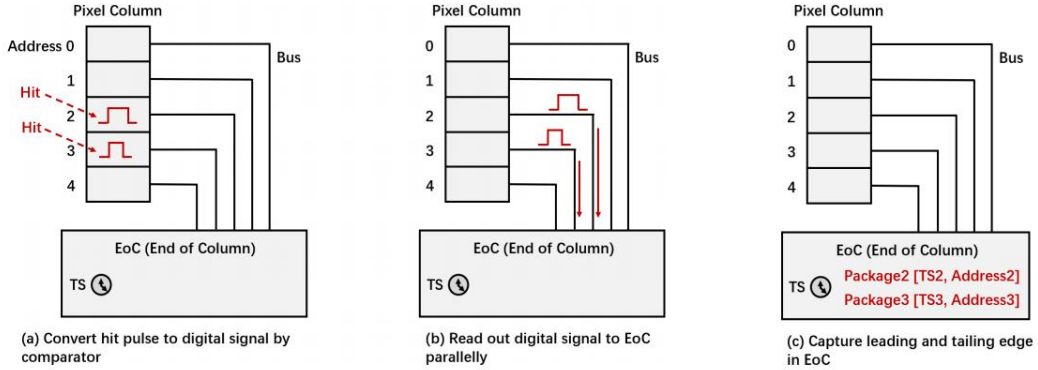
(b) Capture leading and tailing edge and store time stamp in pixel

(c) Read out package(time stamp and address) to EoC in priority order

Readout concept of Architecture 2, similar with Timepix, RadPix, MonoPix, etc.

- *More possibilities & High hit density processing capability*

Architecture 1： In-pixel NMOS design, after digitization, each pixel data is transmitted in parallel to the bottom of the array, where time stamps are added.



(a) Convert hit pulse to digital signal by comparator

(b) Read out digital signal to EoC parallelly

(c) Capture leading and tailing edge in EoC

Readout concept of Architecture 1, similar with ATLASPix, MightyPix, MuPix, etc

Targets:

- *Potential for Low power consumption and high position accuracy*

COFFEE2: in-pixel Ana/Digi-circuit X-talk

- Laser test : JINST 20 (2025) C10011
  - NMOS comparator work well
  - Crosstalk issue seen among CMOS comparator and CSA.
  - Potential flip in digital circuitry cause the disturbance between N-well of PMOS bulk terminal and deep N-well

