A Methodology for Determining Pixel Chip Circuit Parameters from Vertex Detector Design Requirements

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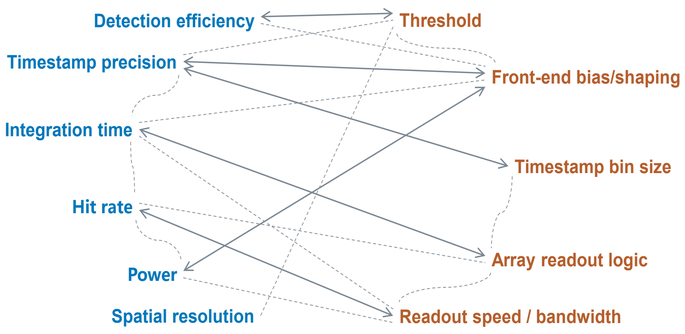
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We present a quantitative methodology for determining pixel-chip circuit parameters from vertex-detector design requirements. Collected-charge statistics and threshold-crossing response connect power, threshold and integration time to timestamp precision and occupancy.

01 Background & Design Targets

Precision electroweak, Higgs and flavour studies at CEPC/FCC-ee require precise impact-parameter measurements and secondary-vertex reconstruction. The AGORA vertex detector must combine fine spatial resolution, high efficiency and a low material budget. Charge sharing, discriminator threshold and front-end response speed affect spatial resolution, detection efficiency, timing, power consumption and readout requirements. These coupled trade-offs motivate a unified method for selecting compatible circuit parameters.



Coupling Between Detector Performance Requirements and Circuit Parameters

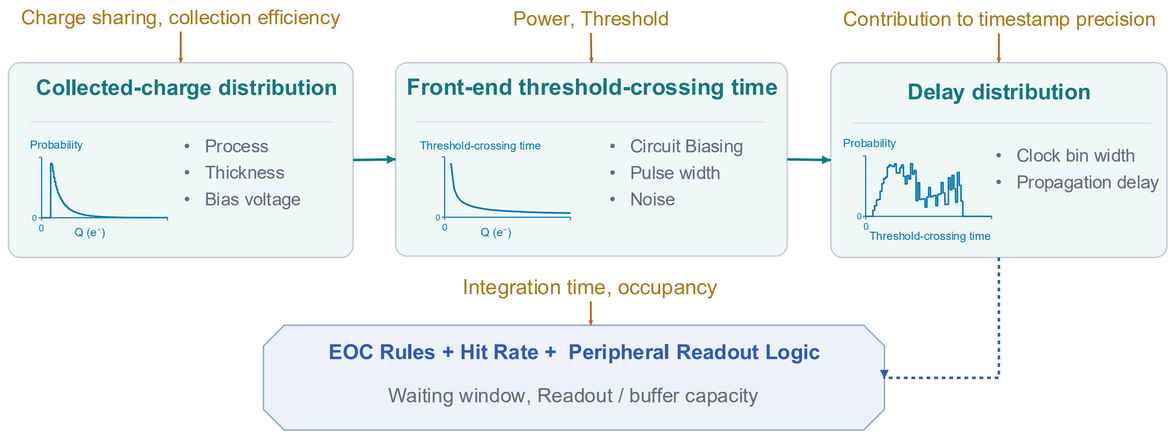
AGORA vertex-detector requirements

Requirement	Target
Spatial Resolution	~ 3 μm
Power density	≤ 40 mW/cm²
Integration time	< 1 μs
Timestamp precision	< 100 ns
Pixel hit rate	~ 200 MHz/cm²
Material budget per layer	< 0.2% X_0

02 Methodology

Propagate collected-charge statistics through the threshold-crossing response to obtain a delay distribution. Combine its timing contribution with the EOC rules, background hit rate and readout organisation to infer compatible front-end settings, waiting windows and readout capacity.

$$Q \sim f_Q \quad \longrightarrow \quad t = d(Q; P, Q_{\mathrm{th}}) \quad \longrightarrow \quad f_t$$



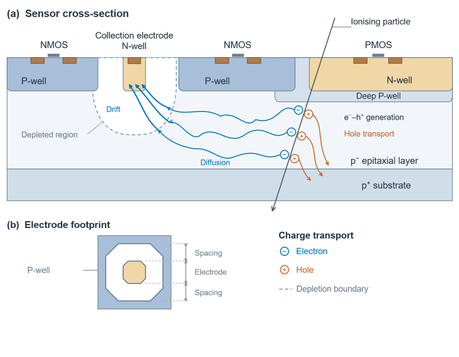
03 Methodology illustrated with a simplified model

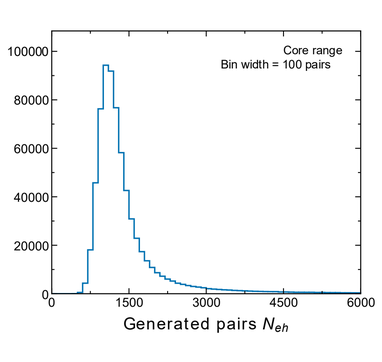
A Sensor and collected-charge statistics

Ionisation creates carriers that reach the collection node by drift and diffusion.

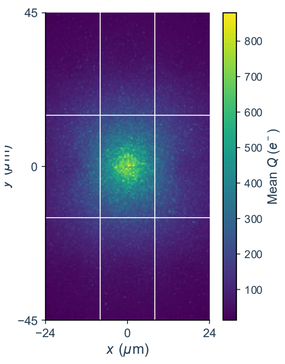
Energy-loss fluctuations and charge sharing shape the collected-charge distribution.

A simple 3×3 pixel array model supplies the example for this methodology demonstration.

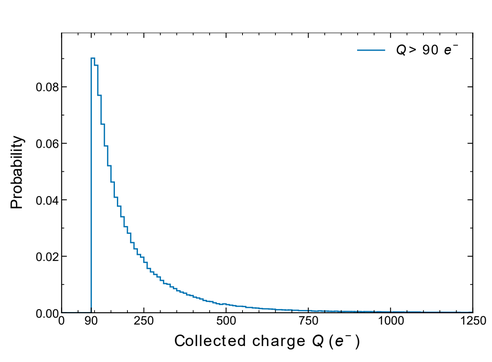




Generated charge



Collection map



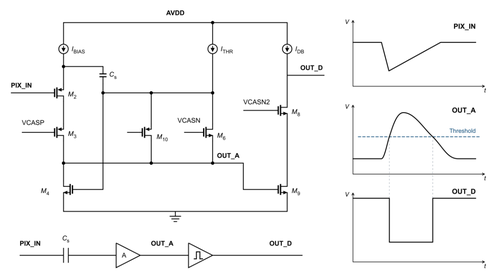
Collected $Q > 90\,e^-$

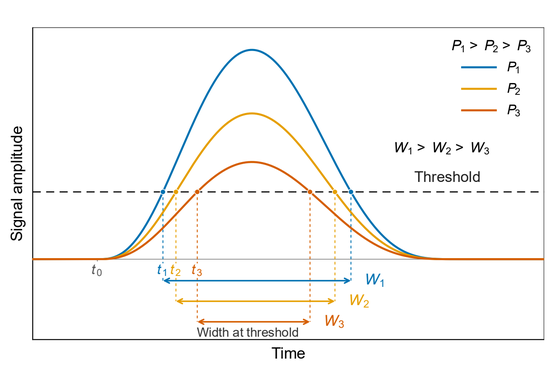
B Analogue front-end response

A source follower and amplifier drive a leading-edge discriminator.

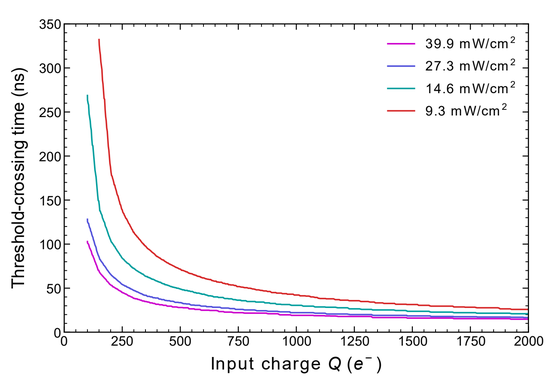
Higher power or a lower threshold shortens crossing time in this reference circuit.

The simulated charge-to-time curves provide the mapping used below.





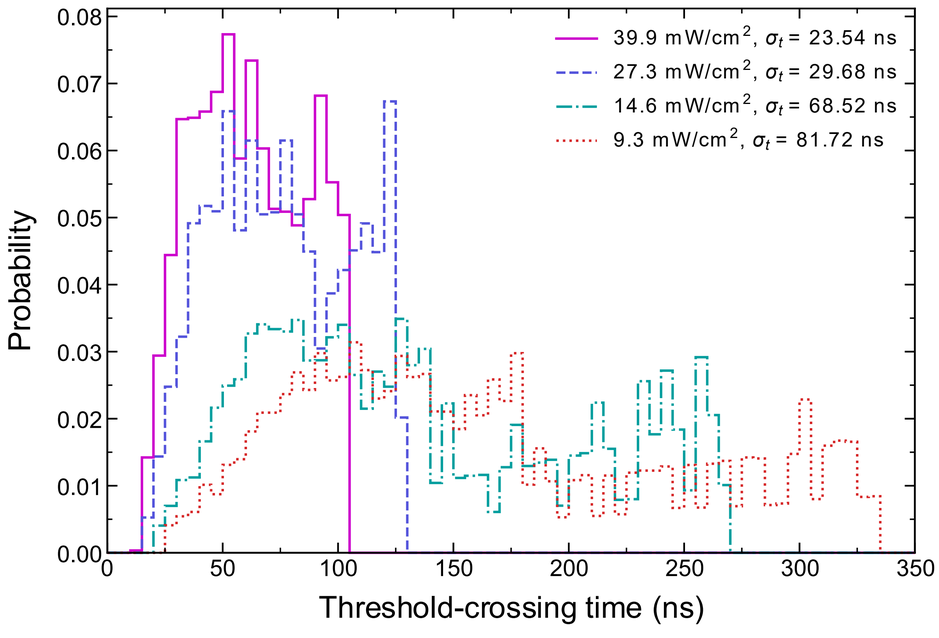
Analog Front-End Signal



Charge-to-time curves

C Delay statistics and timestamp precision

Mapping the collected-charge distribution through the simulated front-end response gives the threshold-crossing-time distribution. For a design with 14.6 mW/cm² power density and a 100 e⁻ threshold, the time-walk contribution to timestamp precision is 68.5 ns.

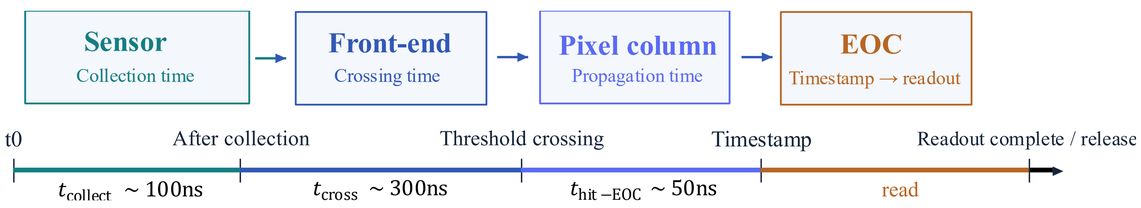


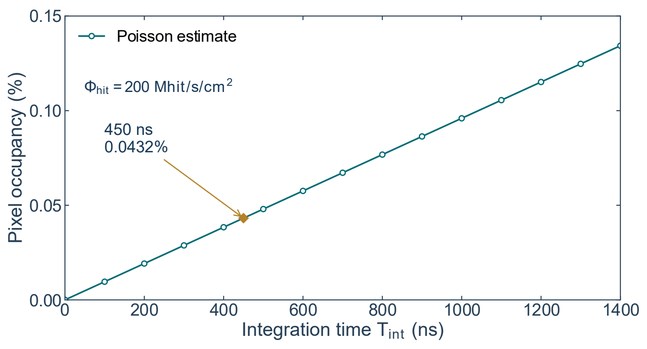
D Integration time and occupancy

Integration time is the difference between the timestamp and the true event time.

For the PRECISE architecture under development, a 450 ns integration time gives an estimated 0.0432% pixel occupancy at 200 Mhit/s/cm². The occupancy allowed by track reconstruction can conversely constrain the integration-time range.

$$t_{\mathrm{int}} = t_{\mathrm{collect}} + t_{\mathrm{cross}} + t_{\mathrm{hit-EOC}} \approx 450\ \mathrm{ns}$$





04 Outlook

Future work will incorporate the actual sensor structure and transient charge collection into a process-specific TCAD–Geant4 model to obtain accurate and reliable distributions of collected charge and threshold-crossing time.

Subsequent measurements will validate the performance of the complete PRECISE sensor–front-end–readout chain and assess the feasibility of the proposed methodology.