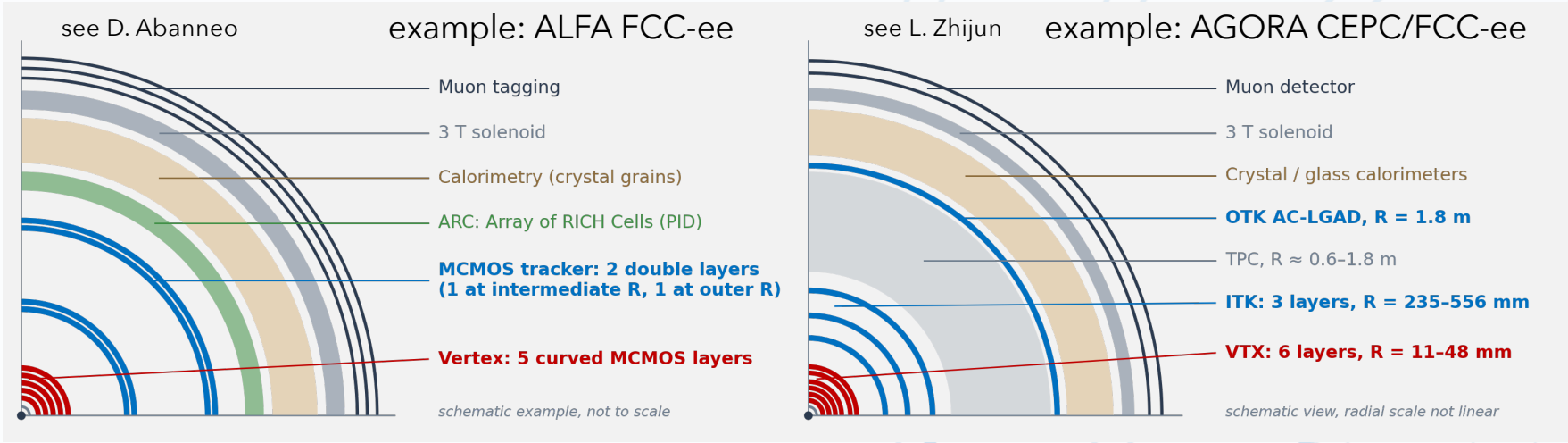
Vertexing and tracking at future e^+e^- colliders with Monolithic-CMOS pixel sensors from the OCTOPUS and MANTA projects

CEPC Workshop, Oct. 22-26 2026, Shanghai

D. Contardo (IP2I) on behalf of the OCTOPUS and MANTA collaborations

e^+e^- colliders detector concepts: vertex and tracker

- ALFA/CLD: MCMOS VD and TK (see D. Abanneo/J. Brau)
- AGORA/ILD: MCMOS (VD + InnerTK) + TPC + Si-OuterTK (see J. Guimaraes da Costa- Y. Li/M.C. Fouz)
- ALLEGRO/IDEA : MCMOS (VD + InnerTK) + Drift Chamber + Si-OuterTK (see E. Monnier/F. Bedeschi-A. Andreazza)



Major challenges*

- vertex targets: ≃ 0.1% X/X_0/layer* at ≃ 3 μm spatial precision, power consumption ≲ 50 mW/cm^2
- tracker targets: ≃ 0.3% X/X_0 /layer* at ≃ 5 μm spatial precision, power consumption down to 20 mW/cm^2
  - ➢ TPSCo 65nm to optimise competing: high channel density, low power, timing precision

** Material budget is also a challenge for system design, mechanical structures, cooling, electrical powering…*

OCTOPUS and MANTA at a glance

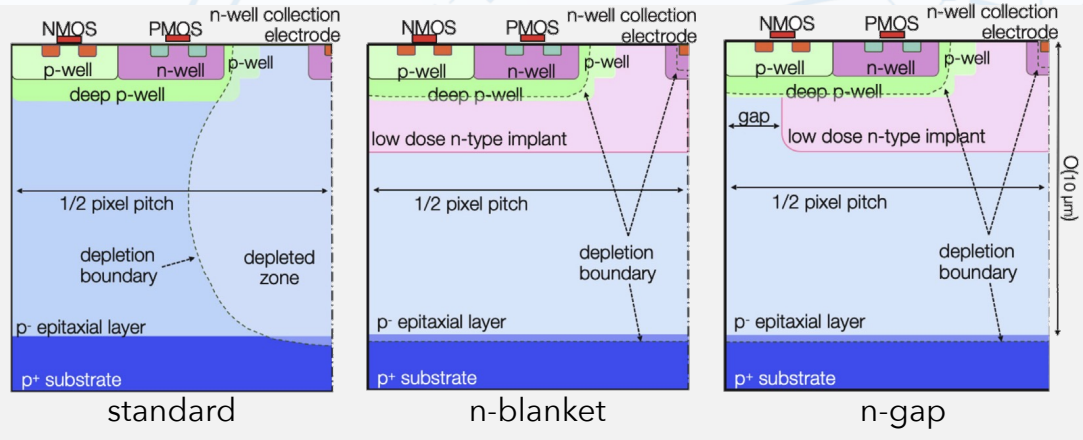
Optimised **C**MOS **T**echnology f**o**r **P**recision in **U**ltra-thin **S**ilicon
Monolithic **A**synchronous sensor for **N**ext generation **T**r**A**ckers

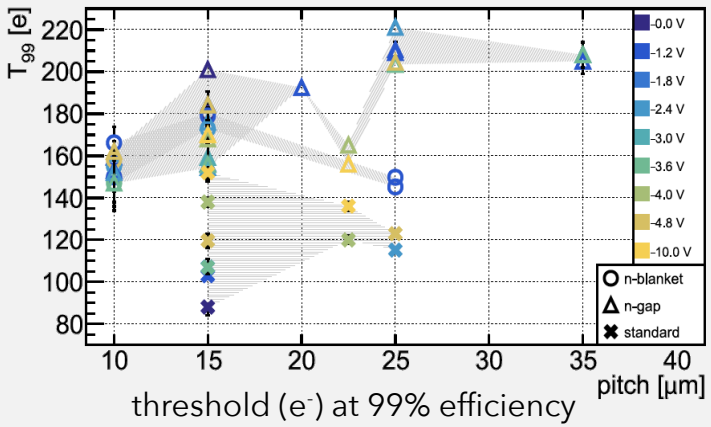
- OCTOPUS & MANTA are DRD3 projects
  - in the TPSCo 65 nm CMOS Image Sensor process
- OCTOPUS targets vertex detector at an e^+e^- collider experiment
- MANTA has a multi-experiment purpose
  - embedding configurability to different performance requirements and variability of operation conditions, as typically expected across layers of a tracker at e^+e^- colliders
  - exploring digital implementation for sub-ns timing measurement precision, targeting ToF precision $\lesssim$ 100 ps at low momentum for PID OTK layers
- Common features of the two projects allow
  - sharing the sensor diode design, the Front-End electronics and some IP blocks
    - while exploring different designs in the digital periphery architecture

TPSCo 65 nm CIS technology features and validation

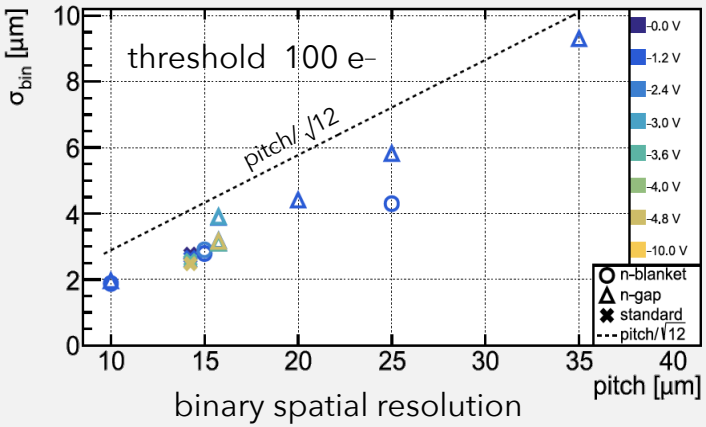
https://doi.org/10.1016/j.nima.2026.171672

- In the context of CERN EP R&D projects and the ALICE ITS3 upgrade (see W. Snoeys)
  - process features 10 µm epitaxial layer
    - small diodes 3(2) fF @ -1.2 (-4.8) V
  - validation
    - process optimisation (blanket, gap)
    - small pixel pitch studies 10 to 35 µm
    - intrinsic time precision ≃ 70 ps (@15 µm pitch)
    - reticle stitching to full wafer size sensors
    - thinning down to 20 µm for bending
    - radiation tolerance up to 10^{15} neq/cm^2

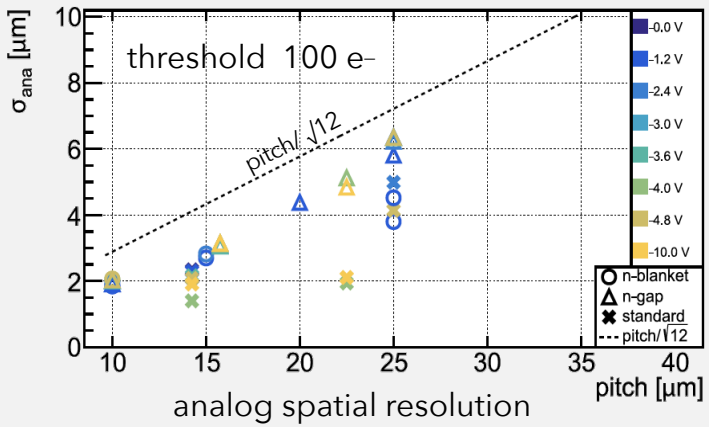




threshold (e^-) at 99% efficiency



binary spatial resolution



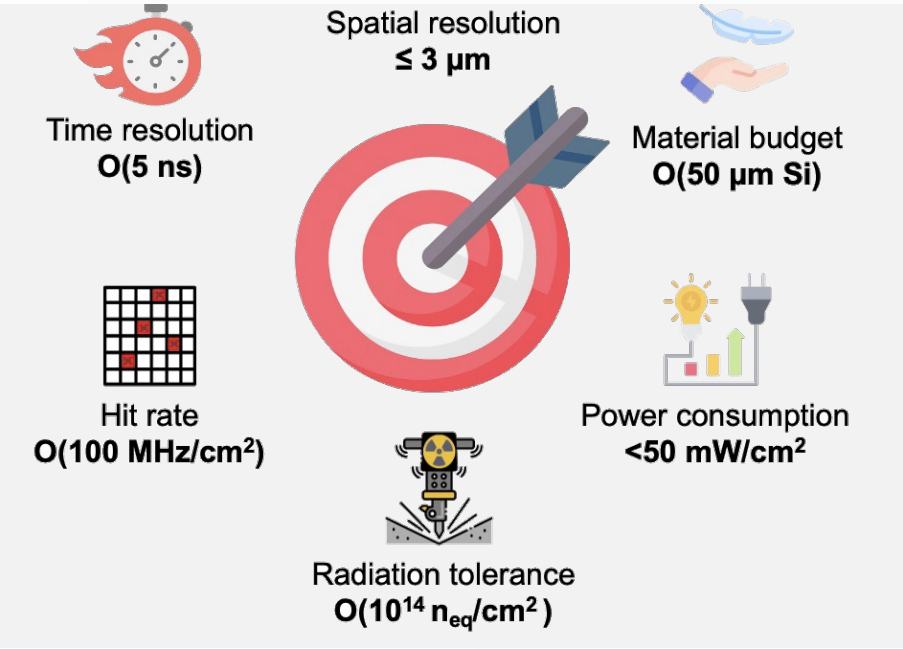
analog spatial resolution

FCC-ee Performance/Requirements/Constraints targets

Machine Detector Interface region - backgrounds - still under study

impact of competing parameters & interplay w/ overall configuration studies in physics simulations

OCTOPUS



MANTA

Project	Belle II trk	CBM MVD	CBM STS	LHCb UT	FCC-ee trk	FCC-ee PID
Spatial res. [µm]	<15	~5	10	10	~5-10	<10
Hit rate [MHz/cm²]	<1	~80	~10	90	0.1-5	0.01-0.5
Time res. [ns]	~1	~10	~10	1	5-25*	0.03-0.1
Trigger	Yes	No	No	No	No*	No*
Power [mW/cm²]	<50	~100	50	200	~20	tbc
Rad. tol. [kGy]	10	500	170	2000	150	<150
Rad. tol. [neq/cm²]	1e12	1e15	3e14	4e15	<<1e14	<<1e14

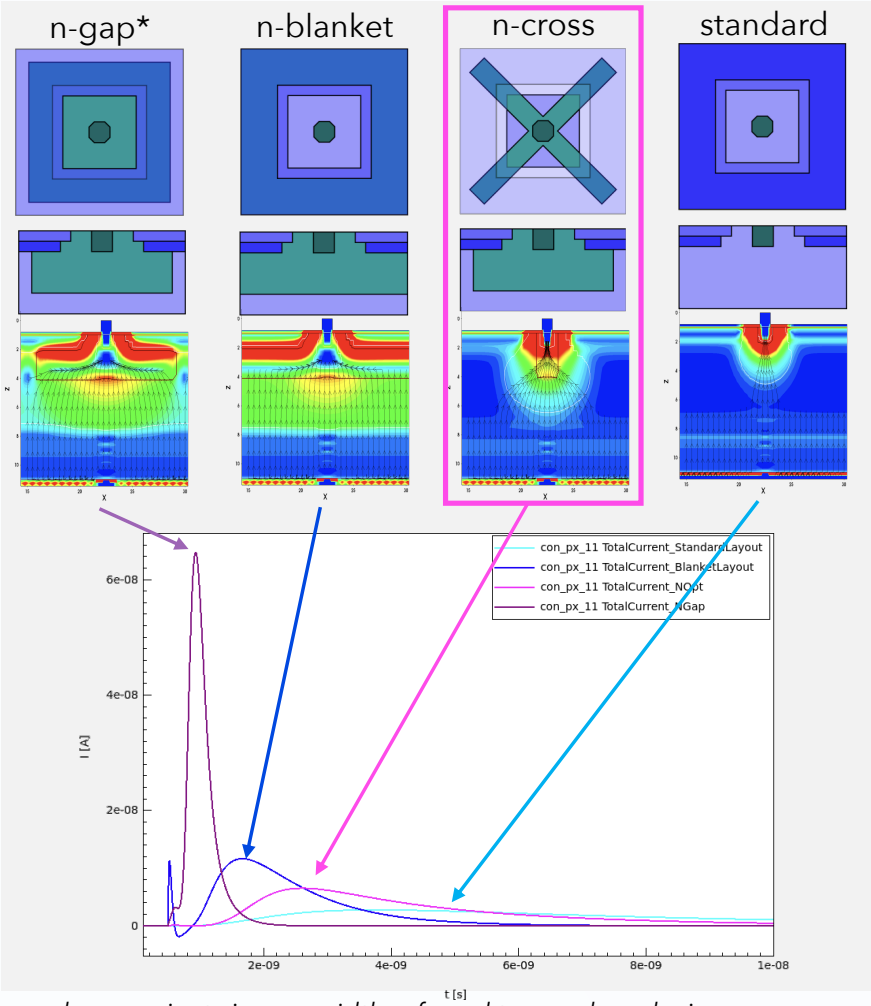
→ configurable bias, data format & serialising

first foundry submission (MPR2) will be a shared fraction of reticle for demonstration
w/ relaxed power consumption, w/o trigger capability

** tbd driven by beam structure and backgrounds*

OCTOPUS n-cross: ≃ 3 µm precision at ≃ 20 µm pitch

https://indico.cern.ch/event/1519426/contributions/7162418/attachments/3339762/5985204/VelykaPIXEL26.pdf

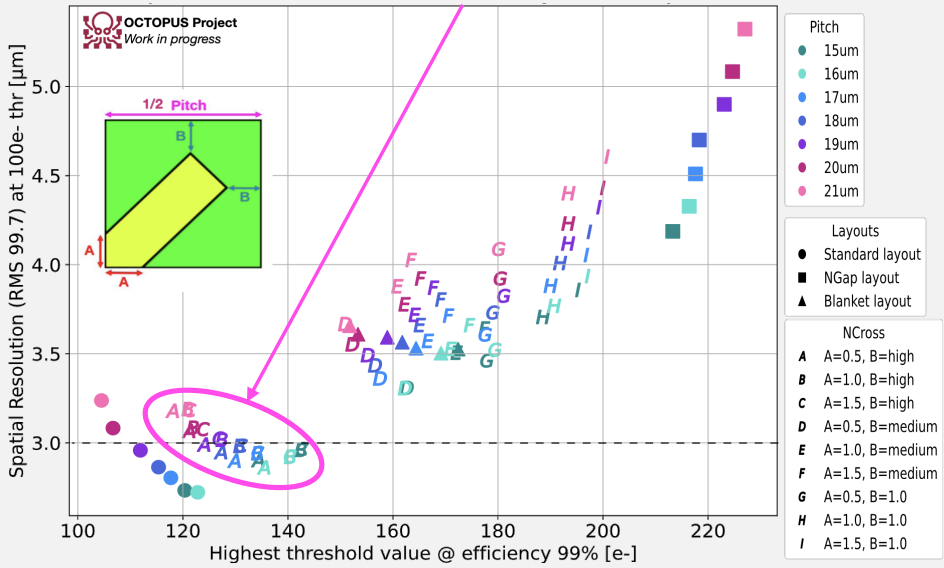


n-gap can have variants in gap width referred to as n-box design

sensor configuration optimisation is a trade-off:

- larger charge sharing (standard) - better analog resolution
- smaller charge sharing (n-gap) - better efficiency & time precision
- lower capacitance with smaller deep n-implant width

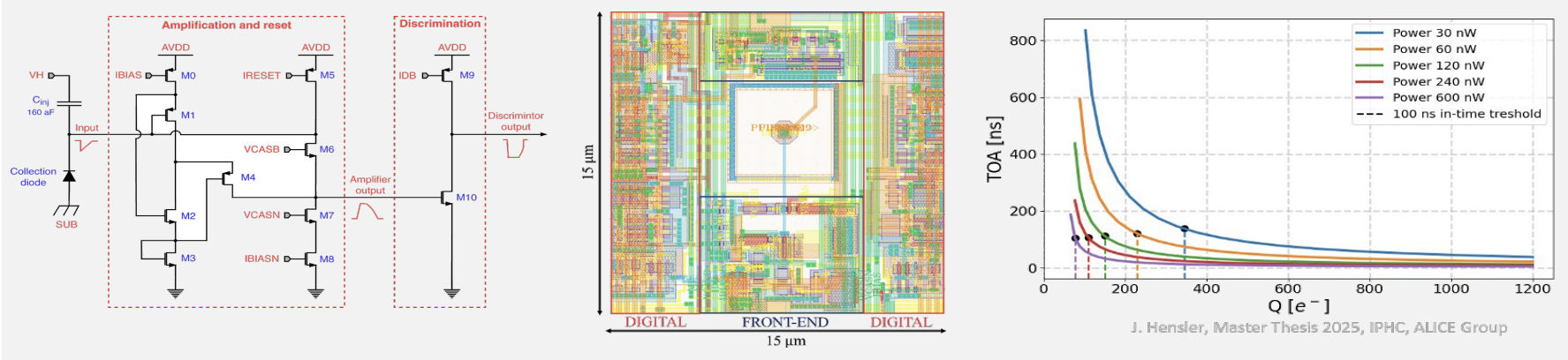
n-cross simulation w/ TCAD + ALLPIX2
(analog readout for charge sharing position weighting)
spatial precision ≃ 3 µm at ≃ 20 µm pitch



OCTOPUS and MANTA: pixel analog FE and logic

https://cds.cern.ch/record/2876300/files/A_Compact_Front-End_Circuit_for_a_Monolithic_Sensor_in_a_65-nm_CMOS_Imaging_Technology.pdf

- Analog FE based on DPTS amplifier + discriminator (CERN)*
  - tunable power 12 nW to 5 µW;
  - ➢ example @120 nW tuning : ≃ 30 mW/cm^2 for 20 x 20 µm pixels; Time of Arrival (ToA) max. prob. ≃ 30 ns (seed pixel charge) w/ precision ≃ 6 ns after Time-Walk (TW) correction**



- In-pixel logic
  - OCTOPUS each pixel address - MANTA 2 (rows) x 2 (cols) = 1 macro-pixel (40 x 40 µm pitch)
  - separate Leading Edge (LE) and Trailing Edge (TE) for Time over Threshold (ToT) measurement
    - ➢ weighted pixel cluster positions for spatial precision, time walk correction of Time of Arrival

OCTOPUS and MANTA current stage of layout 21.8 x 21.8 µm pitch

** Possibly MOSAIX ITS3 FE if IP validated, ** a faster and lower power FE will be needed for ToF PID, possibly with sensor amplification studied in DRD3 (see P. Schwemling)*

OCTOPUS and MANTA: clock-less data-driven readout

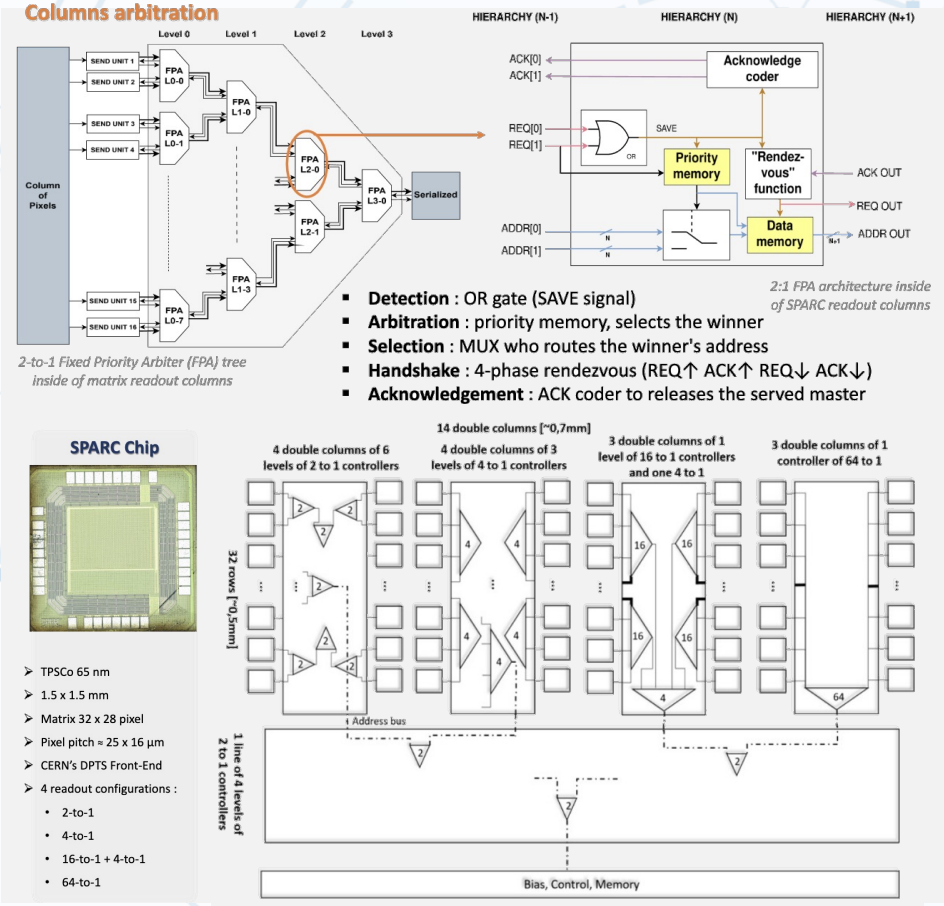
Asynchronous Priority Arbiter (APA) architecture

https://indico.cern.ch/event/1519426/contributions/7162502/attachments/3342882/5991698/Poster_FOURNIER_26_final-1.pdf

- Data driven RO no clock in matrix
  - tree structure: pixel RO request, arbitration at each stage and address forwarding, acknowledge to release master group
  - multiplexing balancing bandwidth (BW) – RO time
- LE and TE sent separately with pixel address
  - expected time precision ≃ 6 ns*
  - pixel dead time driven by pulse length (ToT)**
    - ➢ Time Stamping (TS) at EoC at 160 MHz

APA OCTOPUS & MANTA: 4 to 1 master tree in 3 stages

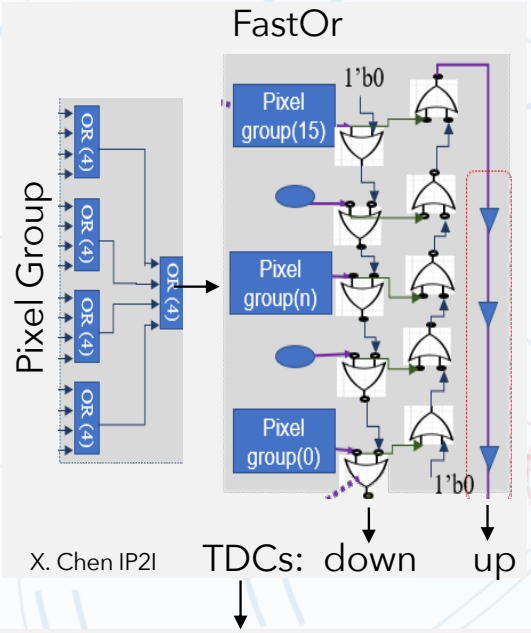
- SPARC demonstrator
  - 4 tree configurations studied
  - ER2 run submission received
    - chip fully functional
    - CARIBOU lab. test consistent with simulation
    - beam test @DESY good efficiency – analysis on going



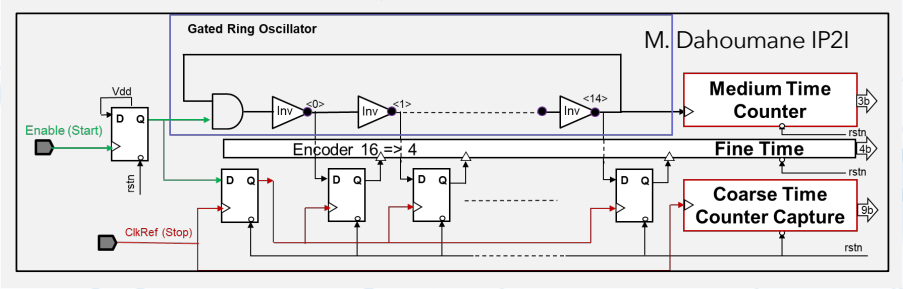
** consistent with DPTS resolution with tuning at 120 nW/pixel; ** O(1-10) µs depending on FE tuning*

MANTA: Gated Ring Oscillator TDC architecture for precise timing

- FastOr concept
  - drive pixels LE "or" to TDC at EoC
    - for time precision below the APA limit ≃ 6 ns
    - ➢ targeting ToA (TW corrected) digital precision ≃ 20 ps
  - groups of 16 pixels spaced by ≃ 50 ps to FastOr lanes
  - 2 FastOr lanes up/down towards 2 TDCs
    - ➢ pixel group time offset to EoC in calibration mode
    - ➢ group address (by difference) in particle mode



- TDC Gated Ring Oscillator design
  - time binning (LSB) ≃ 70 ps
  - dead time ≃ 6.25 ns
  - Stat. power ≃ 400 µW/TDC ≃ 25 mW/cm²
  - Dyn. power 10 pJ/hit - few mW/cm² @100MHz/cm²



OCTOPUS and MANTA: Matrix Layout

OCTOPUS sub-matrix = 4 pixel columns

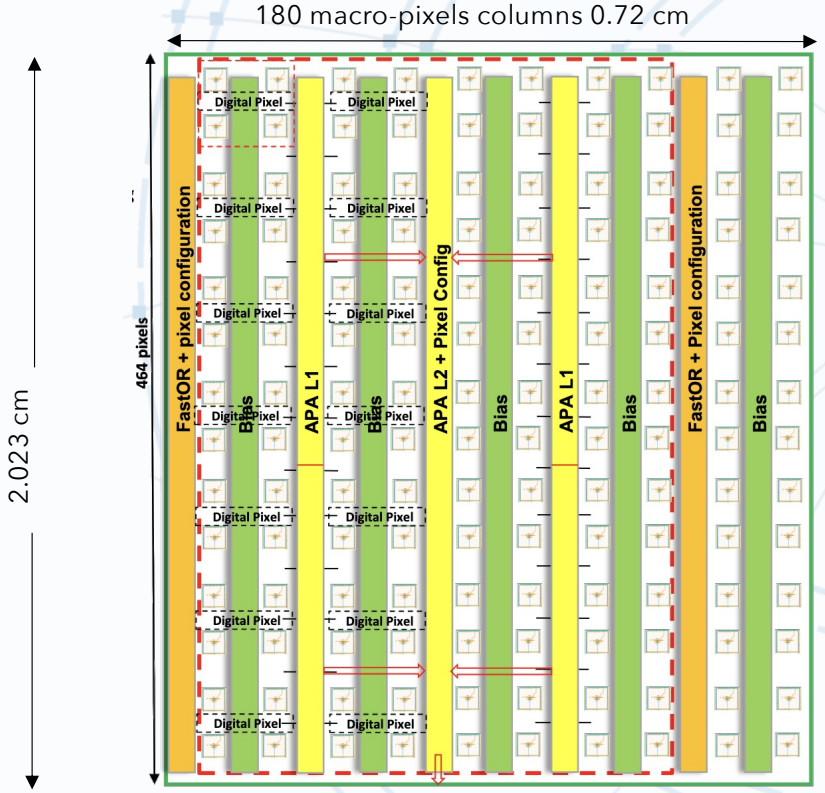
- APAL1 = 32 blocks of 29 pixel rows
- APAL2 = 32 APAL1 blocks



X. Fang IPHC

MANTA sub-matrix = 4 macro-pixel columns

- APAL1 = 29 block of 16 macro-pixel rows
- APAL2 = 2 x 29 APAL1 blocks
- 1 FastOr = 2 macro-pixel columns*



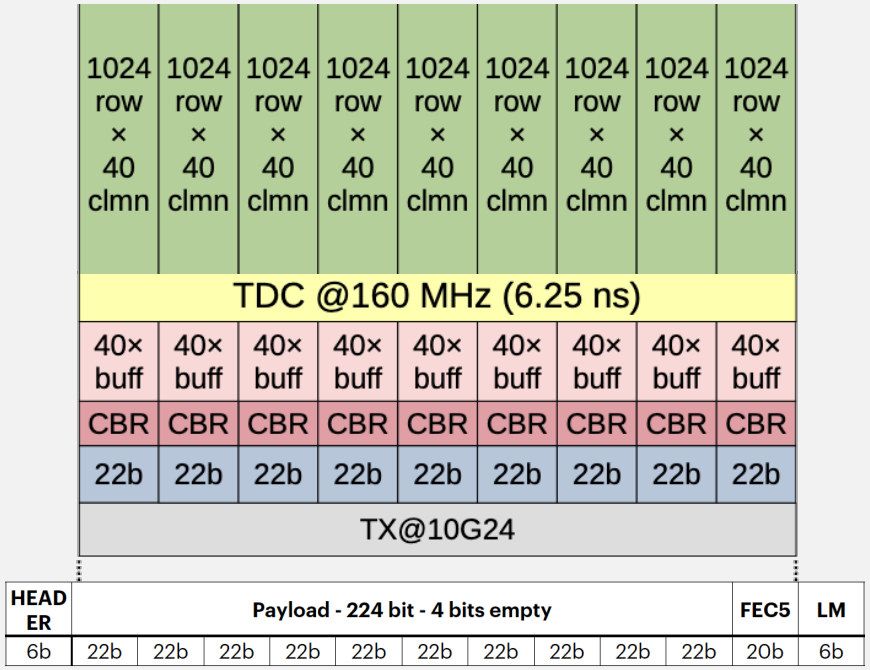
** 2 columns in FastOr are in OR at TDCs (up/down) with 2b encoding*

OCTOPUS and MANTA: End of Column

OCTOPUS

- bitmap data compression (no empty words)
  - alternative: round-robin APA

360 pixel columns in 8 EoC blocks



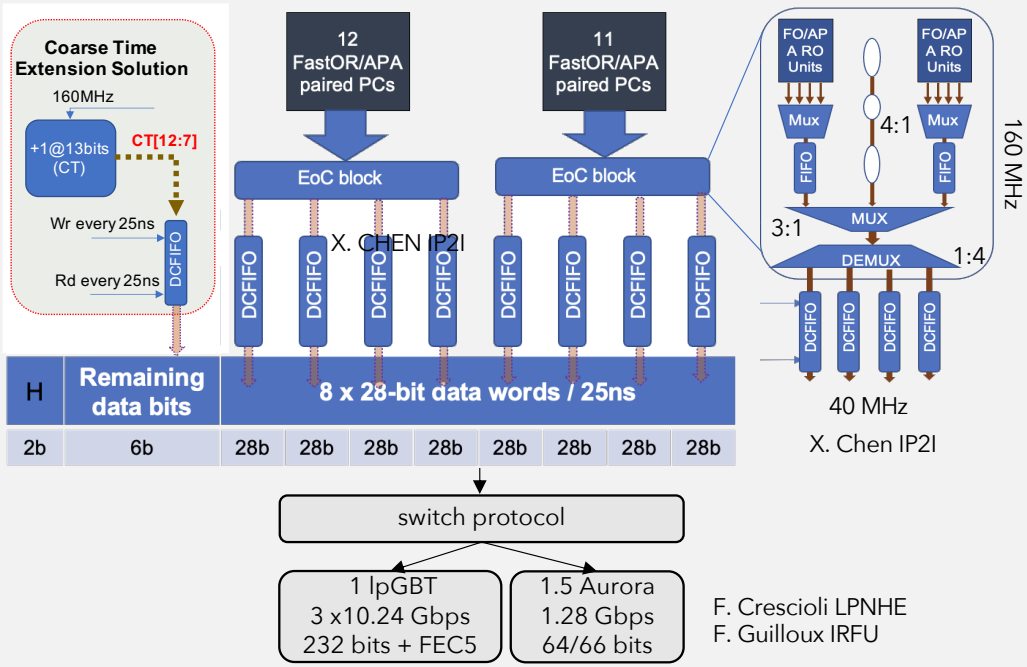
- 224 bits payload for forward error correction of up to 5 wrong bits (FEC5) + header + latency measurement LM

Z. Janoska

MANTA

- data compression in 2 multiplexing stages
- configurable output 1-2 x 10.24 or 1-2-3 x 1.28 Gbps
- empty word suppression in DCFIFO for 1.28 Gbps

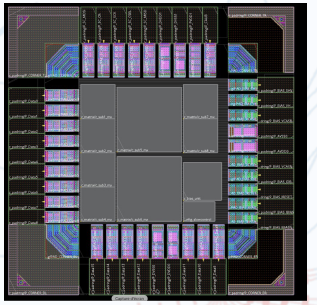
180 macro-pixels columns in 8 EoC blocks



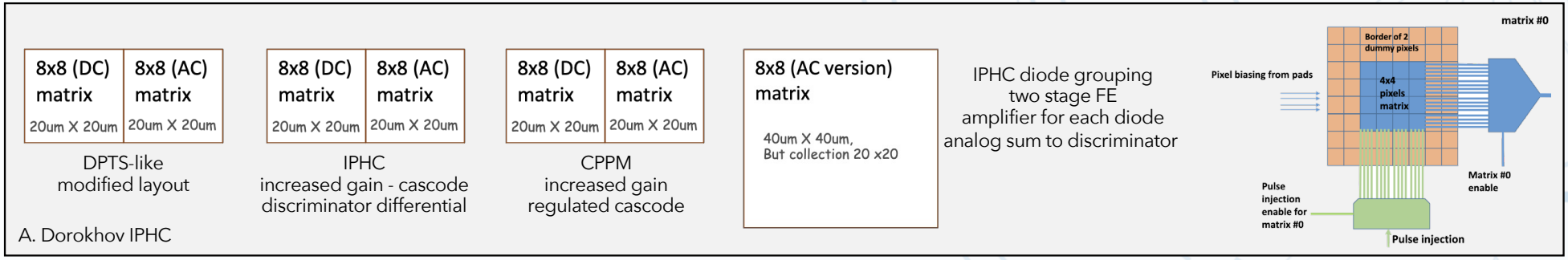
OCTOPUS and MANTA: OCEAN-65 test chip

explore sensor and Front-End variants

- 7 matrices of 8x8 pixels - 20 x 20 µm - of which 4x4 active; parallel digital RO
  - n-gap or box layout
  - different amplifiers-discriminators, AC and DC coupling of diodes
  - 2 matrices 4x4 active pixels - 20 x 20 µm
  - N-cross layout
  - APTS amplifier
- design completed validation on-going
  - considering with foundry (constraints) submission possibilities in ER3 (ALICE ITS3)



G. Bertolone IPHC



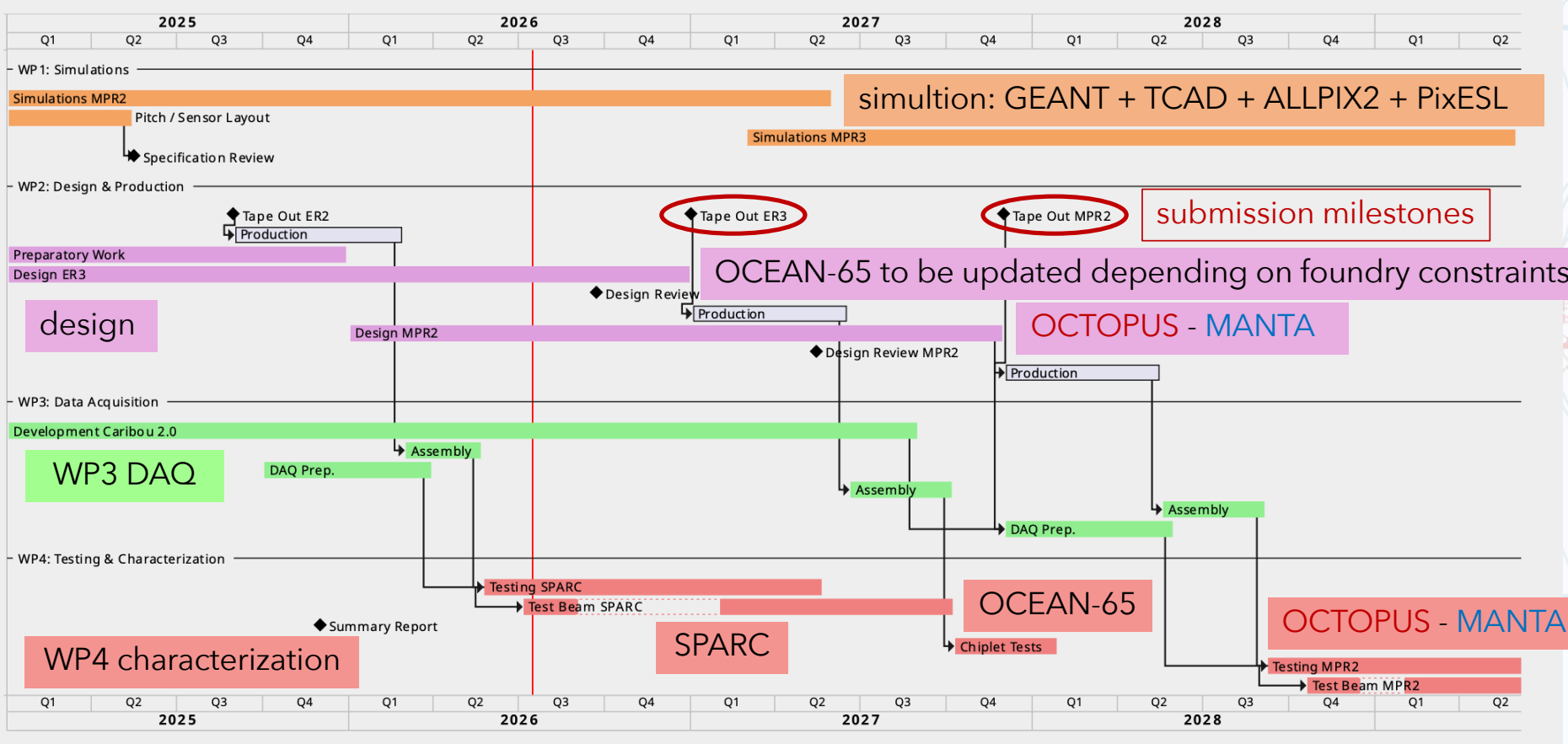
A. Dorokhov IPHC

OCTOPUS and MANTA at a glance

	OCTOPUS	MANTA
Target	Vertex detector at an e^+e^- collider	Tracker: multi-experiment purpose, configurability and option for time-of-flight measurement
Pixel	20×20 μm pixels, spatial precision target ≲ 3 μm	2 × 2 pixels (20 μm pitch) = 1 macro-pixel (40×40 μm),
Time information	Leading & Trailing Edge (ToA and ToT) precision ≃ 6 ns	Leading & Trailing Edge (ToA & ToT] precision ≃ 6 ns FastOr line + TDC, ToA digital resolution ≲ 30 ps
Matrix RO	Data-driven, clock-less APA tree (4-to-1 tree in 3 stages); time stamping at EoC @ 160 MHz	Same APA tree; groups of 16 pixels spaced by ≃ 50 ps to 2 FastOr lines, 2 TDCs up and down
End of column	Bitmap data compression (alternative: APA-like); Data transfer serializers @ 10.24 Gbps	Data compression in 2 multiplexing stages; Data transfer 1–2x10.24 Gbps or 1–2–3×1.28 Gbps
Common	TPSCo 65 nm CIS process, DPTS CERN front-end, SPARC APA prototype, OCEAN-65 sensor and FE test-chip	

Outlook: OCTOPUS planning by WPs

similar structure and overall timeline for MANTA



Summary and next steps

Key messages

- The TPSCo 65 nm process is suitable for vertex detectors and trackers at e^+e^- colliders
- OCTOPUS explores sensor variants to reach ≃ 3 μm spatial precision at ≃ 20 μm pitch
- A common low-power, data-driven APA readout adapts to the data rates; MANTA adds flexible end-of-column data transfer and time-of-flight capability
- Layout is in progress, full simulation framework (GEANT + TCAD + ALLPIX2 + PixESL) is available, challenge to minimize diode pitch
- SPARC (APA) prototype chip is fully functional

Next steps

- SPARC: analysis of the DESY beam test and characterization
- OCEAN-65 test chip: submission tbd, possible earlier than MPR2
- OCTOPUS - MANTA submission (MPR2) Q4-2027
- Longer term (next submission): minimize power consumption - building on DRD7 & DRD3 developments