Design and Test Results of the SIPAC: A Prototype SiPM Readout ASIC for CEPC Calorimeters

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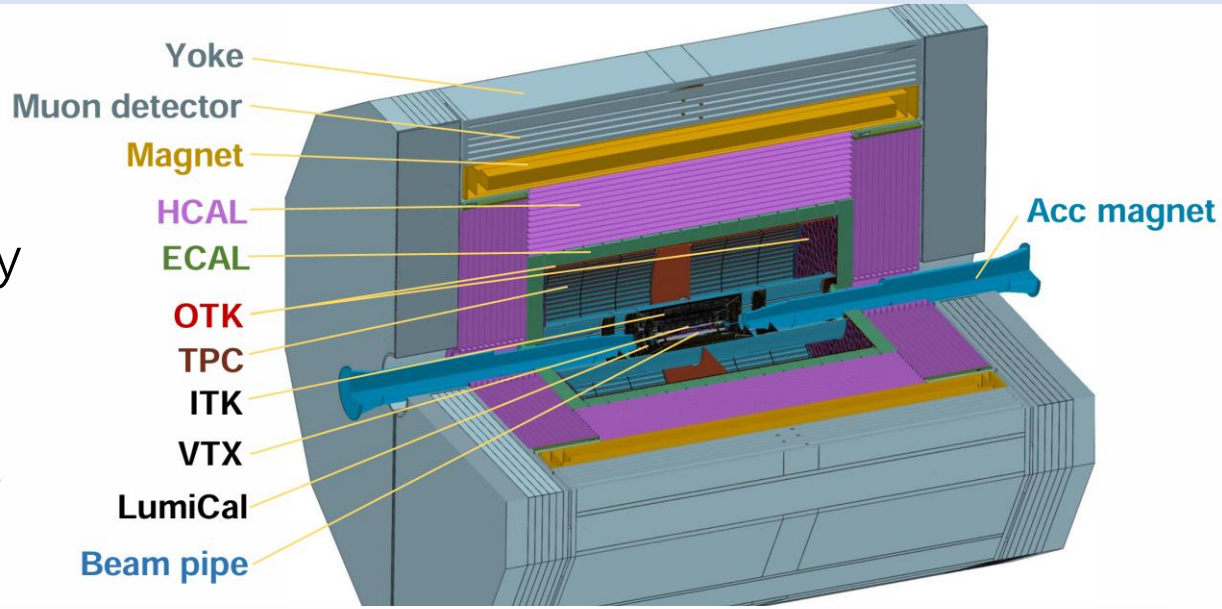
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Background

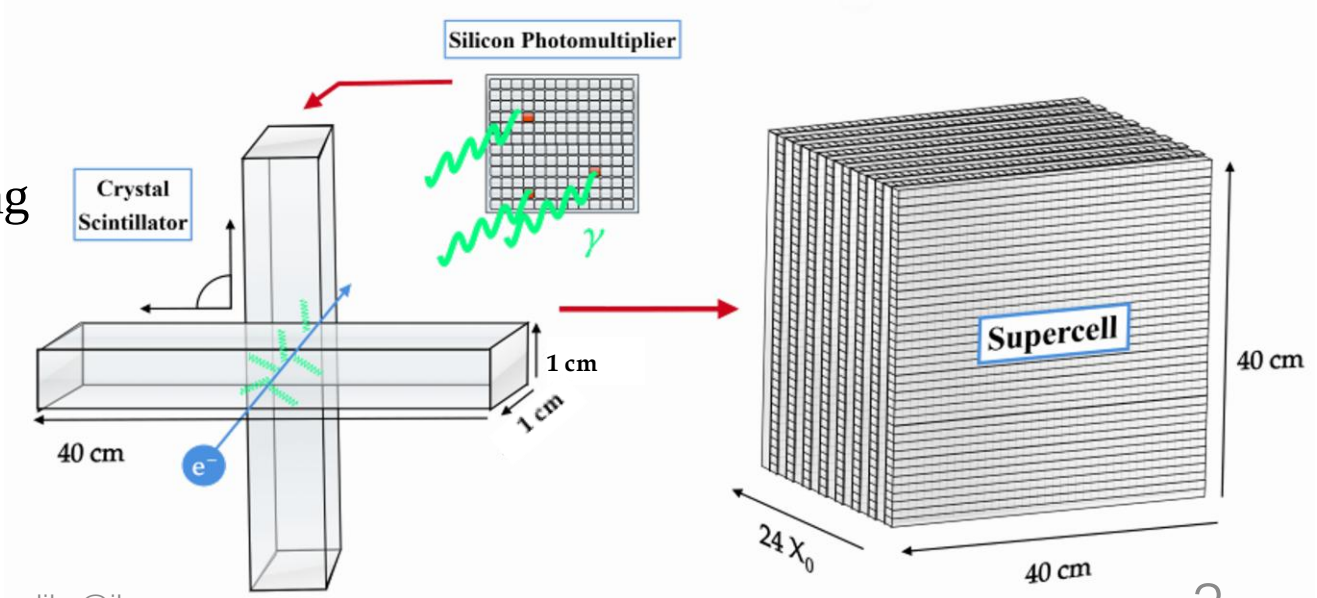
➢ CEPC: Circular Electron-Positron Collider

- A next-generation large collider for high energy physics proposed by China. Its primary scientific goal is to operate as a high-luminosity "Higgs factory", enabling precision measurements of the Higgs boson properties



➢ ECAL: Electromagnetic Calorimeter

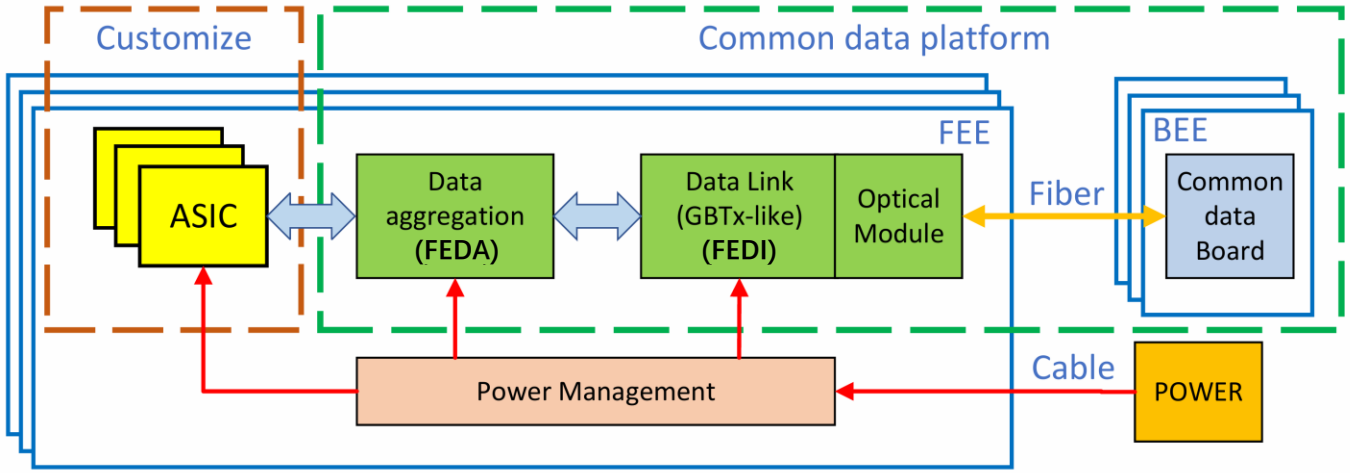
- Made of orthogonally arranged long scintillating crystals (BGO), each was read out by silicon photomultipliers (SiPMs) at both ends
- Providing both position and energy resolution



Background

➢ Schematic of the ECAL readout electronics

- Divided into front-end electronics (FEE) and back-end electronics (BEE), communicating via optical fibers
- Front-end ASIC: extracts timing and amplitude information from the detector output signals



➢ Performance requirements of the ECAL front-end electronics

- Challenge 1: wide dynamic range of 30000
- Challenge 2: SiPM output pulse widths ~1 μs for wide pulses

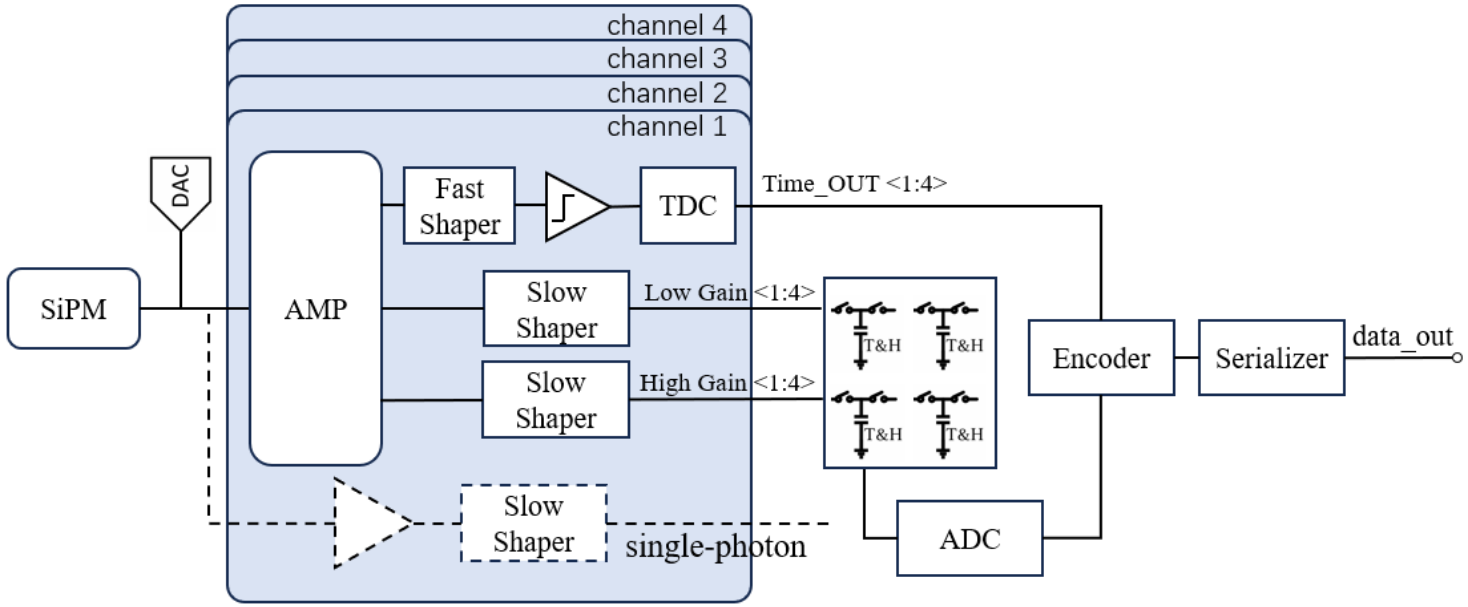
Parameters	Requirements
Charge Range	0.128 pC~ 3.84 nC (0.1~3000 MIP)
Charge Resolution	10 % (1.0 MIP), 1 % (100 MIP)
Timing Resolution	200 ps (1 MIP), 100 ps (12 MIP)
Integral Non-linearity	< 1 %
Average Event Rate/channel	13 kHz
Max Event Rate/channel	230 kHz
Typical Signal Rising Edge	40 ns
Typical Signal Width	~ 1 μs

Chip Design

➢ SIPAC — SiPM readout ASIC for the CEPC detector

- The dynamic range is covered by three gain paths, jointly achieving a 30000× input dynamic range
- Switched-capacitor sampling array and ADC for amplitude measurement, accommodating pulses of different widths and handling baseline drift
- TDC for time measurement
- DAC for gain uniformity among SiPMs

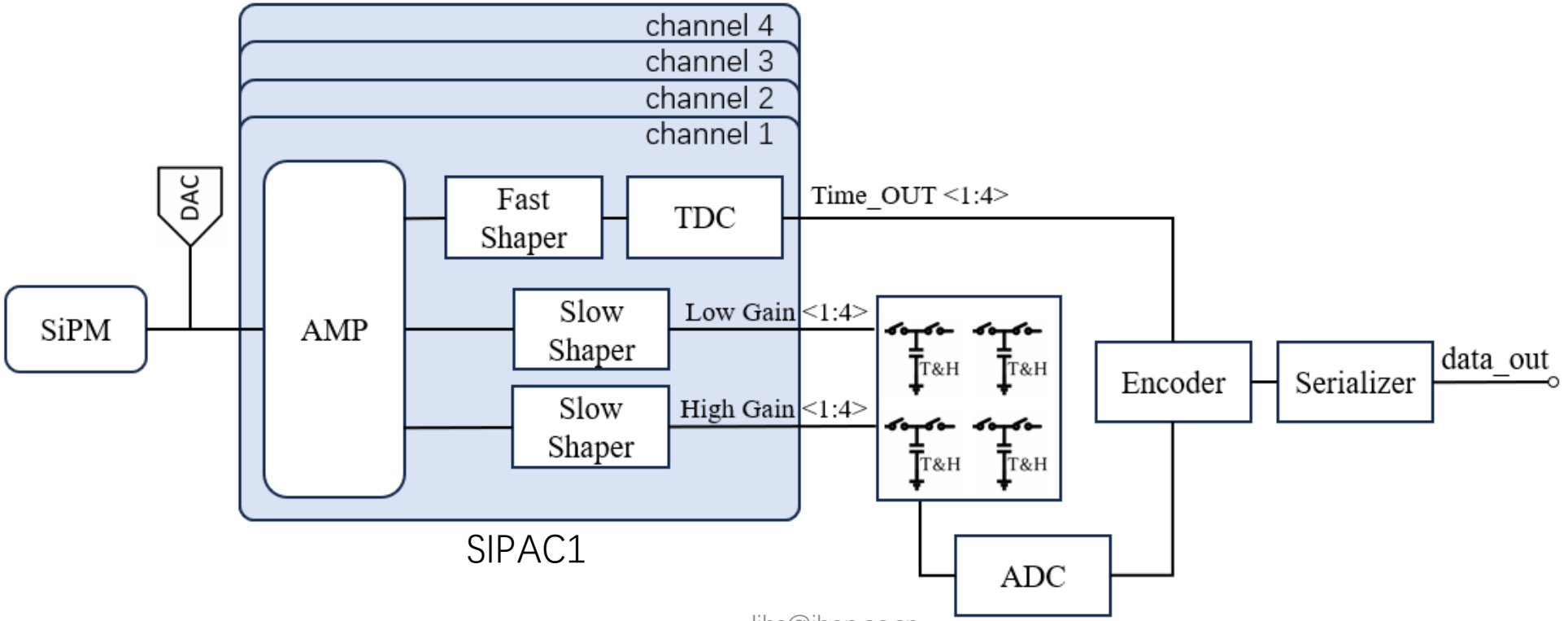
Characteristics	Value
Charge Dynamic Range	1.28 pC∼3.84 nC
Charge resolution	10%@1.28pC, 1%@128pC 1%@100 MIPS
Time resolution(RMS)	200 ps @1.28pC, 100 ps @12.8pC
Detector Capacitance	≤ 100 pF
Max signal rate/channel	500 kHz/ch
ADC	10-bit
TDC resolution	8-bit
TDC bin width	100 ps
Power consumption	15mW/channel
Num. of channels	4



SIPAC0

Chip Design

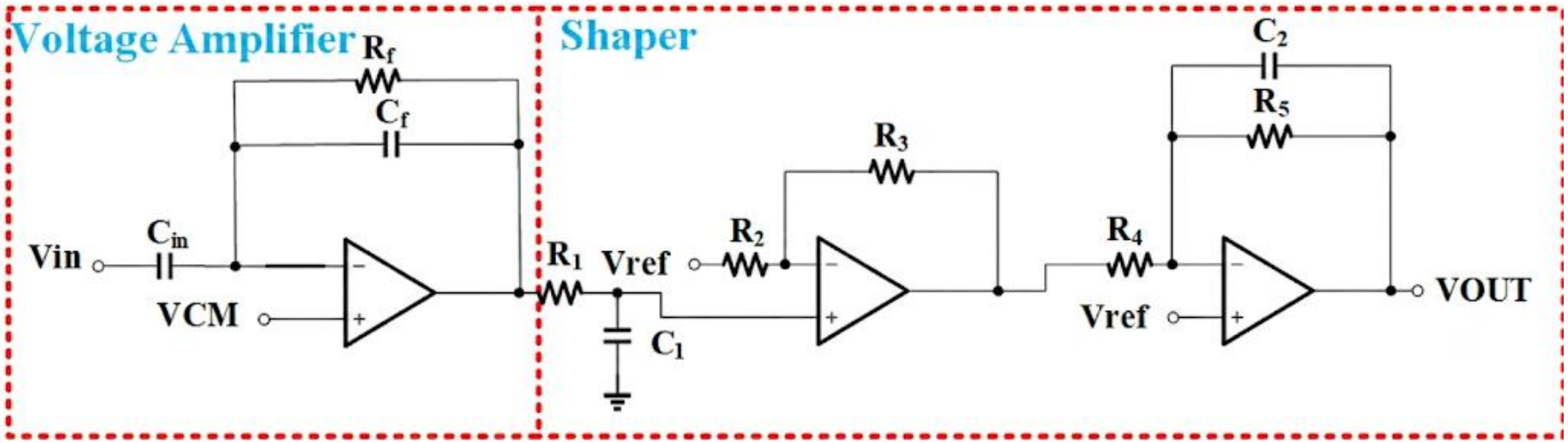
- DAC: 6-bit, adjusts the SiPM bias voltage
- Preamp: voltage amplifier
- Two gain paths: high and low
- Shaper: 2nd-order RC integration
- SCA: sampling depth of 9
- ADC：12-bit SAR ADC，40MHz
- TDC：100 ps
- Serializer: 1.3 GHz



Chip Design

- ➢ Preamp: voltage amplifier
- Initial amplification of the signal
- AC coupling required to isolate the DAC voltage

- ➢ Slow shaper: 2nd-order RC shaping
- Further amplifies the signal
- Improves the signal-to-noise ratio

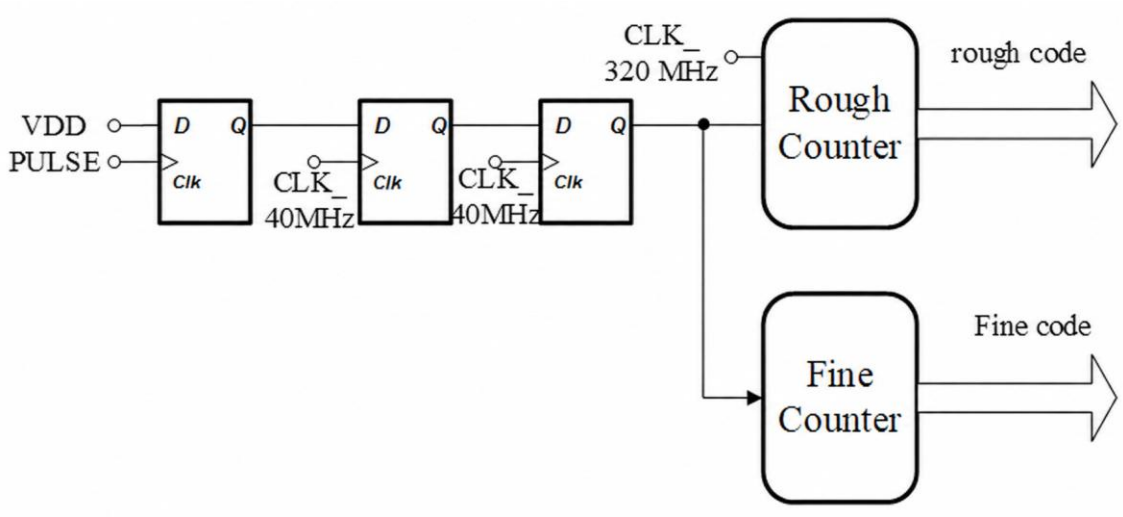


Preamp and slow shaper circuit design

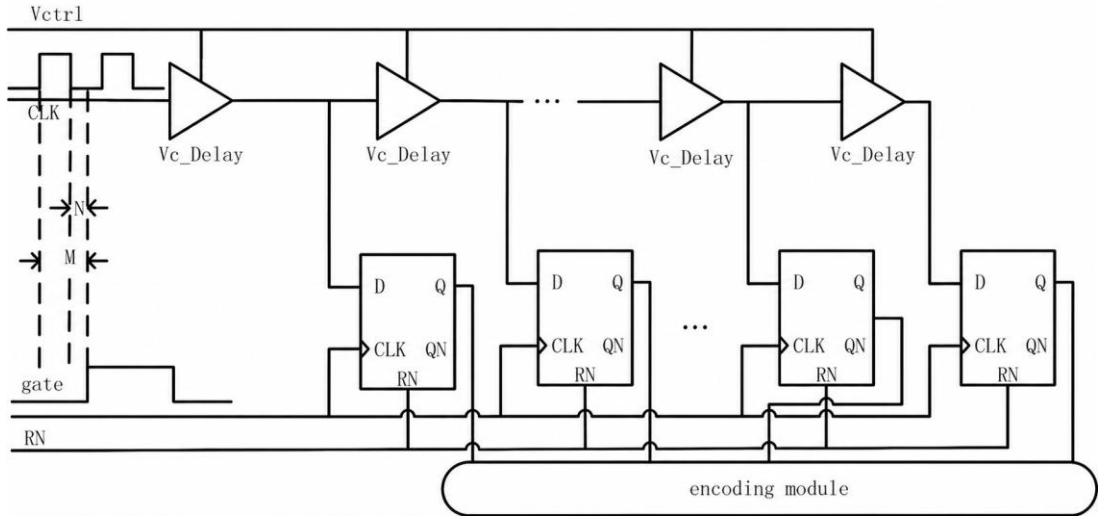
Chip Design

➢ TDC

- Two-step TDC architecture: time measurement is split into coarse and fine counting
- Coarse counting with a counter clocked at 320 MHz
- Fine counting with a delay line, measuring the time difference between the signal and the clock edge



TDC architecture

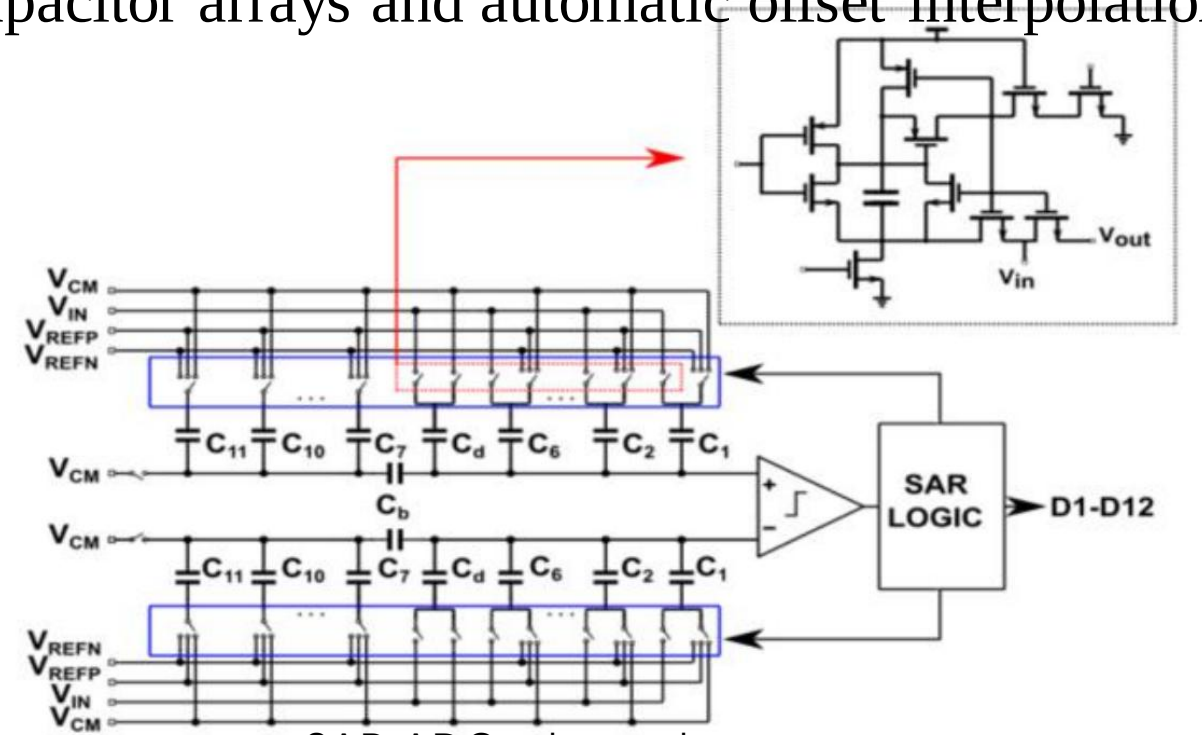


Delay line circuit

Chip Design

➢ ADC

- Successive-Approximation-Register (SAR) ADC
- 12-bit resolution, 10-bit effective (ENOB)
- On-chip single-to-differential amplifier converts the single-ended input to differential
- Employs segmented capacitor arrays and automatic offset interpolation techniques

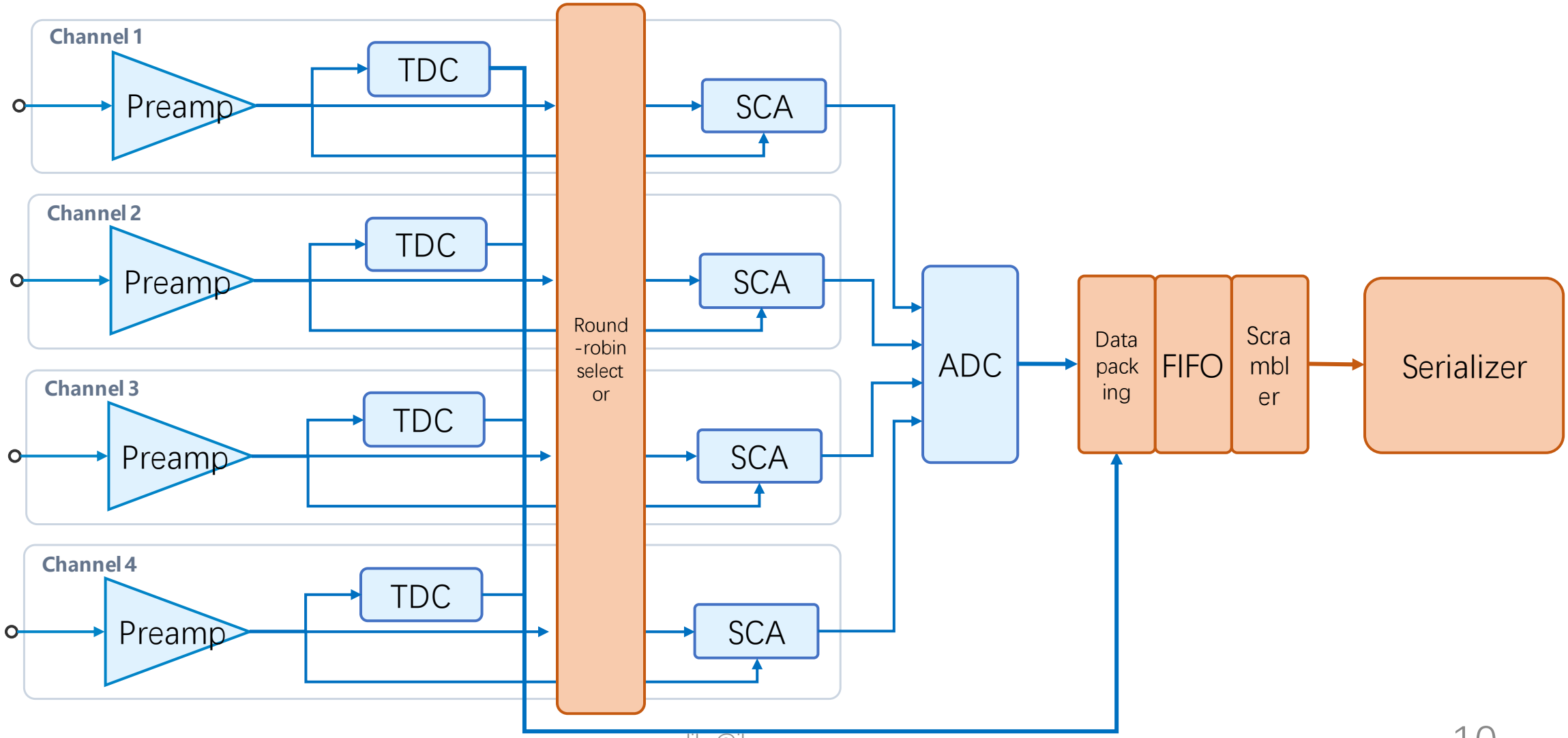


SAR ADC schematic

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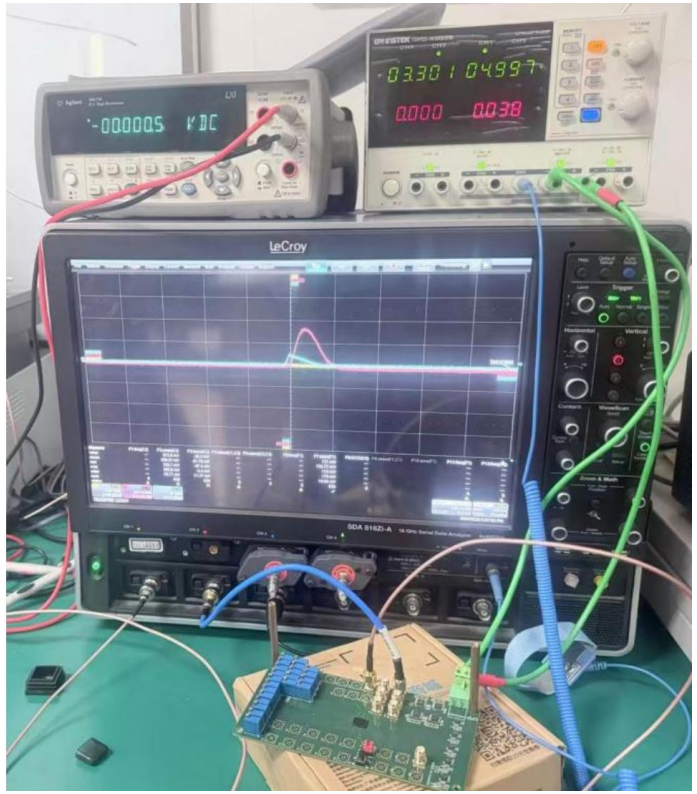
Chip Design

- Digital logic flow



Chip Testing

- SIPAC0 submitted for tape-out in April 2025
- SIPAC1 submitted for tape-out in October 2025



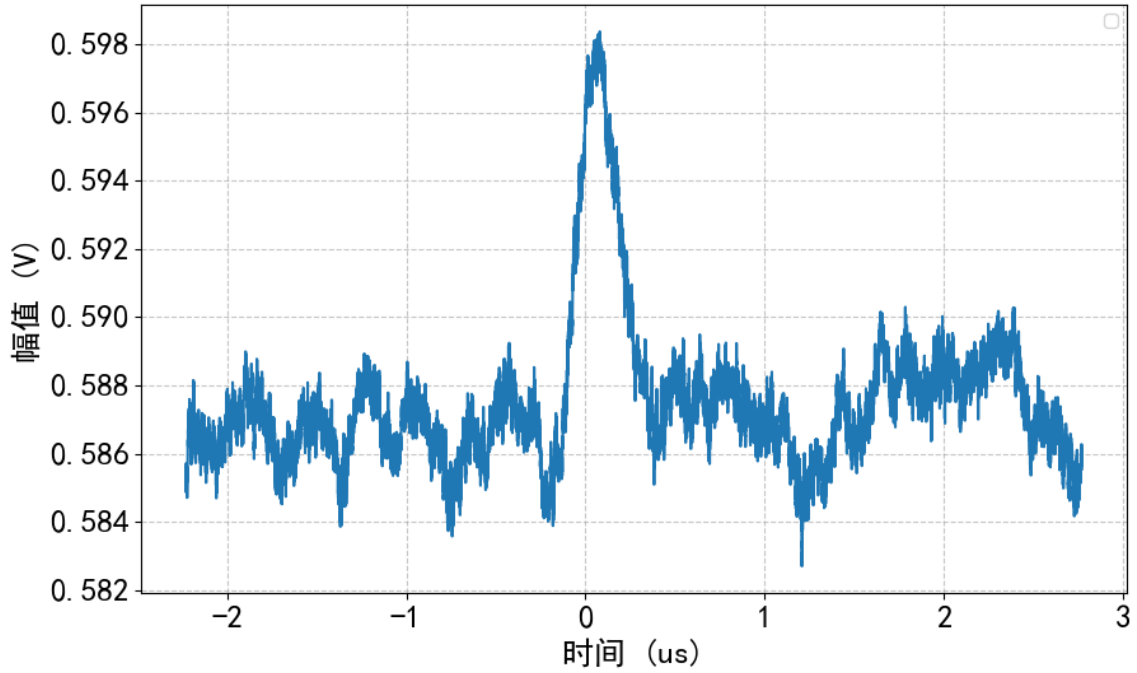
- SiPM (NDL-EQR06): gain of 8×10^4; typical output pulse with 40 ns rise time and 280 ns fall time after BGO crystal
- Amplitude measurement: triangular pulses (40 ns rise, 280 ns fall) generated with an arbitrary waveform generator
- Timing measurement: a 500 kHz square wave from a pulse generator used as the input

SiPM Type	NDL EQR06
Pixel Pitch μm	6
Pixel Quantity in 3 × 3 mm^2	244,719
Pixel Gain	8×10^4
Typical peak PDE	30 % (at 420 nm)
Typical DCR (20 °C)	2.5 MHz
Inter-pixel Crosstalk	12 %
Terminal Capacitance (pF)	45.9 pF

Chip Testing

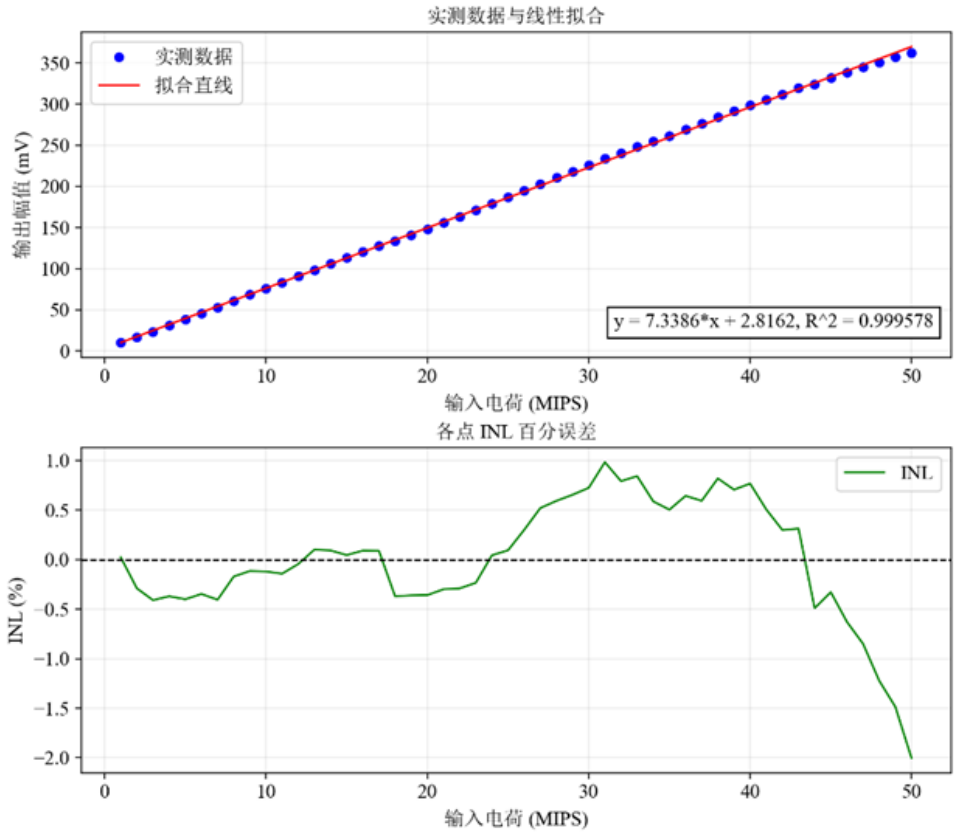
- Analog front-end test (amplifier + shaper) — SNR test

- With 1 MIP input (equivalent to a triangular pulse of 0.3 mV peak), the signal is 11.8 mV, the baseline RMS noise 0.9 mV, giving an SNR of 13.3

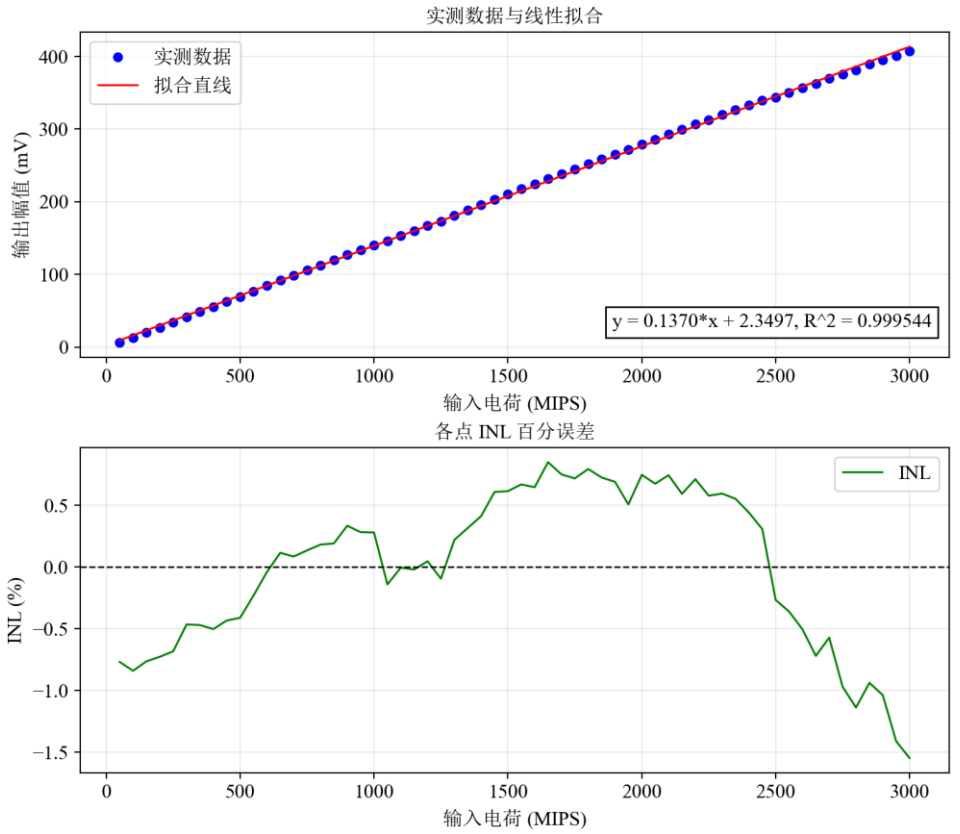


Silicon Testing

- Analog front-end test (amplifier + shaper) — integral nonlinearity (INL) test
- High-gain range: gain of 24.45, maximum nonlinearity error of 2%
- Low-gain range: gain of 0.46, maximum nonlinearity error of 1.5%



High gain



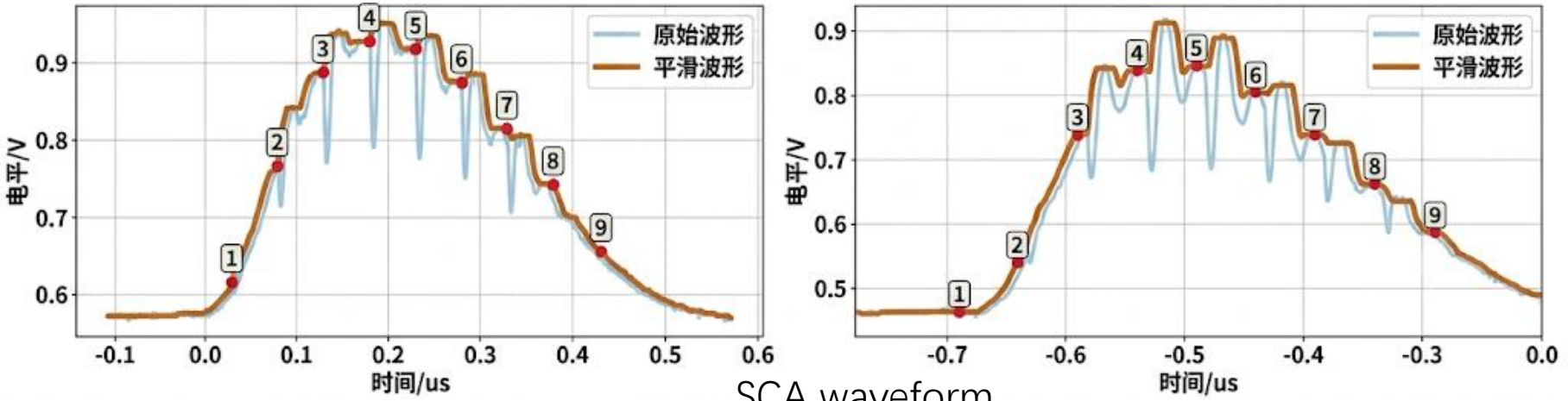
Low gain

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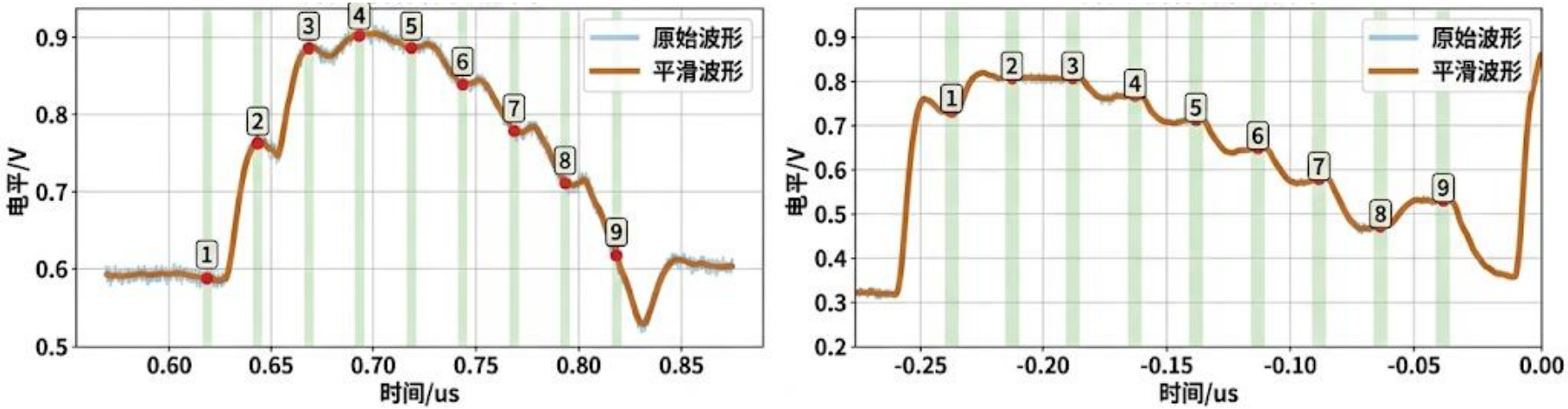
Chip Testing

➢ Analog front-end + SCA test

Analog front-end waveform



SCA waveform



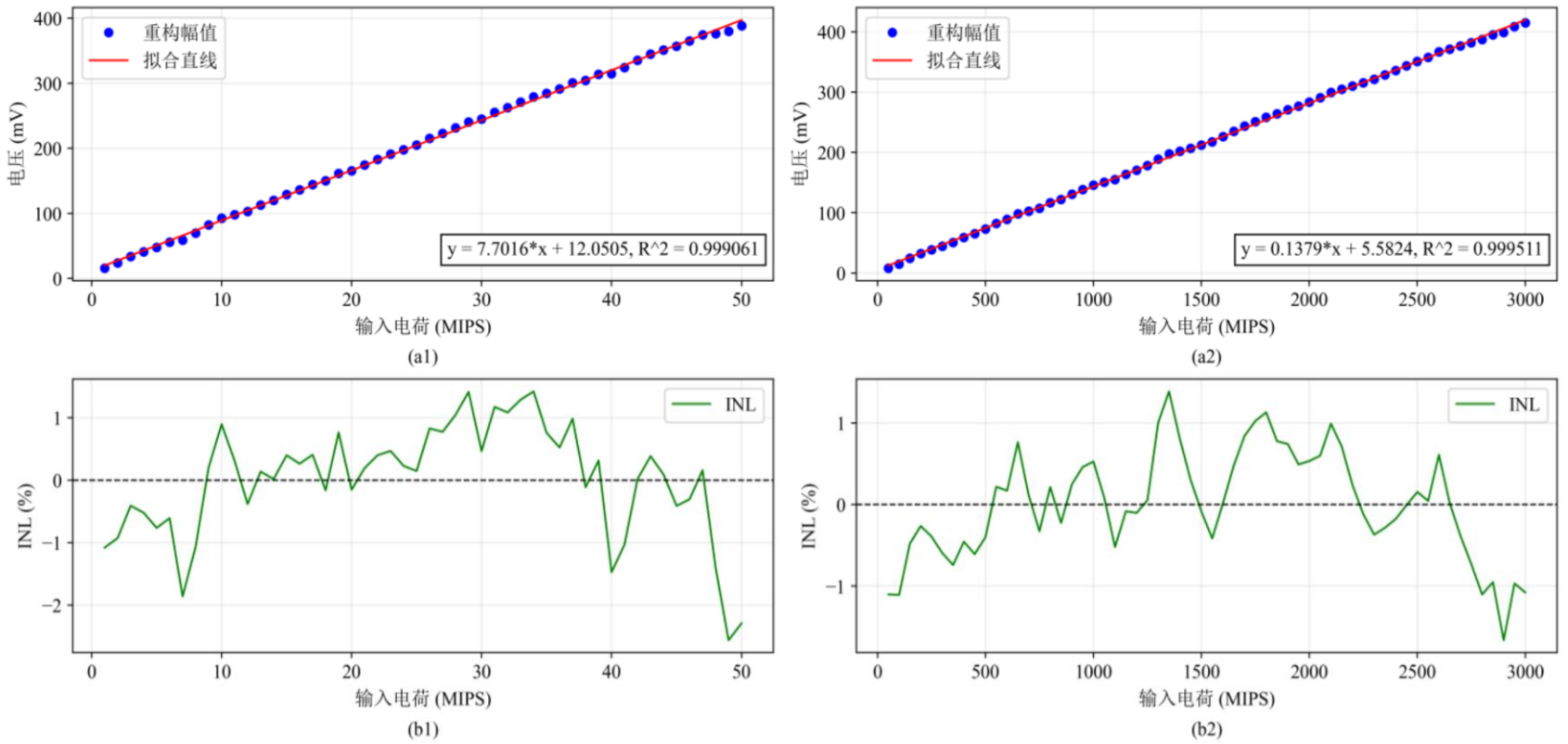
High gain

Low gain

- Local undershoot introduced by the sampling action
- Low-gain points out of order: the 8th and 9th sampling points are shifted forward

Chip Testing

- Analog front-end + SCA + ADC test — linearity test
- Maximum nonlinearity error: 2.5% for high gain, 1.6% for low gain



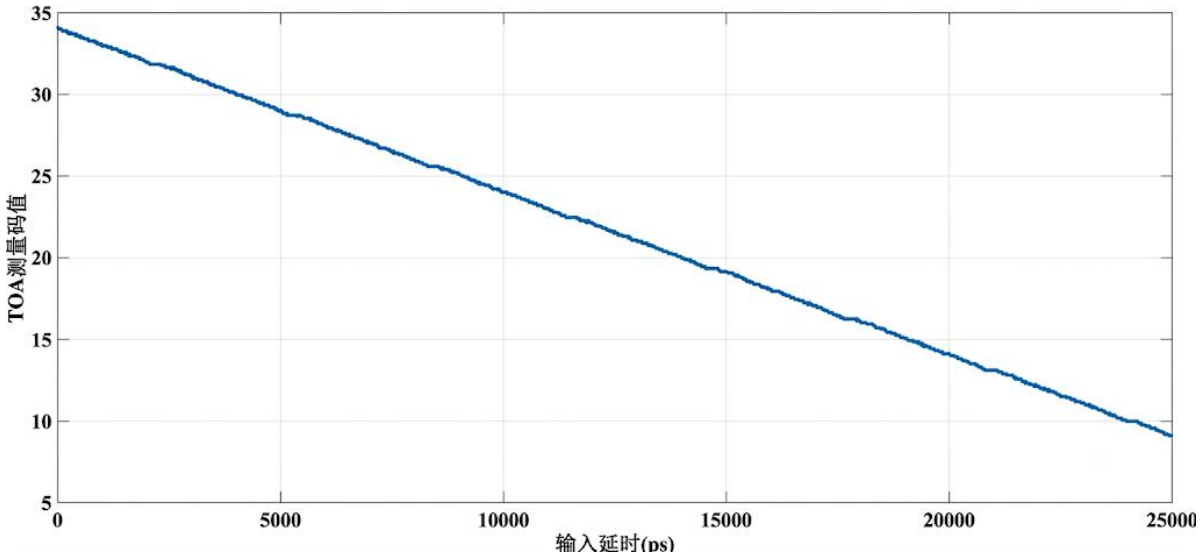
High gain

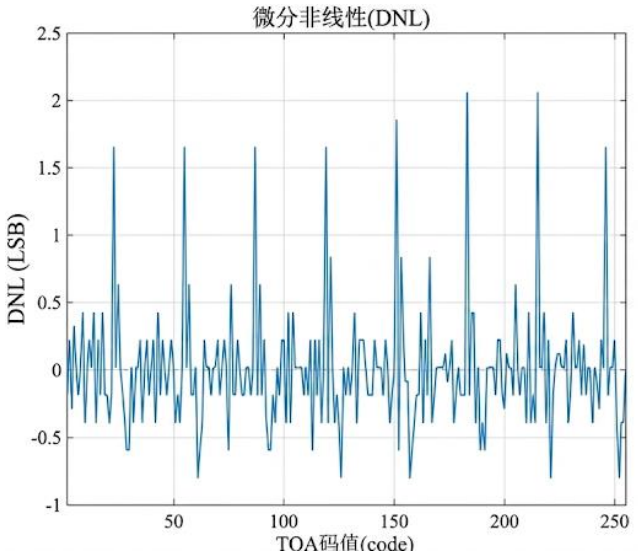
Low gain

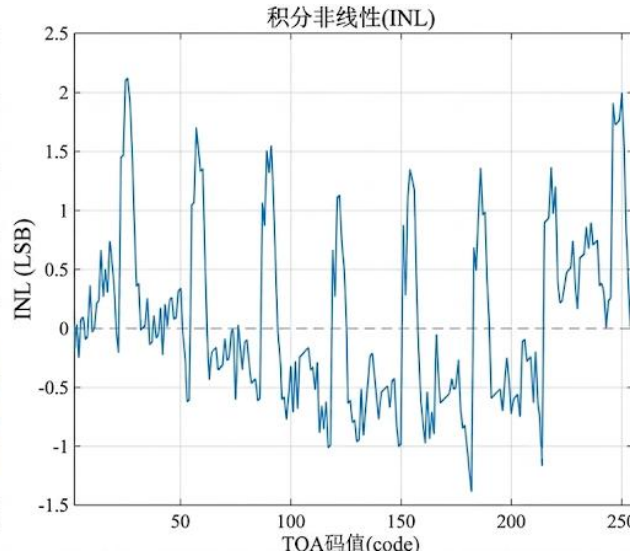
SCA+ADC:
2% → 2.5%
1.5% → 1.6%

Chip Testing

- TDC test
  - The delay of the input pulse relative to the reference clock was scanned from 0 to 25 ns in 20 ps steps
  - No missing codes; 1 LSB = 102 ps
  - DNL and INL show periodic peaks spaced by one coarse-count period — mismatch







Summary

- A SiPM readout ASIC has been designed, capable of simultaneous timing and amplitude measurement
  - Signal input dynamic range of 0.3 mV–900 mV, achieved with high/low gain paths
  - Waveform sampling via SCA and a 40 MHz ADC; INL better than 2.5%
  - On-chip TDC with timing precision better than 100 ps
- Overall meets the design requirements; linearity still needs optimization
- Further studies with SiPMs, such as charge resolution, are planned

	Design spec	Test result
Input dynamic range	1~3000 MIP	1~3000 MIP
Integral nonlinearity	1%	High gain 2.5%, low gain 1.6%
SNR	10	13.3@1MIP
TDC precision	100ps	102ps
Power	15 mW/channel	14 mW/channel
Max event rate	230 kHz	500 kHz

Thank you!

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