CMOS MAPS with and without intrinsic gain layer for tracking and timing

cea irfu

DRD3

Cactus/MiniCactus

Université Paris Cité

IFAE Institut de Física d'Altes Energies

40 anys fent grans les coses petites CNM Institut de Microelectrònica de Barcelona

EXCELENCIA MARÍA DE MAEZTU

CSIC

UNIVERSITY OF LIVERPOOL

CASSIA

CERN

miniel

CPPM

UNIVERSITÄT BONN

GSI Helmholtzzentrum für Schwerionenforschung GmbH

IPHC Institut Pluridisciplinaire Hubert CURIEN STRASBOURG

KEK

KYUSHU UNIVERSITY

筑波大学 University of Tsukuba

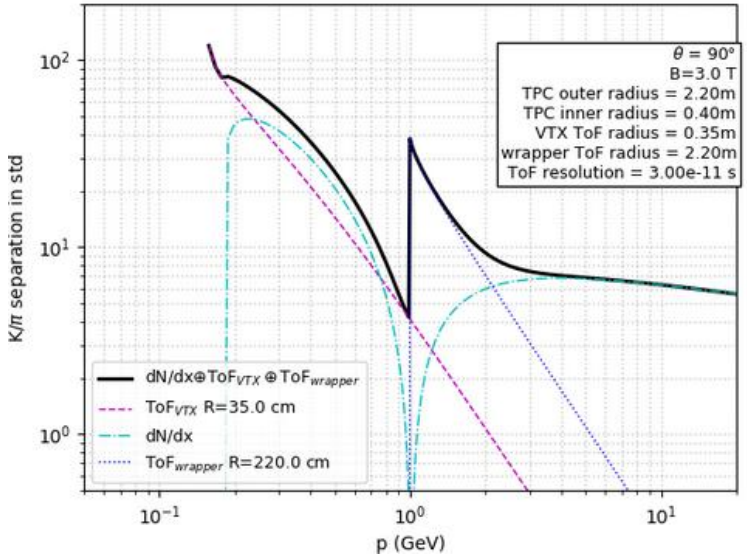
இந்திய தொழில்நுட்ப கழகம் மெட்ராஸ் भारतीय प्रौद्योगिकी संस्थान मद्रास Indian Institute of Technology Madras

University of Glasgow

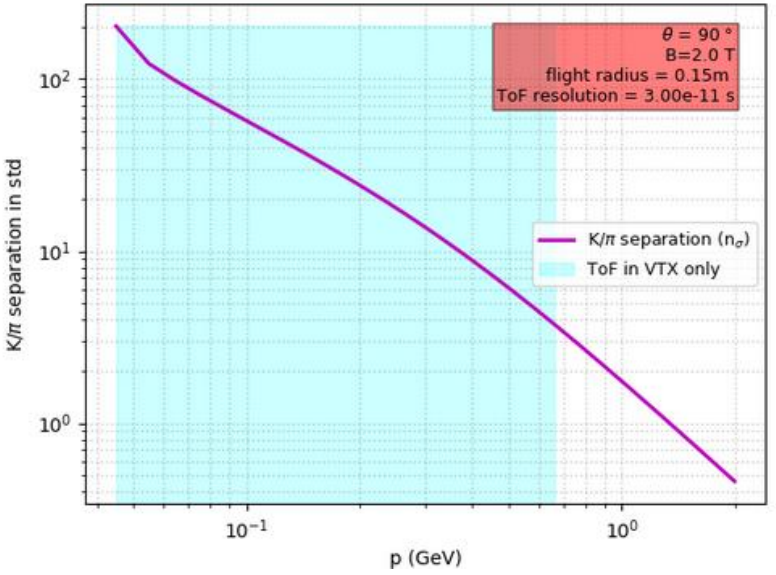
Universität Zürich[UZH]

UNIVERSITÄT BERN

Motivations for a TOF detector



Improve π/K separation at low momentum
TOF wrapper radius 2.2 m



TOF wrapper could be complemented by timing layer (radius 15 cm) for 0.045<p<0.66 GeV/C (not reaching the 2.2 m wrapper)

Physics cases :
H→fermions
Flavour physics
Heavy Neutral Leptons

Also possible to use timing to complement the first layers of a CALICE like calorimeter (5D tracking)

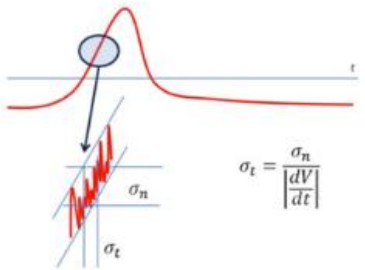
Expression of Interest
« Toward MCMOS Time of Flight Tracking Layers for a detector at FCC-ee », IP2I and Irfu

Features of monolithic CMOS sensors

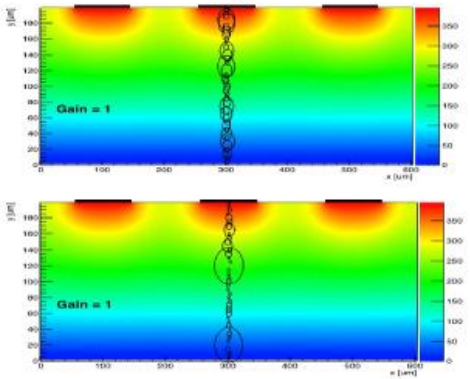
- (Relatively) cheap high volume industrial technology
  - 2-3 k euro/8'' wafer, post-processing and dicing included → bare sensor cost for 100 m^2 : 7-11 M euros
  - Bump bonding operation not needed for fully monolithic architecture
- Stable and easy operation
- HV-HR wafers available, allows charge collection by drift and not only by diffusion → favorable for fast collection (and also for radiation hardness)
- Can in principle be designed as a complete SoC, from sensor to DAQ interface
- Can be thinned down to < 100 µ

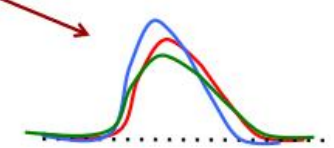
Time resolution ingredients

$$\sigma_t^2 = \left(\frac{Noise}{dV/dt}\right)^2 + (\Delta ionization)^2 + (\Delta shape)^2$$



"Jitter" term





Signal shape is determined by Ramo's Theorem

$i \propto qvE_w$

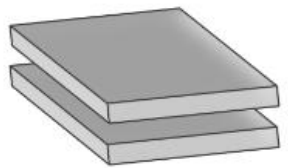


Illustration taken From N. Cartiglia (VCI 2022)

Small noise → choice of technology, small detector capacitance
High dv/dt →
High electric field (but Vd saturates around 1 V/µm)
Intrinsic amplification ?

Amplitude variation → Timewalk, corrected offline

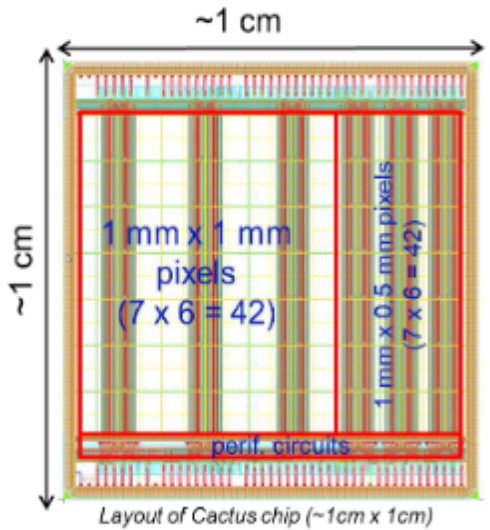
Non-homogeneous energy deposition → cannot be corrected, minimized by design (thin sensor)

Saturated drift velocity in sensor volume → Uniform weighting field

Parallel plate geometry, easier for big pixels → Large electrode designs

Timeline of CACTUS/MiniCACTUS chips in LF150 nm technology

CACTUS demonstrator

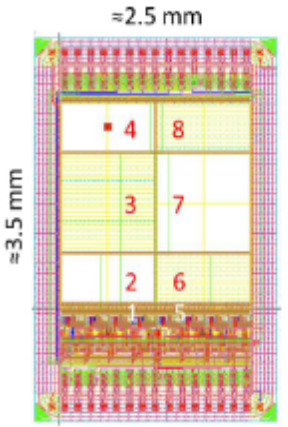


Layout of Cactus chip (~1cm x 1cm)

- Design inspired from LFCPIX/LF-MONOPIX chips
- Initially motivated by ATLAS/HGTD
- High breakdown voltage < -300 V
- Homogeneous charge collection, deep depletion depth
- Good yield (Engineering Run)
- Poor timing performance (≈ 500 ps) due to high in-pixel parasitic capacitances

[Y. Degerli et al., June 2020, JINST 15 P06011]

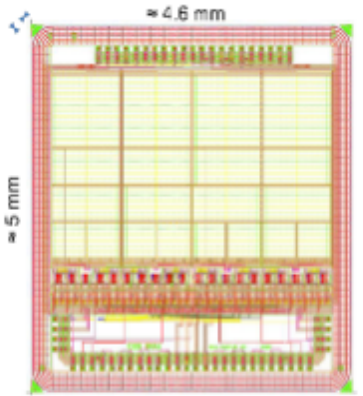
MiniCACTUS_v1



- High in-pixel parasitic capacitance addressed by moving the FEs at column-level
- 100, 200 and 300 µm sensors tested
- Time resolution with MIPs ≈ **65 ps** @ -450V on 0.5 x 1 mm² pixel (200 µm-thick sensor)
- Ringing on digital outputs due to coupling from the digital buffers impacting the time walk correction

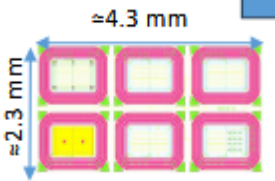
[Y. Degerli et al., Nov. 2023, IEEE TNS, 70]

MiniCACTUS_v2



- Ringing on digital outputs addressed by several modifications. New analog front-ends.
- 150, 175 and 200 µm sensors tested
- Very high breakdown voltage < -500 V
- No analog/digital coupling anymore

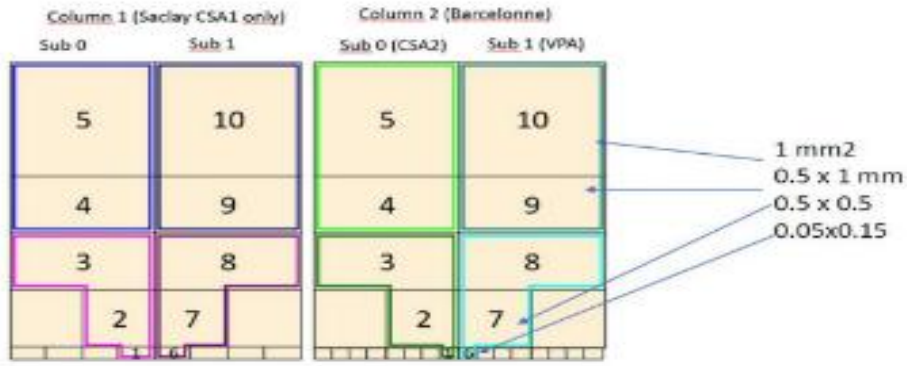
CACTUS-GL



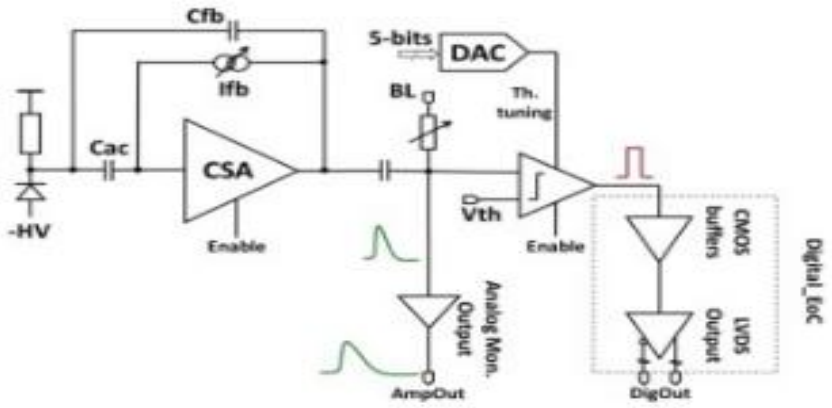
- Implantation of a gain layer
- Deep junction LGAD concept, buried PN junction implemented by the foundry
- 6 different chips with passive diodes

MiniCACTUS_v2

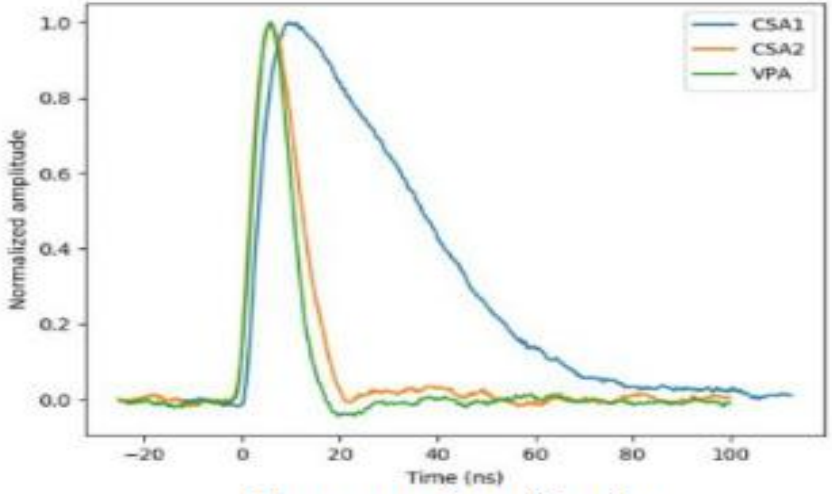
- CEA-IRFU and IFAE collaboration
- Slow control, DACs and bias on-chip
- Pixel sizes: 1x1 mm², 1x0.5 mm², 0.5x0.5 mm²
- Post-processed samples to 150, 175 and 200 µm
- No gain on sensor
- No TDC
- Featuring three pre-amplifiers:
  - Two CSA and one VPA
  - Different return-to-baseline times



Pixels overview



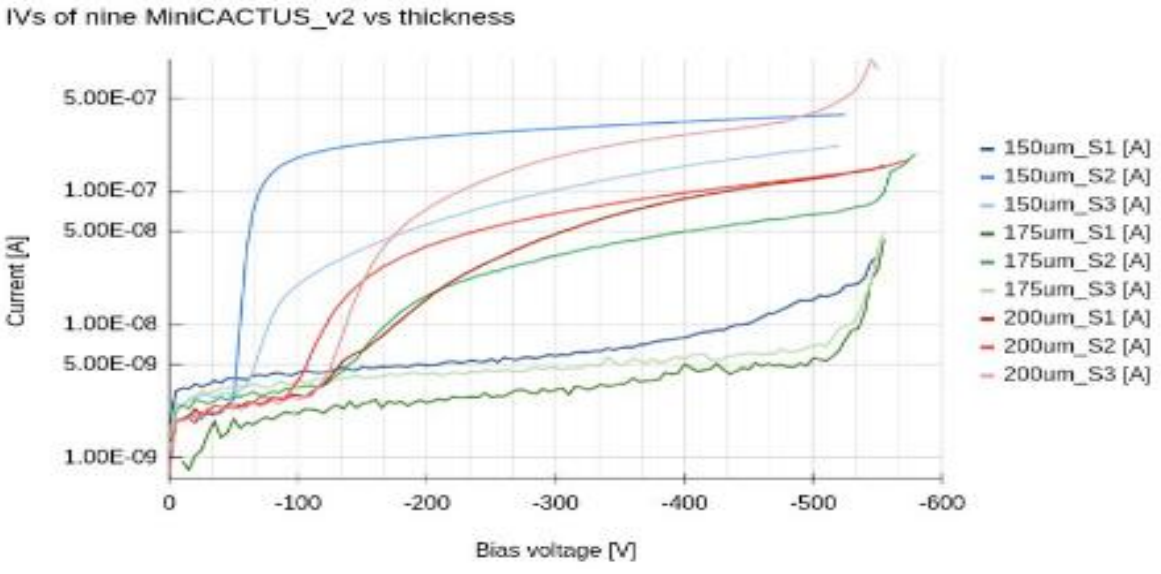
Sensor FE architechture



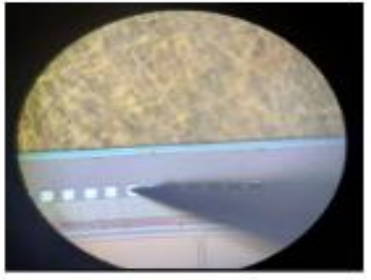
Return-to-baseline time

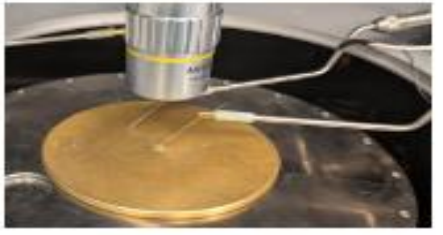
MiniCACTUS_v2 characterization

- In-lab characterization:

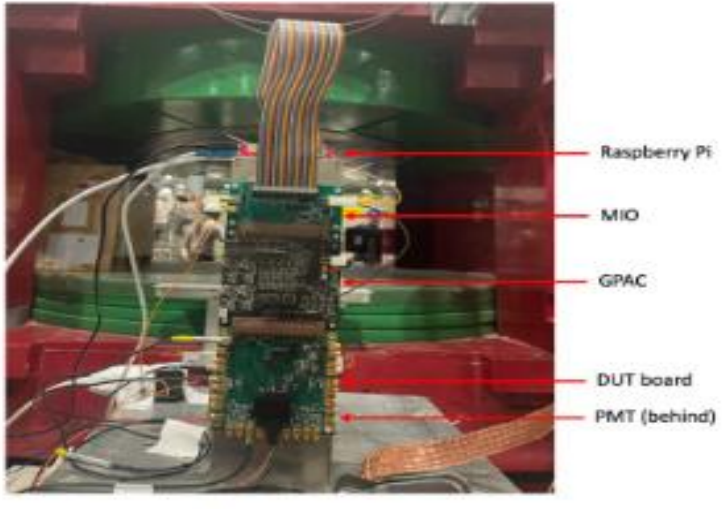


Sensor IVs: breakdown voltages generally > 500V





IV measurement on bare dies with a probestation



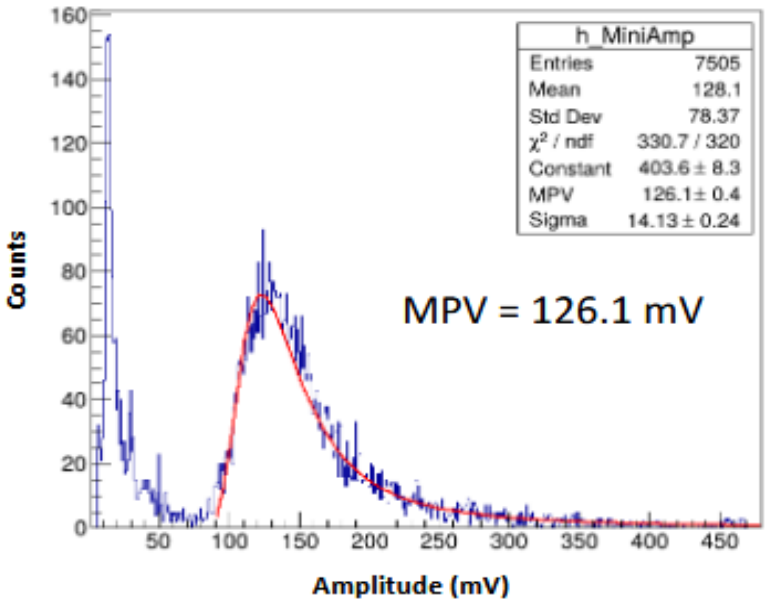
DAQ setup

- Three testbeam campigns at CERN SPS:
  - July 2024 (parasitic DRD1, muons)
  - July 2025 (parasitic DRD1, muons + pions)
  - October 2025 (DRD3, pions)

Test-beam of MiniCACTUS_v2 in July 2025 (DRD1)

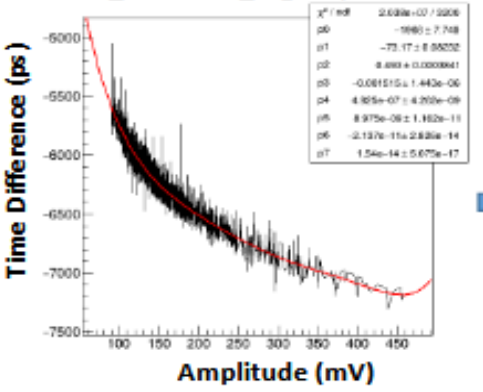
Chip#04B, pixel 1-2, **0.5 x 0.5 mm², 175 µm, -500V** (Back-side pol.)

MiniCACTUS_v2 Analog Monitoring Output (AmpOut)

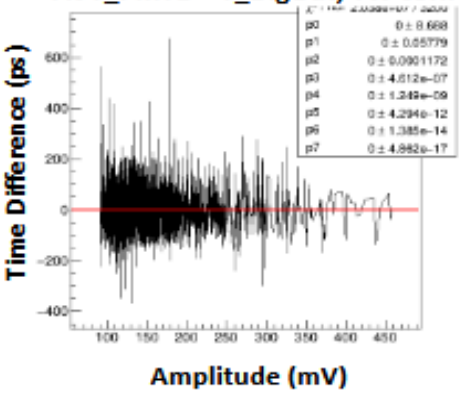


TW corrections

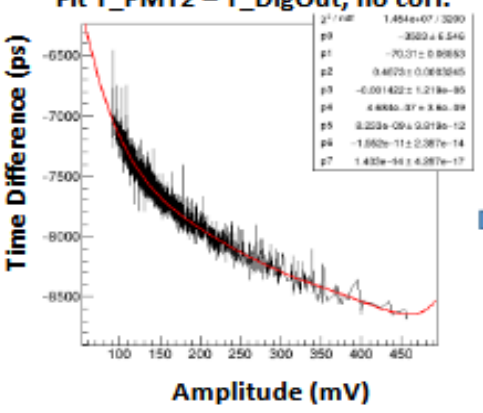
Fit T_PMT1 – T_DigOut, no corr.



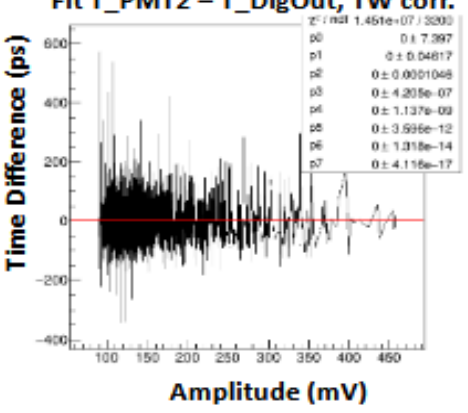
Fit T_PMT1 – T_DigOut, TW corr.



Fit T_PMT2 – T_DigOut, no corr.

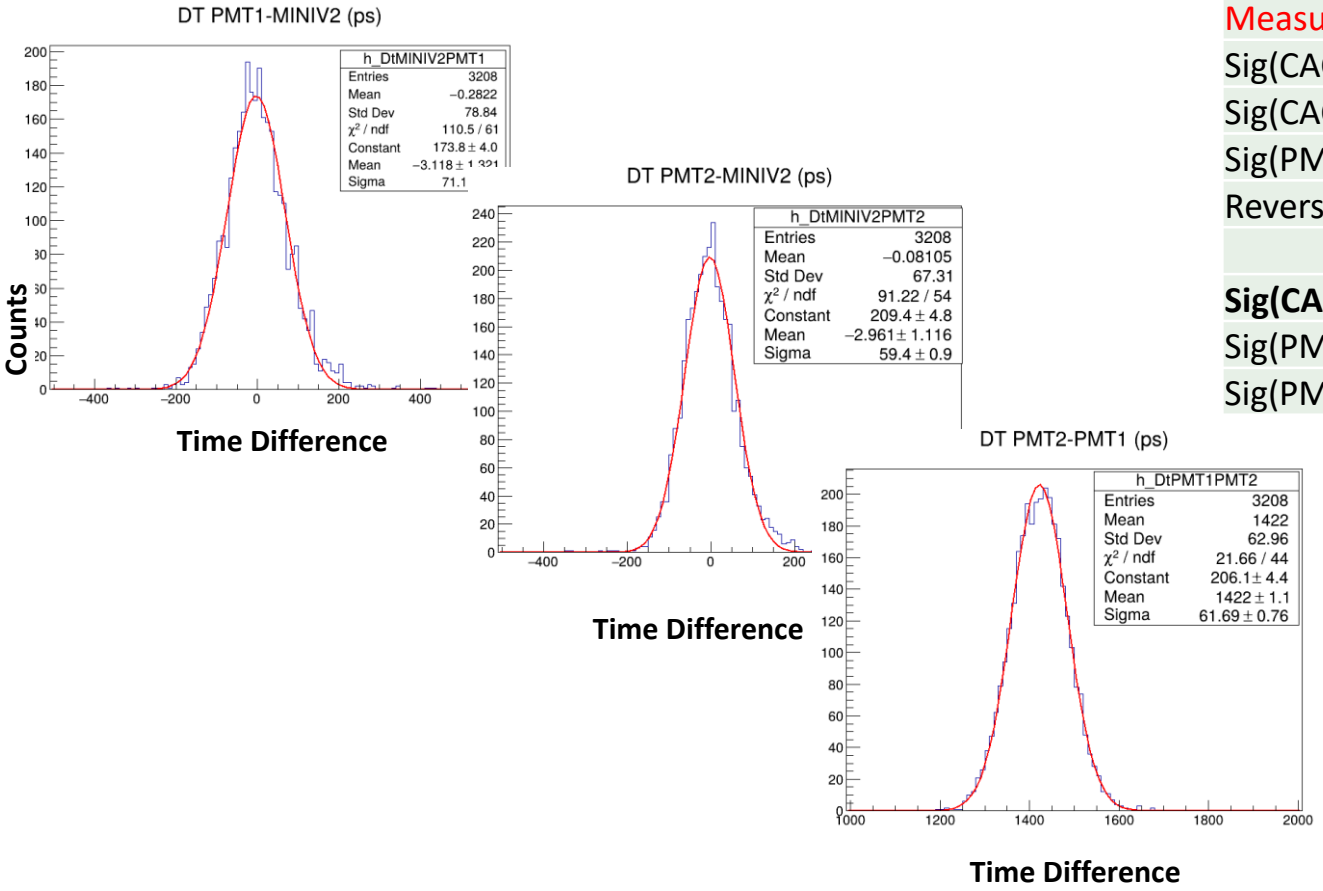


Fit T_PMT2 – T_DigOut, TW corr.



Test-beam of MiniCACTUS_v2 in July 2025 (DRD1)

Chip#04B, pixel 1-2, **0.5 x 0.5 mm²**, **175 µm**, **-500V** (Back-side pol.)

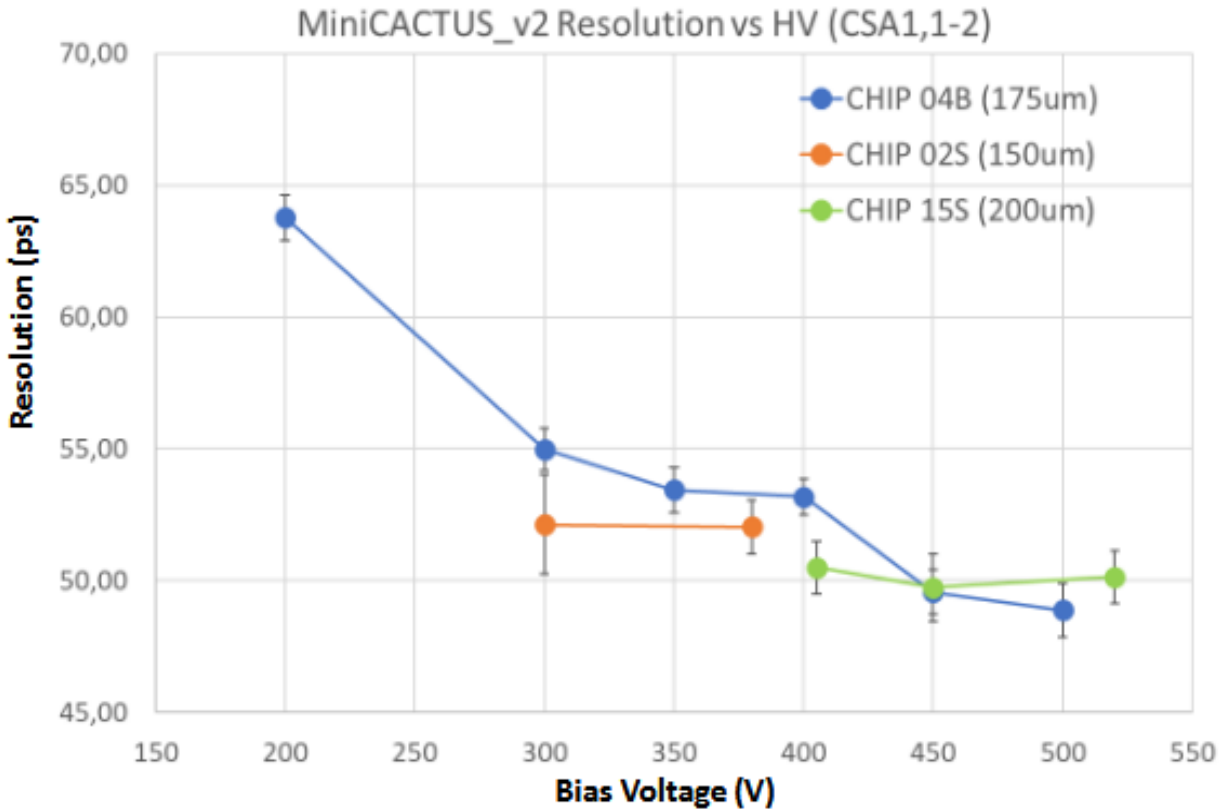


Measured Sigma Matrix after TW correction (ps)		
Sig(CACTUS-PMT1)	71.1	1
Sig(CACTUS-PMT2)	59.4	0.9
Sig(PMT2-PMT1)	61.69	0.76
Reverse of the matrix to get the sigma of each devices		
	Resolution (ps)	Errors (ps)
Sig(CACTUS)	**48.88**	1.03
Sig(PMT1)	51.64	0.97
Sig(PMT2)	33.76	1.49

Power consumption in this configuration : 0.6 W/cm^2

→ The timing resolution measured for this pixel is **48.88 ps** after time walk correction with integrated the on-chip FE and discriminator

Test-beam of MiniCACTUS_v2 in July 2025

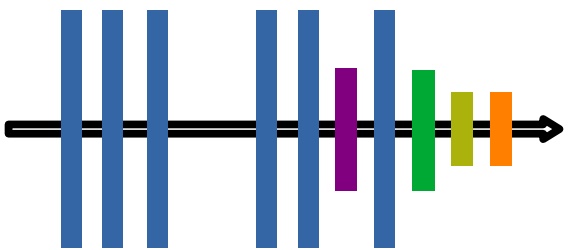


Summary of measurements with the scope for 0.5 x 0.5 mm² pixels

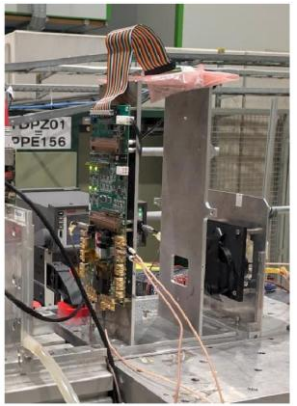
→ The 175 and 200 µm sensors give quite close results at high bias voltages → the optimum thickness seems to be around 175µm

Testbeam October 2025 - DRD3

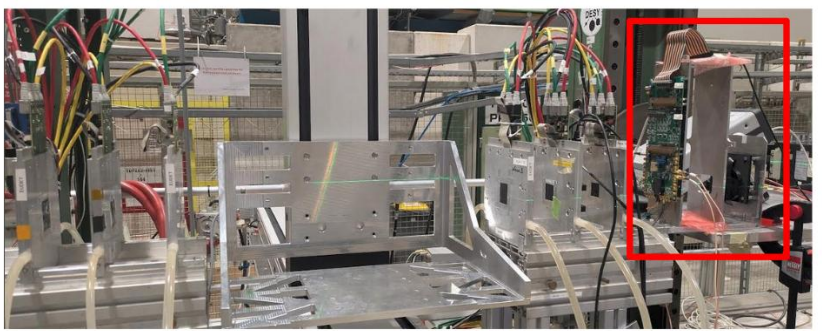
- 12 bit, 50 GS/s, 5 GHz bandwidth scope
- Using EUDAQ framework
  - Adapted producer from HGTD for the scope
  - Allowing to run Corryvreckan
- CERN SPS/H6 North Area with pions
- Detectors setup:
  - **EUDET Telescope**: tracking
  - **CROC**: For triggering ROI
  - **DUT**: MiniCactus_v2
  - **PMT**: Auxiliar timing reference
  - **MCP**: Timing reference



Detectors schematic

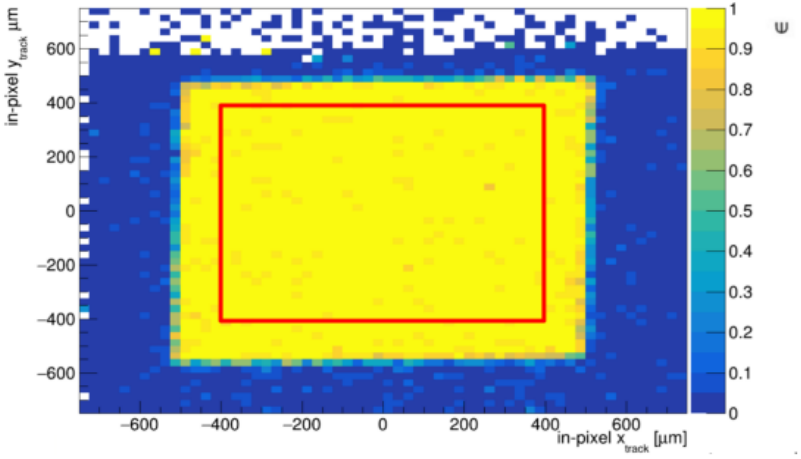


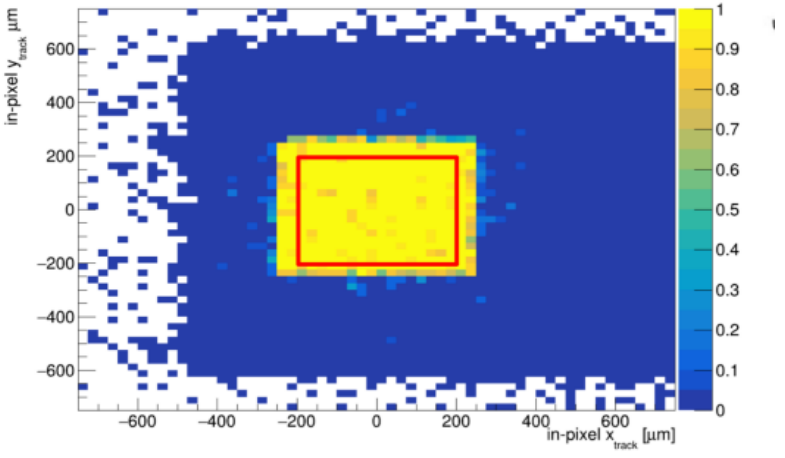
Zoom on DUT setup



DUT setup

MiniCactus V2 detection efficiency





CSA2

1x1 mm²

*ROI of 0.8x0.8 mm²



Hit Efficiency
99.0 ± 0.1 % within the ROI*
@ 350 V

CSA2

0.5x0.5 mm²

#ROI of 0.4x0.4 mm²

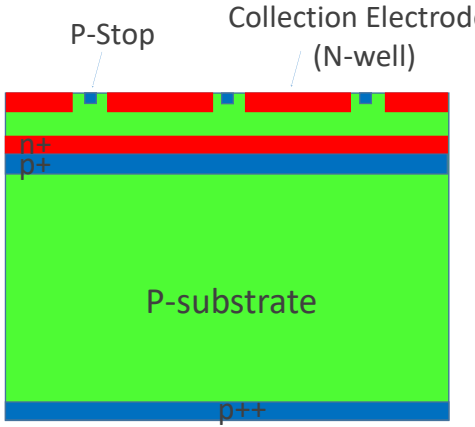


Hit Efficiency
98.6 ± 0.3 % within the ROI#
@ 400 V

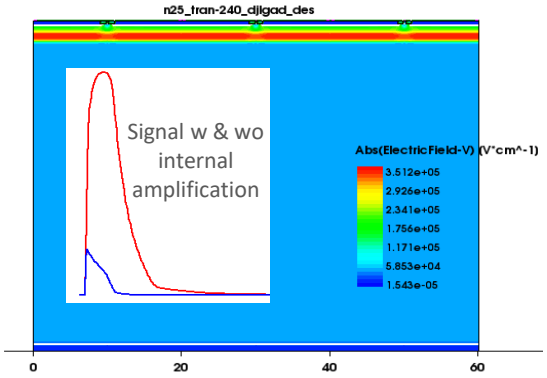
How to improve further the performances: CACTUS-GL

- Add intrinsic gain to:
  - Improve S/N → Potential improvement on time resolution
  - Reduce sensor thickness → Reduce Landau fluctuations
  - Reduce FE power consumption
  - Reduce pixel pitch
- Ultimate goal is to reach <30 ps resolution
- CACTUS-GL prototype submitted to fabrication in May 2024 (MPW run)
  - Deep junction LGAD concept with buried PN-junction
  - TCAD simulations done with Sentaurus
  - Charge multiplication factor of ~10 expected from these simulations
  - PN junction implemented by the foundry (2 different P-dose versions)
  - Production implied only minimal modifications to LF15A standard process
    - change of implant energy of 1 layer (DNW)
    - addition of 1 customer layer

Cross section of the active area of CACTUS-GL (not to scale)



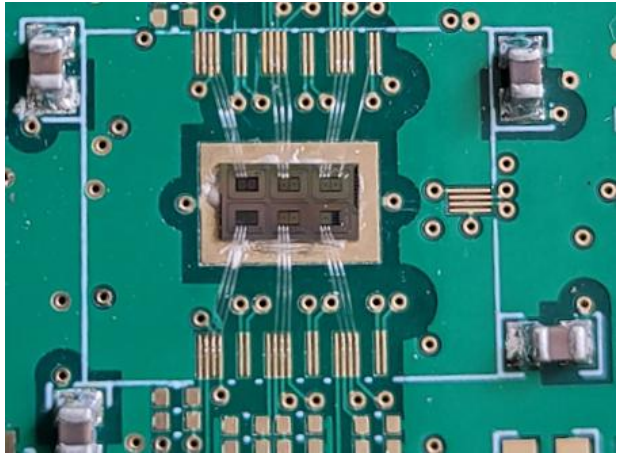
Typical Sentaurus TCAD simulation of a diode with buried PN junction



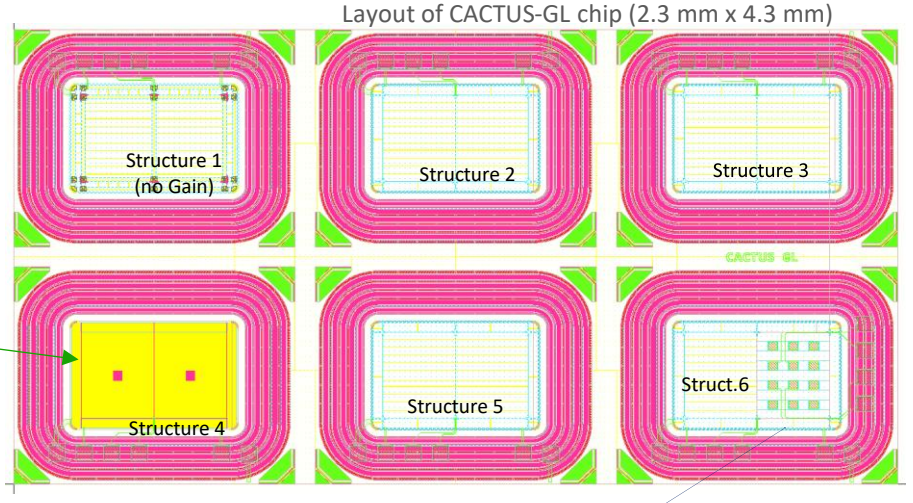
CACTUS-GL Chip layout

- 6 different diode layouts
- Each diode is split in two, and each half can be read out independantly

- One diode (structure 1) has no gain layer, for reference measurements
- Main difference from structure to structure is the guard rings



BV< 50 V
(N+ diode)



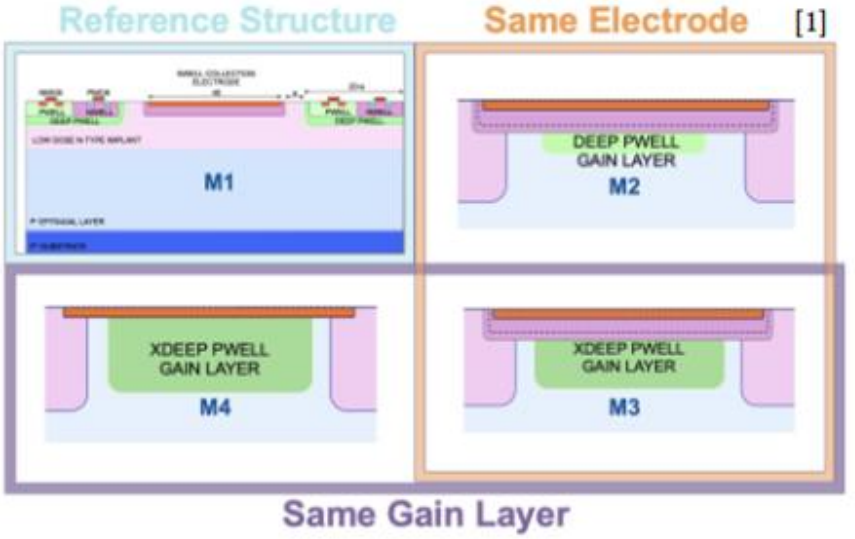
- **Four wafers produced :**
  - **Two HR (two P-doses), thinned to 150 μ, post-processed at IBS (backside boron implant, metallization)**
  - **Two epi (two P-doses), 30 μ, no postprocessing , diced at ALTER UK**

AC-LGAD like structure
Note however that it is possible to have small pixels with ≈100% fill factor

CASSIA project

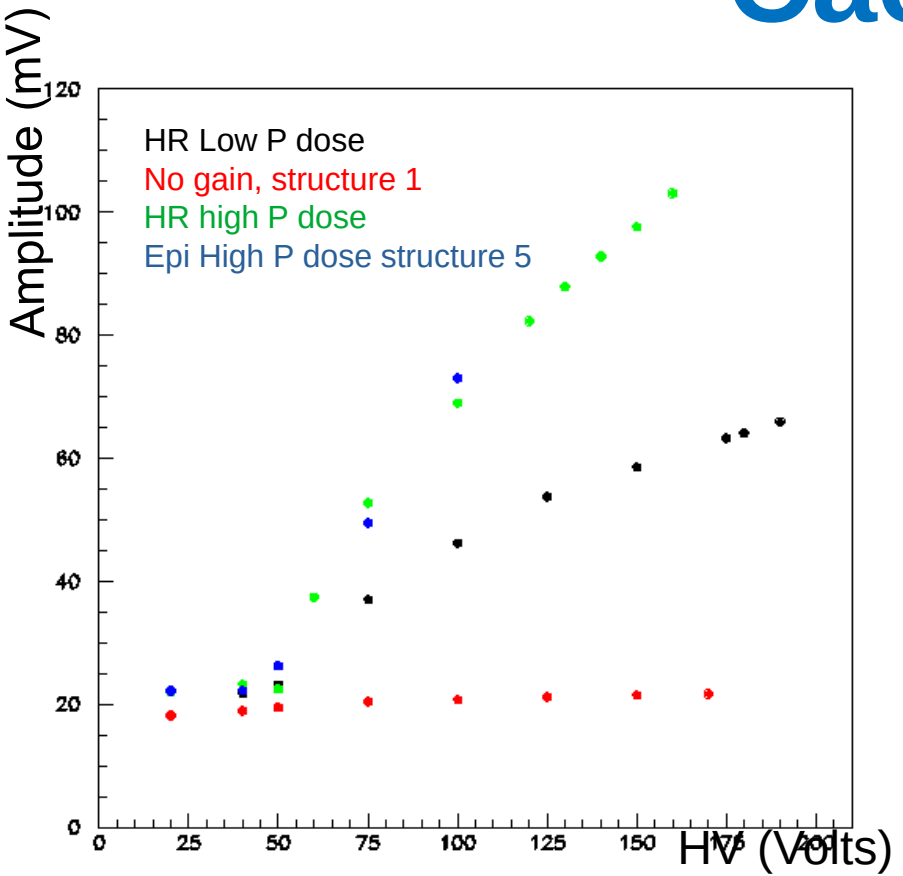
TowerJazz 180 nm CMOS

- The aim of the CASSIA project is to develop a pixelated sensor with a good time resolution and better power dissipation than the current LGAD hybrid solution
- CASSIA1: CMOS pixel with internal gain - fabricated to demonstrate internal amplification feasibility
- CASSIA sensors can be operated both in LGAD mode and in single-photon avalanche diode (SPAD) mode



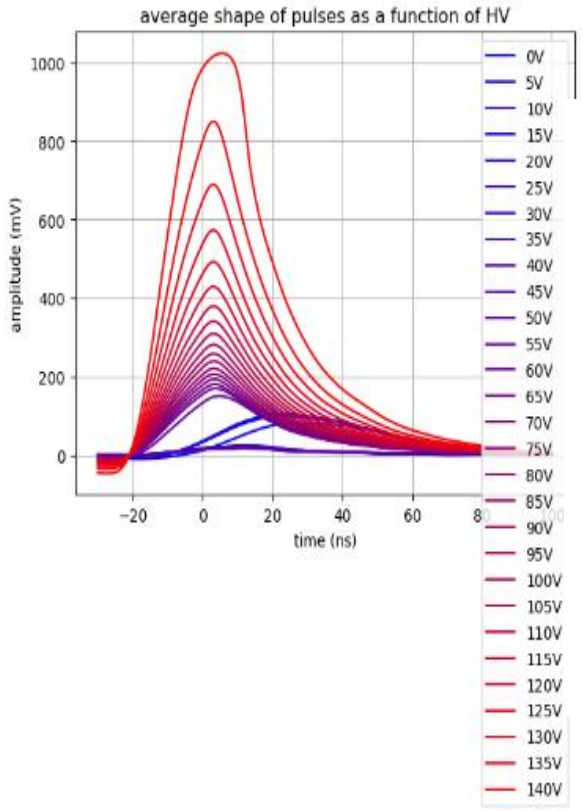
- Different gain layer geometries are investigated (M2-M4), produced alongside a reference structure without gain (M1)

Response to IR LED (940 nm) Cactus-GL

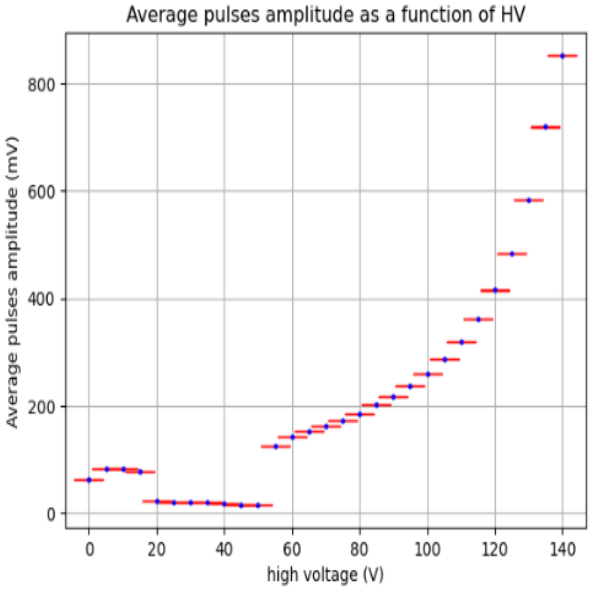


- The clear amplitude vs HV behaviour difference between no gain and gain structure unambiguously proves there is charge multiplication occurring
- Signal amplitude higher for high P dose chips than for low P dose, as anticipated from TCAD
- Charge multiplication starts earlier than predicted by TCAD, around 50 V instead of 100 V
- Epi high P dose gives interestingly high signals, given the low thickness of collecting diode (30 μ only)

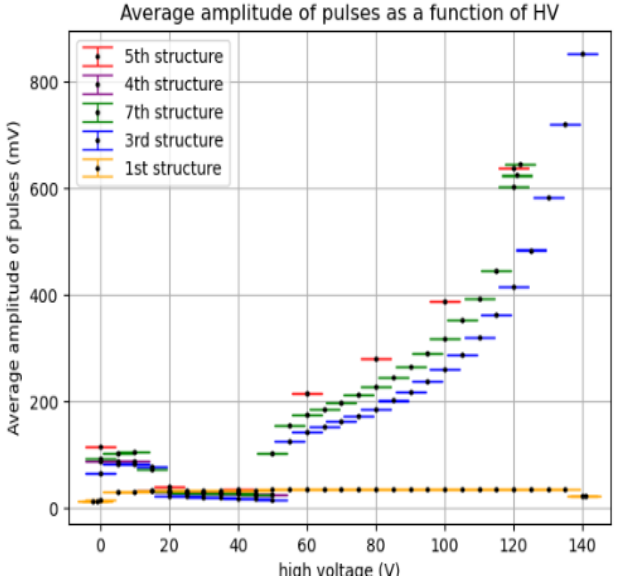
Response to IR pulses (940 nm, approx square, 30 ns long)



Structure 5, HR high P dose (HG) wafer



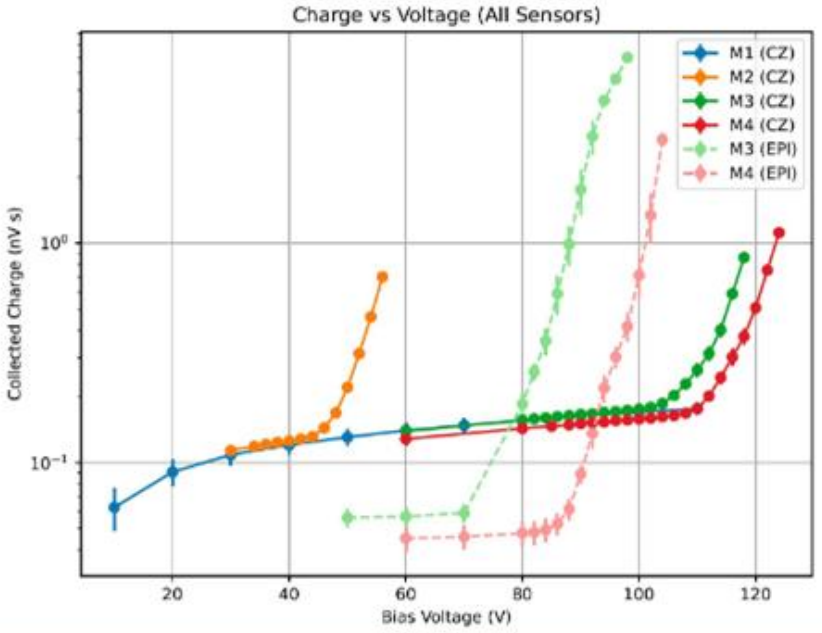
Epi High P dose

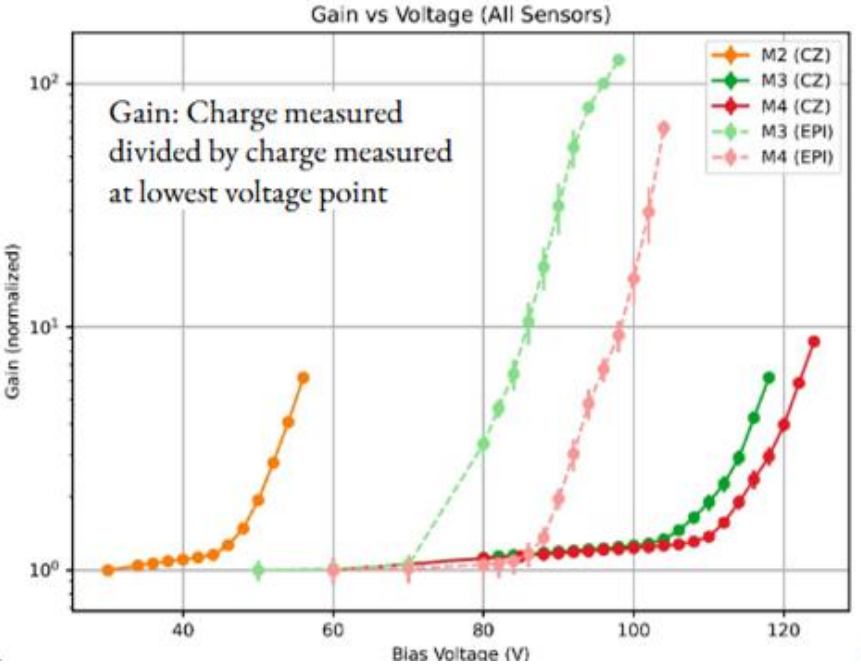


All structures behave similarly

Charge collection and gain measurements (Cassia)

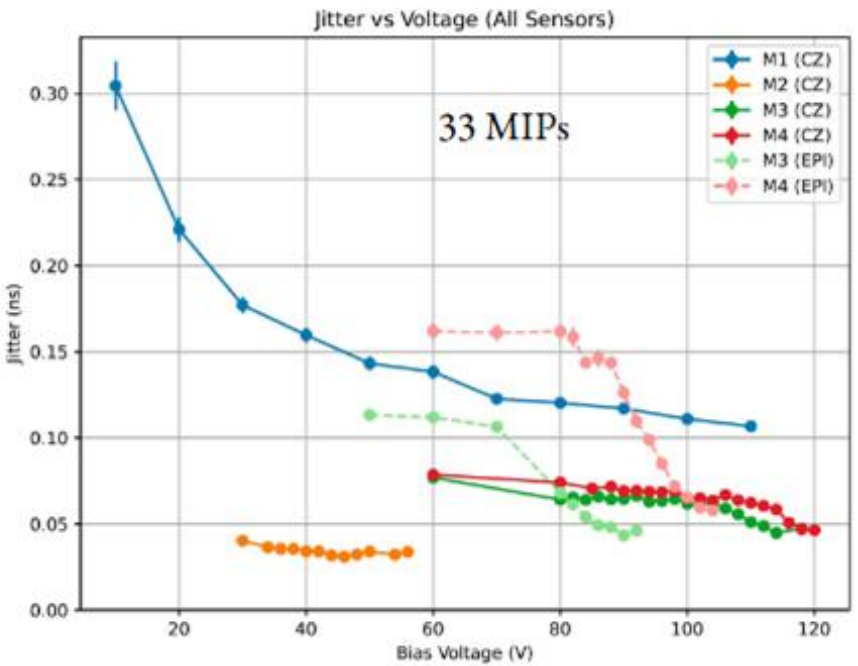
- Measured in only the central channel in the middle of the gain layer (metal opening)
- Measured with a laser intensity approximately equal to 33 MIPs
- Charge measured in CZ M1 (no gain structure) aligns well with the non-gain region of the other CZ matrices
- Lower charge for epi sensors (thinner active thickness), but higher gain reached

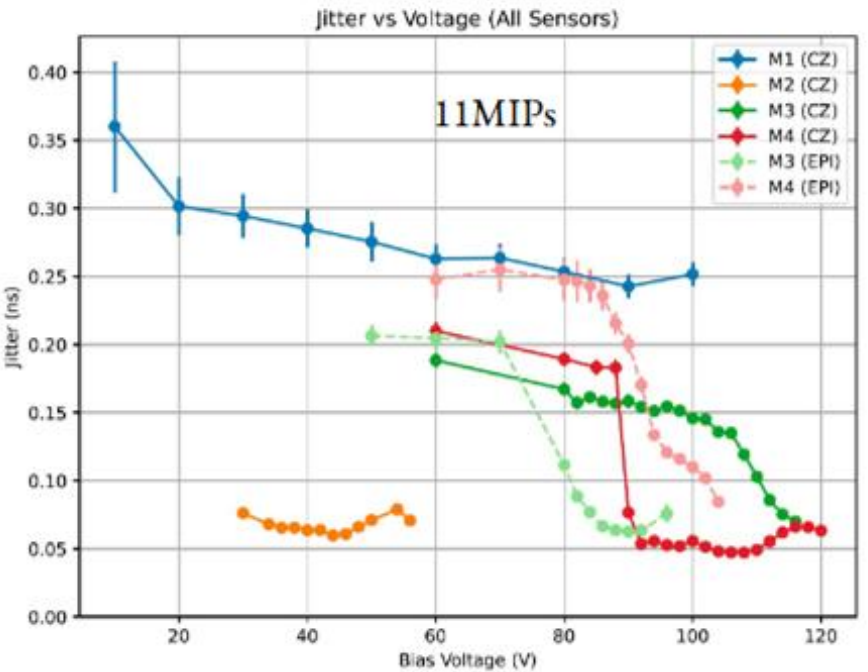




Jitter measurements (Cassia)

- Jitter depends on laser intensity (as expected) but still good results for lower intensity (<11MIPs)
- All matrices with gain reach a jitter <100ps for both laser intensities
- Only valid for gain region - time resolution outside of the gain region is unknown here
  -> to be evaluated in testbeam data

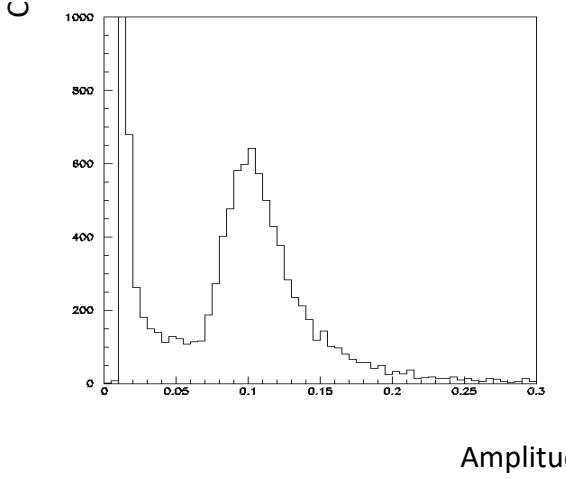


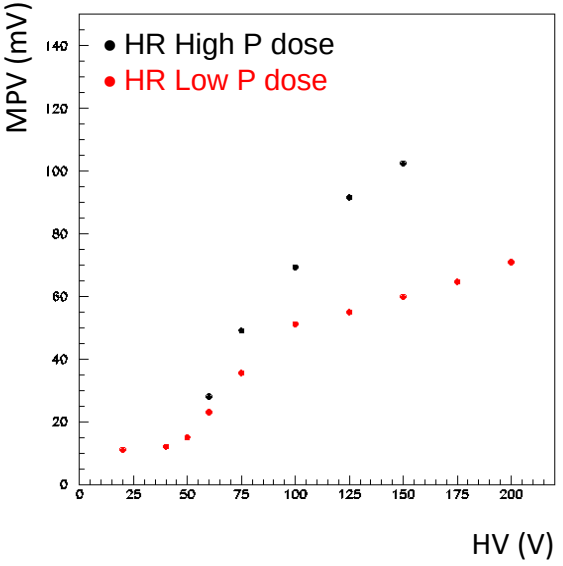


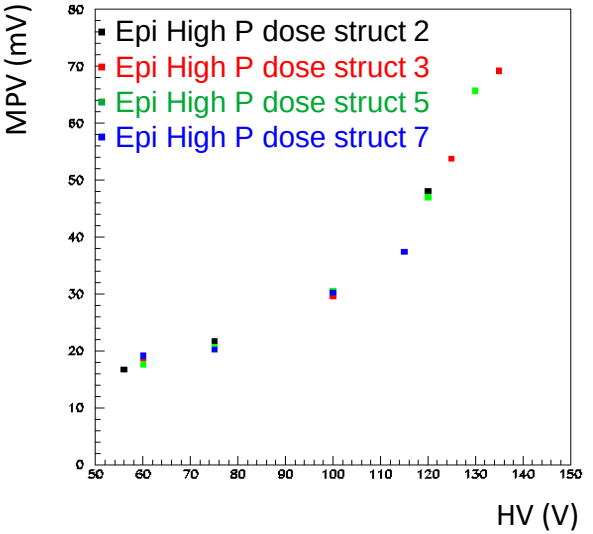
Cactus-GL 90Sr measurements

- ^{90}Sr spectra (*in coincidence with PMT below DUT*) obtained on gain layer diodes from HR high P dose, HR low P dose, and epi high P dose.
- Peak not measurable on the version **w/o gain** (due to S/N of external FE); only the **tail** of Landau visible
- For amplified structures, Landau spectrum visible (and MPV measurable) only above 50 V bias
- Same general trend observed with ^{90}Sr and IR light : high P dose gives higher gain, and lower BV. Trade off to be found
- All structures behave the same, only important parameter is BV

Typical Landau distribution obtained with 90Sr. HR High P dose, 150 V

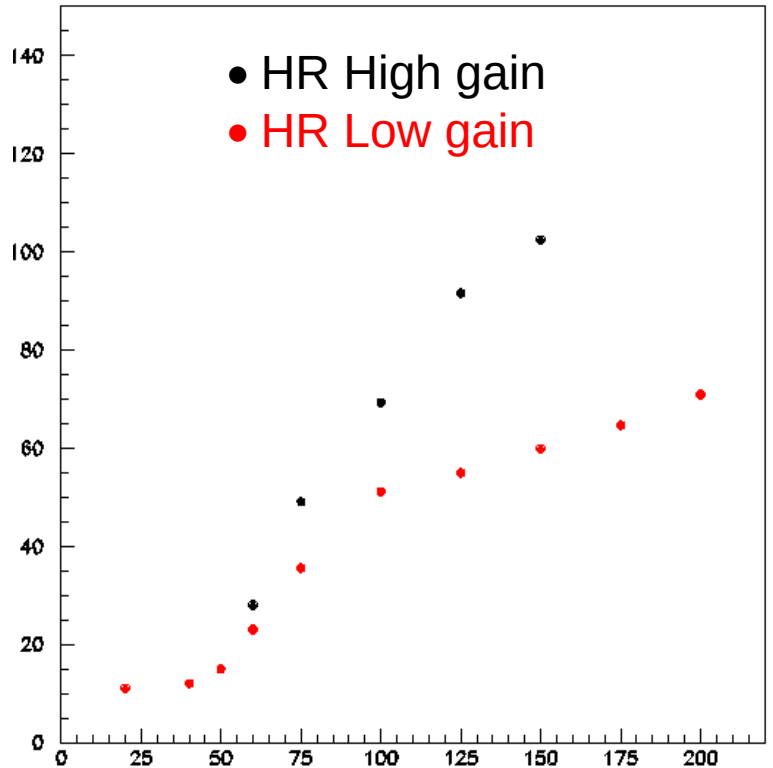






MPV vs HV (90Sr data, PMT in coinc) Cactus-GL

MPV (mV)

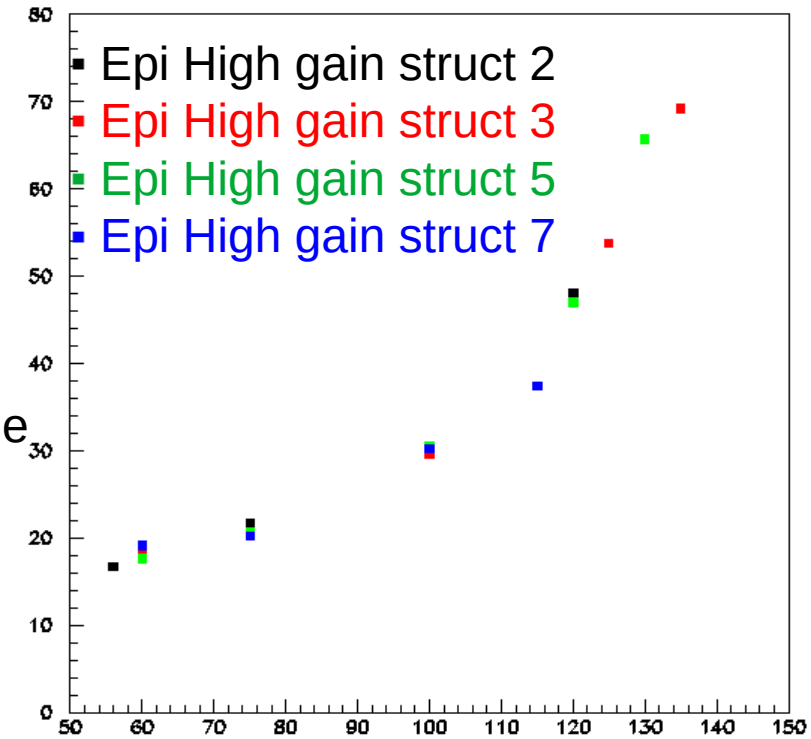


HV (Volts)

MPV can be measured only for amplified structures above ≈ 50 V

All structures have similar behaviour at same HV. Only important parameter is BV

MPV (mV)



HV (Volts)

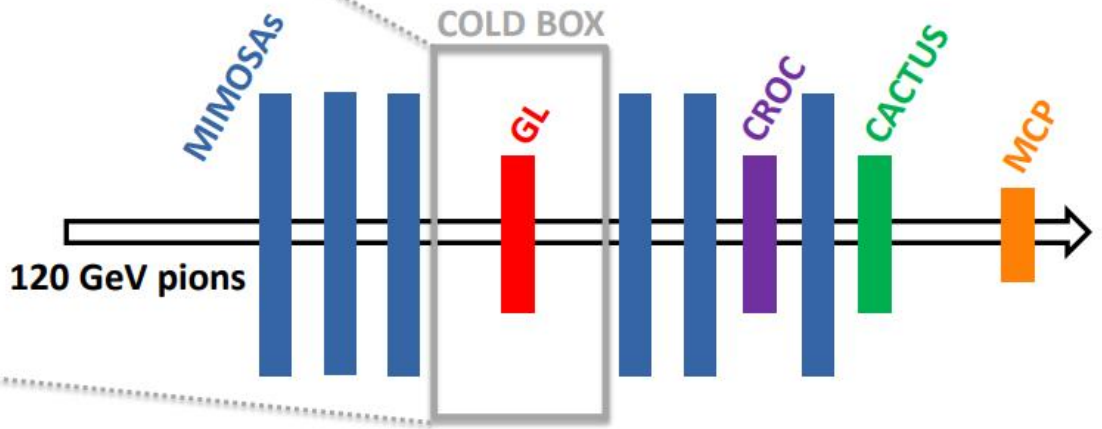
DRD3 Test beam setup May 2026 (Cactus-GL)

- **EUDET** telescope for tracking
- **CMS CROC** as trigger and Region-of-Interest selection (ROI)
- **Mini-CACTUS:** Pre-Amp + Discriminator outputs
- **MCP** as primary timing reference (~10 ps resolution)
- **CACTUS GL** inside the temperature controlled box (~20 ˚C)
  - GL chips mounted on Santa Cruz Boards
    + CIVITEC amplifier (2 Ghz, gain 10)

Readout via Tektronix scope:
12 bit, 50 GS/s, 5 GHz

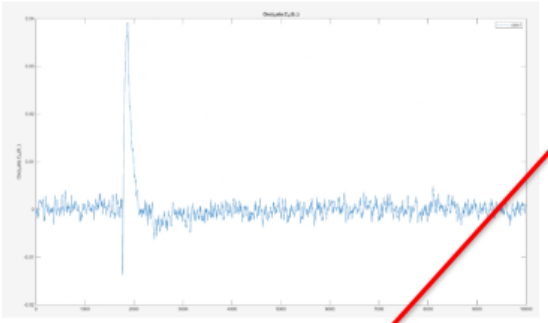


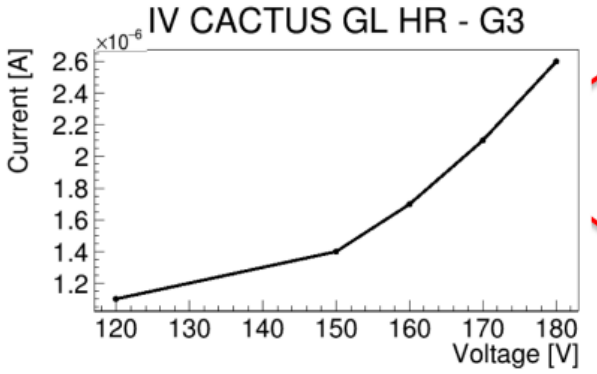
Tested both Epi and High Resistivity (HR) CACTUS Gain Layer (GL) diodes with high p-dose



Cactus GL : timing performance with a HR chip

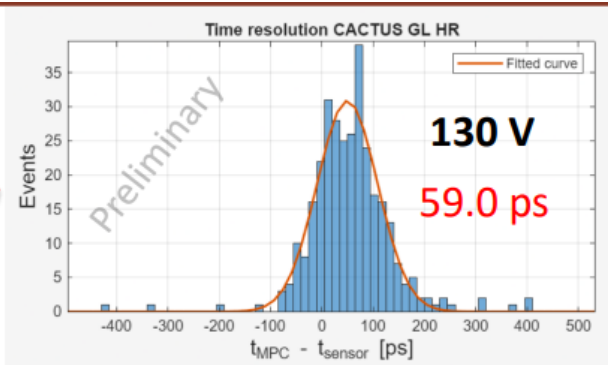
- **HR CACTUS GL analysis**
  - Constant Fraction Discrimination (CFD) at 5%
  - No track selection yet

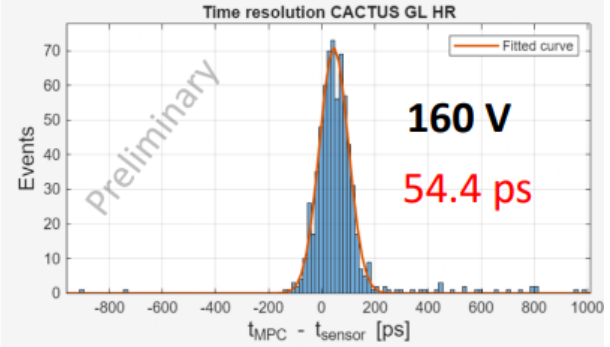


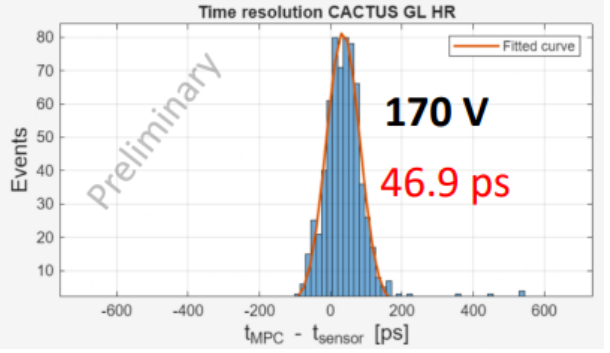


HR CACTUS GL time resolution:

~47 ps @ 170 V

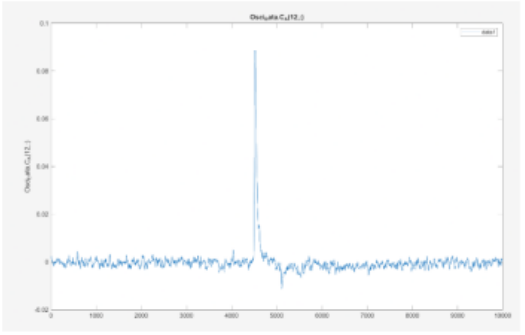


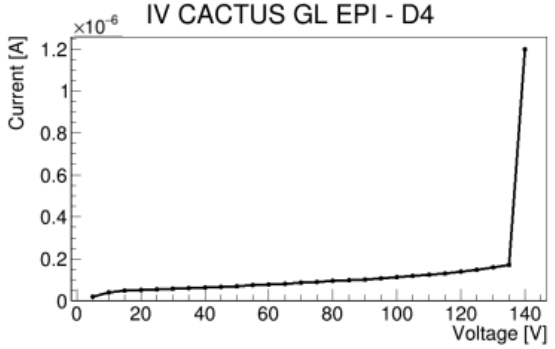


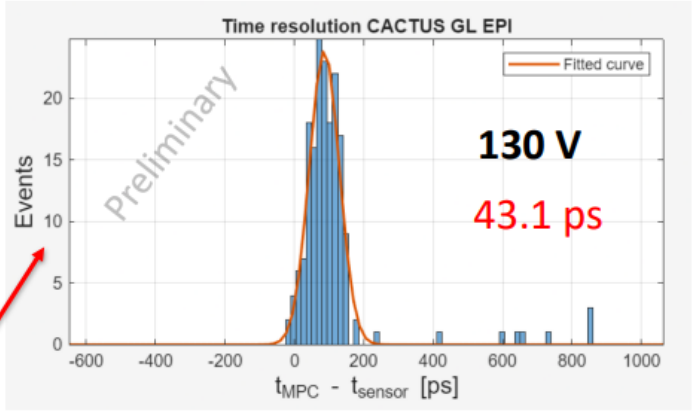


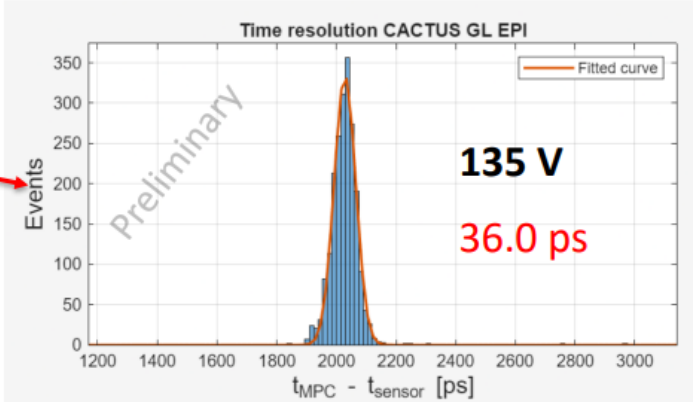
Cactus GL : timing performance with epi chip

- **EPI CACTUS GL analysis**
  - Constant Fraction Discrimination (CFD) at 10%
  - No track selection yet









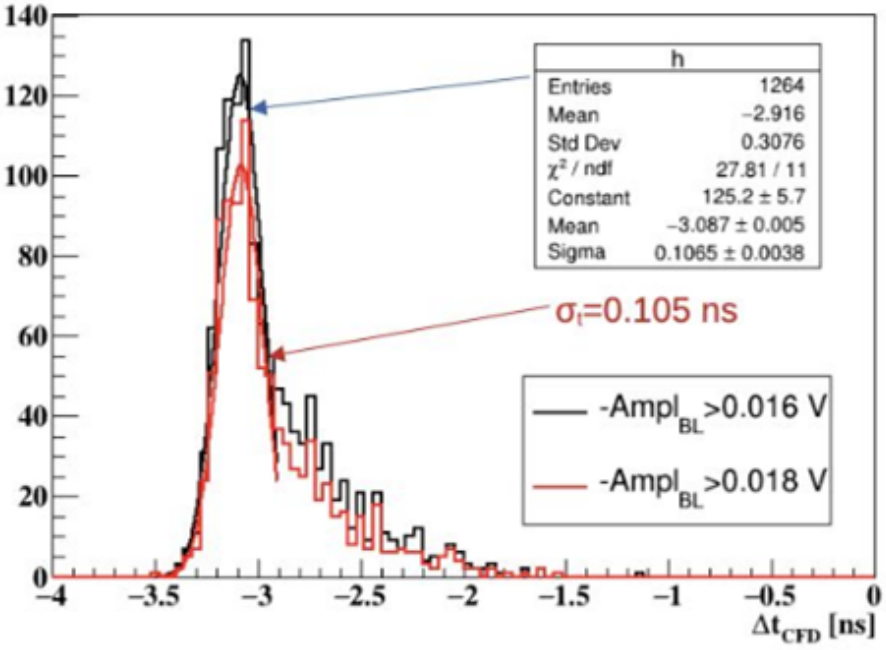
EPI CACTUS GL time resolution:

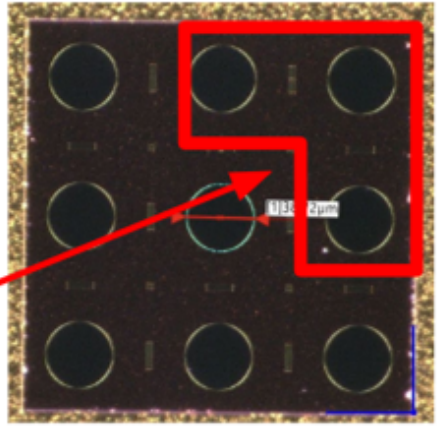
~36 ps @ 135 V

Preliminary results from testbeam - first look

(Cassia)

- No position reconstruction yet - event selection based on amplitude to cut out noise
- Time resolution of 3 pixels bonded to the same readout channel -> might have a negative effect on the timing
- Unclear if contributing signals are from all regions, or only the gain region of the sensor





Sample: CZ M3 at 108V
Readout here: 3 outer pixels in one channel

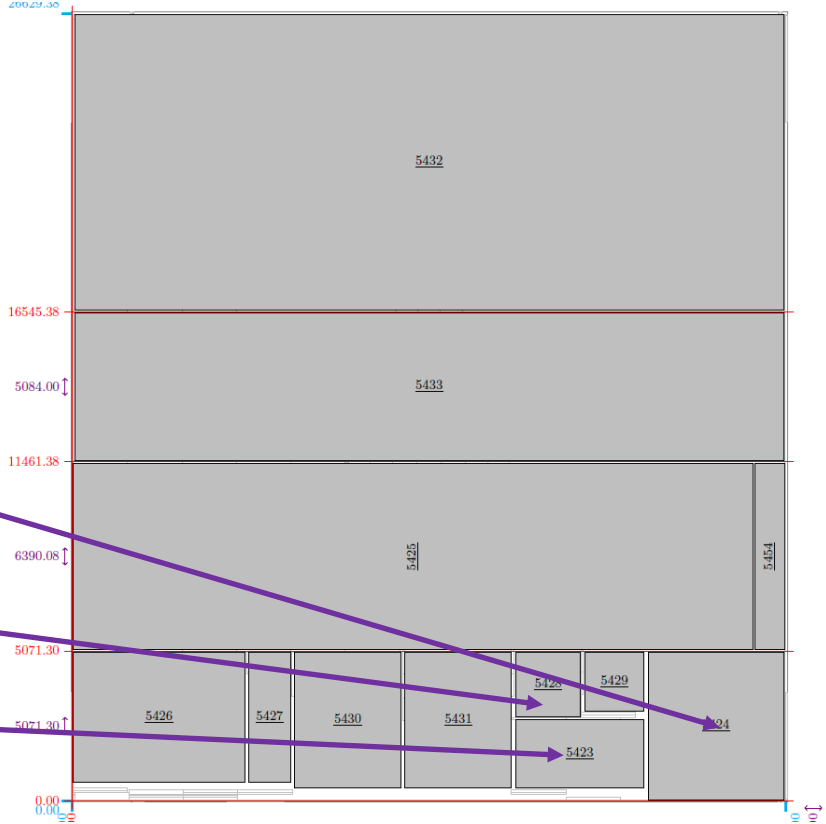
Increasing the amplitude threshold only improves the resolution by few ps

Time resolution around 100ps is a promising result and in agreement with TCT measurements

Further analysis (especially from single pixels) ongoing

Future developments

- Many studies to be done in lab and with testbeam :
  - Uniformity, especially for chips with gain layer
  - charge collection studies, time resolution with 90Sr and testbeam
  - TCAD
- DRD3 common submission (tape-out September 2026 : DESY, ETHZ, IFAE, IHEP, IRFU, KIT, PSI, Liverpool)
  - MiniCactus V2 with gain layer (with integrated FE, suitable for timing)
  - TDC design (as a separate chip, to be integrated later on in MiniCactus) by IFAE
  - Improved test structures (higher BV than 2024 MPW test structures)



Conclusions and perspectives

- Non amplified MiniCactus V2 has a time resolution of about 50 ps, very good uniformity and fill factor.
- Test structures produced with LF15A process clearly show charge multiplication above 50 V. First testbeam results of epi high P dose chips very promising (36 ps)
- Next iteration being produced, chips expected beginning of 2027
    - MiniCactus V2 with gain layer and integrated analog front-end
    - Improved gain layer parameters
    - Next step : TDC integration
- Cassia 1 (TJ180) also clearly shows charge multiplication
- Cassia 2 production with integrated analog readout to come soon