Serial Powering for the Front-End Electronics

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Powering Delivery Problem of Front-End

- **Driver:** more pixels and functions into the front-end detectors (10-100m^2)
- **Pain:** single-chip detector integration rises ➔ power rises to ~W level
- **Constraints:**

vacuum ➔ heat management ➔ cooling material budget,

cable I^2R loss ➔

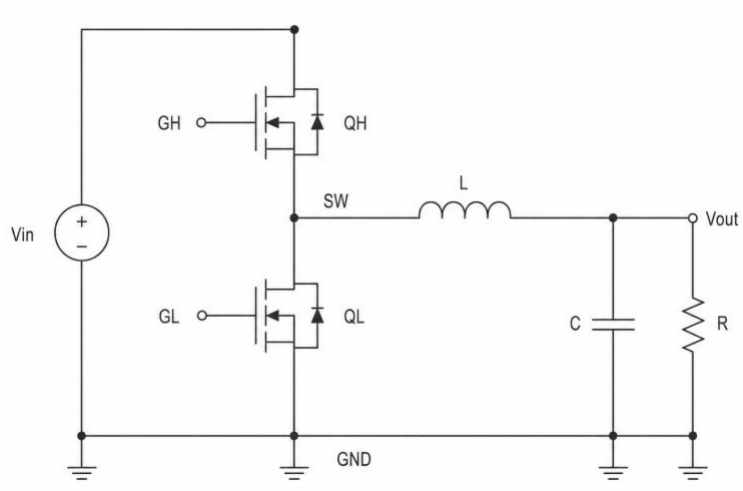
strong magnetic field ➔ topology limited

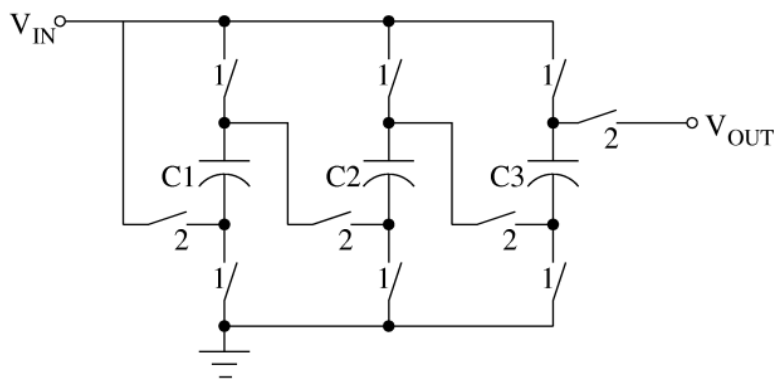
low noise ➔

Goal: modules need 2V 24A -> cable supply 48V 1A

(high-voltage low-current transfer to reduce cable I^2R loss)

• Traditional Topologies : Buck DC-DC vs Switched-Capacitor





Buck DC-DC (inductor)

+ High efficiency, large current, ~95% at small step-down

– Parasitic at SW point grow with convention ratio; (24V/2V = 12)

– Magnetic core is limited in strong magnetic field

Switched-capacitor (capacitors)

+ High integration, smaller size

+ No inductor, unsensitive to magnetism.

– Fixed ratio (or highly limited);

– lower efficiency than Buck at high ratio;

– needs many caps & high switching frequency

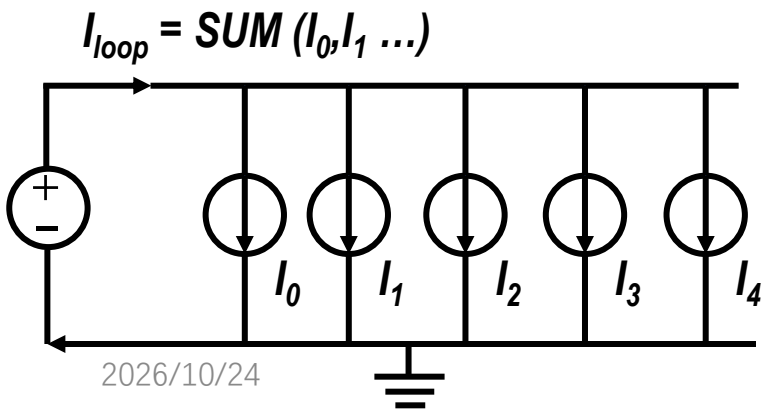
Topology switch: Parallel Powering to Serial Powering

- Parallel (Const Voltage) :
  - fixed voltage rail, currents sum-up

+ Easy topology extension (existing circuits are designed on a fixed rail)

+ Reduce branch current to save energy

– Cable problem $P=I^2R$



- Serial (Const Current) :
  - fixed current path, voltages add

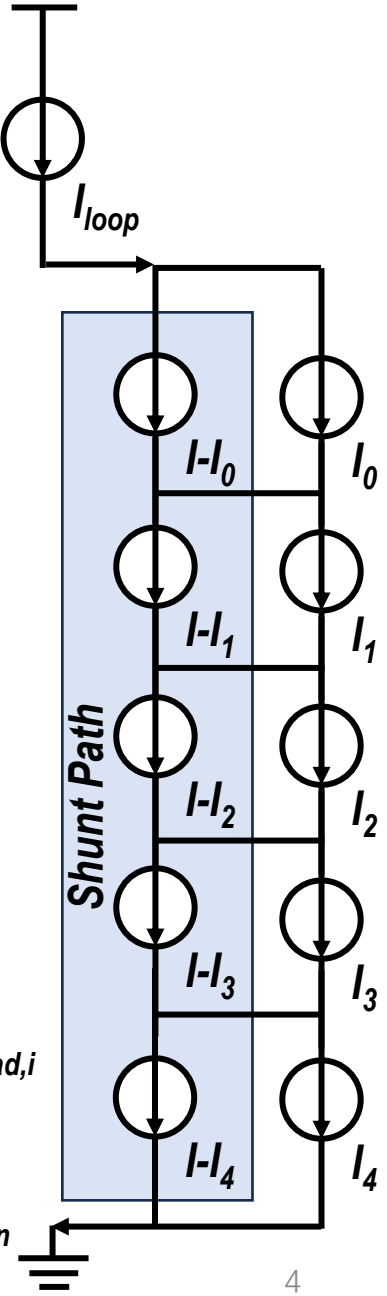
+ Solves the cable problem

+ Need less energy storage components.

– Shunt branch losses

– uncontrolled open circuit

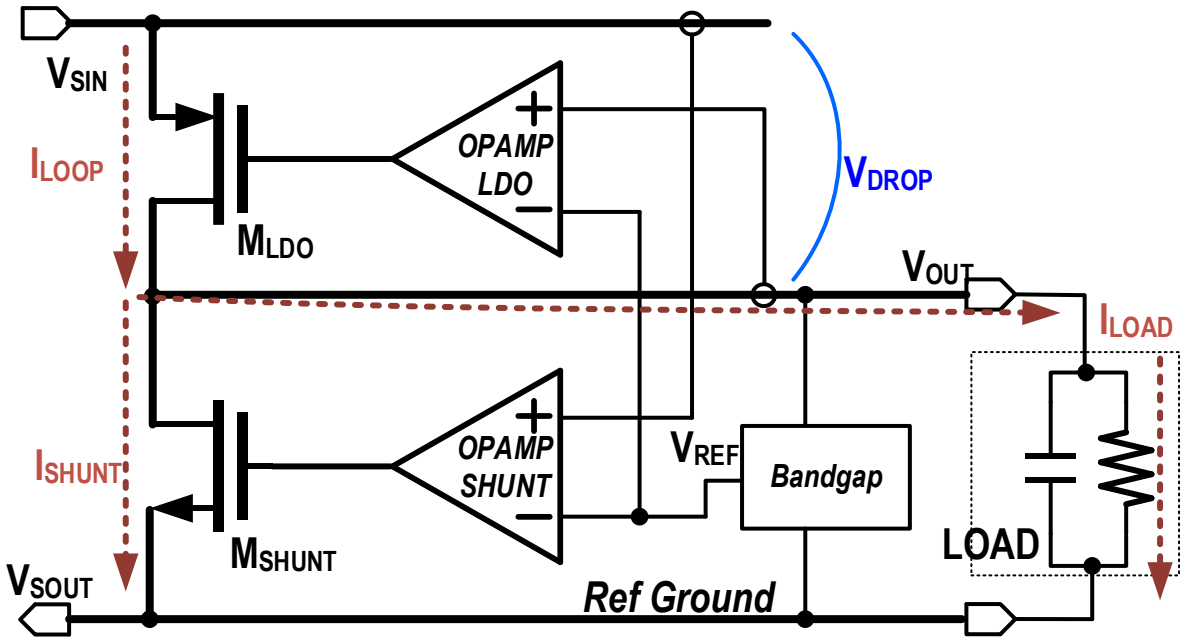
– no common reference ground, noise may rise

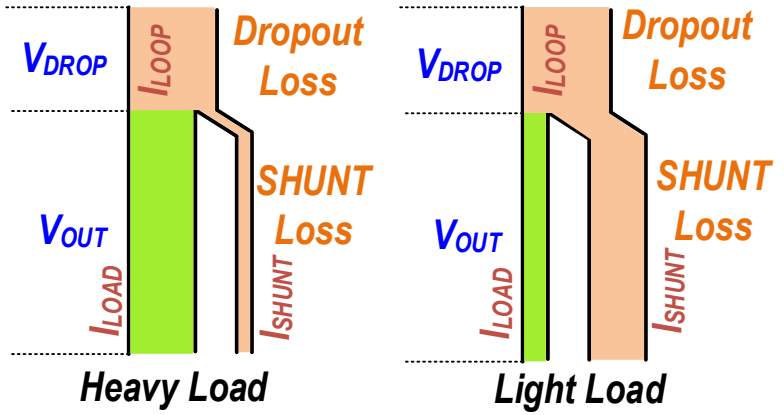


$I_{shunt,i} = I_{loop} - I_{load,i}$

$I_{loop} = max(I_{load,i}) + I_{margin}$

Current Approach: Shunt LDO





$$I_{loop} = I_{load} + I_{shunt}$$

$$P_{shunt} = V_{out} \times I_{shunt}$$

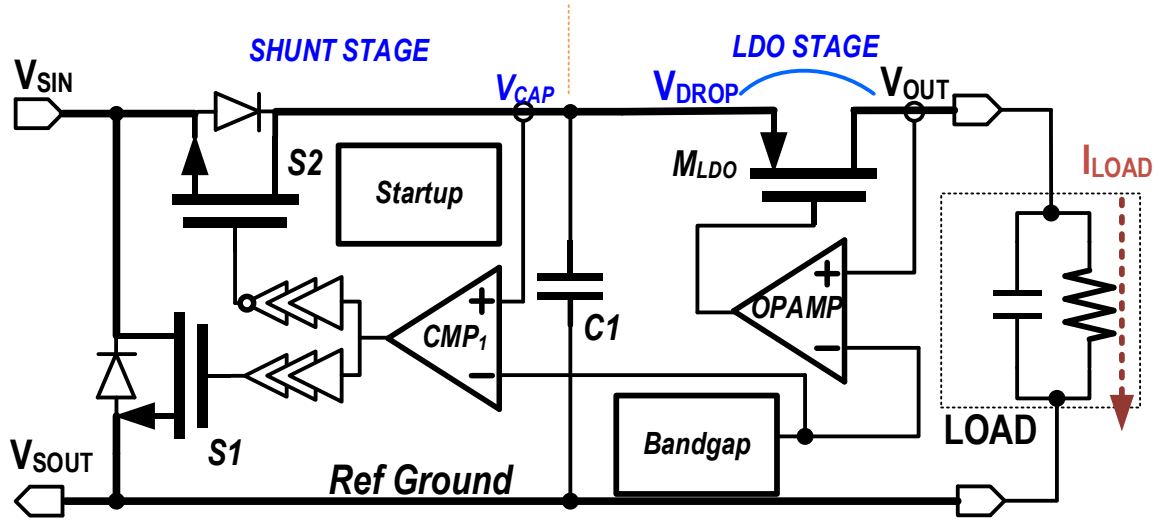
$$P_{drop} = V_{drop} \times I_{load}$$

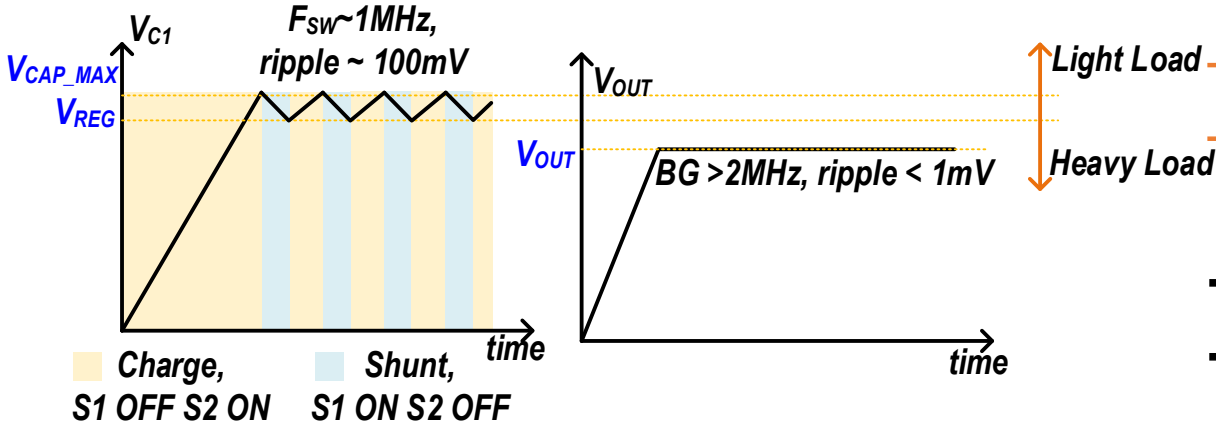
Keep large V_{drop} to cover the fabrication mismatch and load transitions

Keep I_{shunt} to maintain stability

Efficiency: light-load loss from I_{shunt}; heavy-load risk from $V_{dropout}$ shrinking

Proposed Approach 1 : (Inductor Free) Delta-Modulated Switched-Capacitor + LDO





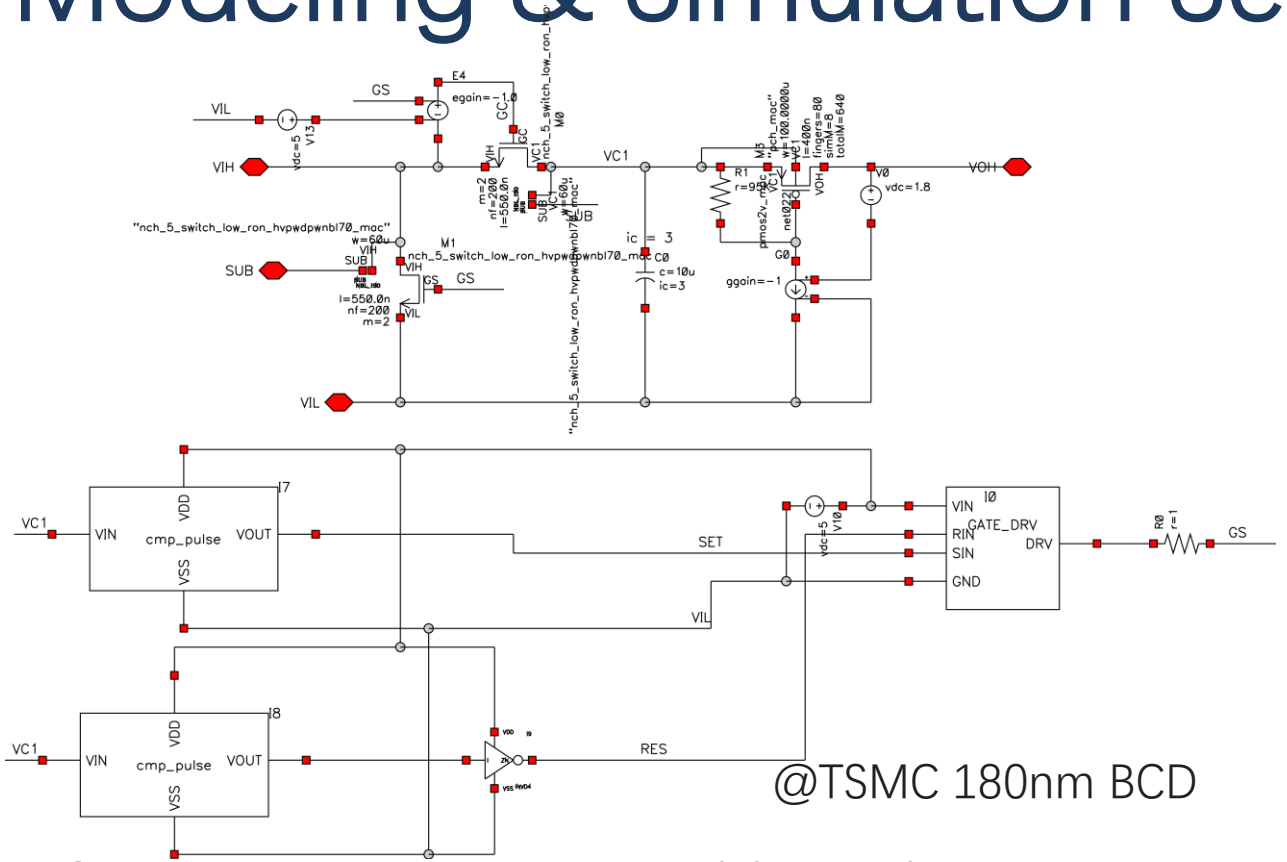
+ No inductor, serial powering;
+ Constant-current charging lowers hard-charge loss
+ Efficiency ≥ 80% (≈ 2-stage high-ratio Buck);
+ Load-adaptive dropout
+ Low ripple ~500uV;

– Transient response limited by LDO dropout;
– needs to trade off with efficiency
– Poor short-burst (Burst) response;

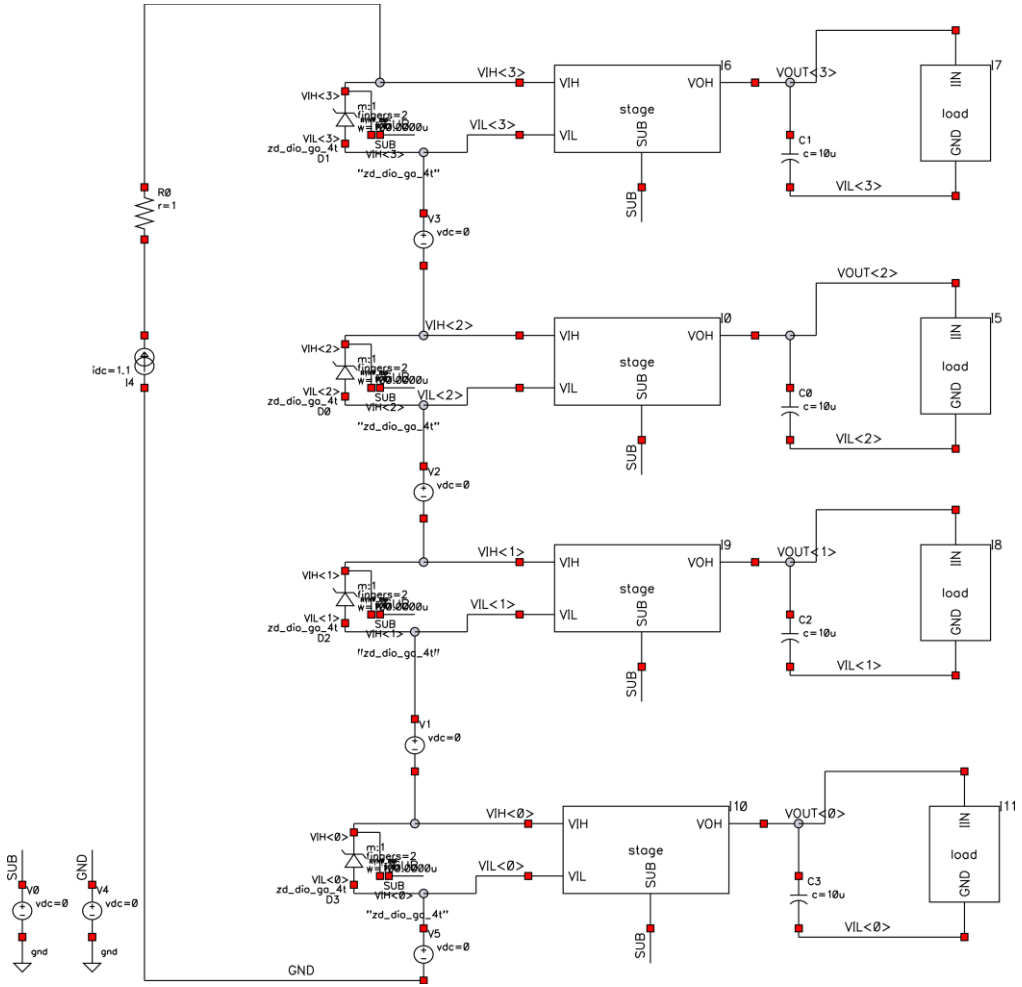
➔ needs redundancy current (15~20%)
➔ needs more capacitors(~50uF/1A)

Mid nodes allow larger ripple (~100mv @1MHz Fsw), suppressed by LDO to <1mV
(depends on PSRR / load spectrum / caps)

Modeling & Simulation Setup



@TSMC 180nm BCD

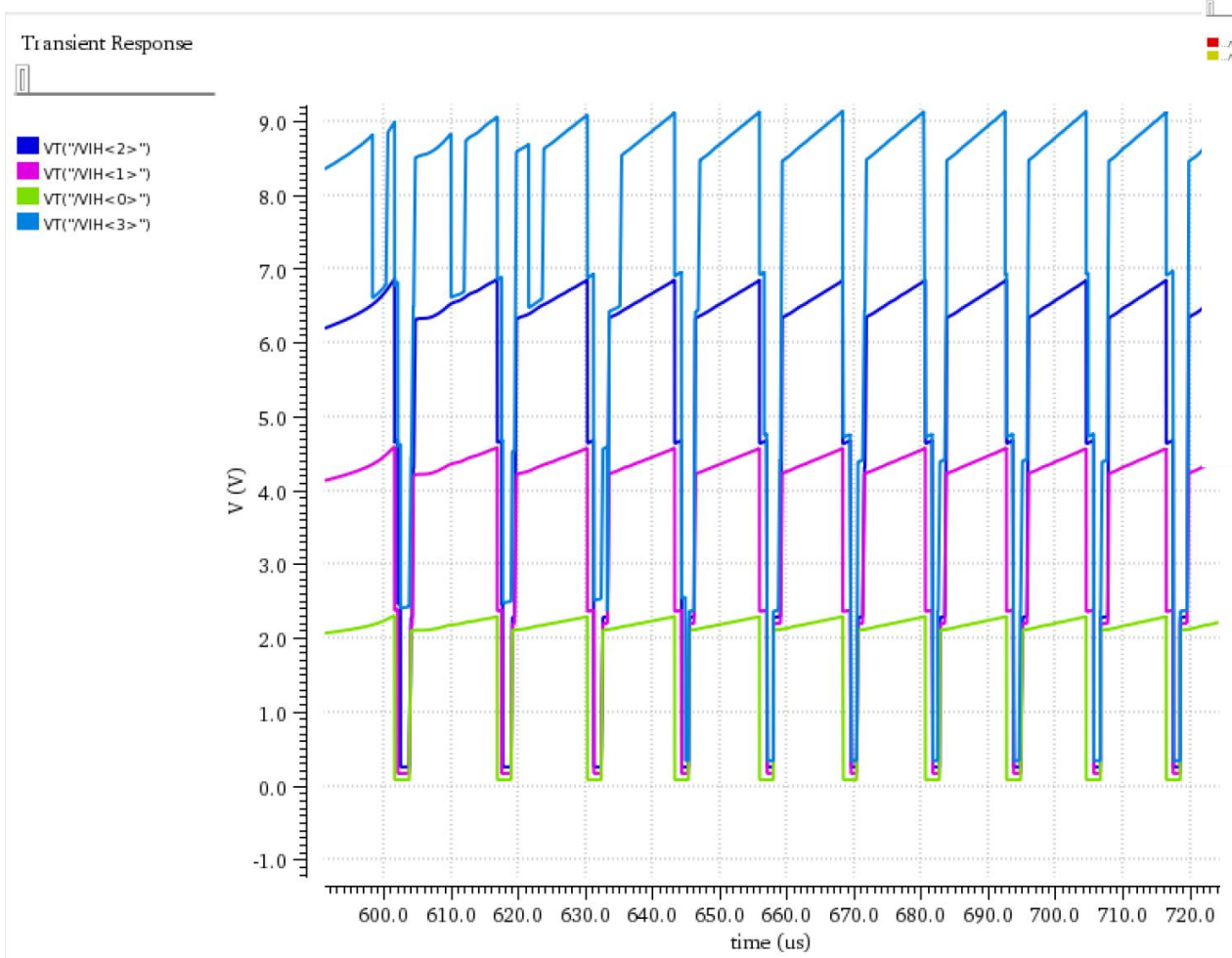


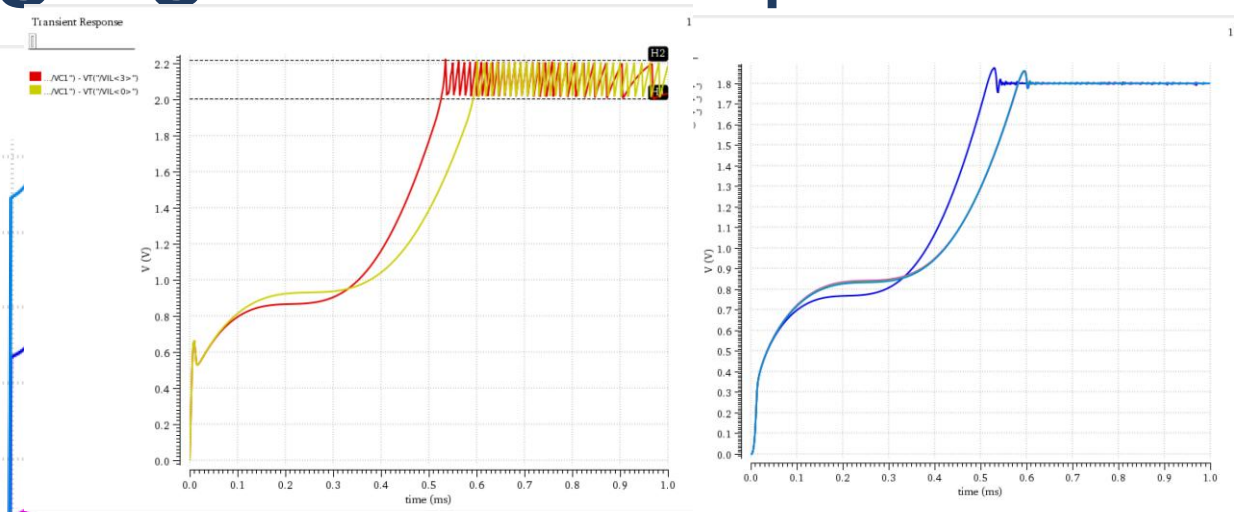
Topology: 1.1A constant-current serial powering, 4-stage

Each stage: 1.8V output, 1A load

LDO: loop gain 60dB, OPA 20uA, bandwidth 2MHz

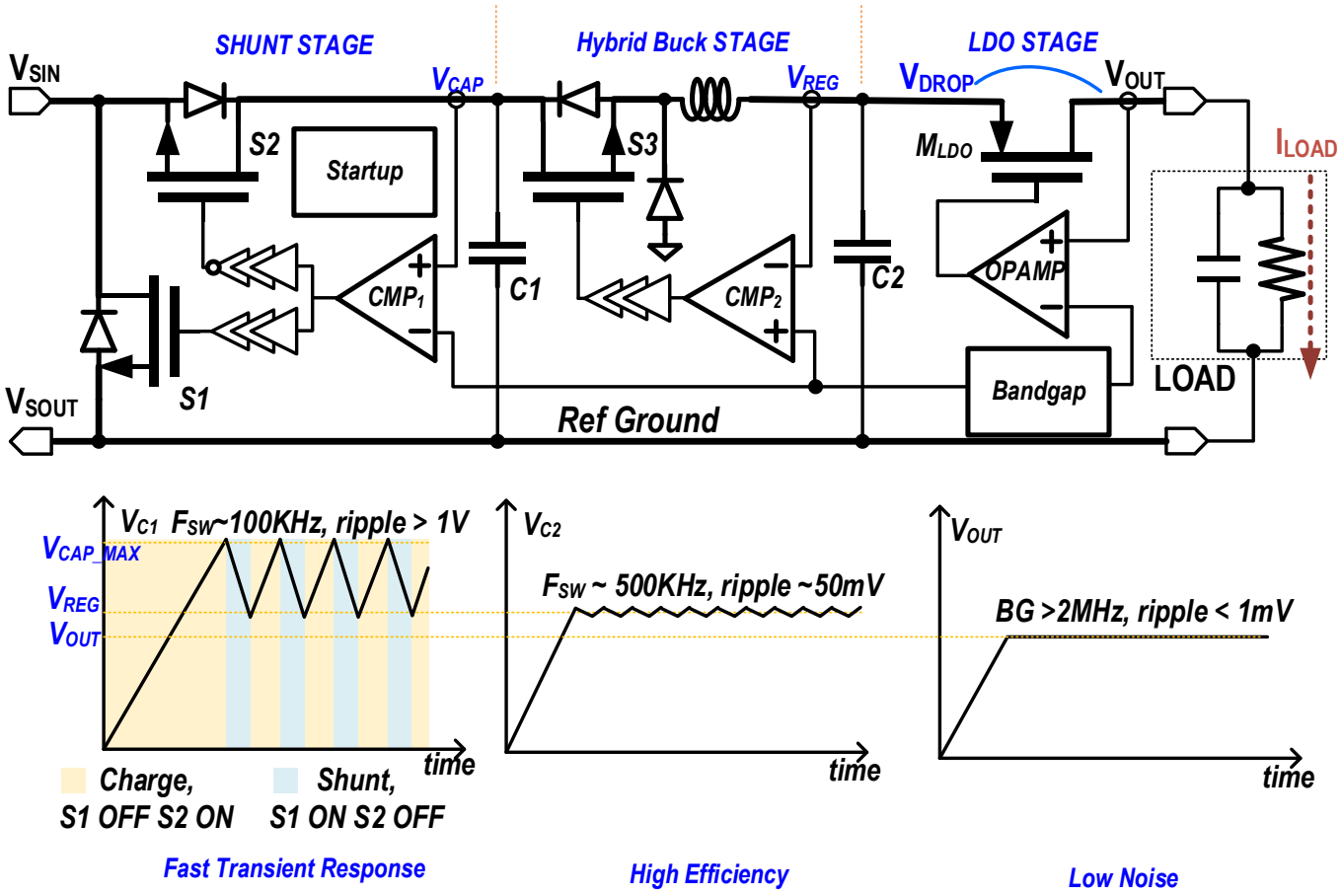
Simulation Results:
Rails / Capacitor Charging / LDO Output





- The four stage rails build up sequentially, each settling near 1.8 V.
- Capacitors charge under constant current (no hard-charge spike);
- the LDO settles the output to <1 mV ripple.

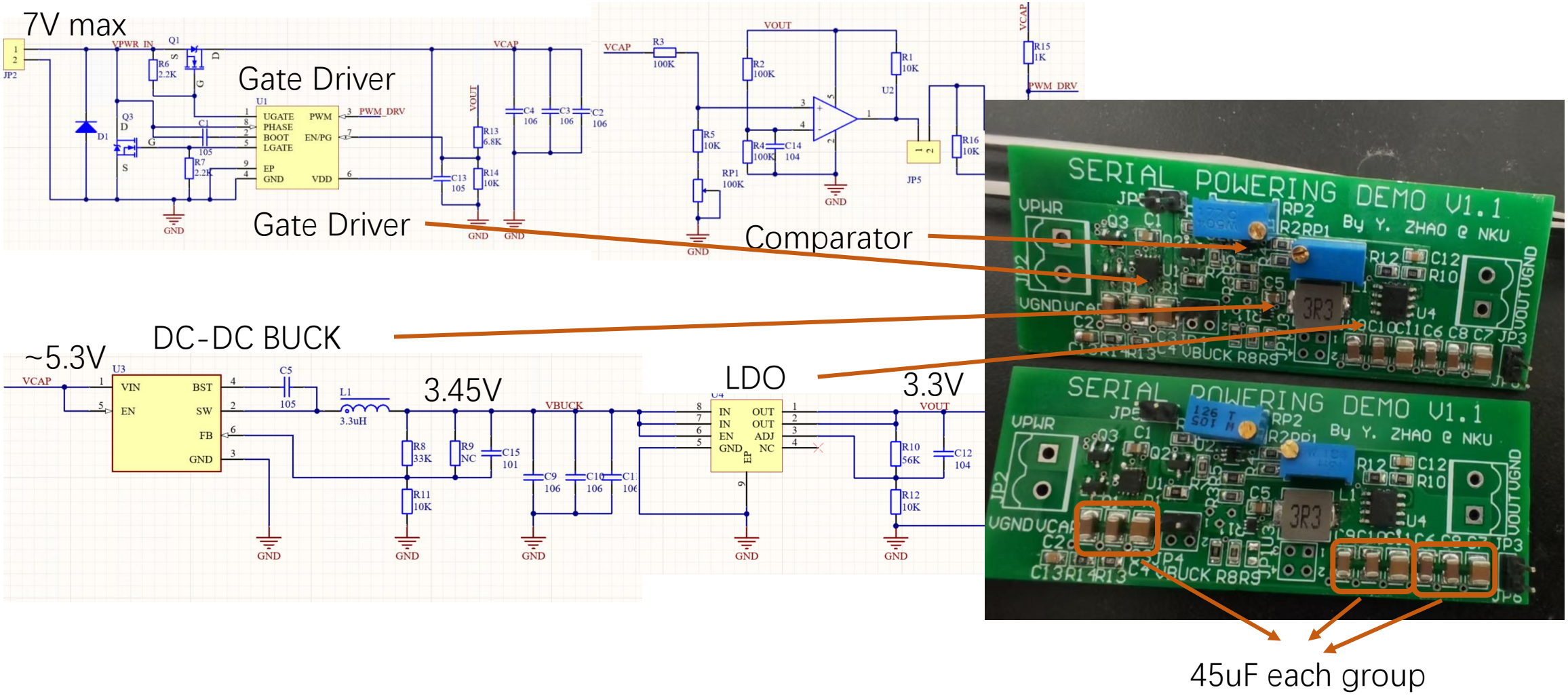
Proposed Approach 2 : (Air-core Inductor) Constant-Current SC + Hybrid Buck + Ultra-Low-Dropout Regulator



+ Serial powering
+ A small air-core inductor (~0.5uH) to buffer hard charging
+ Efficiency ≥ 90%; ripple ~100uV ;
+ Load-adaptive voltage headroom
+ Good short-burst (Burst) response, no efficiency trade-off needed
+ Only average current required, less current margin (~5%)

– Complex structure, relatively large active area (~1.5mm²);
– Air-core inductor is large even 0.5uH

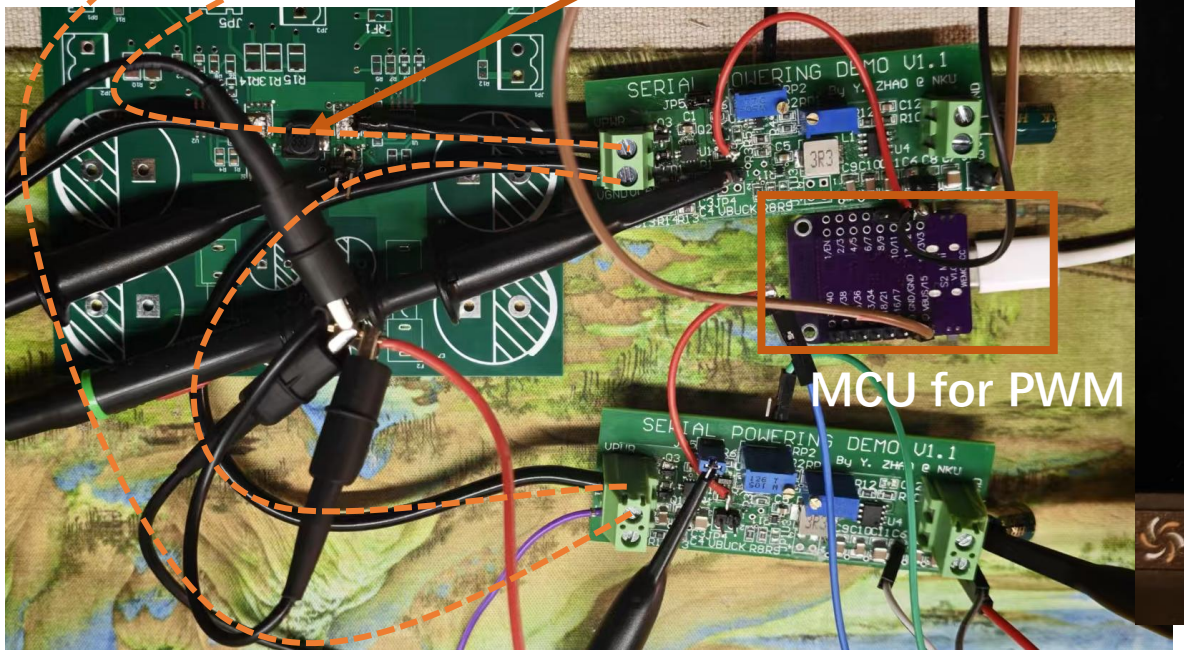
PCB Demo Design V1.1: DC-DC Cascade

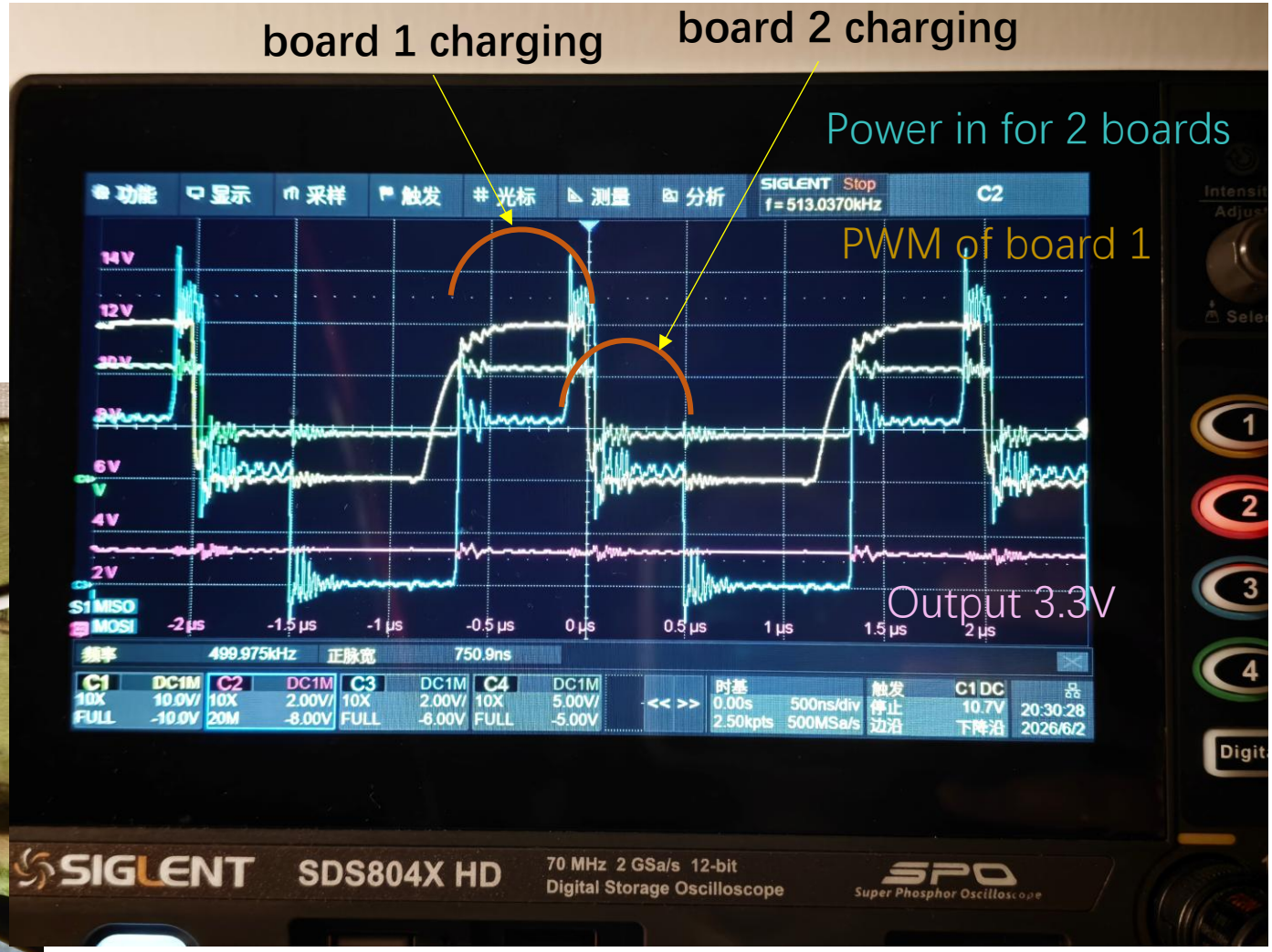


Test For 2 Stage V1.1 @ 0.1A

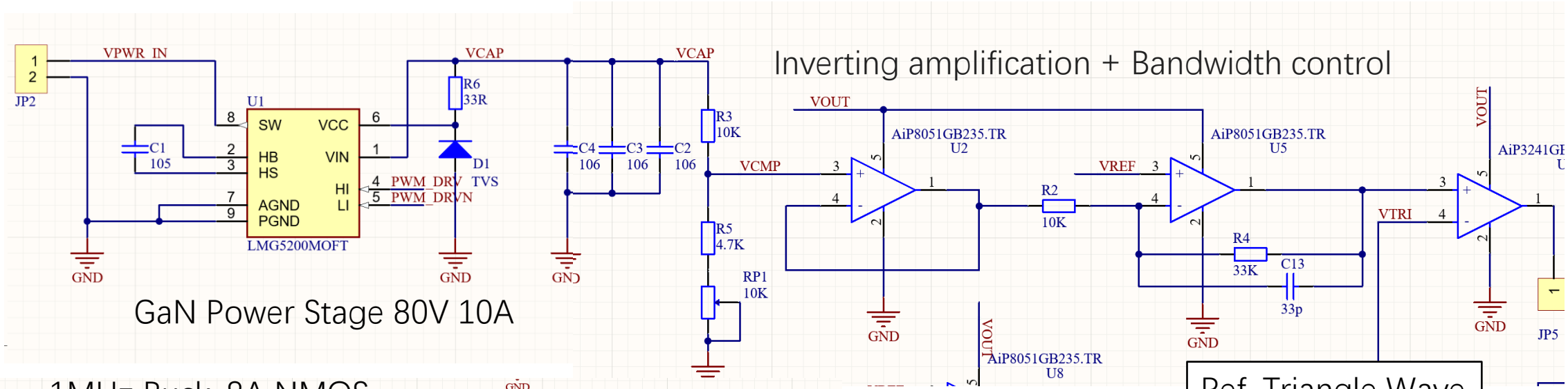


L=33uH



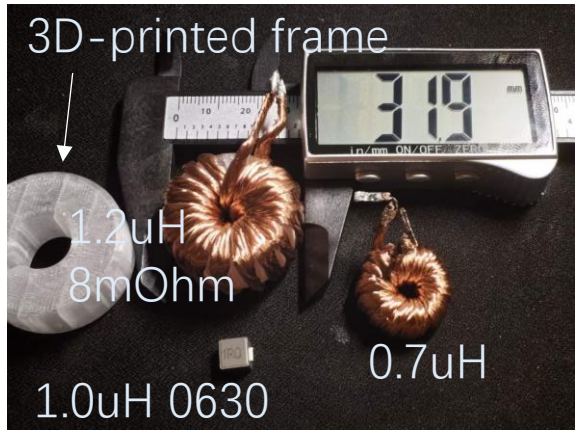


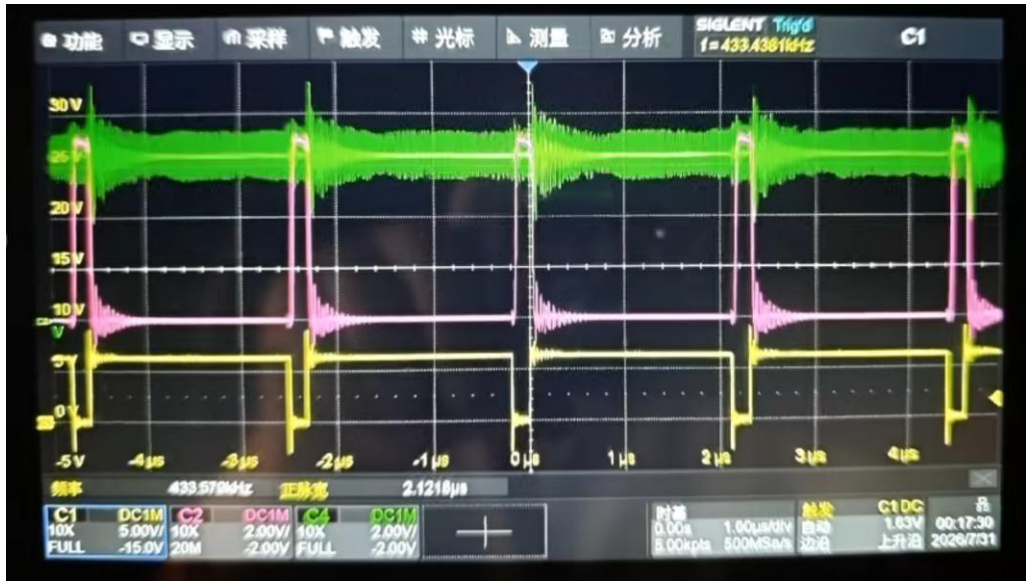
PCB Demo Design V1.4:
GaN Power Stage / Buck + LDO

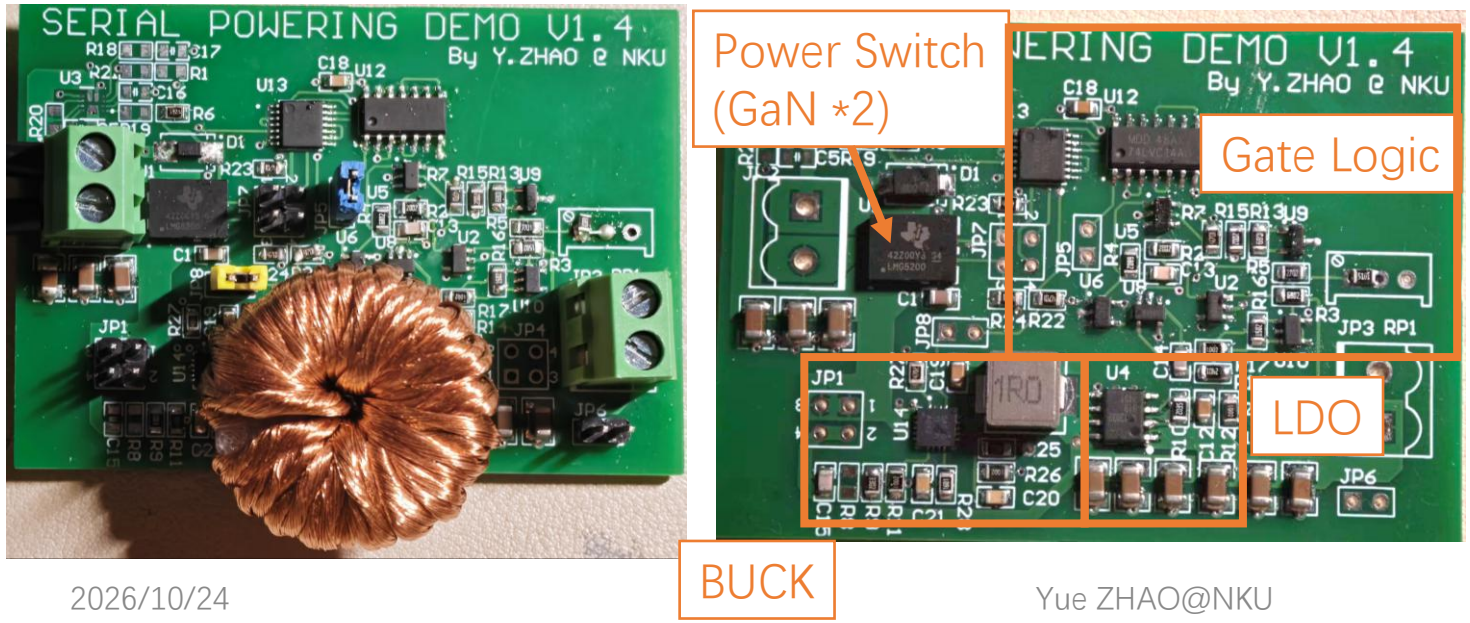


Test For V1.4 @ 1A



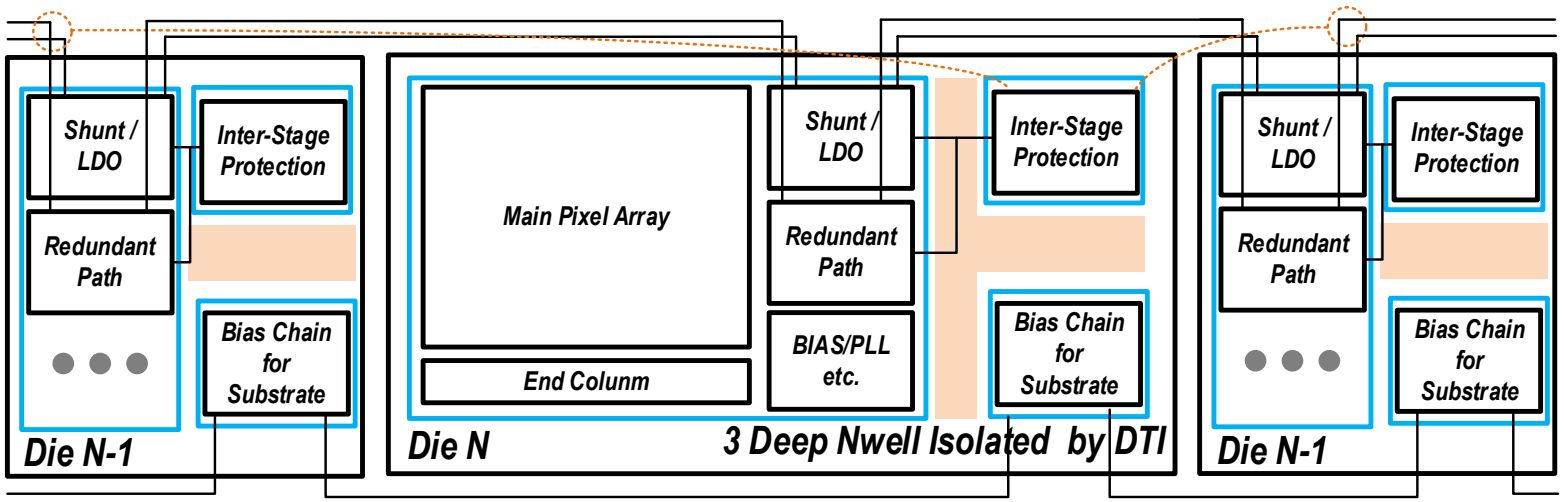


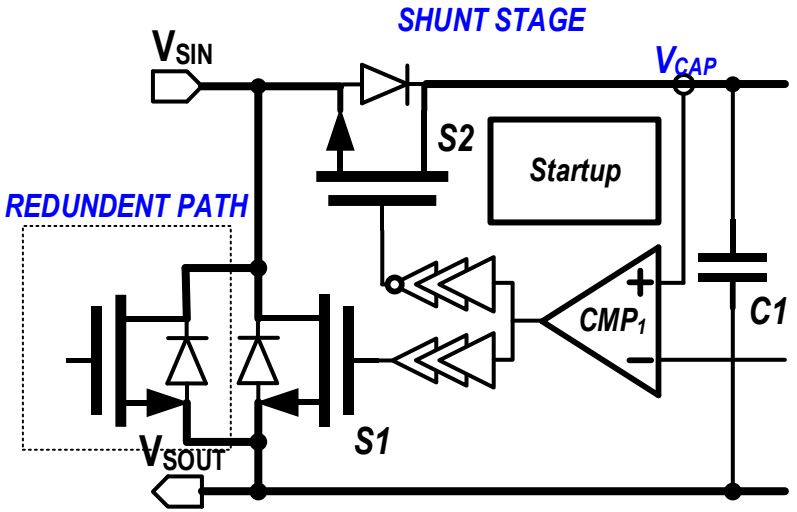




Problem:
Limited by the regulation bandwidth of current source.
➔ **Build a customized current source based on BUCK topology. (Simulation OK, under design)**

Solution for Open-Circuit Problem : Monitoring & Redundancy





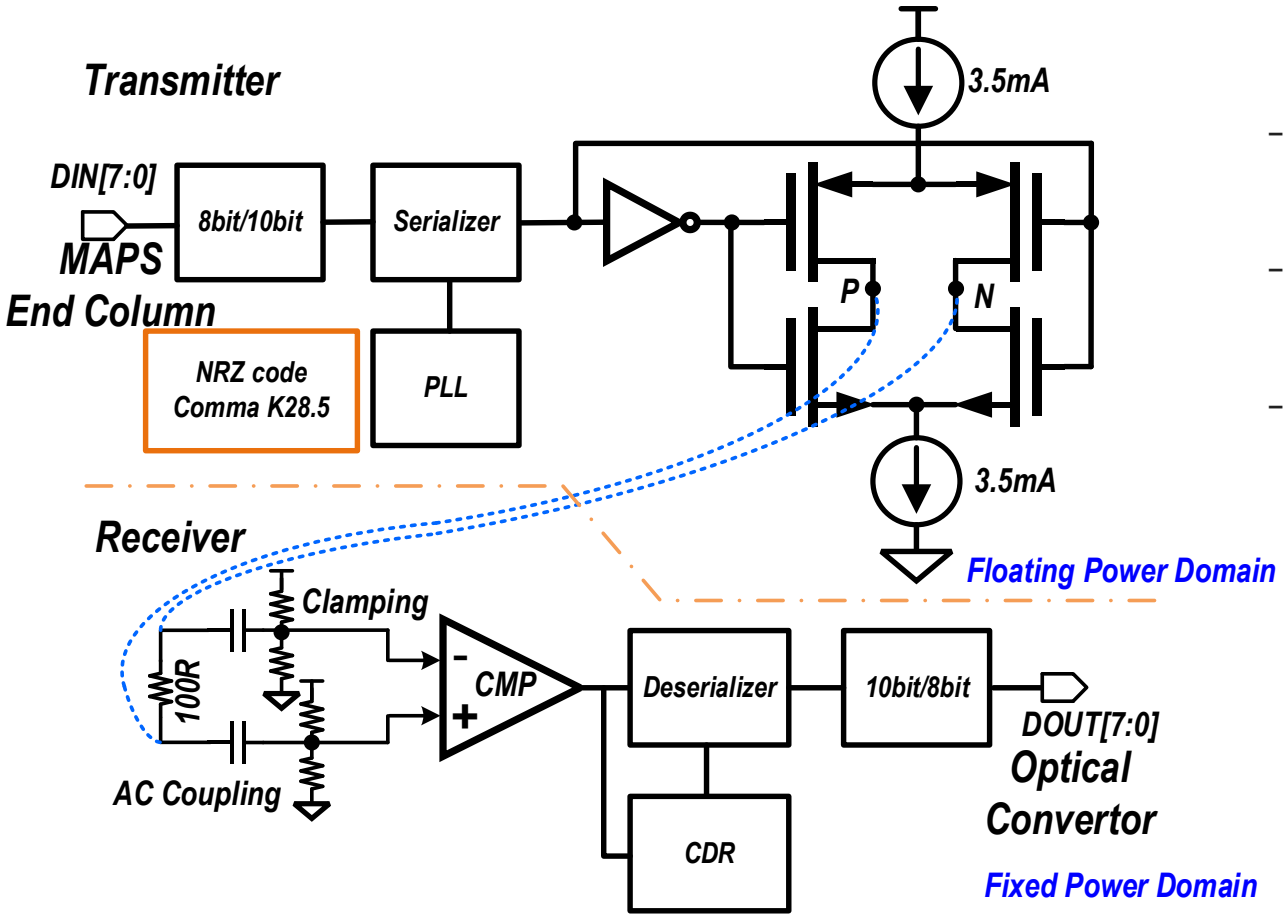
DTI isolation of three independent voltage domains: pixel/power, bias generation, inter-stage detection

Inter-stage detect powered independently by upper & lower stages

Short mechanism: before a stage trips on over-voltage, short it locally via a redundant path

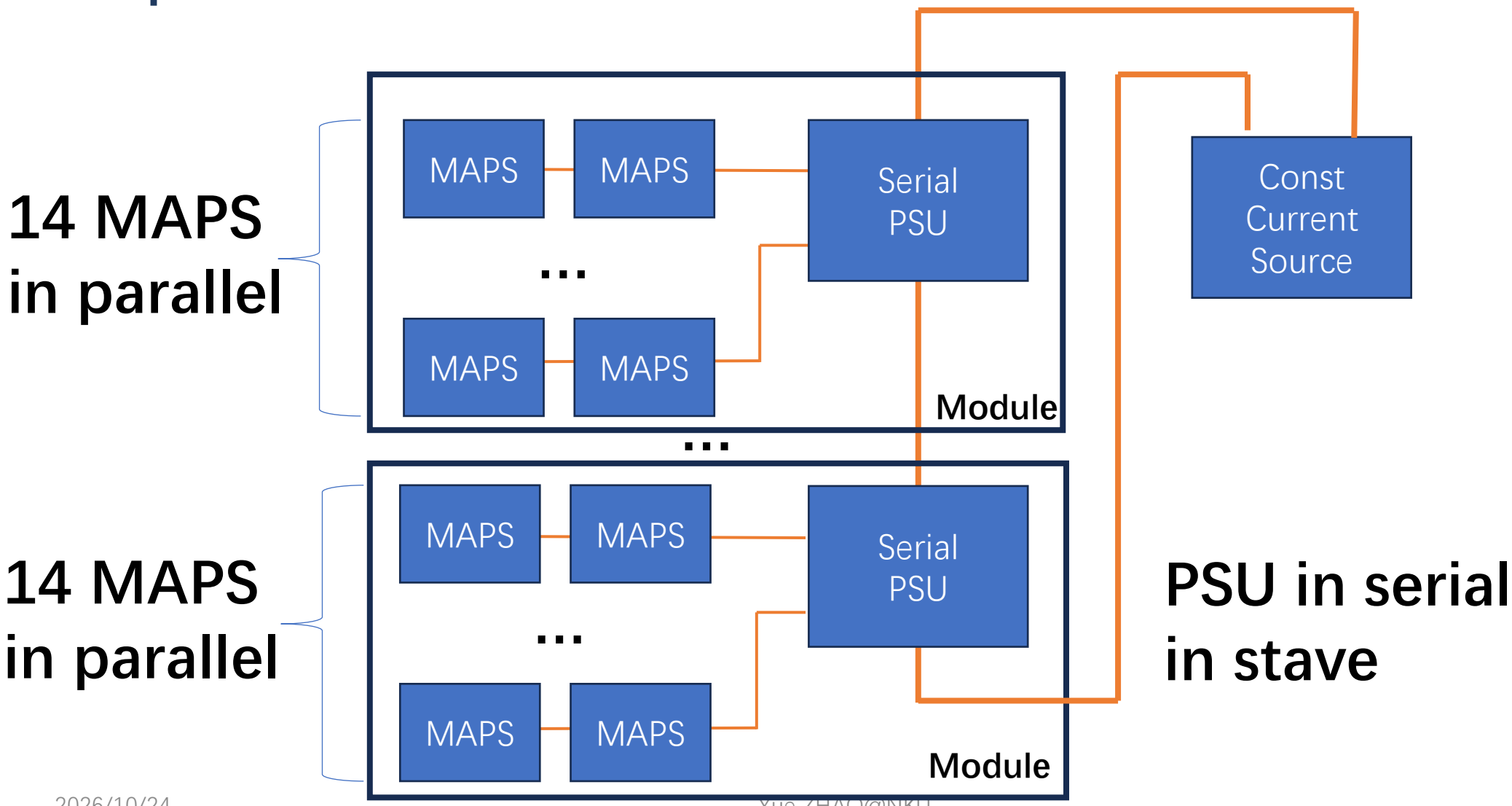
-> keep chain current stable

Solution for Data transfer links: LVDS link with AC coupling



- Floating ground across the chain → transmitter and receiver sit in different power domains.
- AC coupling blocks the common-mode voltage, passes the high-speed LVDS data.
- 8b/10b + CDR recover the clock on the far side; the receiver clamp isolates common-mode swings.
- The serial powering structure can interfere with LVDS signal integrity; transmission is gated off during power-rail switching (**less than 1% of transmission time**) to trade a tiny duty cycle for signal stability.

Implementations in ITK



Future works

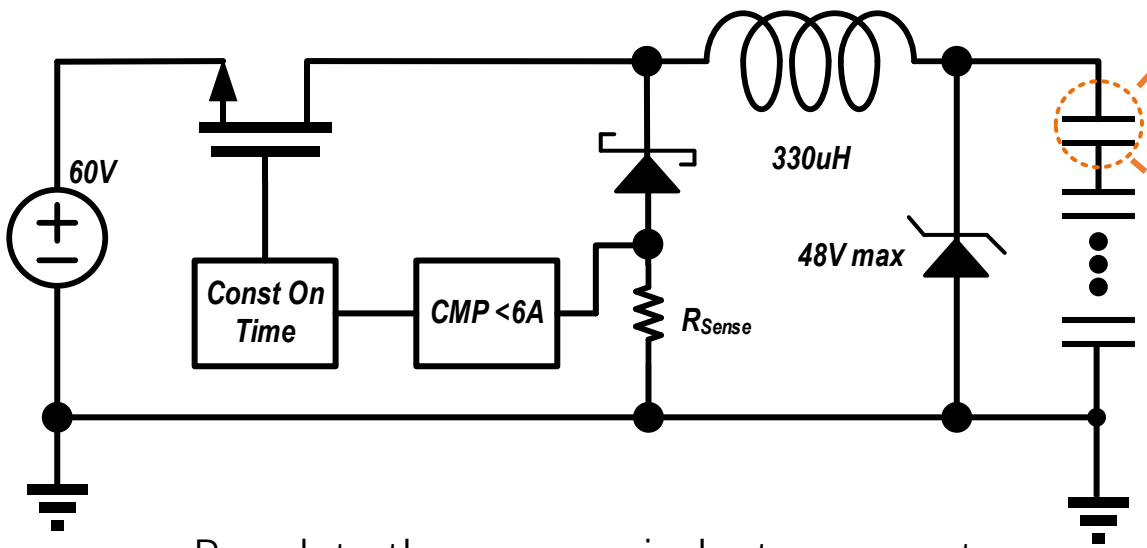
- ASIC under design, type-out @ Spring 2027.
  - Integrated Proposed Approach 2
  - Integrated an ultra-low dropout regulator (V_{DROP} ~150mV)
  - Integrated open-circuit monitoring
  - Integrated data transfer links

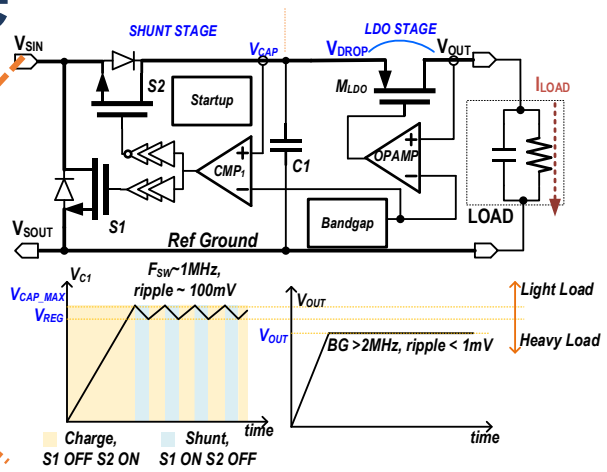
- Implement a current source with high bandwidth.
- Evaluation of noise levels and sources.
- Radiation effects and radiation hardening.

Thank you all for attention.
Questions ?

BACKUPs

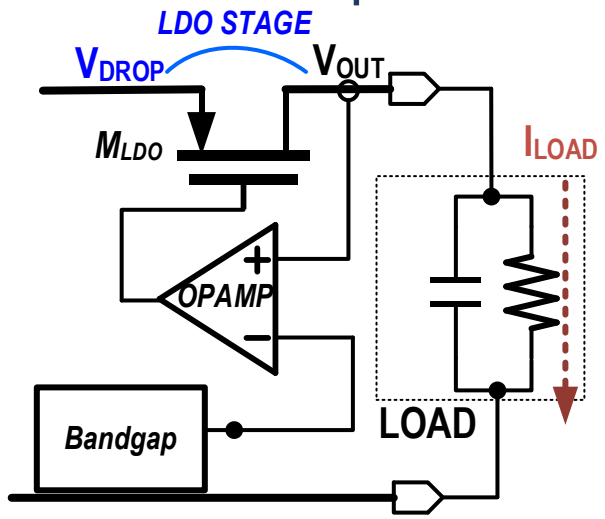
Buck Based Current Source





Regulate the average inductor current.

Ultra-Low-Dropout Regulator: Reducing V_{drop} Loss



Problem:

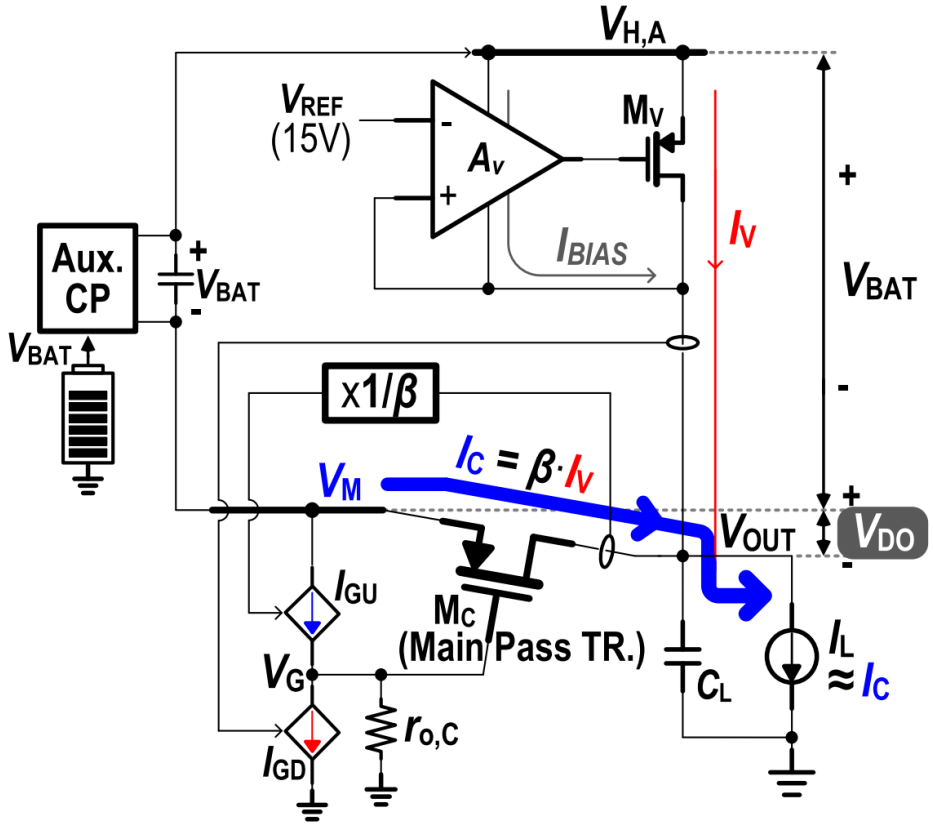
$P_{drop}=I_{load}\times V_{dropout}$;

$V_{dropout}\downarrow$ ➔ MLDO deep linear region

➔ gm/ro drop

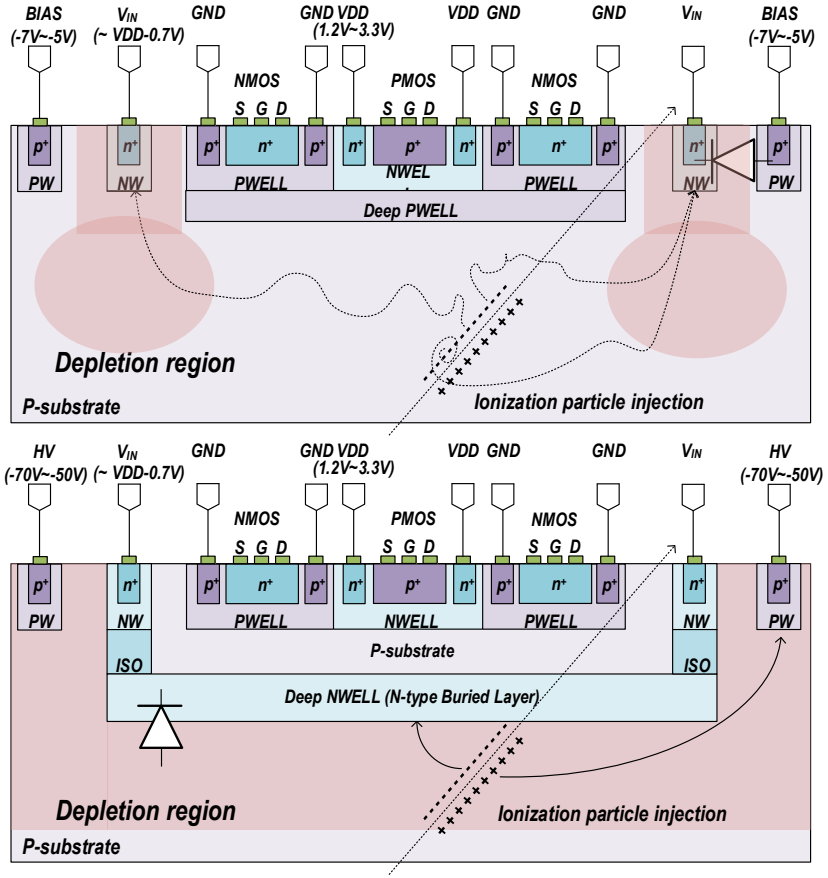
➔ worse loop gain & load regulation

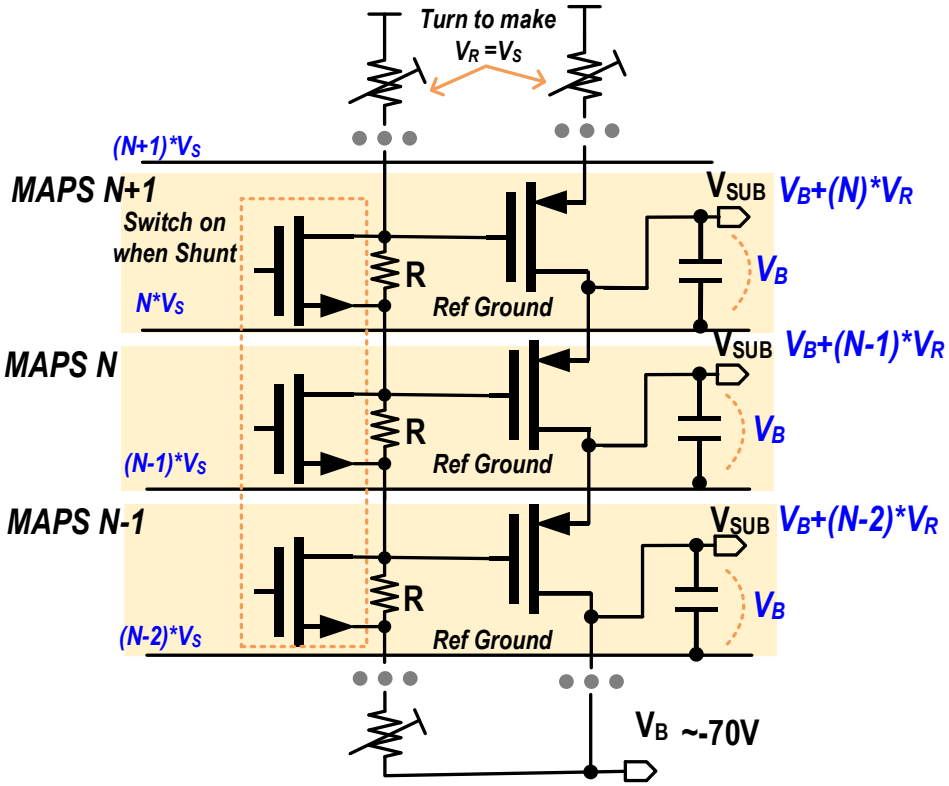
$V_{dropout}\uparrow$ ➔more power loss



Solution: a higher-voltage rail to generate gain (Iv), replicated onto the energy-transfer rail (I_{GD}), resolving the conflict between output-stage gain and efficiency.

Solution for Floating Reference Ground : Bias Generation

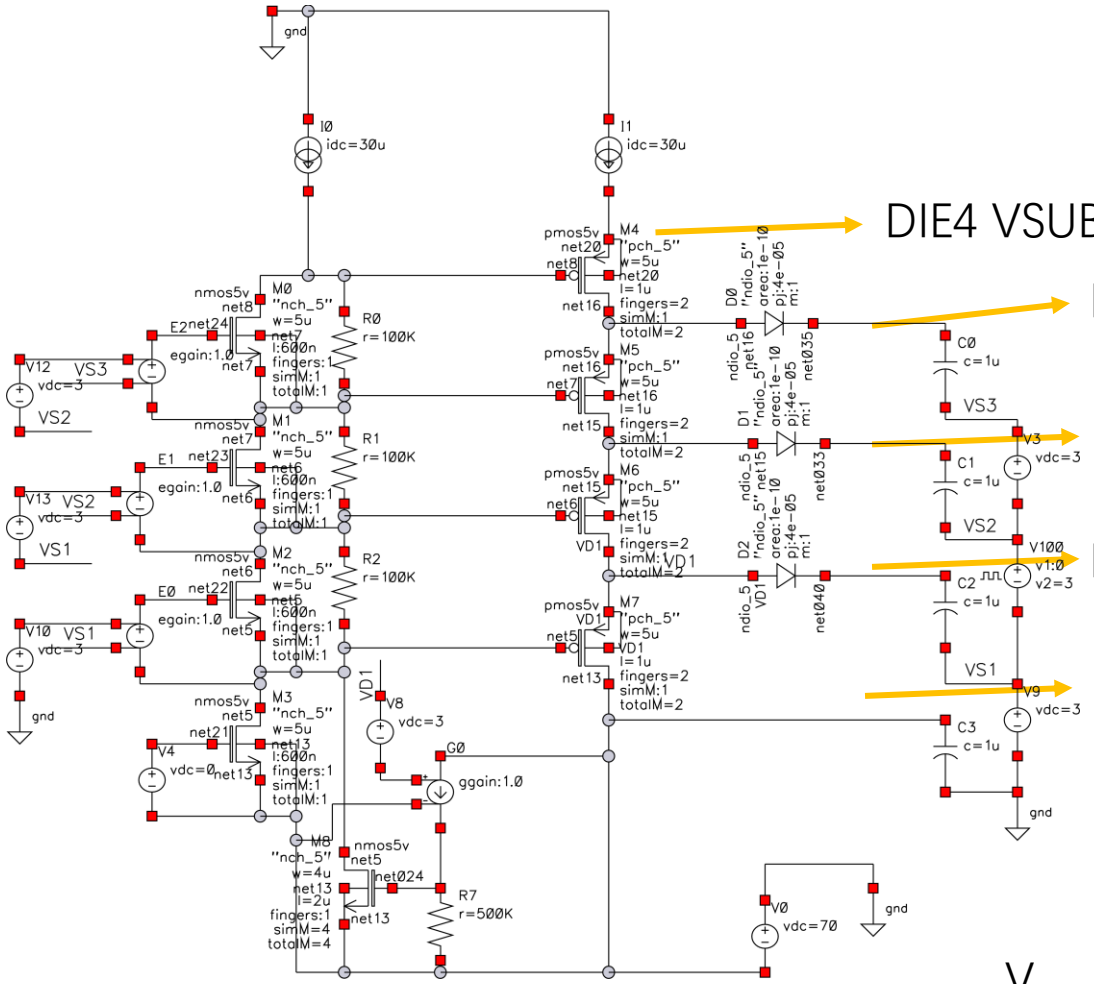




MAPS: Substrate needs bias to fully deplete the bulk (conventional MAPS ~−6V , HV MAPS -60V ~ -200V)

Serial powering: floating reference ground -> each DIE needs independent bias voltage for collection efficiency

Simulation Results



DIE4 VSUB = -58V

DIE 3 VSUB = -61V

DIE 2 VSUB = -64V

DIE 1 VSUB = -67V

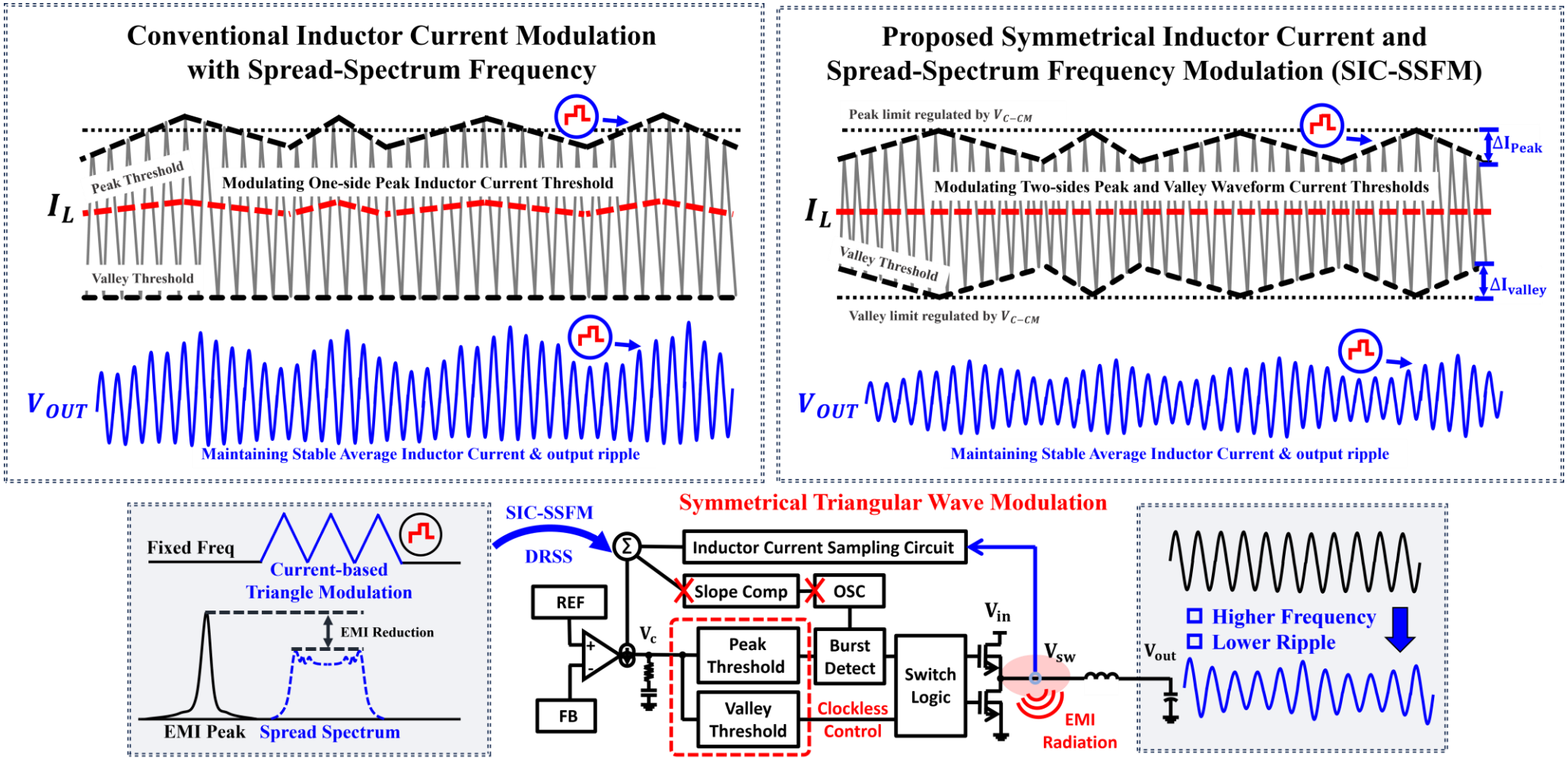
DIE 0 VSUB = -70V

- Each stage generates −70 V locally from small 1 nF cell stacks, keyed to its own floating ground.
- Because the reference floats, every DIE needs its own independent bias voltage.
- The −V trickle guarantees full-depletion collection efficiency across the chain.

- Each stage biases its local substrate to a fixed −70 V relative to its own ground, so Vsub,local = −70 V.
- Away from the chain input the absolute substrate voltage rises (DIE4 ≈ −58 V) as the local ground floats up.
- The generator keeps Vsub,local constant across the floating chain

$$V_{sub,local} = V_{sub,abs} - GND_{,local} = -70\ V。$$

Solution for EMI Noise : Spread-Spectrum



More Results



