环形正负电子对撞机
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A 20-Gbps PAM4 transmitter with 2-tap FFE in 55 nm for high-energy physics experiments

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Outline

- Data transmission in HEP experiments
- Common data transmission ASICs for CEPC …
- Design and measurement of a PAM4 transmitter
- Summary

Data transmission in HEP experiments

- **The NRZ data rate primarily depends on the process node**

➢180 nm:	4~5 Gbps	
➢130 nm:	5~6 Gbps	(GBT、LOCx)
➢65/55 nm:	10~12.5 Gbps	(lpGBT…)
➢28 nm:	25.6 Gbps	(DART28、SPRINT)
➢……		

Smaller process node

Funds

Data transmission in HEP experiments

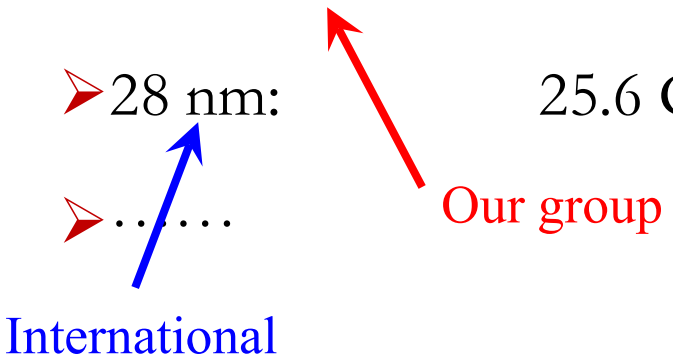
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  - 65/55 nm: 10~12.5 Gbps (lpGBT…)
  - 28 nm: 25.6 Gbps (DART28、SPRINT)

  } → PAM4

  - ……

Data transmission in HEP experiments

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  - ……

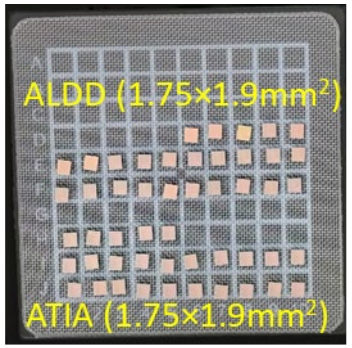


Common data transmission ASICs

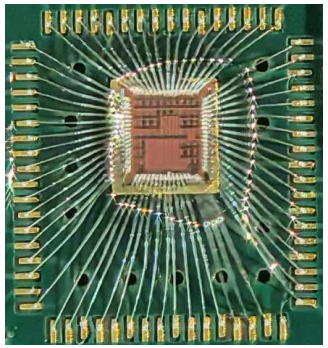
- **10.24/11.09-Gbps fiber data trans. ASICs**
  - ALDD (25.10): 4-ch array laser driver
  - ATIA (25.10): 4-ch array laser reciever
  - FEDA (25.10): FE data aggregator
  - FEDI (26.7): FE data interface

  } Preparing for testing

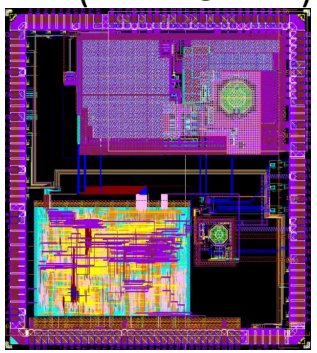
  - Collaborating institutions: CCNU, NPU, HBPU, WTU…



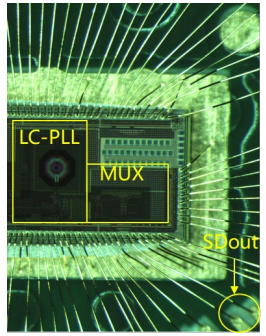
FEDA (1.3×1.4mm²)

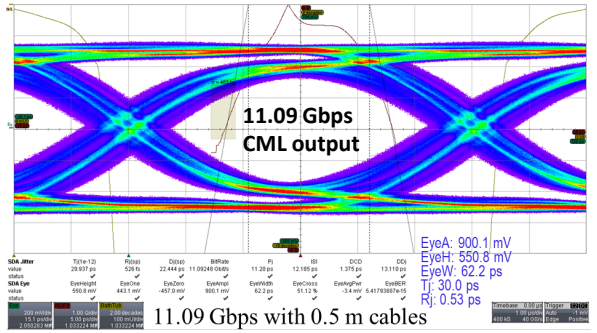


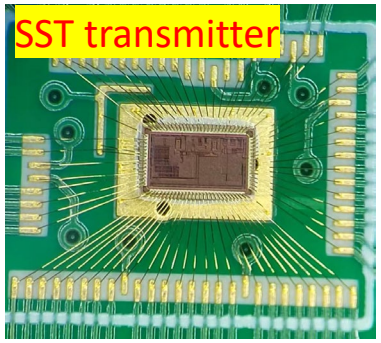
FEDI (2.7×2.5mm²)

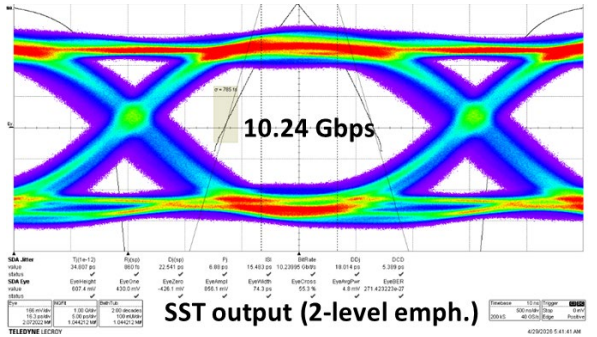


- **Other SER or SerDes developments (55 nm)**
  - Standard data communication (Aurora 64/66B)
  - Integrated data interface: TDC/ADC/…
    - ↓ 11.09-Gbps Serializer core (24.7) 30-ps Tj, 97.4 mW
    - ↓ 10.24-Gbps SST driver/transmitter (25.10) 35-ps Tj, 67.5 mW
    - ↓ 10.24/11.09-Gbps SST SerDes (27.?)
  - Radiation evaluation



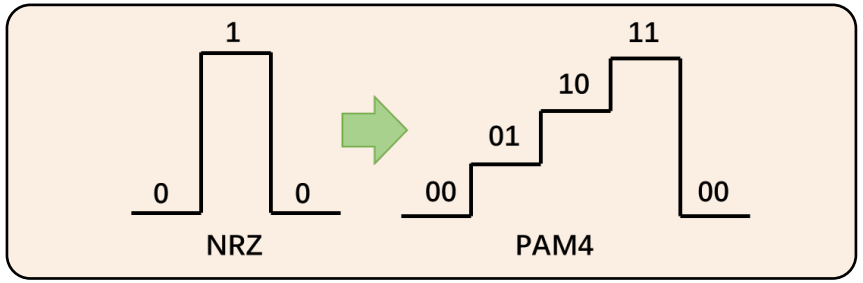


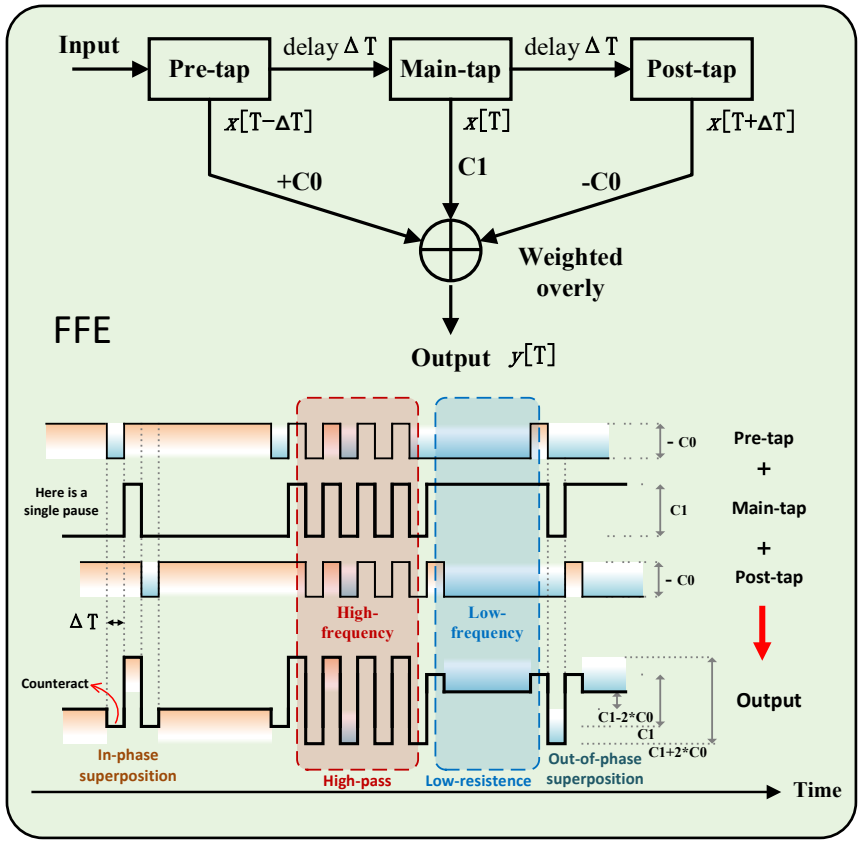




NRZ to PAM4

- **PAM4 technology**
  - Same analog bandwidth
  - Double the output data rate
  - Fewer cable channels
  - Linearity requirement
- **Feed-forward equalizer (FFE)**
  - Compensate for channel loss at low and high frequencies
- **Receiver**
  - FPGA
  - Custom PAM4 receiver ASIC

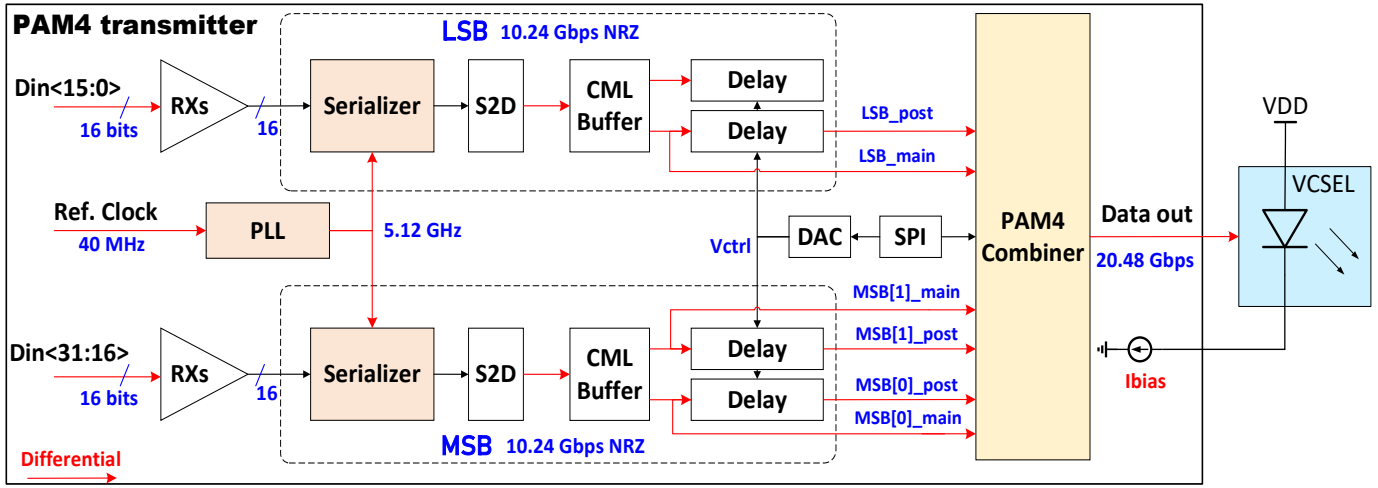




PAM4 transmitter development

Overall Architecture

- A shared PLL
- Two serializer channels (MSB and LSB)
- A PAM4 combiner with FFE
- Buffers & LVDS RXs
- SPI configuration



Initial prototype

- To verify combination and FFE functions
- Using PRBS-7 generators instead of the Serializers
- External high-frequency clock

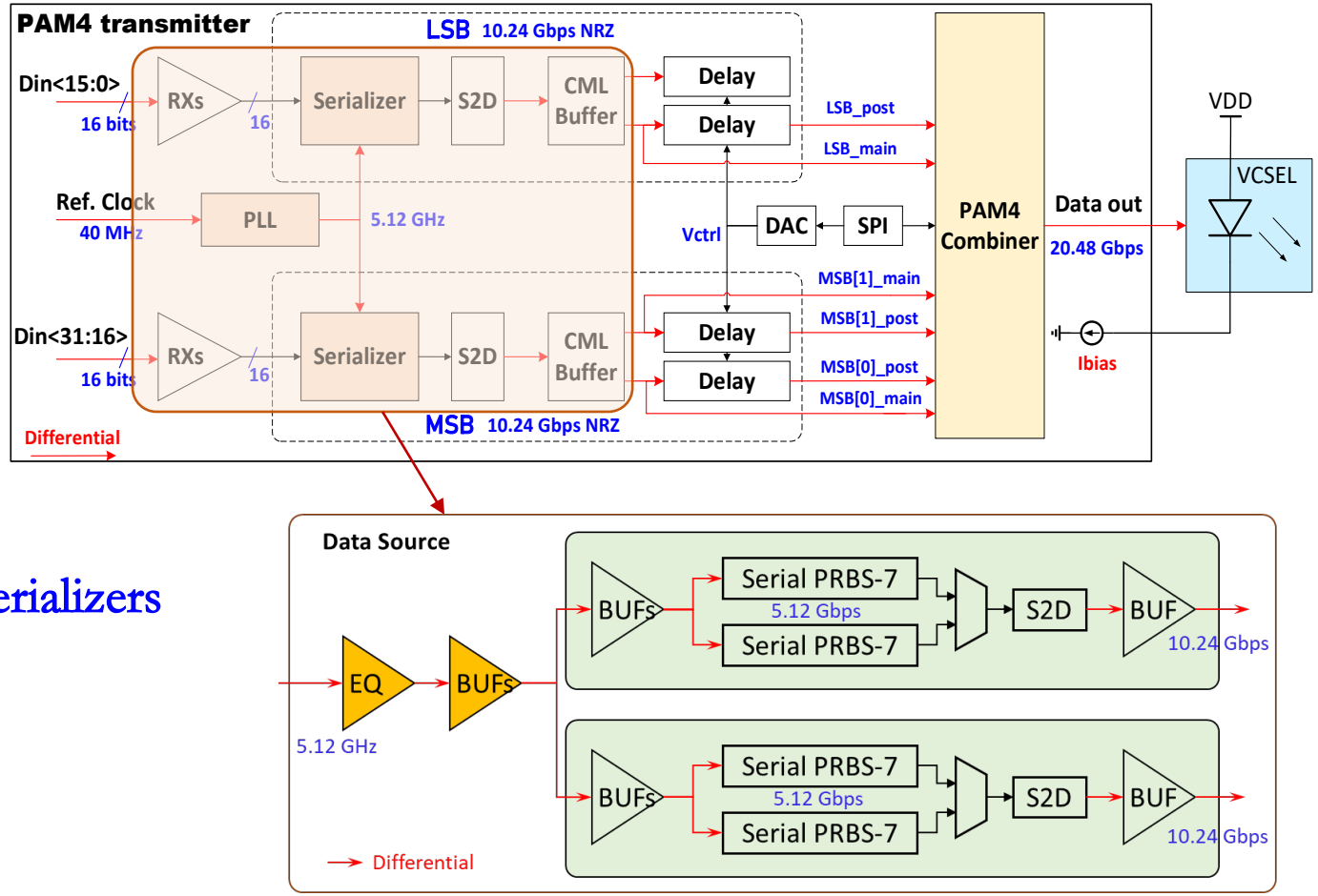
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Initial prototype

- To verify combination and FFE functions
- Using PRBS-7 generators instead of the Serializers
  - tspc DFFs improve the data rate
  - Data source: 15.6 mA @ 10 Gbps/ch
- External high-frequency clock



PAM4 transmitter development

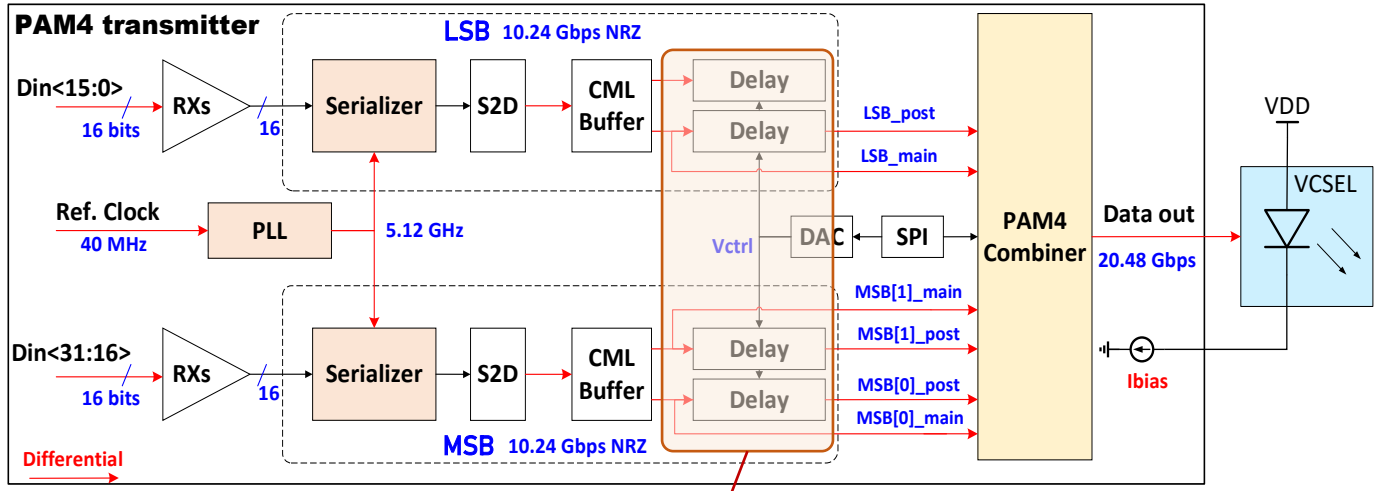
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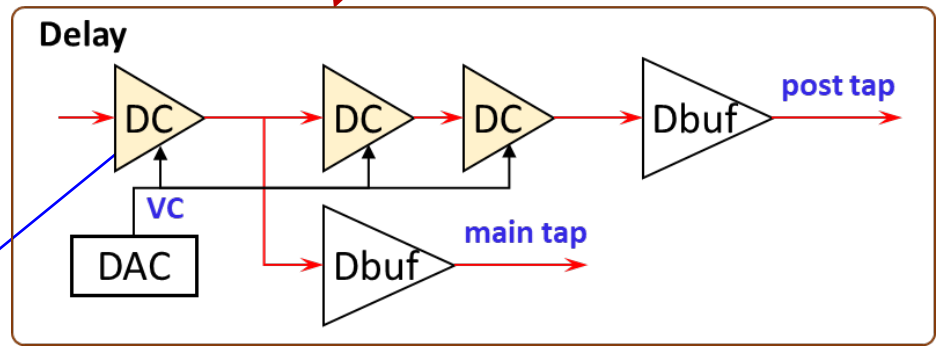
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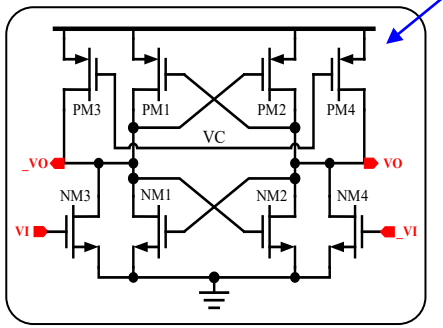
Initial prototype

- To verify combination and FFE functions
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- External high-frequency clock
- Voltage-controlled delay cell
  - delay range: 29~102 ps

  (10-bit voltage DAC)



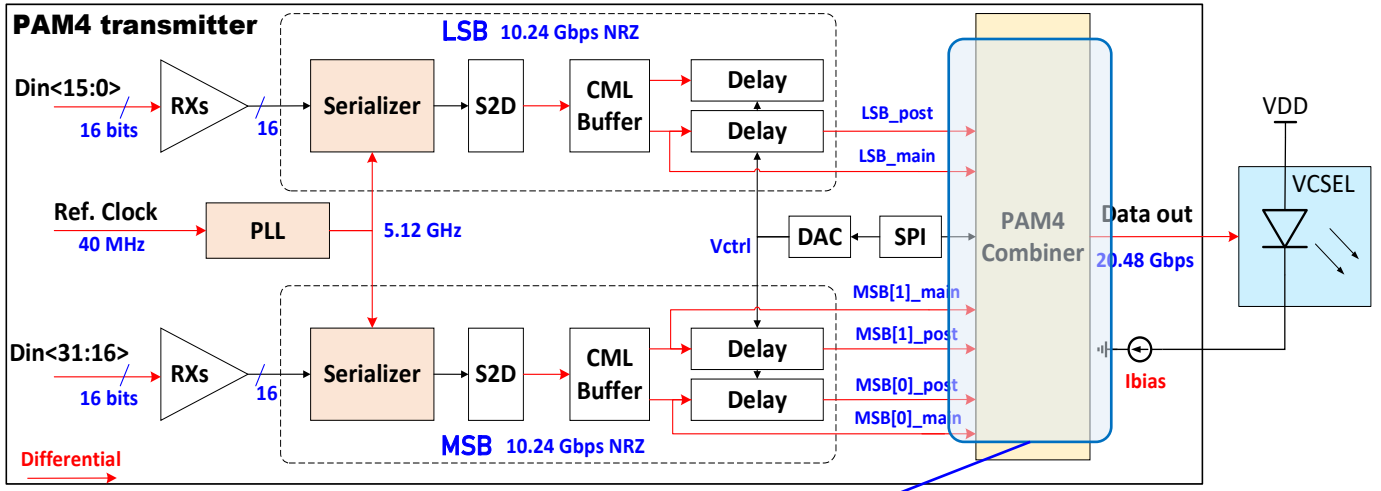


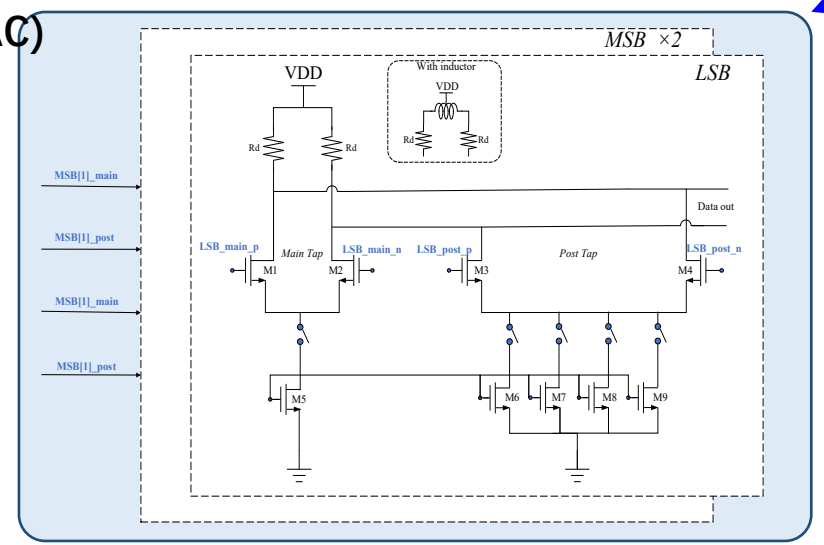


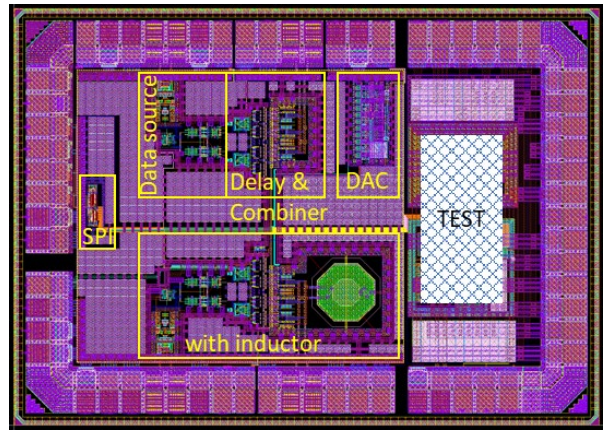
PAM4 transmitter development

Initial prototype

- To verify combination and FFE functions
- Using PRBS-7 generators instead of the Serializers
- External high-frequency clock
- Voltage-controlled delay cell
- CML-based combiner
  - **Main tap: 6 mA**
  - **Post tap: 0~1.5 mA (4-bit current DAC)**
  - Two versions for comparison
    - w/o inductor
    - with inductor
- Bias generator
  - For combiner
  - A biasing current output for VCSEL (0.4 ~ 9.8 mA)



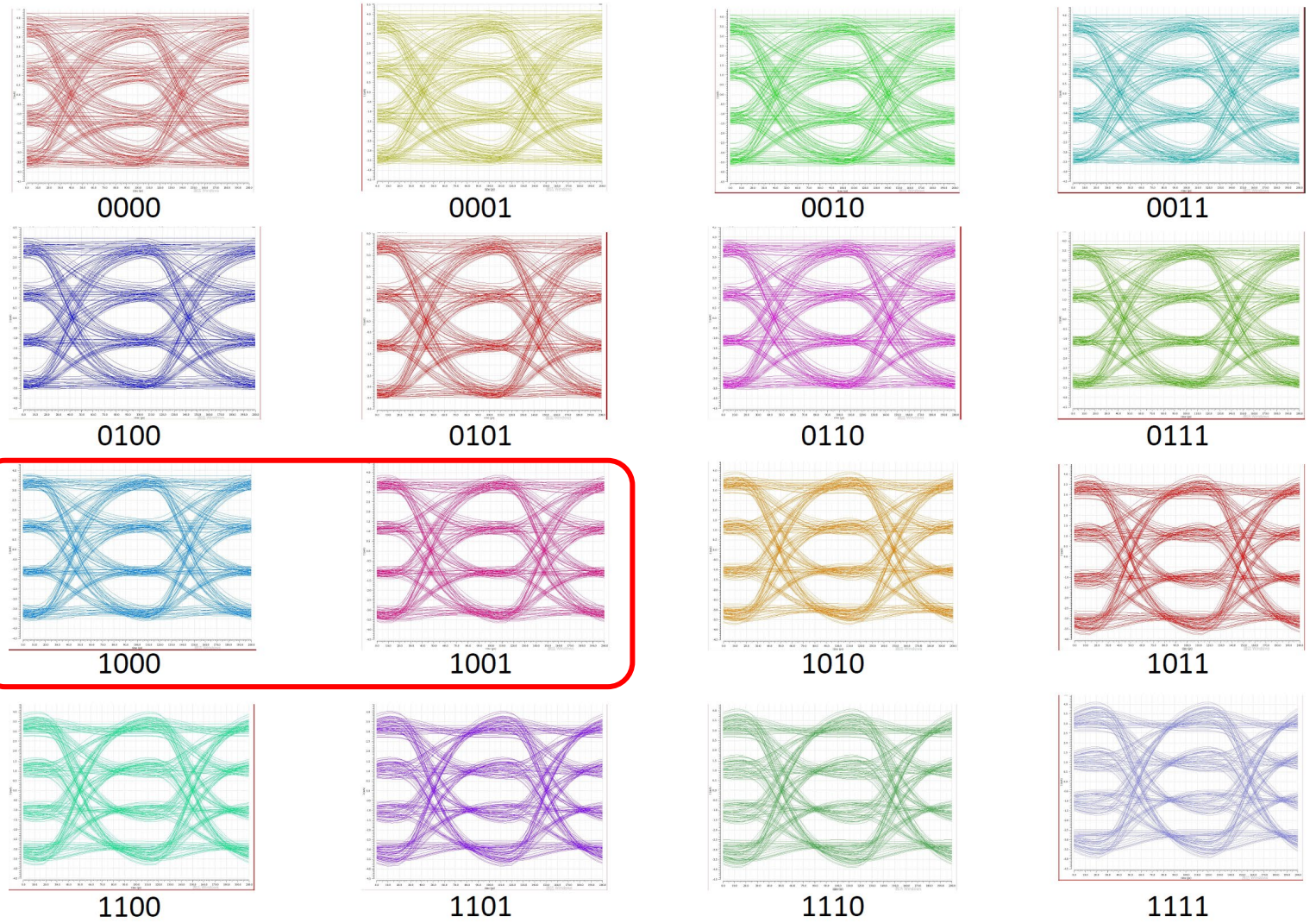




Core area: 260 × 660 μm²

Simulations

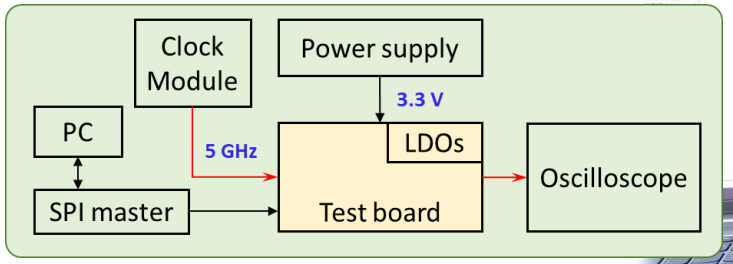
- no-inductor version
- 20 Gbps
- 0.5-m transmission line
- delay: 1UI
- Eye diagrams vs. FFE strength

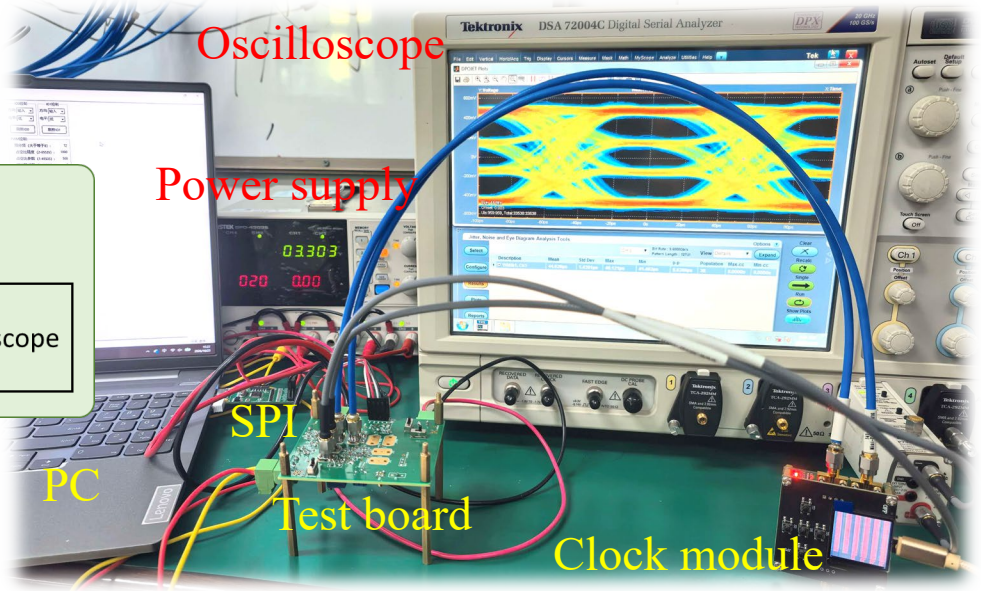


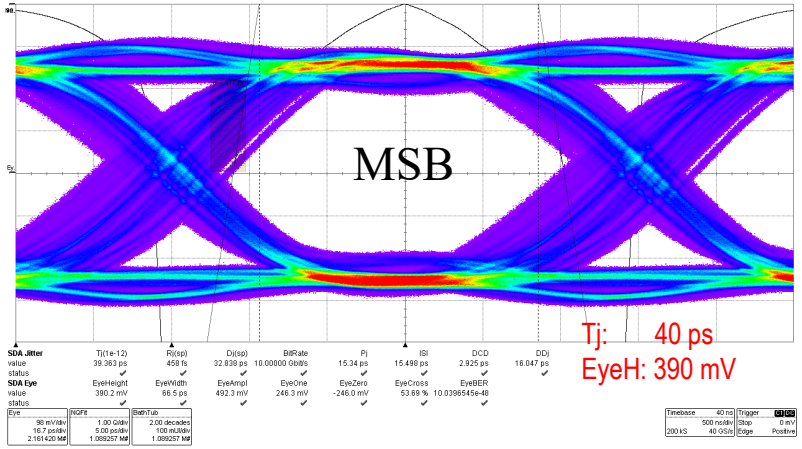
PAM4 transmitter test setup

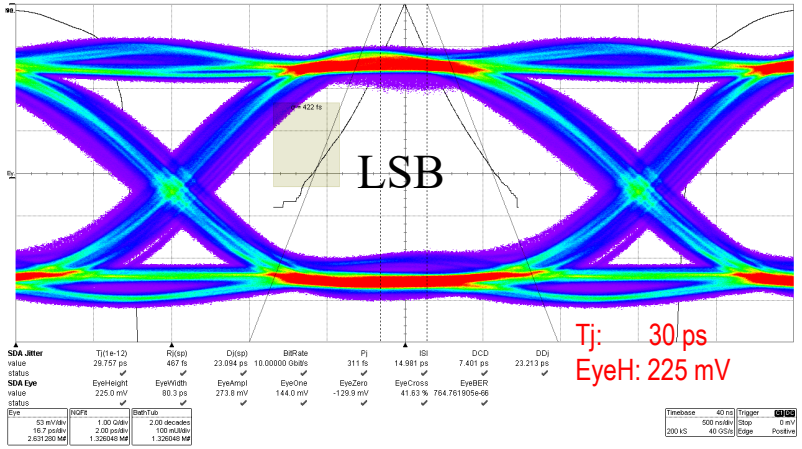
Electrical test

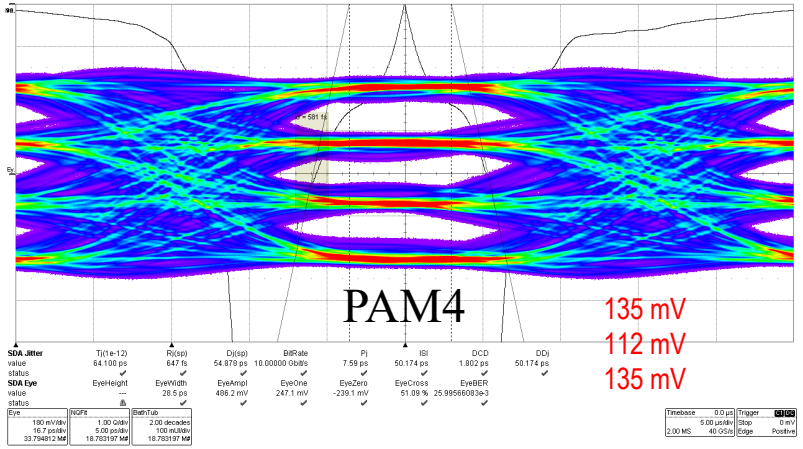
- LMX2594: external clock (5/5.12 GHz)
- LDO: 1.2-V core supplies
- Function verified
- Power consumption
  - Combiner: 18 mA (FFE-off)
    20 mA (FFE-0110)
  - Delay + Data source: 58 mA @VC=0.6V
  - Total: 94 mW











Delay: 1UI (VC≈1.19 V); FFE level 8 (1000)

Preliminary measurement

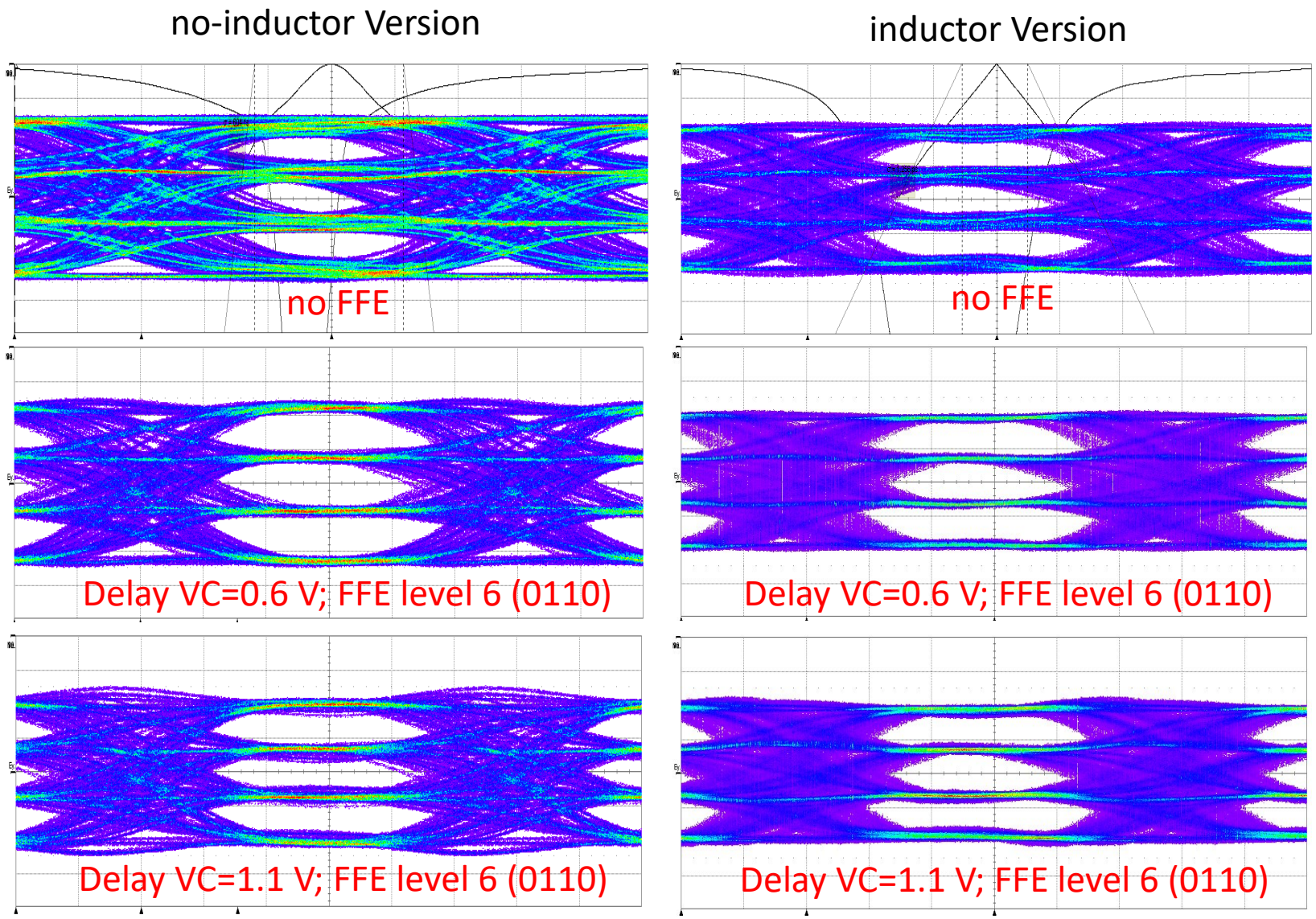
Best configuration

- VC=0.6V
- FFE level 6 (0110)
- Depend on channel loss

	No-inductor Version (mV)	Inductor Version (mV)
Full Eye Amp. (no FEE)	850	880
EyeH-H/M/L (no FEE)	109/102/132	120/120/140
Full Eye Amp. (0.6V-0110)	773	800
EyeH-H/M/L (0.6V-0110)	177/193/193	180/200/180
Ratio Level Mismatch (0.6V-0110)	0.956	0.894

Next step

- Optical test
  - The board is wire bonding



Summary

- In a 55 nm process, a 10-Gbps SST transmitter core and a 20-Gbps PAM4 transmitter core have been successfully verified.
- The serializer core has been integrated into some TDC prototype chips to increase the maximum event rate.
- Next, fully functional SST/PAM4 transmitters will be designed and further radiation evaluation will be carried out.



Thanks very much for your attention!