PERIPHERAL ELECTRONICS BOARD (PEB)

- EXPERIENCE FROM THE ATLAS HGTD IN-DETECTOR ELECTRONICS, PHASE-II UPGRADE

Jie Zhang and Lei Zhang on behalf of the **HGTD Electronics Team** · IHEP / NJU

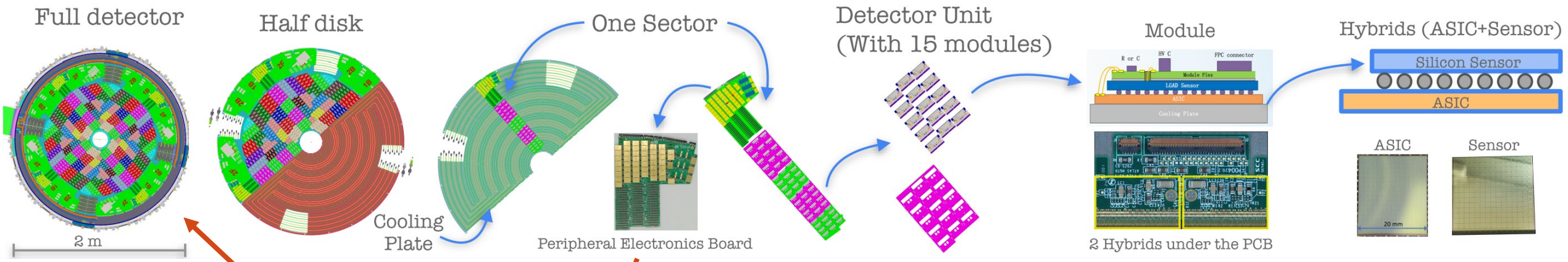
CEPC2026 · Shanghai · 21–26 October 2026

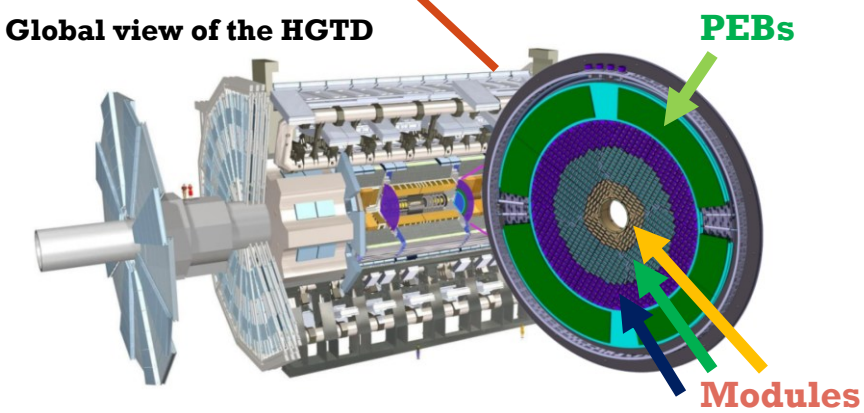
OUTLINE

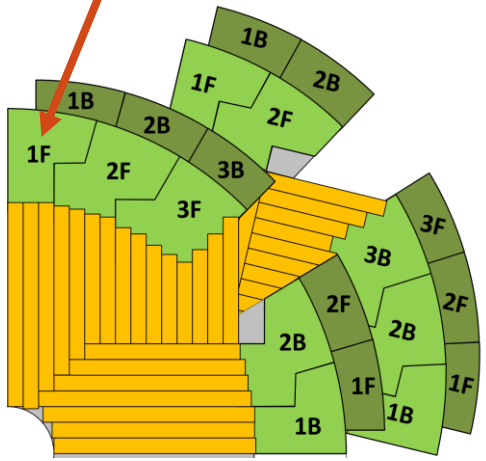
- Where the board sits, and why share it here
  - Constraints → technology choices
  - Five challenges, and two we could not control
- Power: the dominant term, and the AI loop
- Signal integrity
- What we would pass on

WHY THIS BOARD AT CEPC 2026?

HGTD breakdown from M. Leite, ICHEP 2026







- **HGTD**: timing at the HL-LHC — 8032 modules, **30–50 ps per track**
  - **PEB**: the *only* electrical path from those modules to every off-detector system
    - **6 variants, 160 boards**
    - **Δz < 10 mm · 2 MGy · Multi 10.24 Gbps high-speed links** — every choice traces to one of these

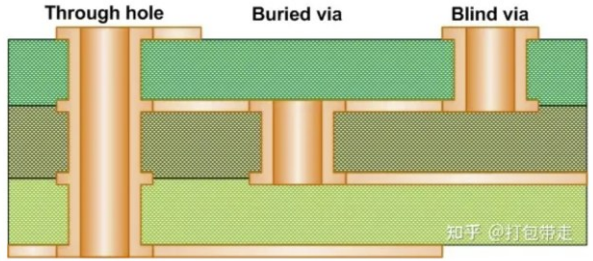
- **Why share it here?**
  - An e+e- detector has a far milder radiation budget — the **density, material, link count and service access** problems are the same.

TECHNOLOGY CHOICES

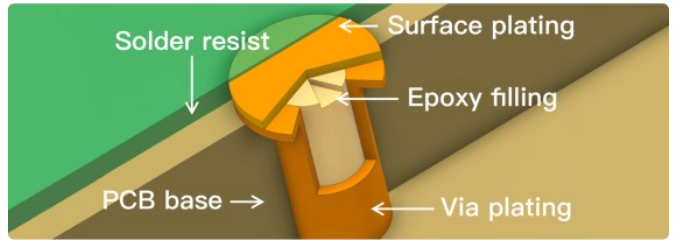
Function	Choice	The number that forced it
Data, clock, control	CERN **lpGBT** + **VTRx+**	10.24 Gb/s up (FEC5), 2.56 down
E-link rate	1280 / 640 / 320 Mb/s by radius	rate set by radial position; >470 mm adds luminosity
Monitoring	**MUX64** (QFN88)	8-ch ADC vs ~400 channels to read
Power	**bPOL12V**, 36–52 converters	11–12 V → 1.2 / 2.5 V, rad-hard; grouped for availability
HV	one channel per module	Up to **550 V** bias each
Halogen free PCB	TU-883 HDI, **20 / 22 layers**	9.7 of 10 mm; function-per-layer
Module interface	FPC at **6.5 mm** pitch	Up to 55 connectors on r ≈ 920 mm arc

- Symbols and nets
  - 3F: 2448 components, 9442 connections
  - 1F： 3386 components, 12996 connections

- 22 layers, includes:
  - 8 layers for signals
  - 2 layer for HV and HV return ground
  - 4 layers for ground
  - 8 layers for power



- HDI (High Density Interconnector)
  - Micro via



- VIPPO / POFV: Via-in-Pad Plated Over PCB

FIVE CHALLENGES

1. **Space** — bounded in r and z. → 9.7 mm stack; FPC connector pitch → 6.5 mm
2. **Radiation** — bPOL12V time-to-failure after 10 Mrad, wide spread. → board-level mitigation and a footprint valid for both V6 and the FX1 redesign
3. **Power integrity** — point-of-load means large currents on short planes. → next section
4. **Signal integrity** — 12 gigabit pairs → next section
5. **Availability** — → distributed converters, scattered e-links

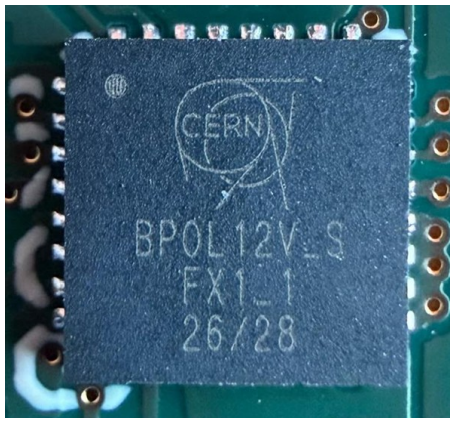
TWO CHOICES WE DID NOT CONTROL

	PCB material & fab	bPOL12V FX1
What happened	**fab A** dropped — capacity reallocated to **AI board orders**; re-routed to **fab B**	Fab: IBM → Onsemi, new import license needed
Why it bites	TU-883 low-loss HDI is the same tier AI servers now consume	PEB assembly is one SMT build — one missing part class stalls the board
Our response	freeze the stack-up early · second source · stay in a tier two fabs can build	Fall back to V6? — the part with the 10 Mrad concern

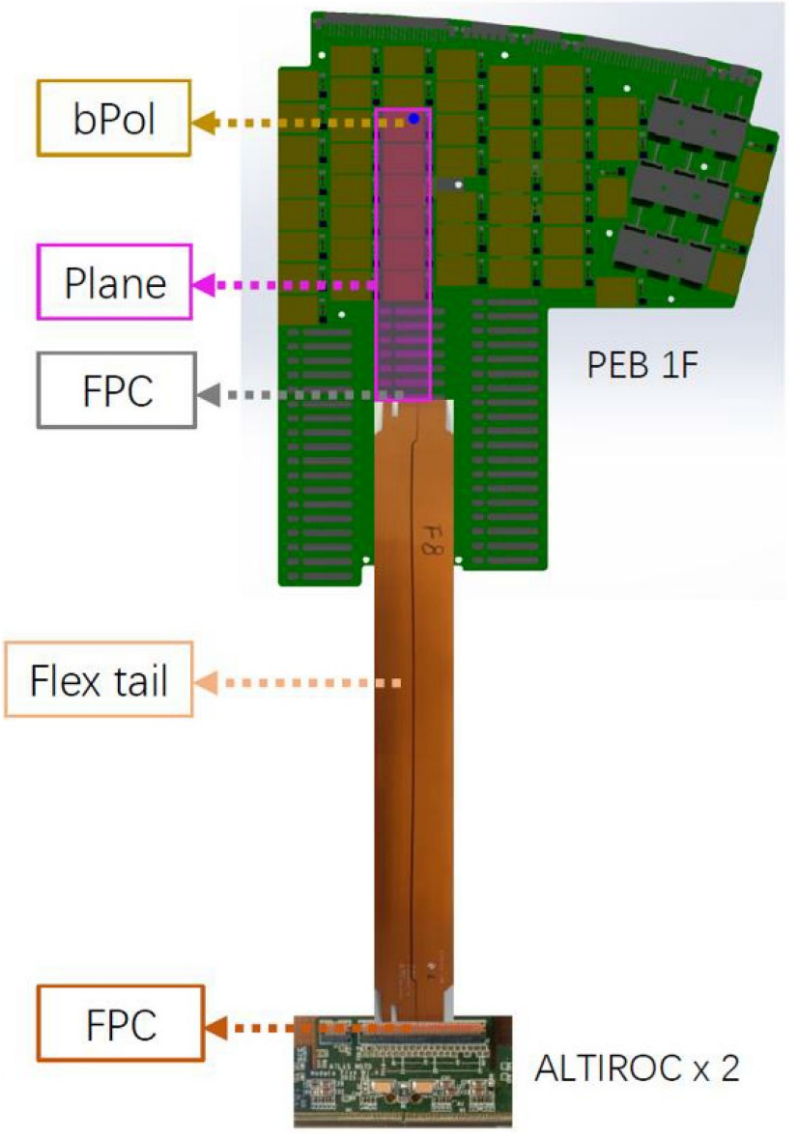
Ref: bPOL12V_FX1_TWEPP_Final.pdf

Very Low Loss and High Thermal Reliability Laminate and Prepreg





POWER: THE BUDGET IS A NUMBER TO HIT, NOT A CEILING TO SPEND



Estimated power consumption

	Module			Flex	PEB			Total
	Quantity	Sensor [W]	ASIC [W]	Power [W]	Type	Power [W]	Input LV [A]	[W]
Front side	55	44	132	8	1F	85	18.6	
	53	42	127	8	2F	81	17.8	
	36	29	86	5	3F	56	12.3	
	53	42	127	8	2B	81	17.8	
	53	42	127	8	1B	85	18.6	
Back side	55	44	132	8	1F	87	18.9	
	53	42	127	9	2F	86	19.1	
	37	30	89	6	3B	57	12.6	
	53	42	127	7	2B	76	16.5	
	54	43	129	8	1B	83	18.2	
Quadrant		400	1,200	75		780		2,450
End Cap		3,200	9,600	600		6,200		19,600

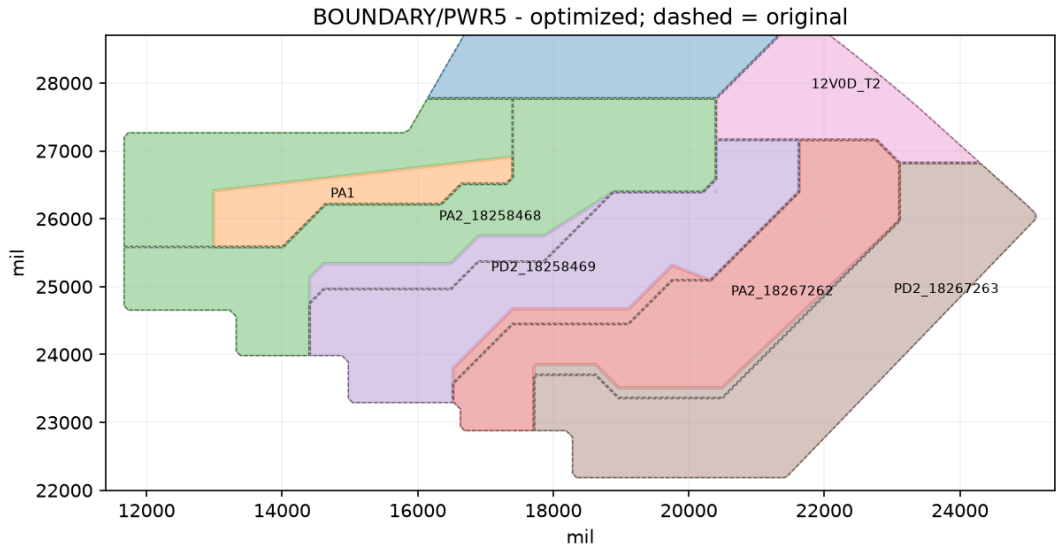
Inputs:

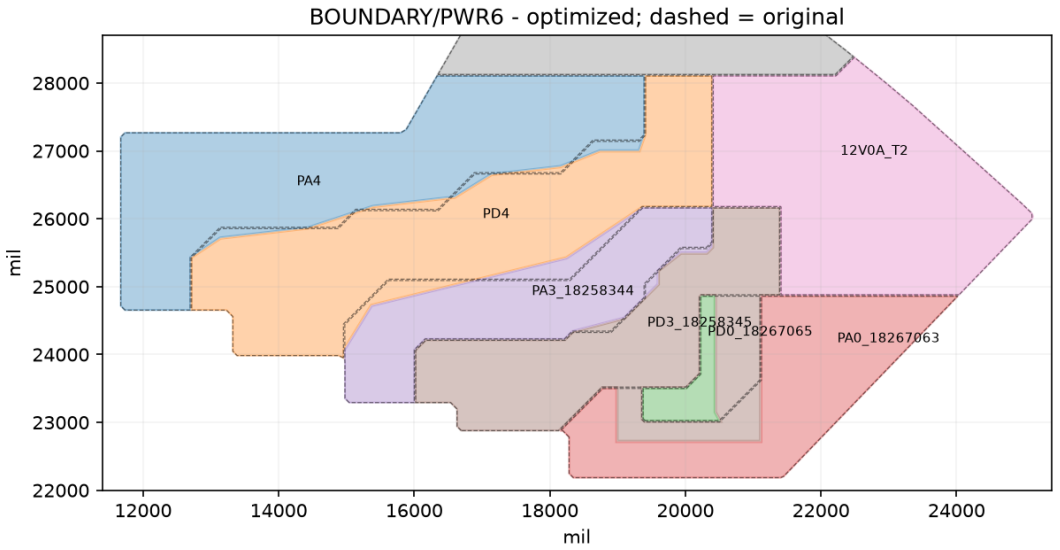
- ALTIROC accepts **1.25–1.35 V**;
- Module power consumption
- Internal resistance of the power plane
  - PEB+flex tail+module flex
- **How to organize the bPOL?**

path drop *d*	**allowed δ**
0	**±3.85 %**
11 mV	±3.81 %
50 mV	±3.70 %

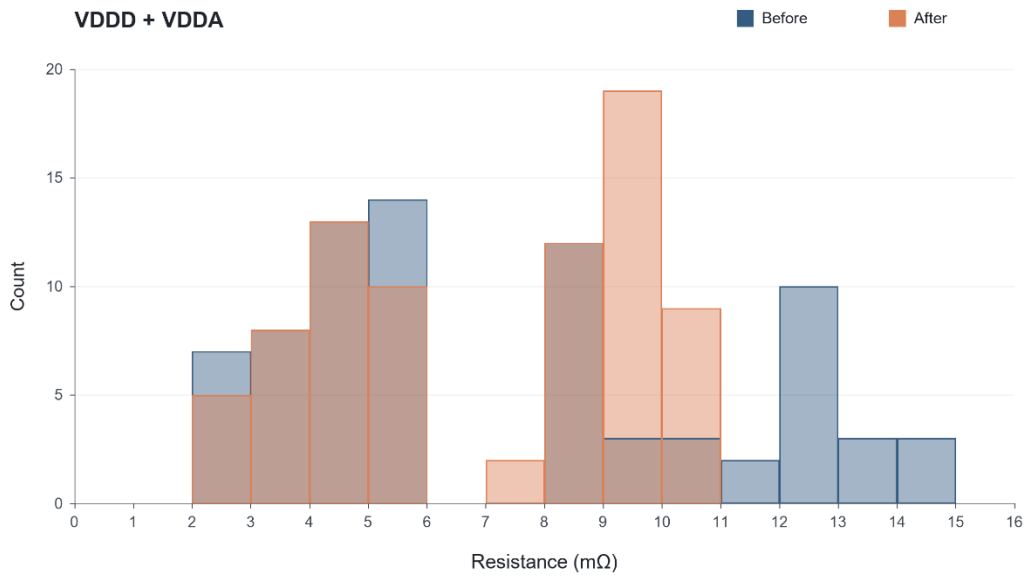
But the bPOL is quoted at ±5 % — a 1.3× shortfall. So the output must be **trimmed per group to ±3.7 %**

POWER: AN AI-ASSISTED LOOP, NOT A ONE-OFF STUDY





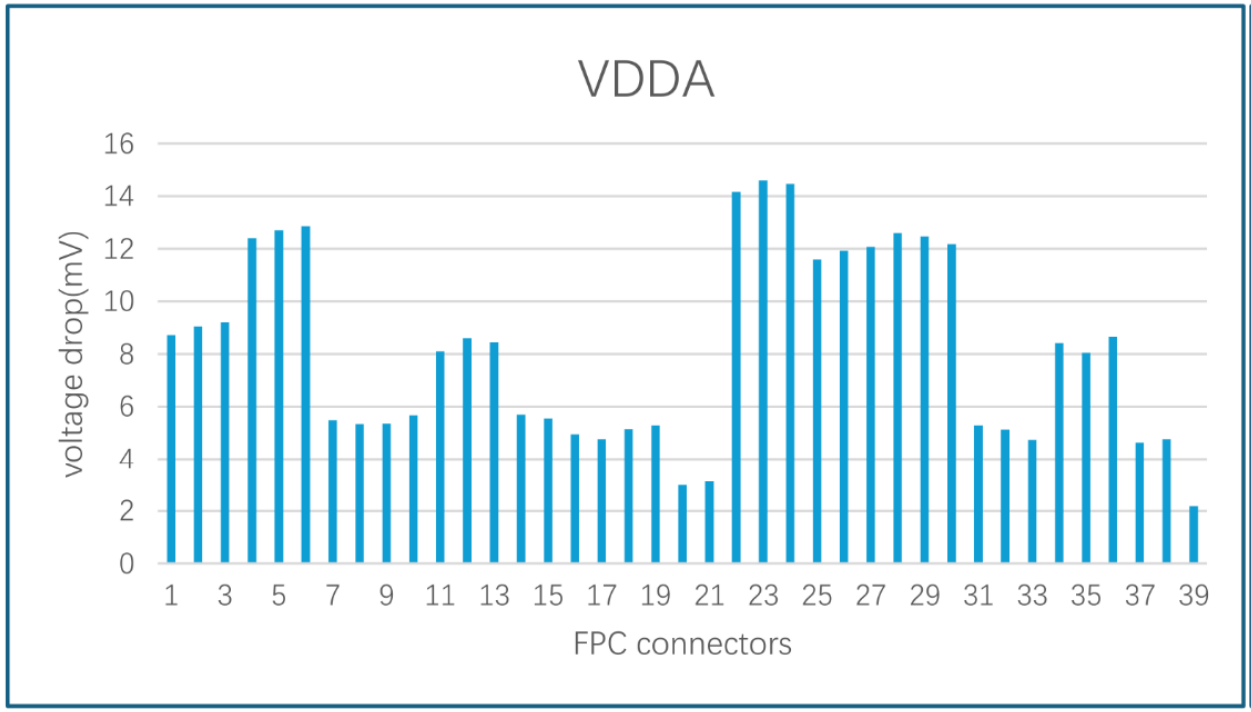
Step	What the AI does	Result
① Script	writes one Allegro .scr per net (on GitLab)	30 nets, no GUI work
② Run	batch runner drives Allegro, parses reports	**~20 min**, 4–5× faster
③ Act	reads the drop map, re-shapes splits, re-runs	**15 mΩ → 11 mΩ (–27 %)**

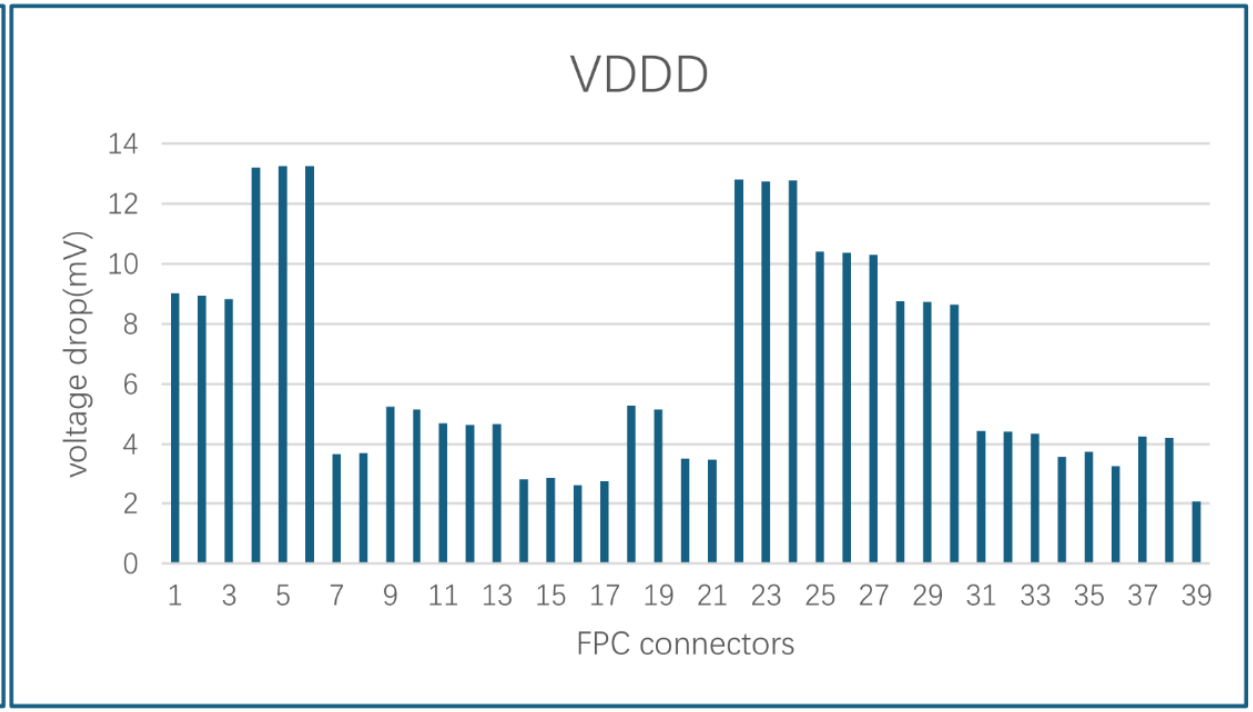


By Jiawei Wan(NJU)

POWER: CONFIGURATION AND RESULT

- Static IR drop · 30 VDDA/VDDD planes · 1 A per FPC connector (39) · fail above 10 mV

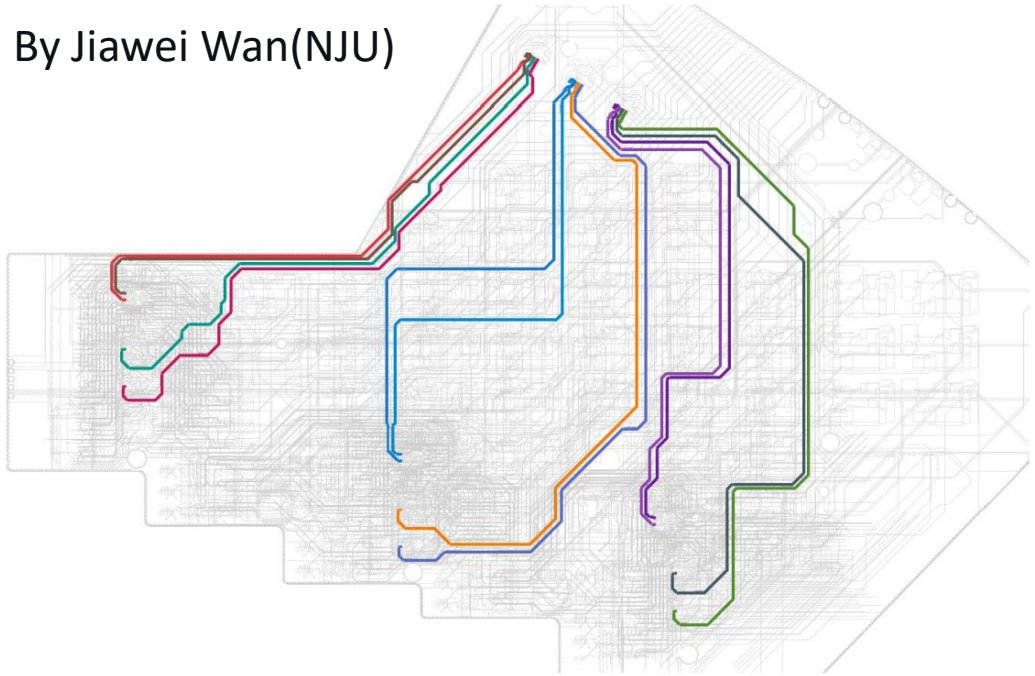




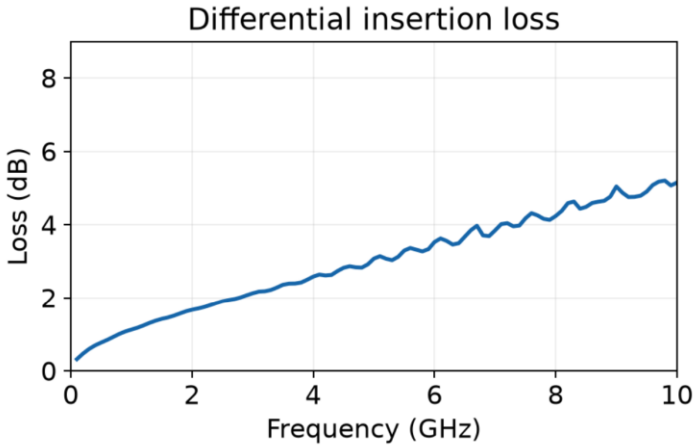
SIGNAL INTEGRITY(SI): SETUP AND RESULTS

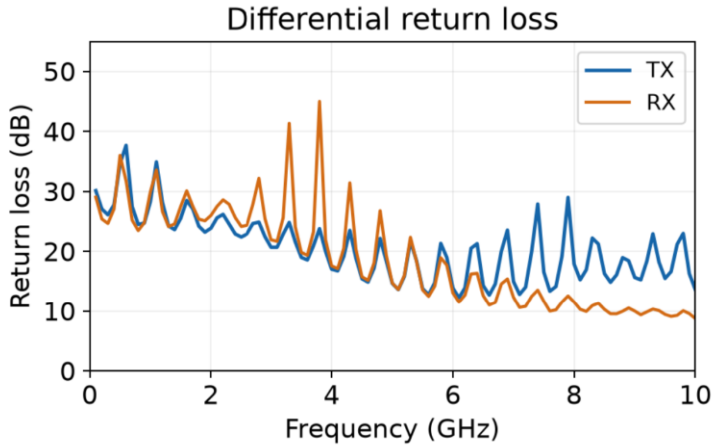
routing of the 12 channels

By Jiawei Wan(NJU)



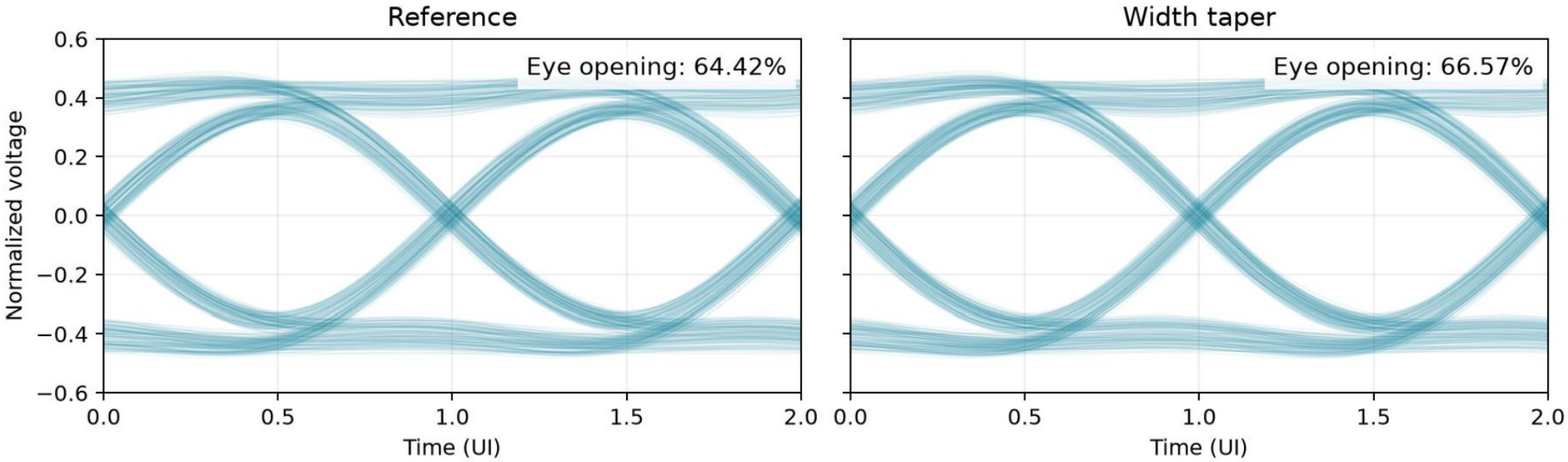
- **SI** Simulation Method
  - PCB interconnect S-parameter extraction
  - Frequency range: 0.1–10 GHz
  - Four-port representation of each pair
- Simulation Objects
  - 12 lpGBT–VTRx+ differential links
  - 9 uplinks (L2V) and 3 downlinks (V2L)
- One sample by AI in figure below





- Across 12 nominally identical uplinks the 10 GHz loss spans **4.59–6.18 dB** — 1.6 dB of pure routing and via variation (best L2V_0_1, worst L2V_2)
- Nyquist 1.93 / 3.13 dB @ 2.56 / 5.12 GHz (L2V_0); every eye open, **≥ 64 % of ideal**

SI: DELEGATE REPETITIVE TASKS TO AI



- Two changes paid: escape-width taper 0.109 → 0.203 mm (**−1.03 dB, +2.14 pp**) and route length (**−0.15 dB, +1.47 pp**)
- **AI searched the geometry space and ranked the candidates —** the rest (bends, antipads, via pitch) returned −0.06 / +0.004 / −0.03 dB
- Details in backup

By Jiawei Wan(NJU)

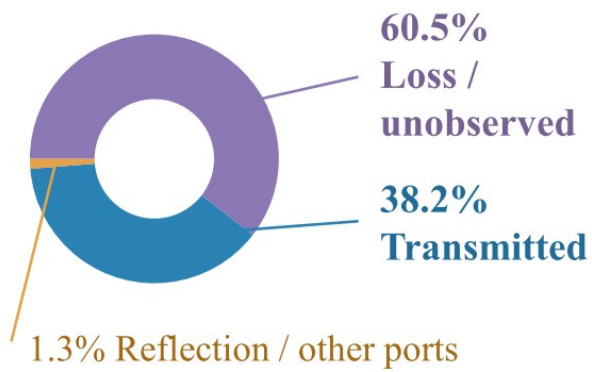
WHAT WE WOULD PASS ON

- **Qualify every radiation-tolerant part before you commit to production.**
  - For us it was the bPOL12V: it failed after 10 Mrad, and a footprint valid for two parts saved the schedule — the redesigned FX1 has since shown zero failures in 119 chips to 80 Mrad.
- **Automate with AI — then let it act.**
  - Two uses paid off: a 20-minute IR-drop loop that delivered a 27 % reduction inside the design cycle, and one SI search that picked 2 effective changes from 5 candidates.

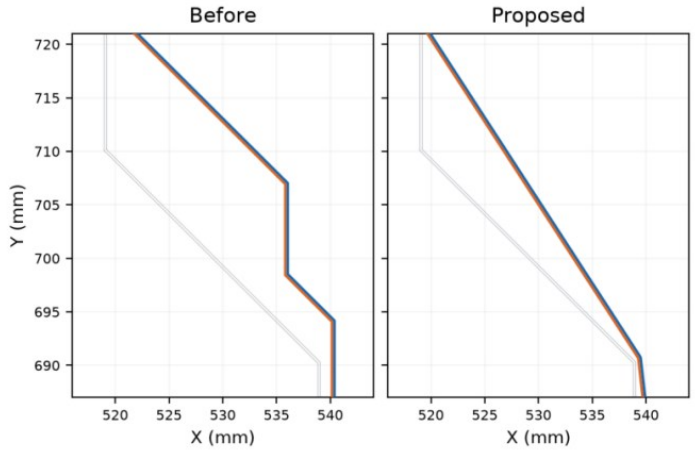

THANK YOU
FOR YOUR ATTENTION

SI: ROUTE-LENGTH OPTIMIZATION

1 Power balance at 5.12 GHz

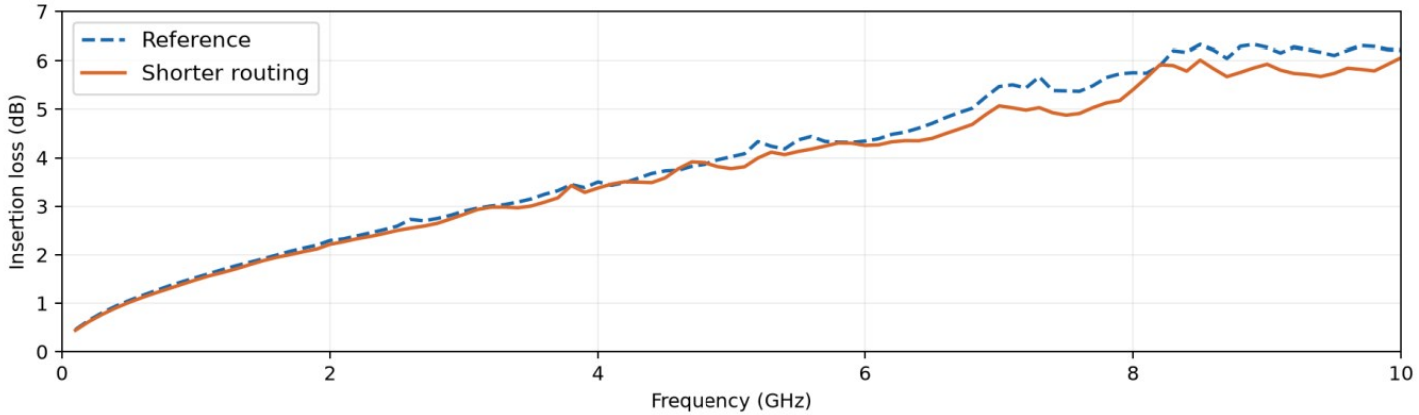


2 Proposed route

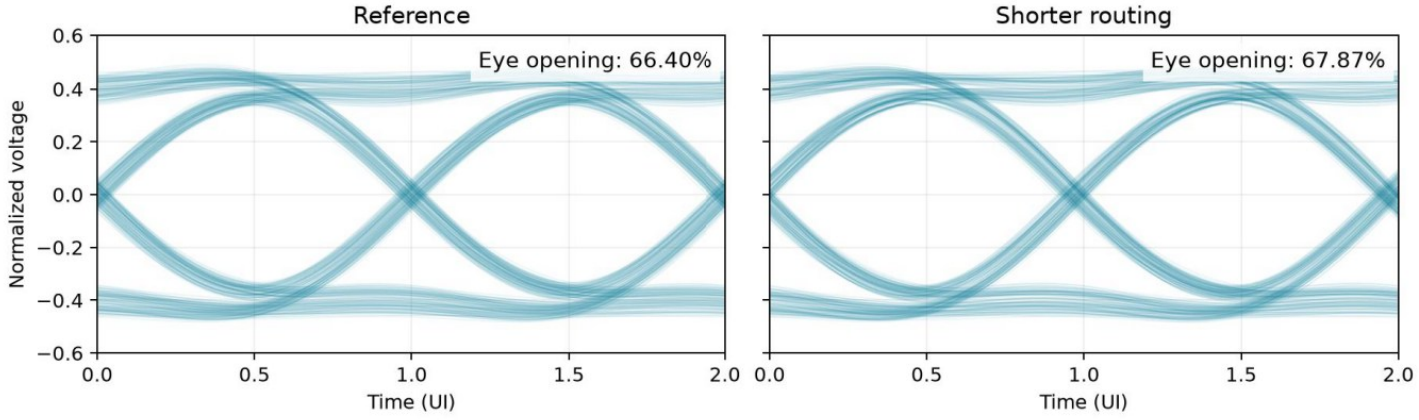


3 Previous route: simulation results

10 GHz: 6.210 → 6.063 dB



Previous eye result: 66.40% → 67.87% (+1.47 pp)

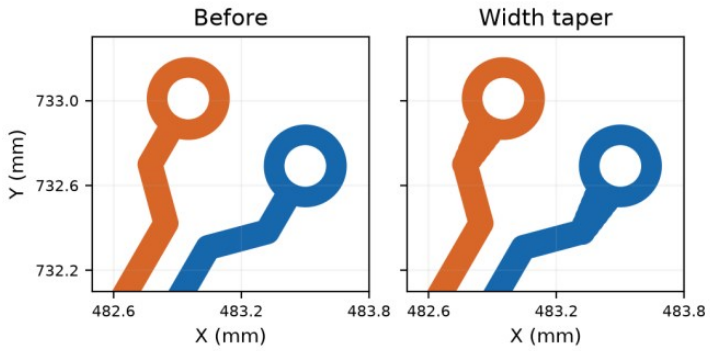


By Jiawei Wan(NJU)

SI: ESCAPE-WIDTH TAPER

1 Smooth the width transition

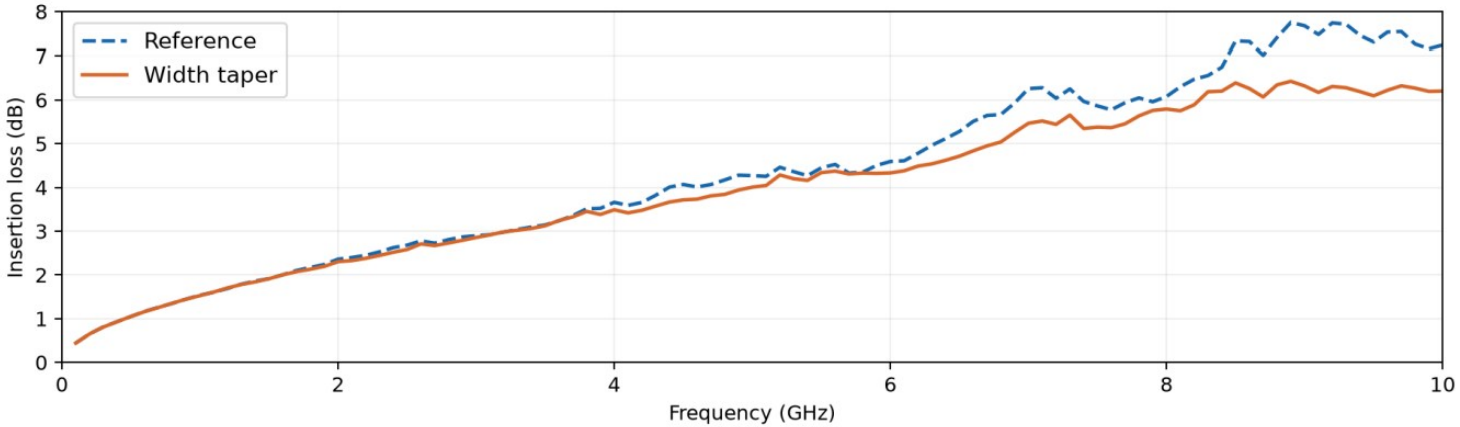
0.109 → 0.203 mm
Over ~0.358 mm, 10 steps



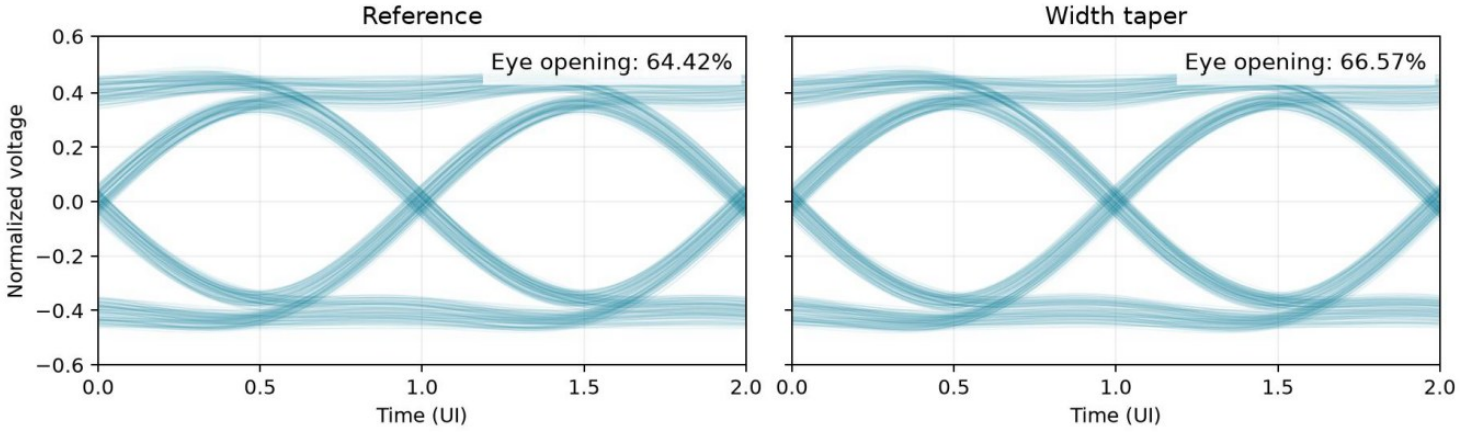
Fixed: route, vias, planes
and material properties

2 Insertion loss · matched compact test

10 GHz: 7.238 → 6.203 dB (−1.034 dB)



3 Eye opening: 64.43% → 66.57% (+2.14 pp)



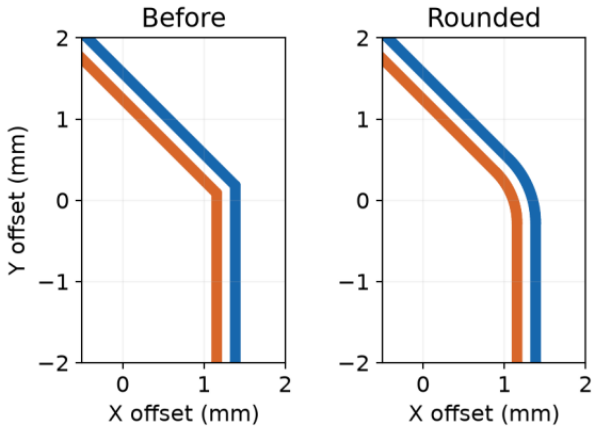
By Jiawei Wan(NJU)

GEOMETRY TRIALS WITH LIMITED BENEFIT

Rounded bends

L2V_2_2

Centerline radius: 1 mm



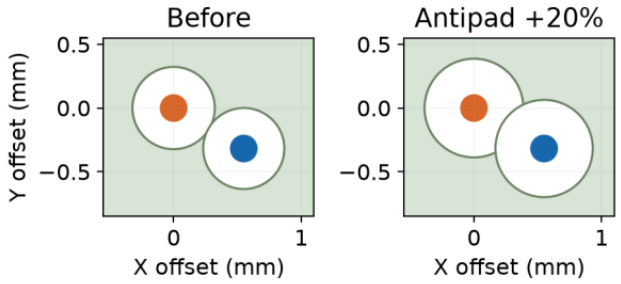
10 GHz loss: 7.238 → 7.176 dB
Eye opening: 64.425% → 64.385%

Negligible eye improvement

Larger antipads

L2V_2_2

GND1–GND4 antipad radii: +20%



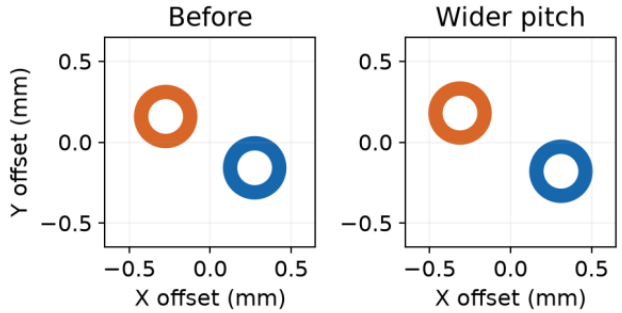
10 GHz loss: 7.238 → 7.242 dB
Eye opening: 64.425% → 64.398%

No meaningful benefit

Wider P/N via pitch

L2V_1_1

Center distance: 0.635 → 0.720 mm



10 GHz loss: 5.854 → 5.826 dB
Eye opening: 71.205% → 71.120%

Small loss gain, slightly lower eye

By Jiawei Wan(NJU)