

CMOS-LGAD & CMOS-AC-LGAD developments at INFN

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The 2026 International Workshop on the High Energy Circular Electron Positron Collider

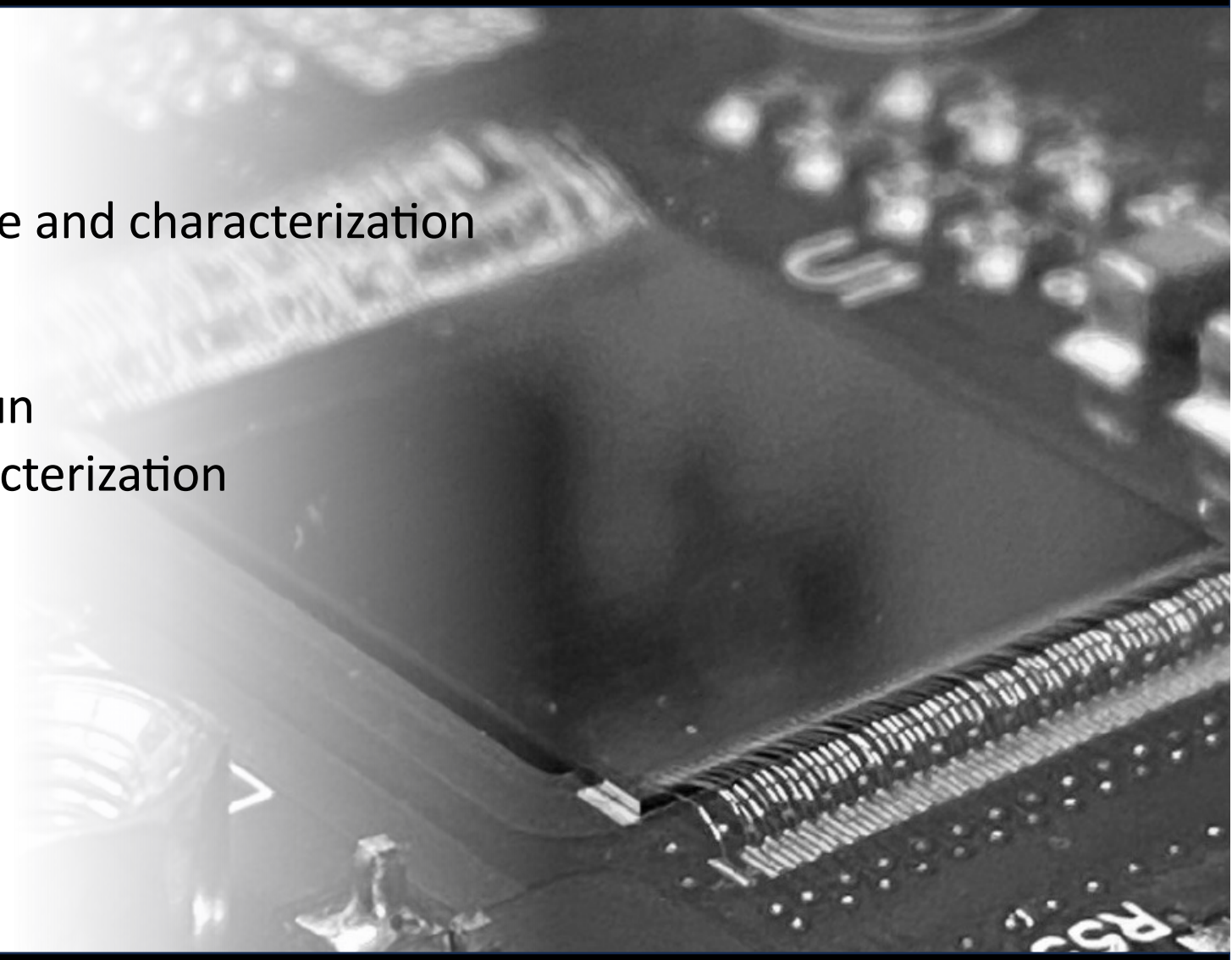
Shanghai, 21–26 October 2026

Outline

I. ARCADIA platform
- sensor concept and substrates
- Main Demonstrator – architecture and characterization

II. Technologies for timing
- the third ARCADIA engineering run
- MADPIX – architecture and characterization

III. Technologies for 4D-tracking
- sensors with resistive readout
- CMOS-RSD development



I. ARCADIA project

Advanced Readout CMOS Architectures with Depleted Integrated sensor Arrays

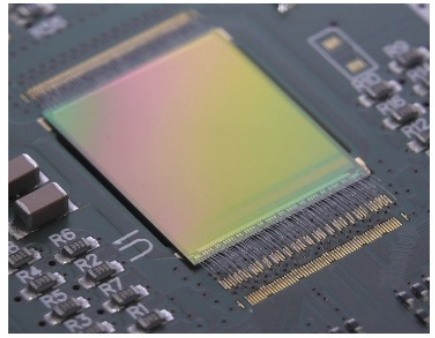
CMOS sensor design and fabrication platform on LF11is technology:

- Sensor R&D and Technology, CMOS IP Design, Chip Integration and Data Acquisition
- Scalable FD-MAPS architecture
- Very low-power sensors: ~10 mW/cm^2

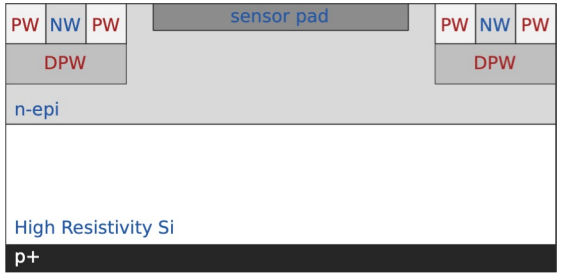


Present and future milestones:

- Main Demonstrator full-chip FD-MAPS for Medical, Future Leptonic Colliders and Space Instruments
- Custom BSI process allow to develop fully-depleted thick sensors for imaging
- Fully-Depleted Monolithic Active Micro Strips (FD-MAMS) with fully-functional embedded readout electronics
- Ongoing R&D on monolithic CMOS sensors with gain layer for fast timing
- High-density, low-power silicon sensors for tracking ionising particles in space



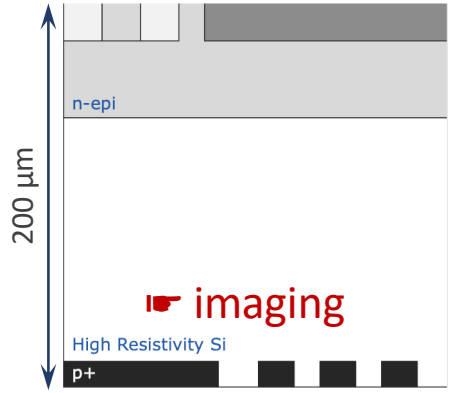
I. Sensor concept and substrates



- *n*-type high resistivity + *n*-epi layer (reduces punch-through current between *p*+ and deep *p*-wells) active region
- sensing electrodes can be biased at low voltage (< 1V)
- reverse-biased junction: depletion grows from back to top
- ongoing R&D: fully-depleted pad sensors with gain layer

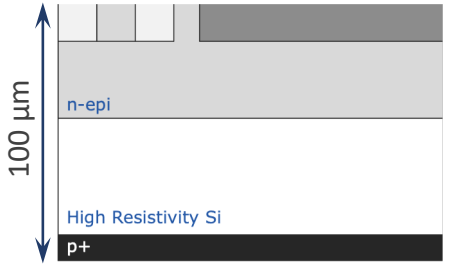
HR wafers - backside litho

thinning, **lithography**, backside ***p*⁺ implantation** and laser annealing, **insulators/metal** deposition and patterning



HR wafers NO backside litho

thinning, backside ***p*⁺ implantation** and laser annealing



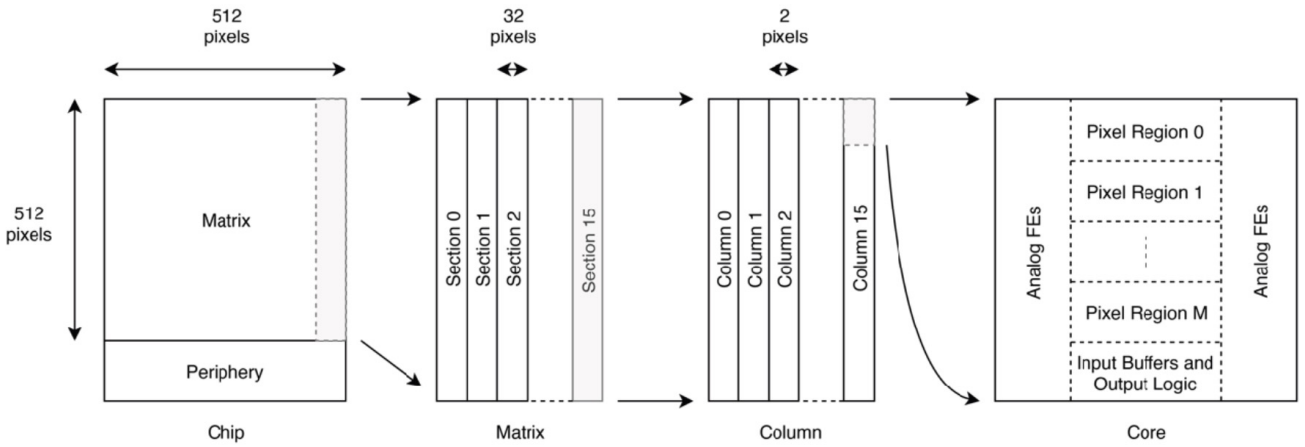
☛ generic particle detection

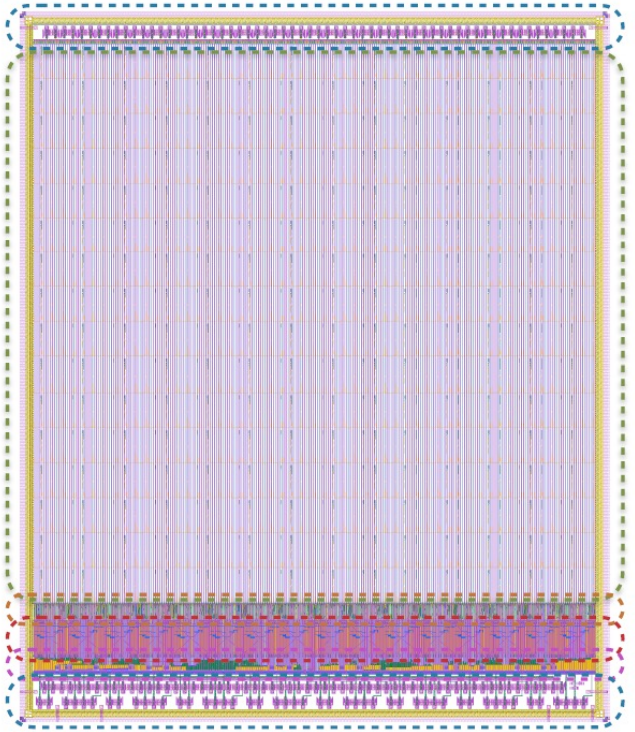
p+ wafers double epi

thinning to 100 or 300 µm total thickness



I. MD3 - chip architecture





top padframe (auxiliary supply)

matrix

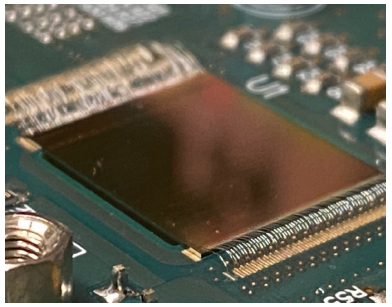
end of sector (reads & configure)

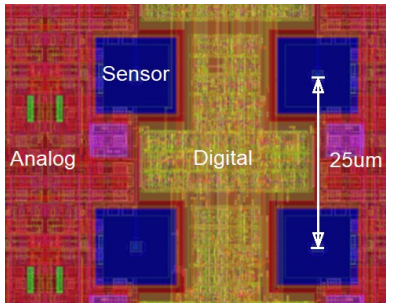
biasing

periphery

bottom padframe (stacked power and signal pads)

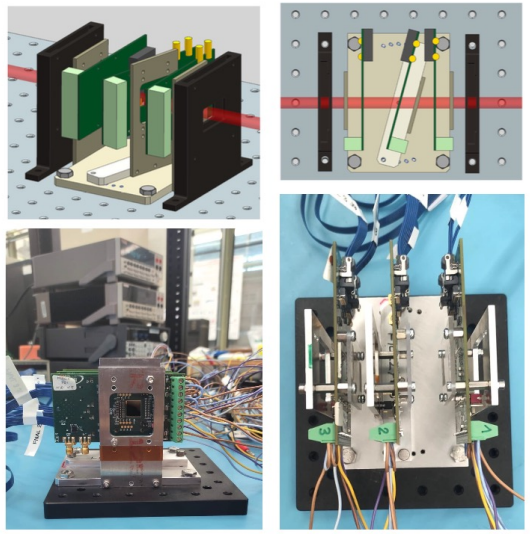
- Pixel **pitch**: **25 µm**
- Array core **area**: **1.28 cm × 1.28 cm** (262144 pixels)
- Electronics: **analog** and **digital**, with in-pixel **threshold** and **data storage**
- Architecture: **event-driven**, with active pixels sending their address to the chip peripheral circuits
- (Low) **power**: **10-30 mW/cm^2**
- (High) **event rate**: **100 MHz/cm^2**

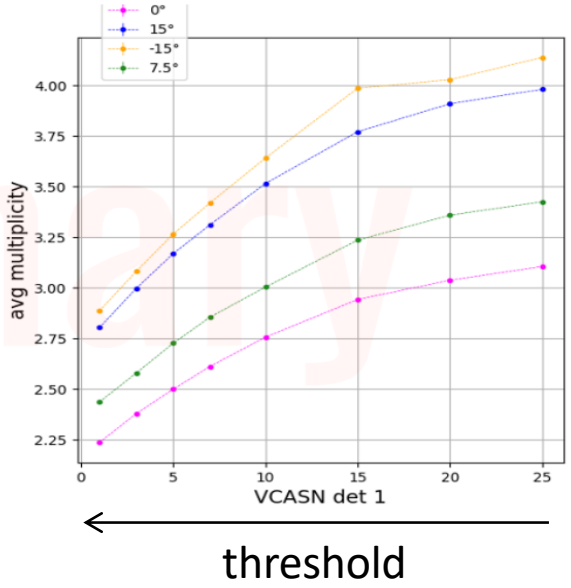


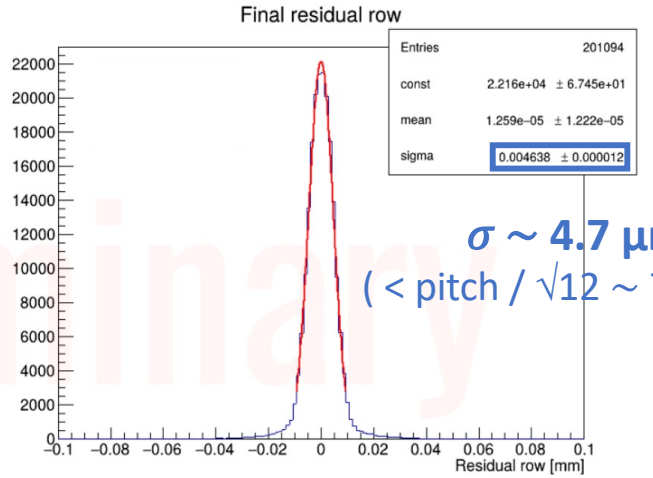


I. MD3 - testbeam @ FNAL

- 120 GeV protons
- Mini-telescope with three 200-µm-thick ARCADIA-MD3 sensors
- Threshold, sensor HV and incidence angle parametrisation: study of cluster size, collection efficiency, spatial resolution

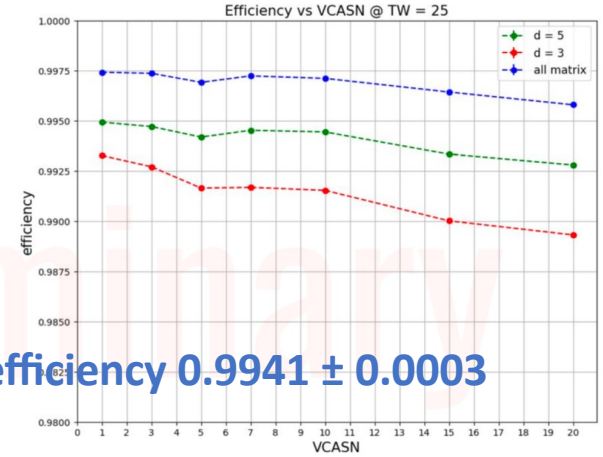






$\sigma \sim 4.7$ µm

(< pitch / √12 ~ 7.2 µm)



average efficiency 0.9941 ± 0.0003

Outline

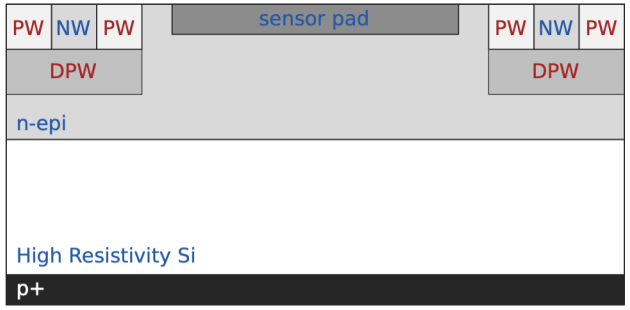
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   - Main Demonstrator – architecture and characterization

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   - sensors with resistive readout
   - CMOS-RSD development

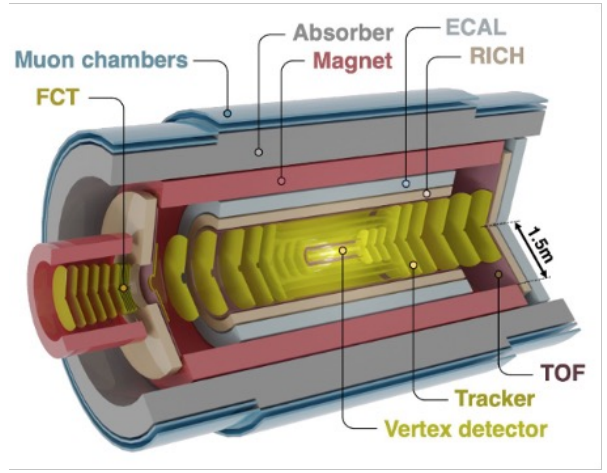
II. Timing: ARCADIA ER3

fully-depleted MAPS

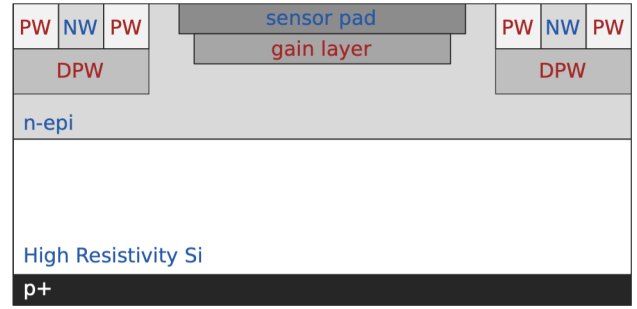


ALICE3 TOF detector:

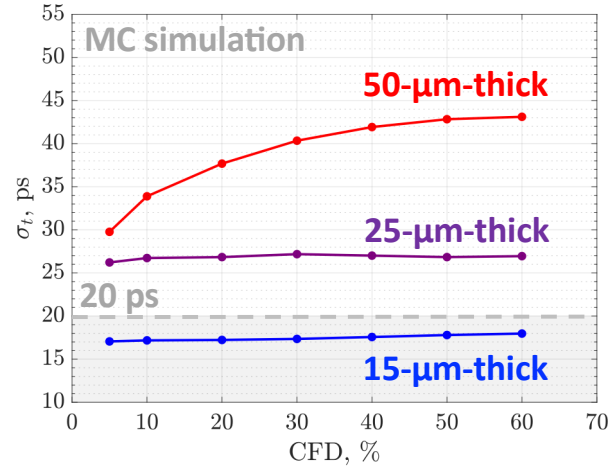
- high-resolution **tracking**
- **particle ID** at low $p_T \Rightarrow \sigma_t \sim$ **20 ps**



CMOS-LGAD

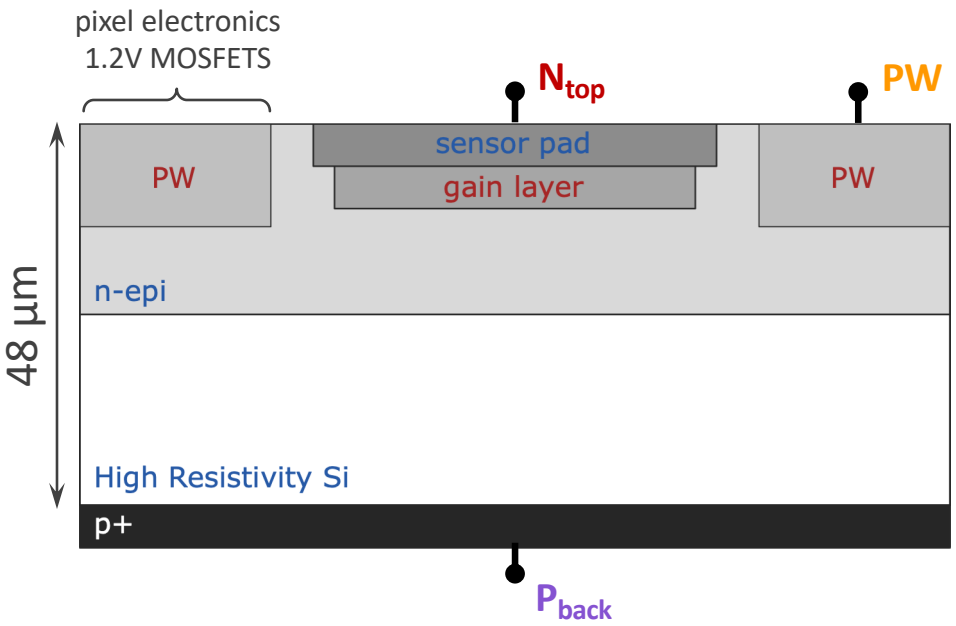


add-on ***p*-gain** implant
(**gain** target: **10 – 30**)

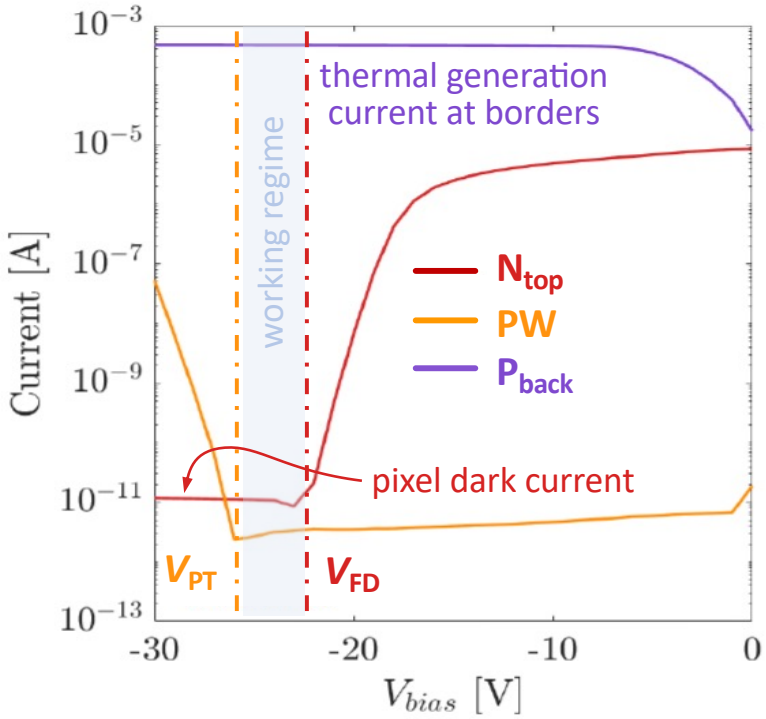


II. Timing: ARCADIA ER3

Sensor layout



Operation regime

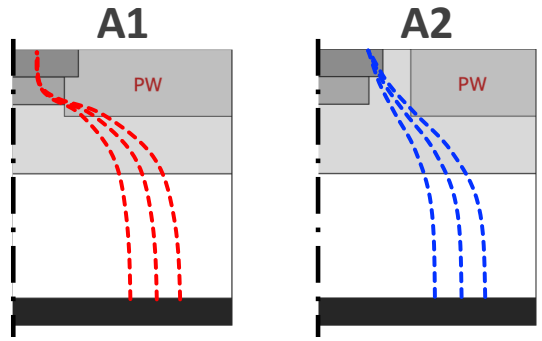


- **full-depletion** condition
- **punch-through** driven by the **backside bias**, which defines the **field** in the substrate
- **edge breakdown** (due to gain) induced by the **topside voltage**

Two border layouts

A1
pros: **uniform multiplication** (high FF)
cons: **delayed signals at periphery**

A2 (std.)
pros: **uniform response**
cons: **increased no-gain zone**



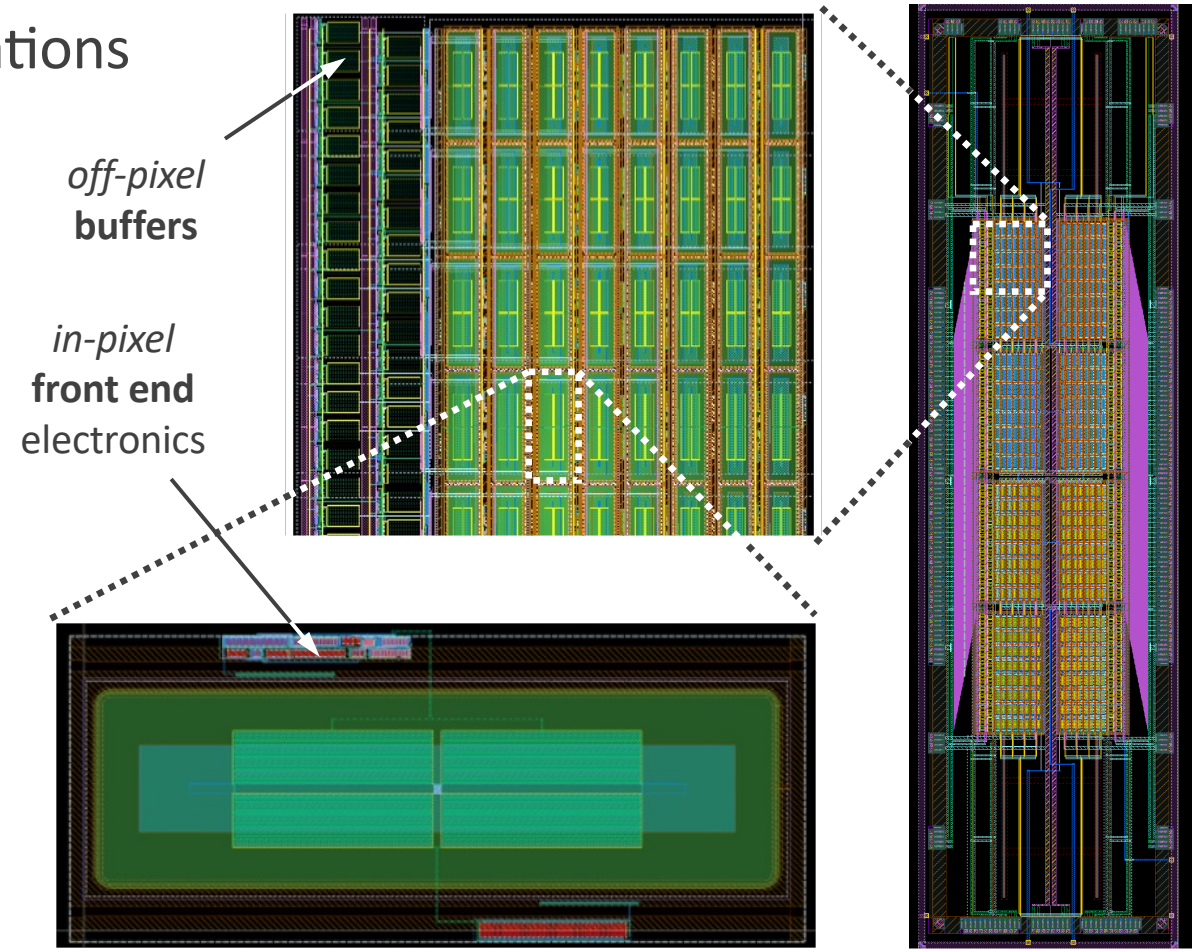
II. Timing: MADPIX architecture

MADPIX: **M**onolithic CMOS **A**valanche **D**etector **PIX**elated Prototype for ps Timing Applications

- **8 matrices** (**64 pixel pads** each) implementing different sensor and front-end flavors
- **250 × 100 µm²** pads
- readout: **64 analog outputs** on each side, **rolling shutter** of single matrix readout

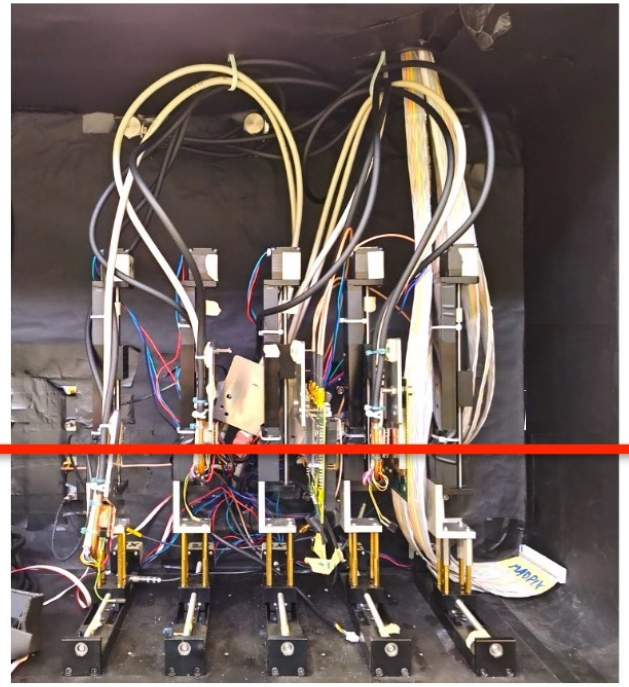
Front-end (*in-pixel*)
- **Cascoded common source** amplifier, followed by a **differential buffer** (1.2V)
- **AC-coupled** with **sensor** (to decouple it from V_{top})
- **Power** consumption: **0.18 mW/ch**

Source follower *off-pixel* **buffers** (3.3V)
- **AC-coupled** with **FE**
- **Power** consumption: **1.65 mW/ch**



II. Timing: MADPIX testbeam @ CERN

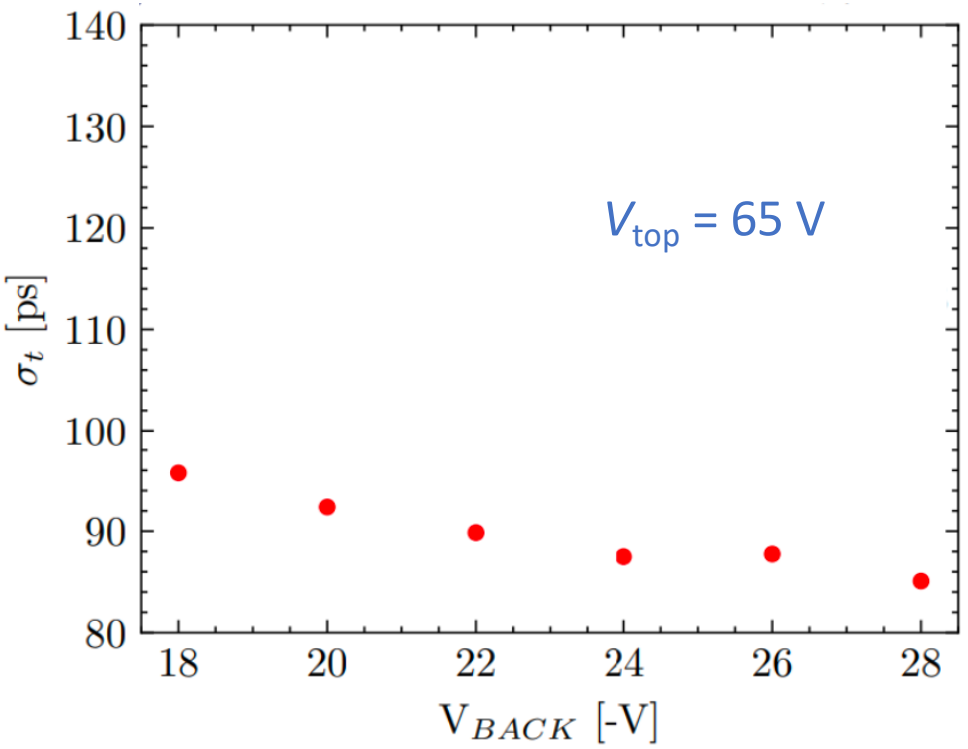
ALICE3 TOF testbeam @ CERN PS in October 2024
10 GeV pions/protons

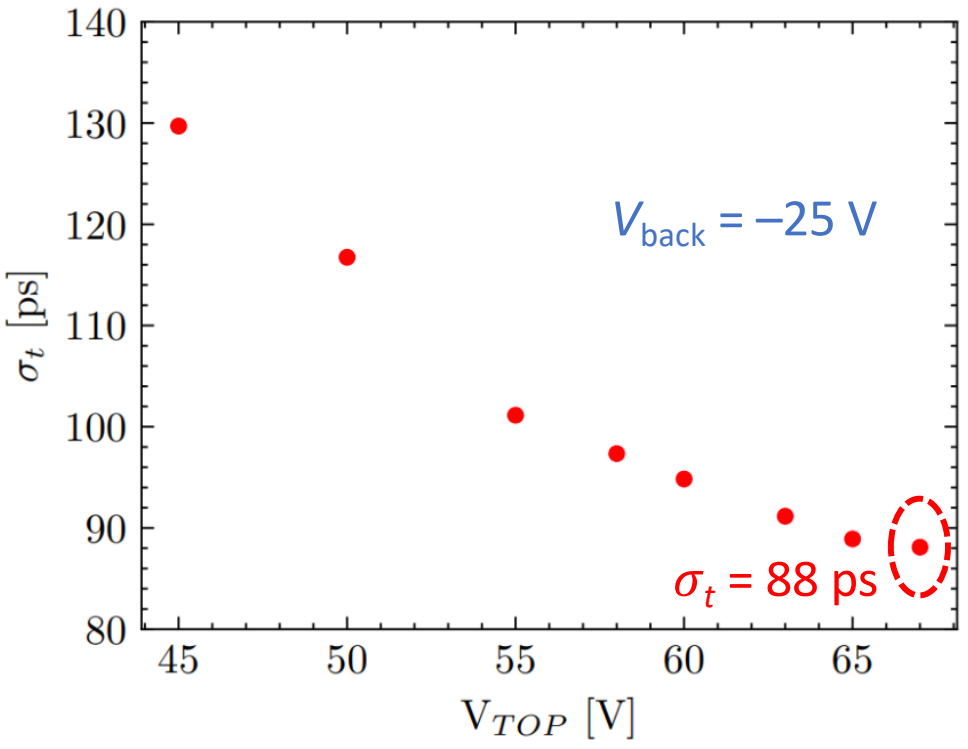




The ALICE3 TOF testbeam team:
M. Bregant, S. Bufalino, Z. Buthelezi, D. Cavazza, M. Colocci, C. Ferrero, U. Follo, J. Goodhead, S. Förtsch, G. Gioachin, M. Mandurrino, B. Sabiu, G. Souza, S. Strazzi, S. Wimberg

II. Timing: MADPIX testbeam @ CERN



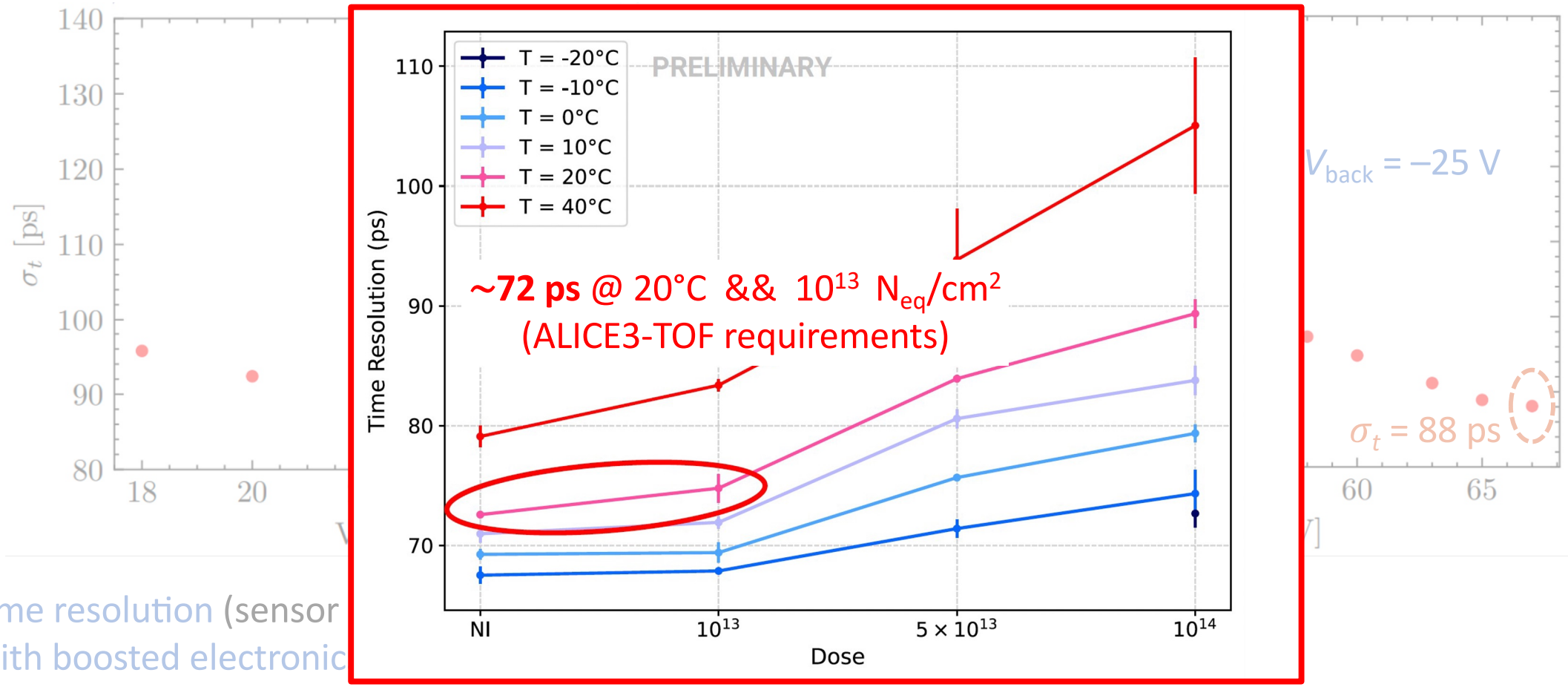


Time resolution (sensor + FE electronics) at V_{top} = 65 V and V_{back} = –25 V is σ_t = 88 ps

With boosted electronics: σ_t = 75 ps

Still not optimized substrate and geometry ⇒ improvements are expected

II. Timing: MADPIX testbeam @ CERN



Time resolution (sensor

With boosted electronic

Still not optimized substrate and geometry ⇒ improvements are expected

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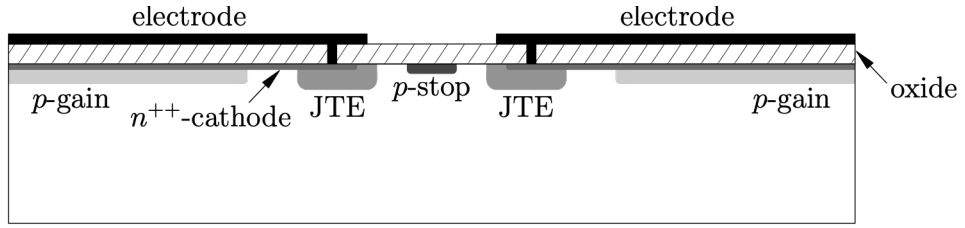
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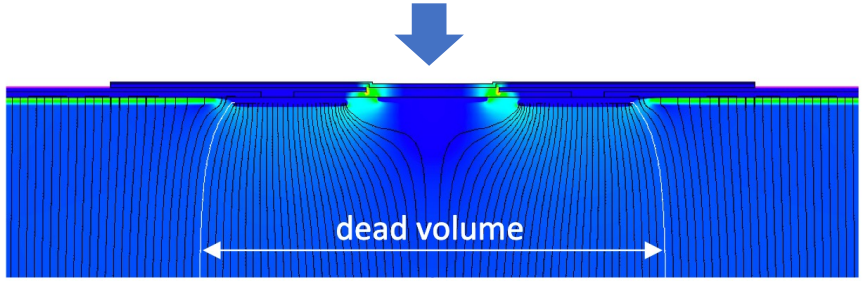
III. Technologies for 4D-tracking
   - sensors with resistive readout
   - CMOS-RSD development

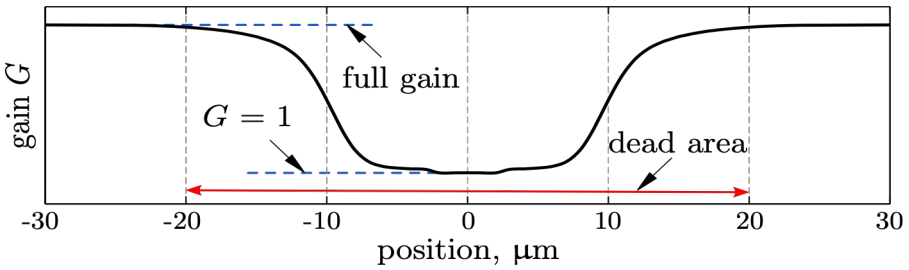
III. Sensors with resistive readout

Main goal: achieve 4D-tracking by increasing the geometrical efficiency

standard (segmented) LGAD





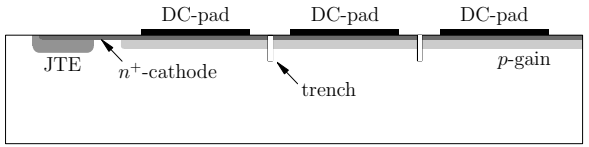


LGAD with resistive cathode (continuous collection)

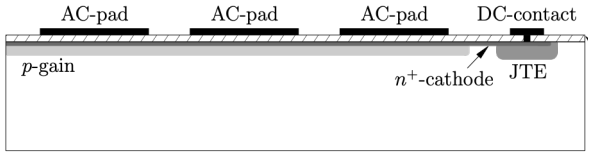


Possible readout schemes:

1. via collection ⇒ resistive DC-LGADs ⇒ FF < 100 %
2. via induction ⇒ RSD ⇒ FF ≡ 100 %



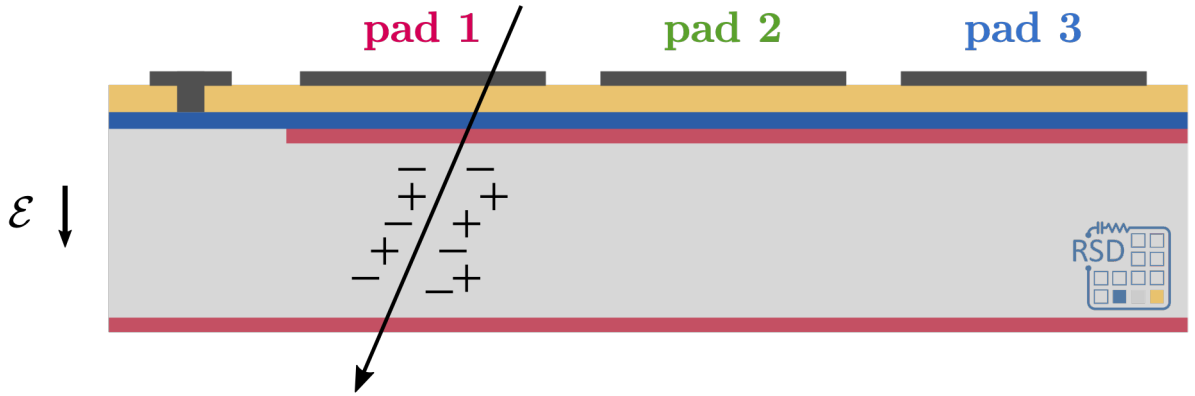
1.



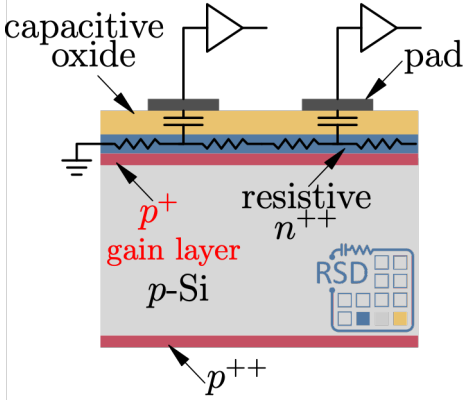
2.

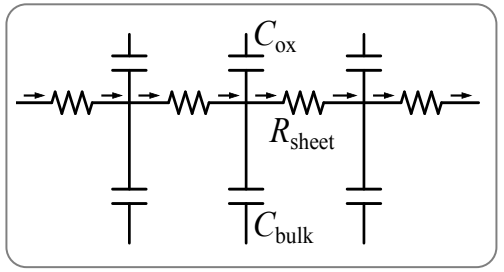
III. Resistive AC-Coupled Si Detectors

Resistive AC-Coupled Silicon Detectors (RSD)



- Developed at INFN Torino starting from late 2017 under the RSD Italian project
- First production (RSD1) in 2019 with FBK, with still cutting-edge performance [link]
- Second production (RSD2) in 2021, exploring optimized layouts [link]

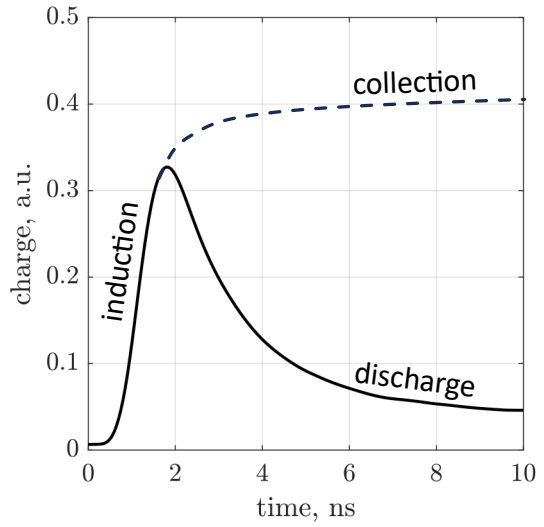


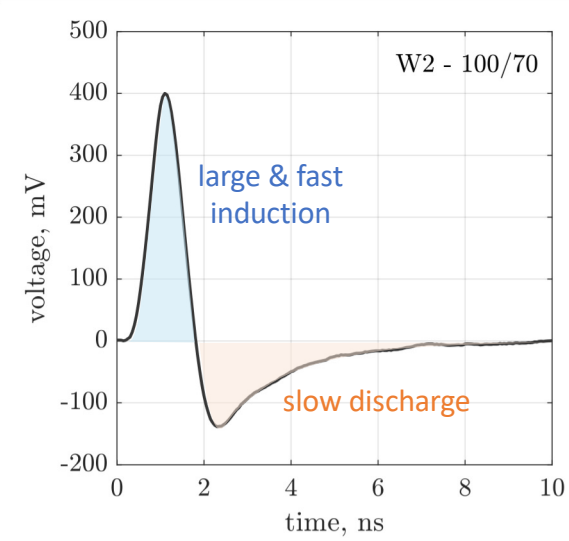


large (> 5 fC, gain 10–30) and fast signals (~ns)

⇩

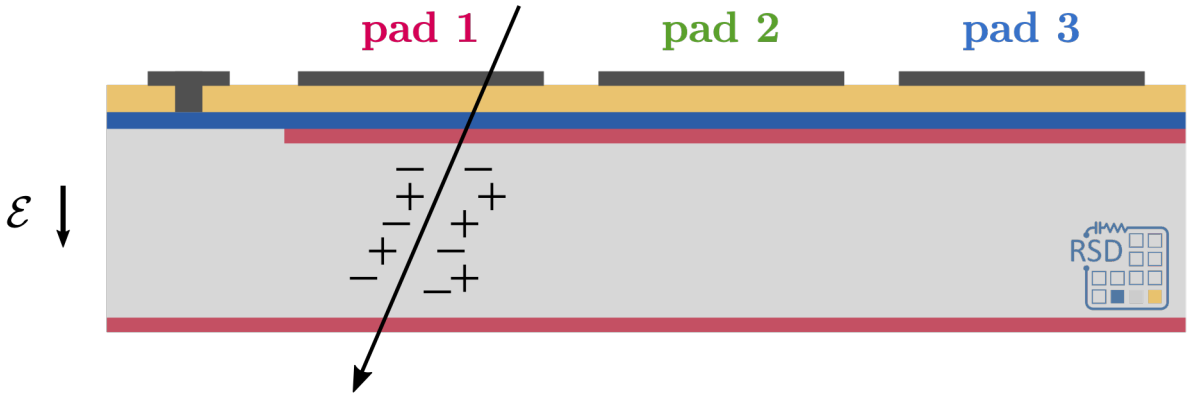
timing

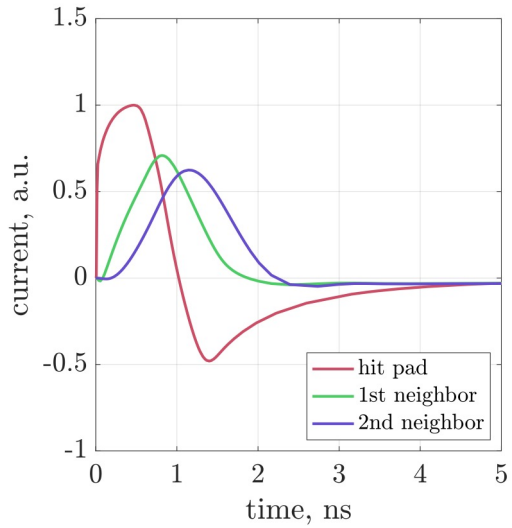




III. Resistive AC-Coupled Si Detectors

Resistive AC-Coupled Silicon Detectors (RSD)

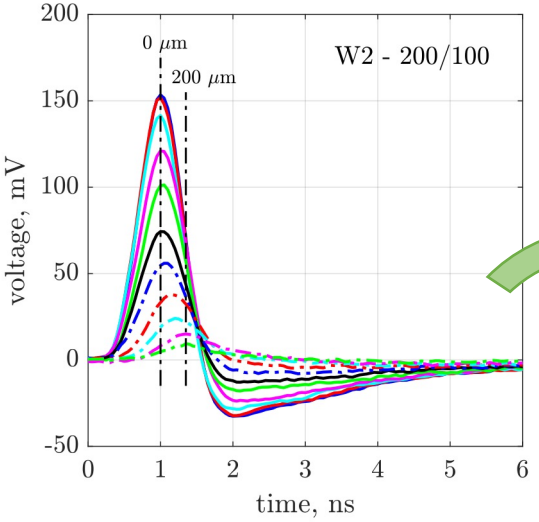


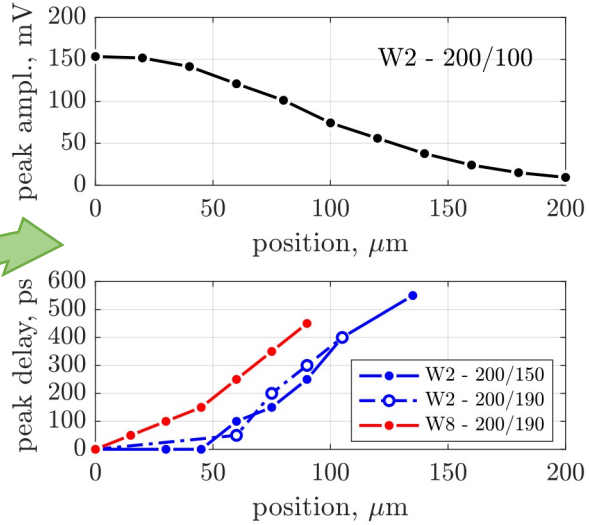


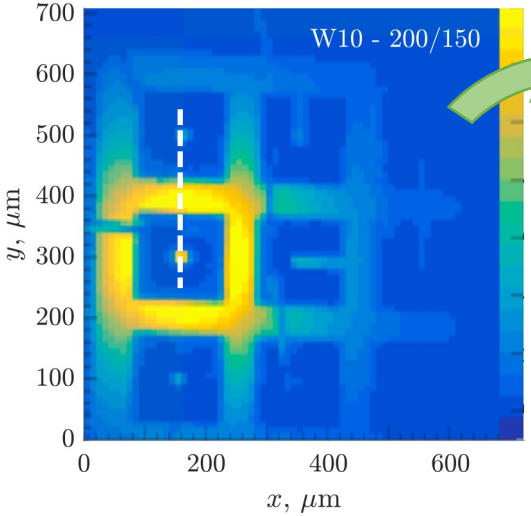
The continuous resistive cathode and the absence of segmentation are responsible for charge sharing

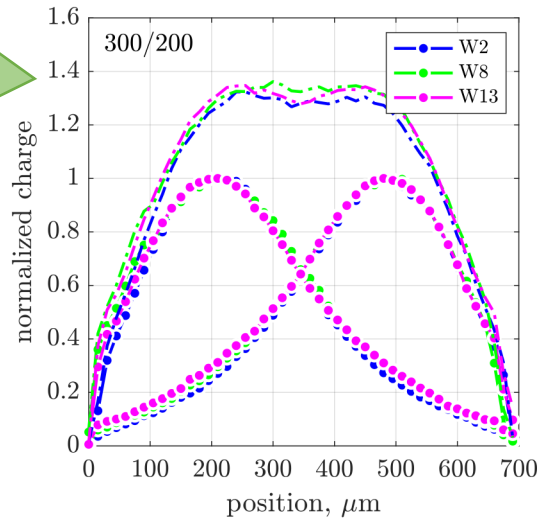
⇩

tracking, 100% FF





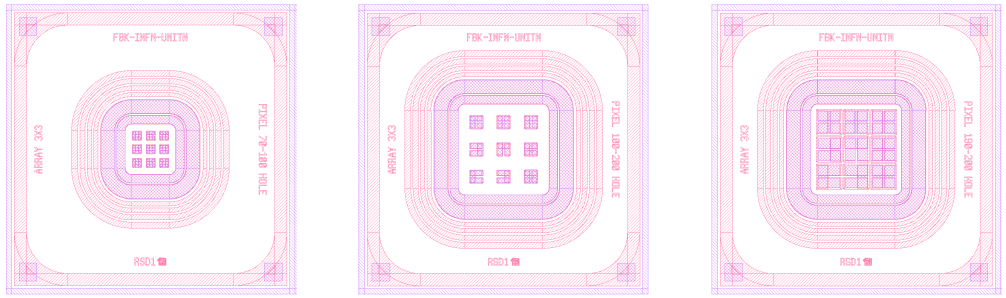




https://doi.org/10.1109/LED.2019.2943242
https://arxiv.org/abs/2003.04838

III. Resistive AC-Coupled Si Detectors

RSD1 (2019) production as a technology testbench of 4D-tracking



- AC-strip and AC-pad arrays
- different pad size and pitch (50- to 500-µm-pitch)
- *p*-gain and n^+ dose splittings
- 2 different dielectric thickness

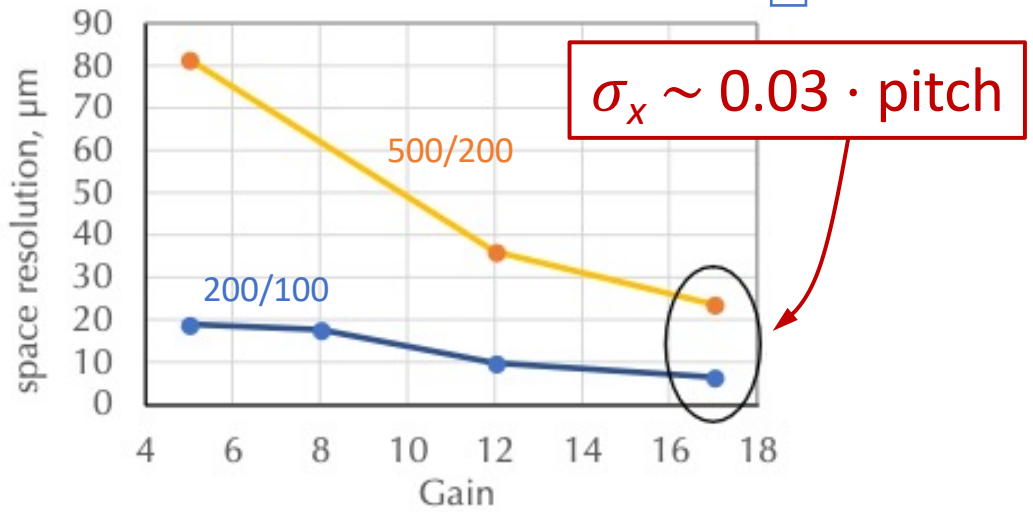
☛ micron-level and sub-20-ps 4D-resolution for smallest geometries and highest gain

RSD1	Gain 12		Gain 17		Gain 24	
	σ_x [µm]	σ_t [ps]	σ_x [µm]	σ_t [ps]	σ_x [µm]	σ_t [ps]
100/70	3.2	17.6	2.8	15.3	2.5	13.9
200/100	8.6	31.1	6.2	22.3	-	-
200/190	17.9	58.7	14.3	62.6	8.8	59.9
500/200	27.3	45.7	20.6	34.6	20.6	32.6

RSD pitch / pad size

4D-resolution depends on pad pitch and size

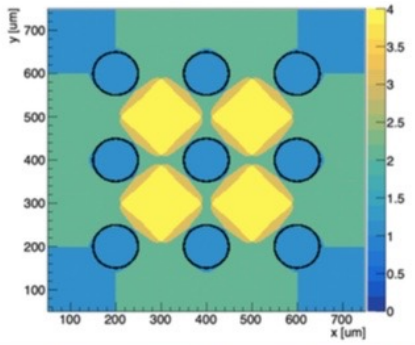
high-resolution @ low channel density



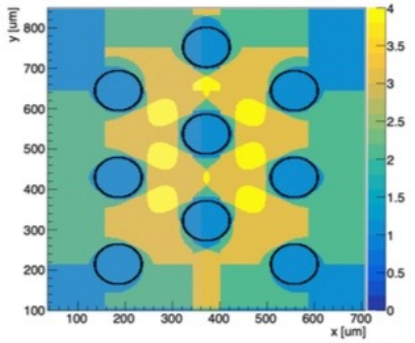
III. Resistive AC-Coupled Si Detectors

RSD2 (2021) production for signal readout optimization

Machine Learning prediction



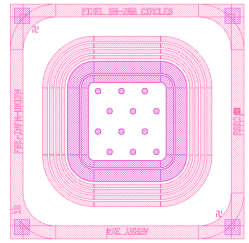
When signals spread over many pads, each one 'sees' a small fraction of the total charge



Optimized geometry (staggered layout) that minimizes the cluster size

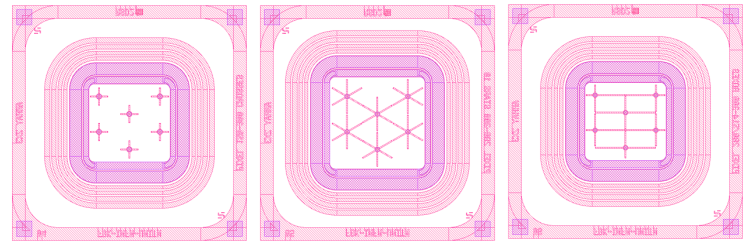
Signal confinement is also preferable to achieve homogeneous response

New array layouts



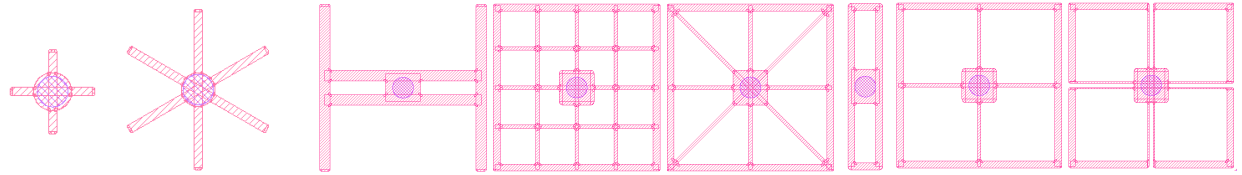
staggered

New pad geometries



rectangular triangular "*tight*" rectangular

New pad shapes*

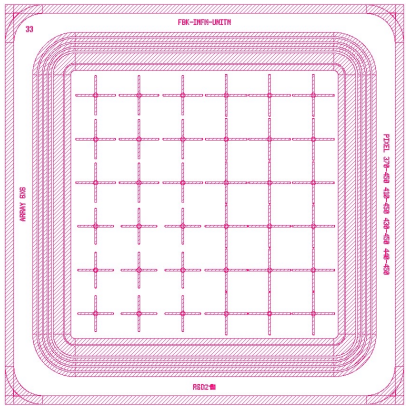


cross star 'cage'-like pads

*Protected by International Patent no. WO 2022/234403 A1

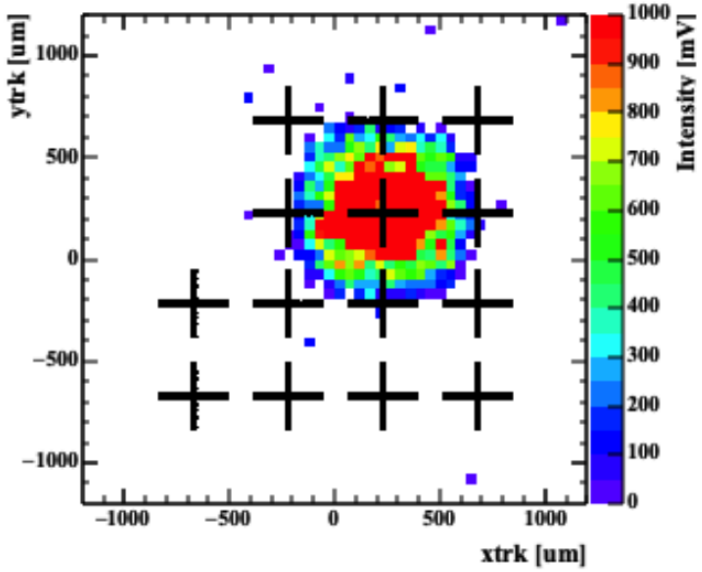
III. Resistive AC-Coupled Si Detectors

Testbeam (DESY) results of a 450-µm-pitch RSD2 with crosses



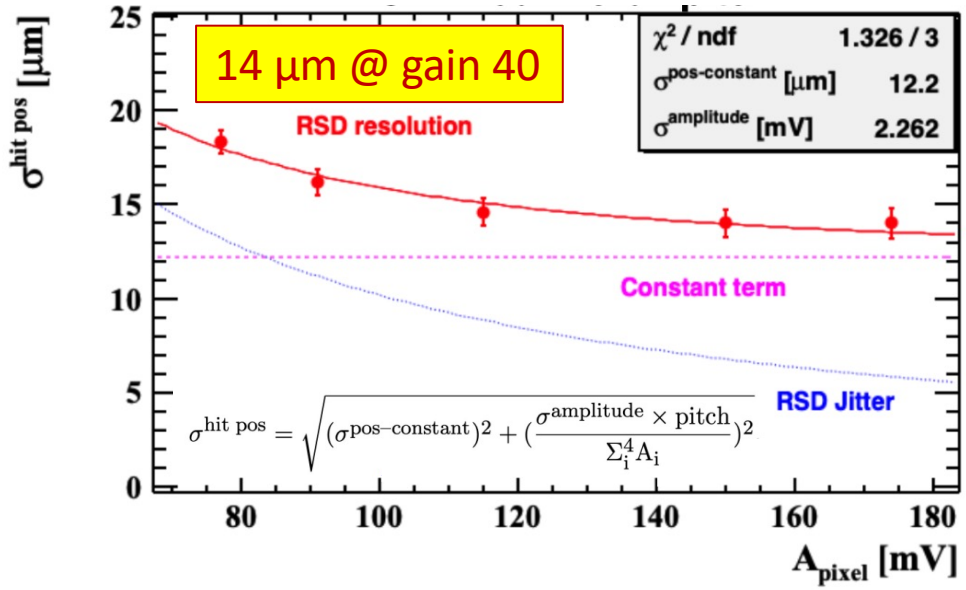
450-µm RSD2
+
16ch FAST2 ASIC
+
digitizer

Amplitude vs hit position



Signal sharing is confined within one pixel

Spatial resolution

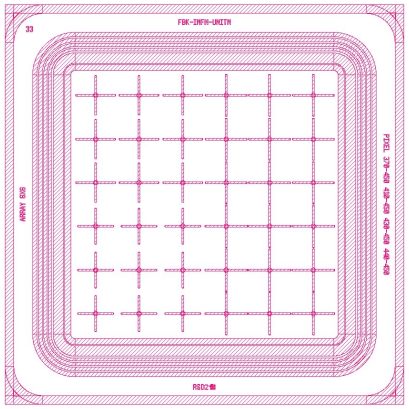


- Hit position reconstruction + correction
- Subtracted tracker resolution (8 µm)
- Constant term due to mis-alignments, non uniformities, etc…

Credits:
https://indico.cern.ch/event/1334364/contributions/5672082/
https://agenda.infn.it/event/40905/contributions/229518/

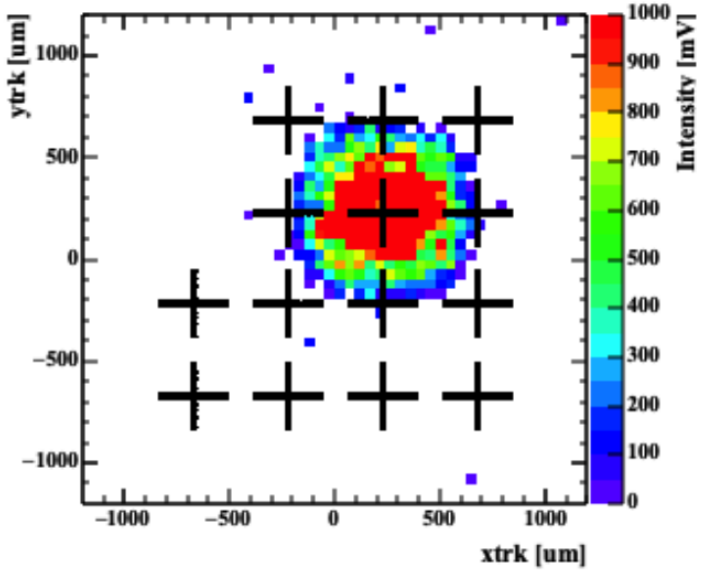
III. Resistive AC-Coupled Si Detectors

Testbench (DESY) results of a 450-µm-pitch RSD2 with crosses



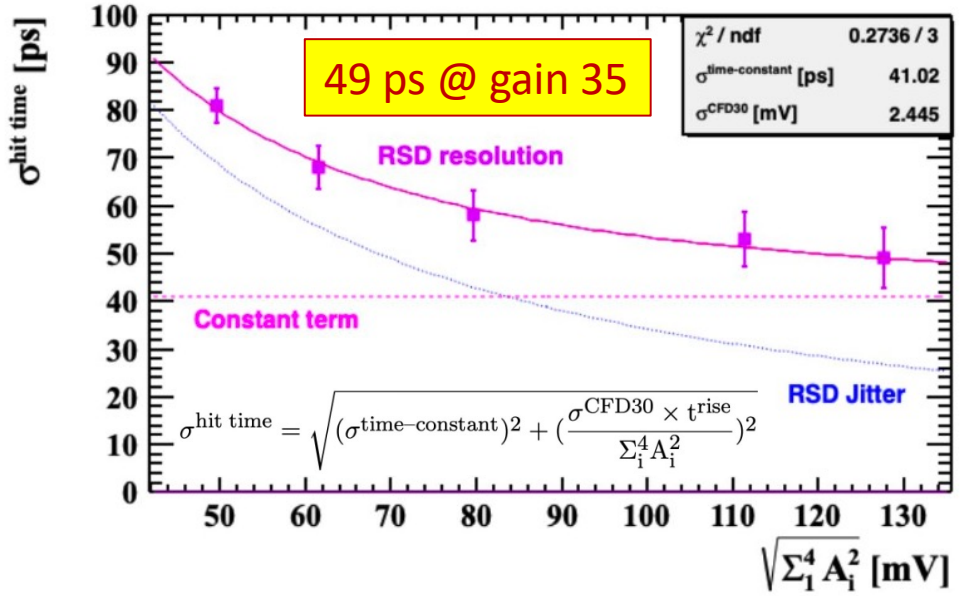
450-µm RSD2
+
16ch FAST2 ASIC
+
digitizer

Amplitude vs hit position



Signal sharing is confined within one pixel

Time resolution



- Hit position reconstruction + correction
- Subtracted reference resolution (38 µm)
- Constant term due to mis-alignments, non uniformities, etc…

Credits:
https://indico.cern.ch/event/1334364/contributions/5672082/
https://agenda.infn.it/event/40905/contributions/229518/

III. Monolithic CMOS-RSD

R&D for a Si-Wrapper with AC-LGADs

Detector requirements:

1. **high momentum resolution** through TOF measurement and extended tracking coverage
2. **large area** (~100 m^2)
3. **high efficiency** with high coverage of the acceptance area

The **IDEA** detector concept @ FCC

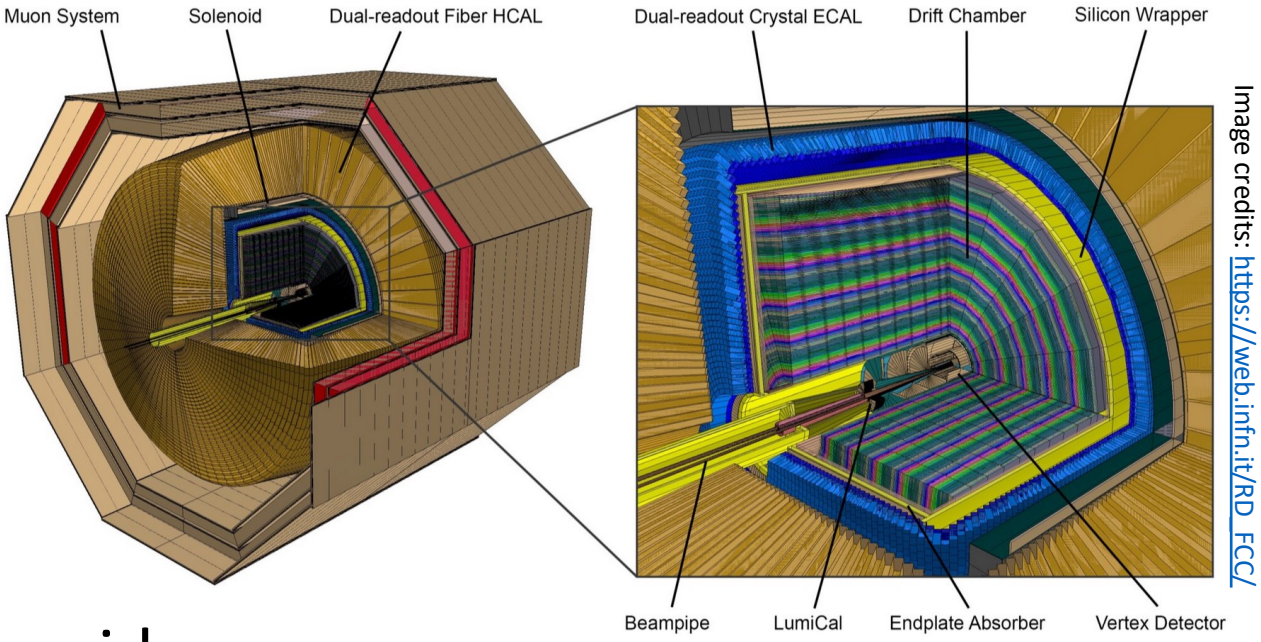


Image credits: https://web.infn.it/RD_FCC/

A good candidate technology should provide:

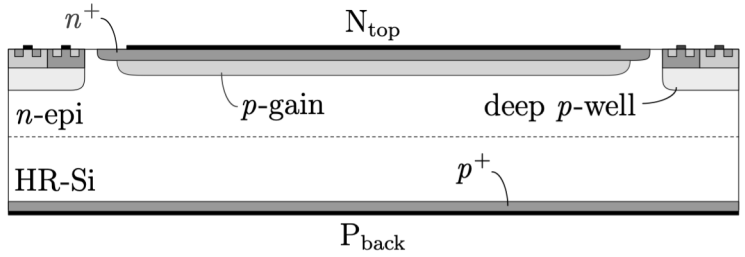
1. **4D tracking capabilities**
2. **monolithic integration** ⇒ **Monolithic CMOS AC-LGAD**
3. **high fill-factor**

III. Monolithic CMOS-RSD

To combine the RSD performance with the advantages of a monolithic integration, we started developing CMOS-RSDs

MAPS w/ gain

CMOS integration of the LGAD technology already demonstrated

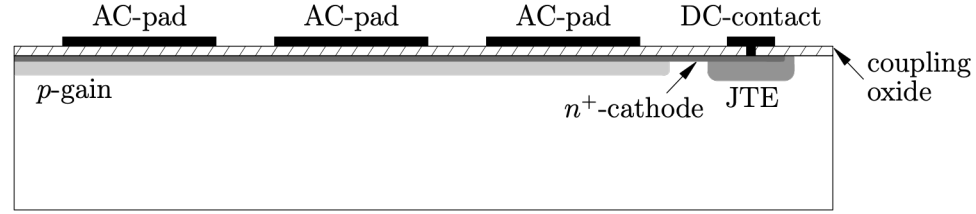


+

RSD

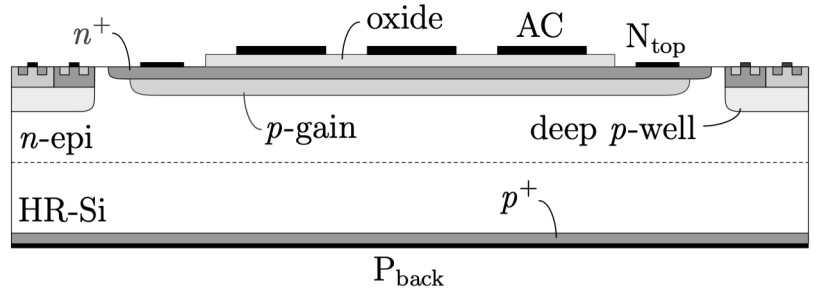
Spatial resolution **~3% of sensor pitch** (relaxed ch. density)

Time resolution similar to standard LGADs: **30-40 ps**



- 110 nm CMOS technology parameters
- µm-level spatial resolution
- 10-20 ps temporal resolution
- low power density (~10 mW/cm²)
- low material budget
- low cost per unit area
- scalable technology
- low complexity (w.r.t. std. integration)

CMOS-RSD



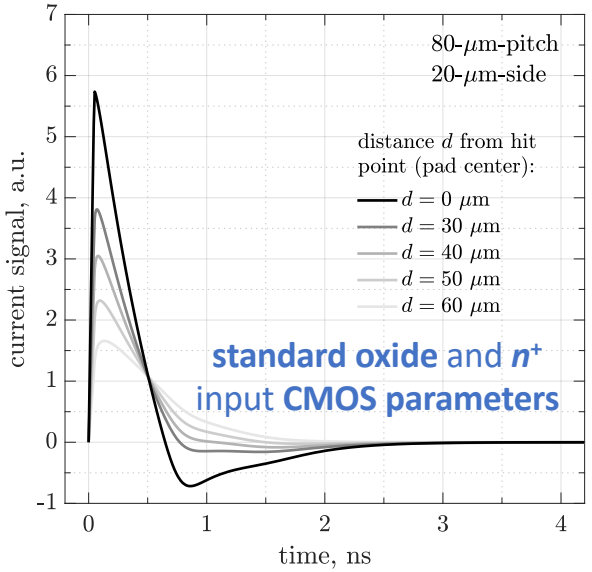
EP4654788A3 - methods and technology enabling the RSD embodiment into the standard CMOS process

III. Monolithic CMOS-RSD

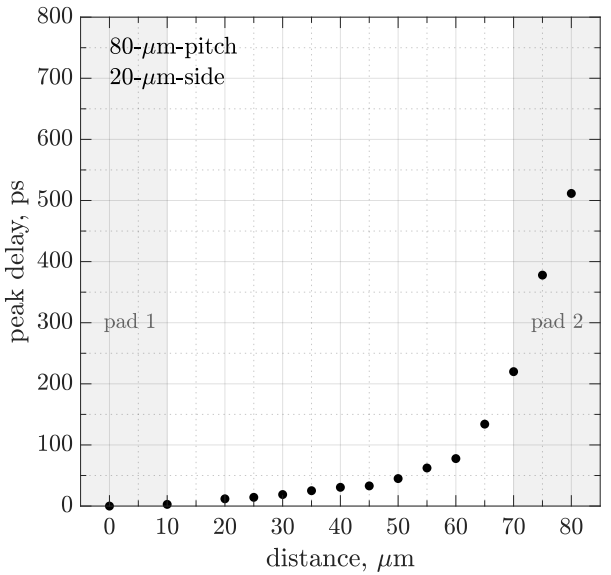
- As a second step, we have numerically proven that the RSD paradigm works within a standard CMOS platform like in the hybrid configuration

TCAD simulation of a **80**-µm-pitch / **20**-µm-pad **CMOS-RSD***

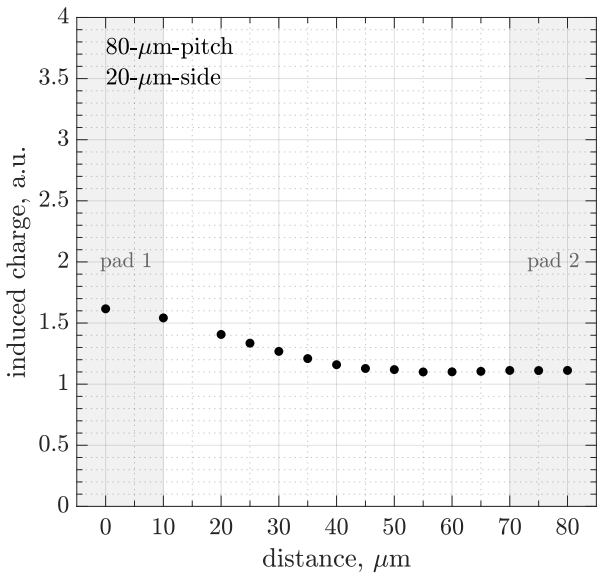
signals during a **MIP scan**



peak delay vs. **hit position**



induced charge vs. **hit position**



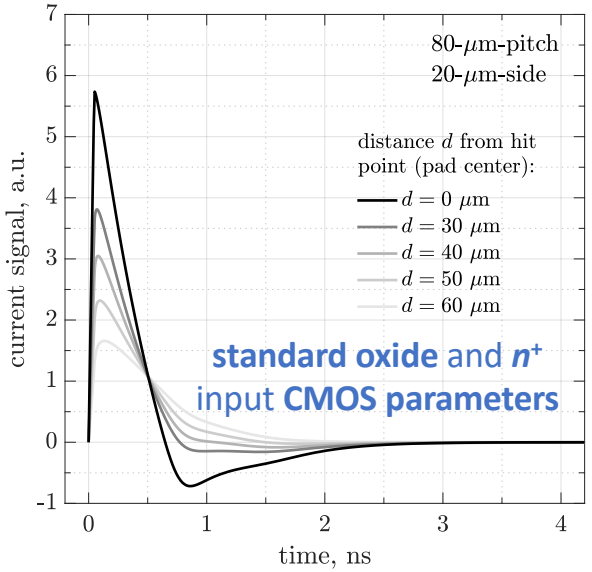
* see also: M. Mandurrino *et al.*, "Numerical Proof-of-Concept of Monolithic AC-LGAD Detectors for 4D Particle Tracking". *Sensors* **2025**, 25, 4185, https://doi.org/10.3390/s25134185

III. Monolithic CMOS-RSD

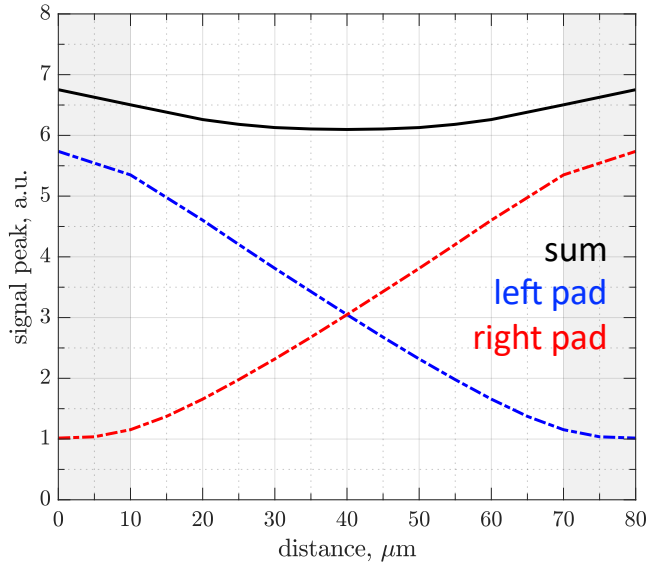
- As a second step, we have numerically proven that the RSD paradigm works within a standard CMOS platform like in the hybrid configuration

TCAD simulation of a **80**-µm-pitch / **20**-µm-pad **CMOS-RSD***

signals during a **MIP scan**



signal amplitude vs. **hit position**



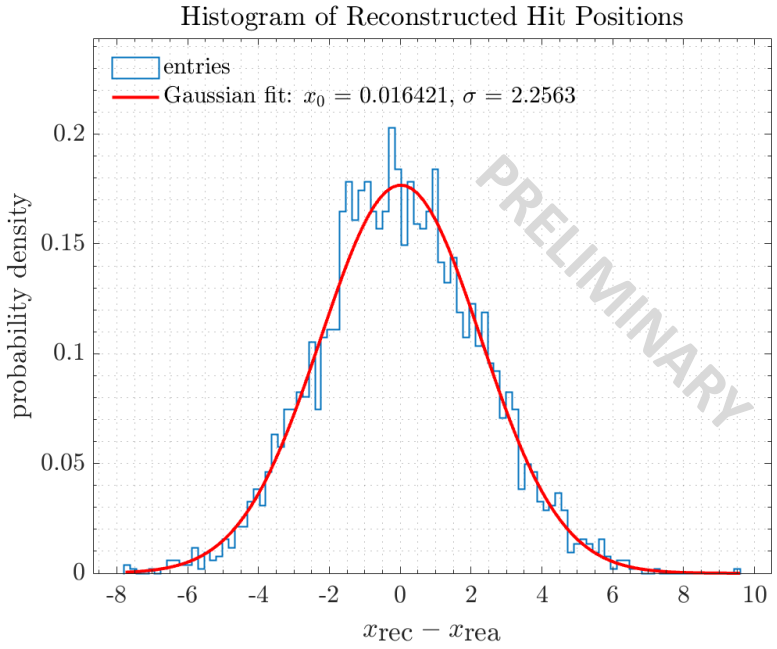
The sum of two adjacent electrode amplitudes (or charge) is quite constant

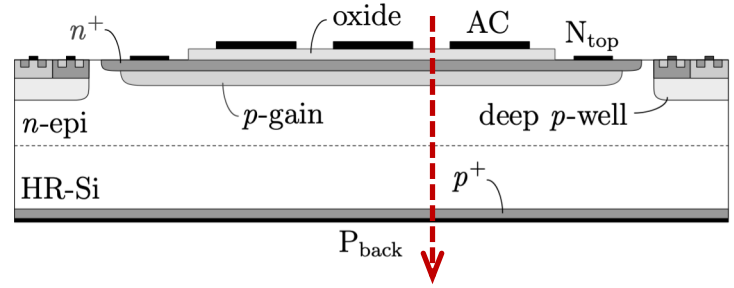
100% FF

* see also: M. Mandurrino *et al.*, "Numerical Proof-of-Concept of Monolithic AC-LGAD Detectors for 4D Particle Tracking". *Sensors* **2025**, 25, 4185, https://doi.org/10.3390/s25134185

III. Monolithic CMOS-RSD

- Now we are working on the design of the layout parameters to be implemented in a first engineering run (within ~1 year)
- Much effort is currently being spent on realistic Monte Carlo simulations to extract detailed figures of merit in terms of 4D-tracking





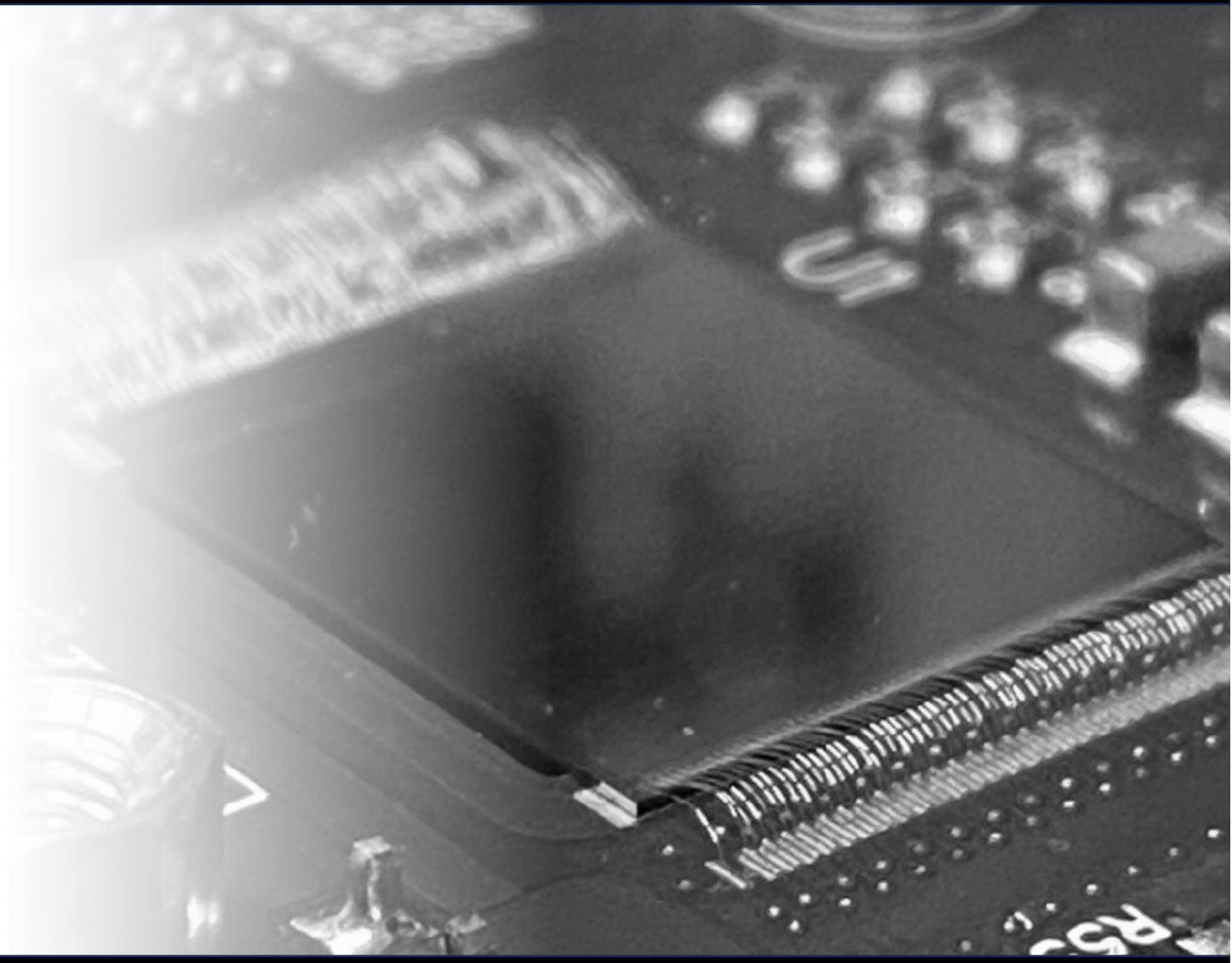
- MIP impinging at fixed position
- MC generation of some kevents
- simple centroid reconstruction w/o correcting for distortions
- difference between reconstructed position and hit coordinate
- spatial resolution: σ_x = 2.25 µm (~2.8% of the pitch)

Next steps…
1. time resolution estimation
2. technological parameters optimization
3. sensor layout design in view of the first ER

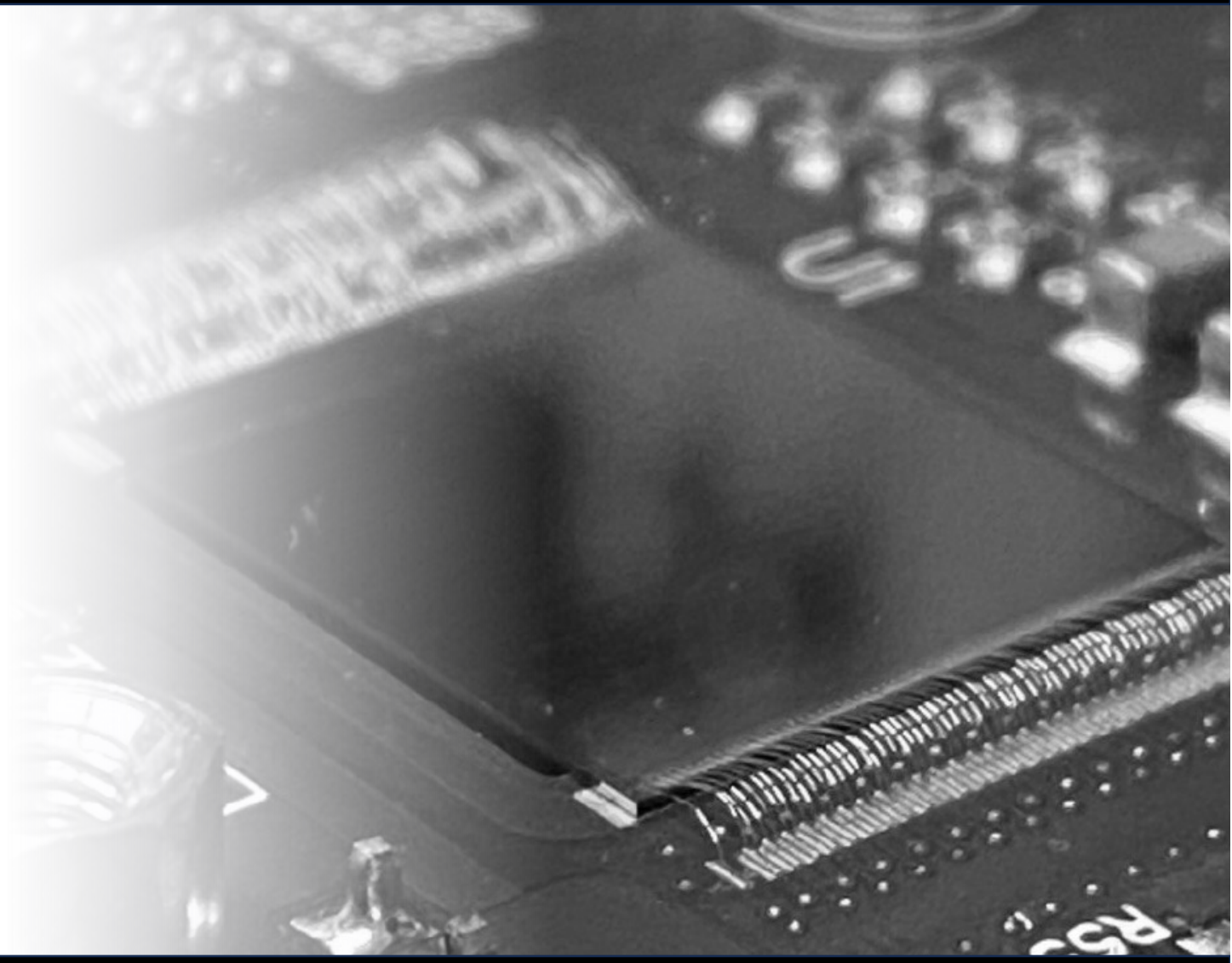
Status and Perspectives

- ARCADIA development with LFoundry 11is
  - INFN platform for R&D in fully-depleted monolithic CMOS sensor technology, IP and ASIC design, DAQ
  - Low-power sensor architectures (10 mW/cm²) for charged particle detectors
  - Innovative monolithic CMOS sensors with gain layer (CMOS-LGAD)
  - MAPS technology for tracking and timing systems in future lepton colliders
  - Time-of-flight detector for ALICE3: ARCADIA CMOS-LGAD is the baseline option for the ALICE3 TOF
- CMOS-RSD (Monolithic CMOS Resistive AC-Coupled Silicon Detectors)
  - High temporal resolution (~20-40 ps) and radiation-hardness like std. LGADs
  - Excellent spatial resolution: units to few tens of µm
  - 100% fill-factor
  - Low channel density required ($\sigma_x \sim 0.03 \cdot$ pitch)
  - Charge induction: suitable for low to moderate occupancy (tiny pads with very-fine pitch) environments
  - Same properties of standard RSDs
  - Advantages of monolithic integration: low-power, low-cost per area, low material budget, low complexity
- Ongoing and financed programs and projects
  - Funding available towards system-grade chips for FCC and sensor tapeout for ALICE3 TOF
  - Full-scale design for a new detector for space applications: SPW engineering run on thick (~700 µm) FZ wafers
  - ARCADIA LF11is FD-MAPS technology support through DRD7.6a
  - Funding request for CMOS-RSD development

Thank you for the attention!

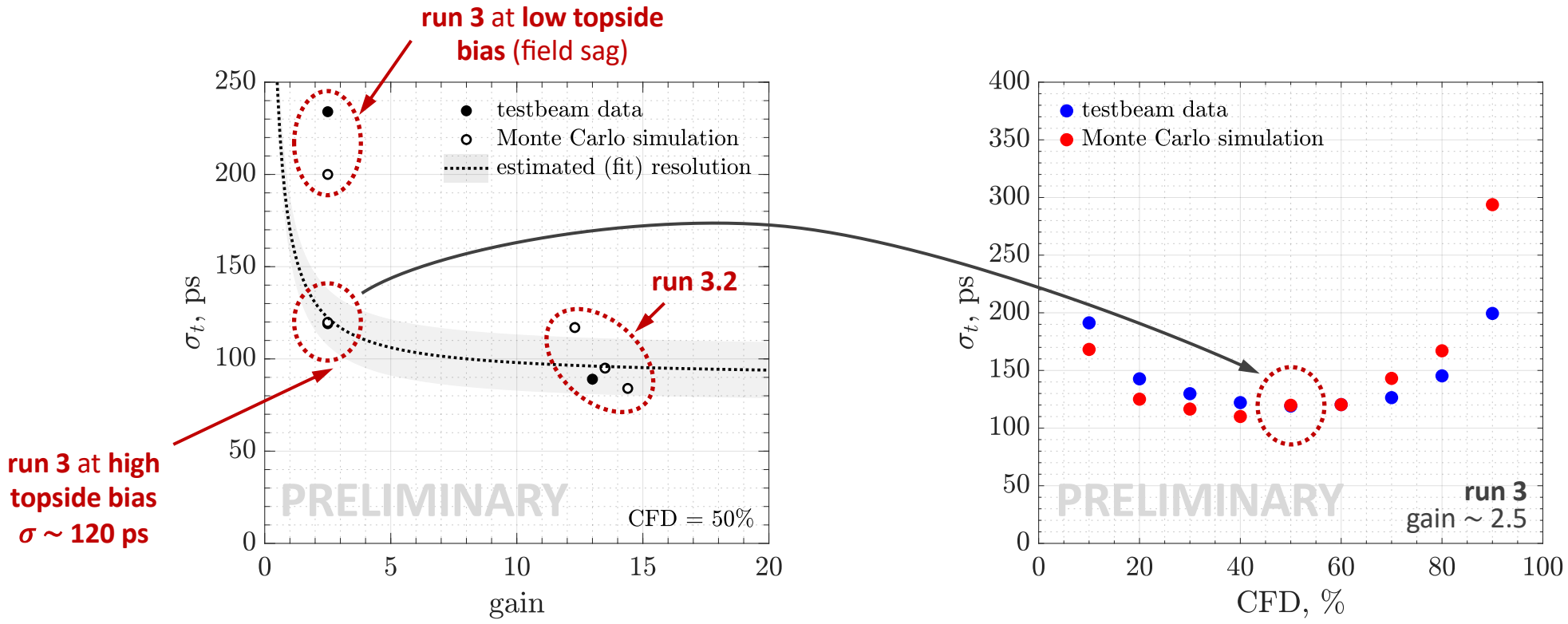


backup



MADPIX time resolution

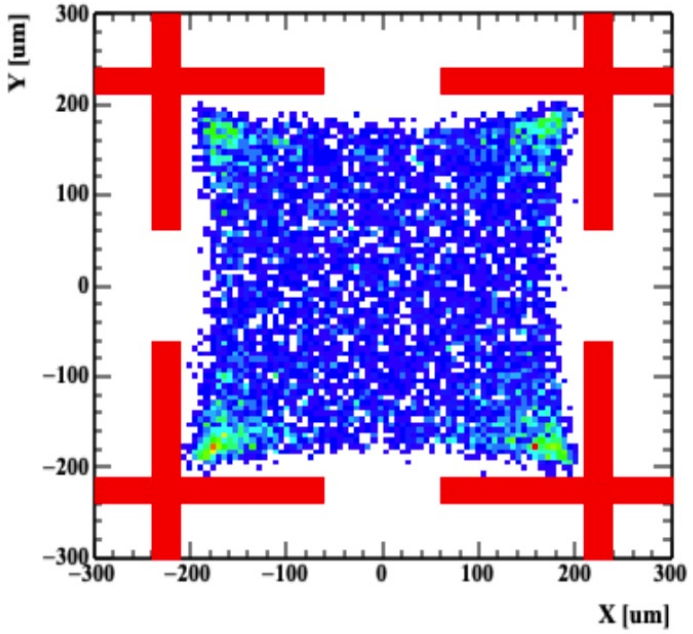
Comparison between Monte Carlo numerical predictions and on-beam measurements



Pincushion effect in a resistive net

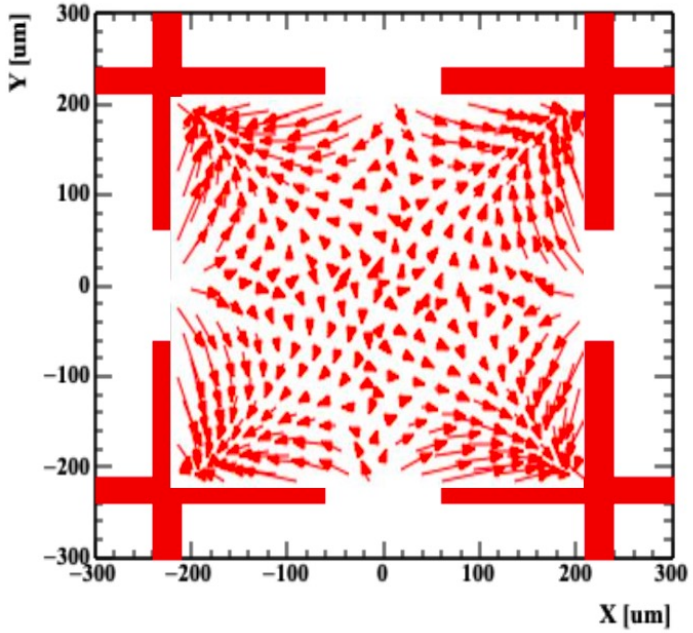
Laser scan over an RSD sensor with cross-shaped pads

2D map of charges



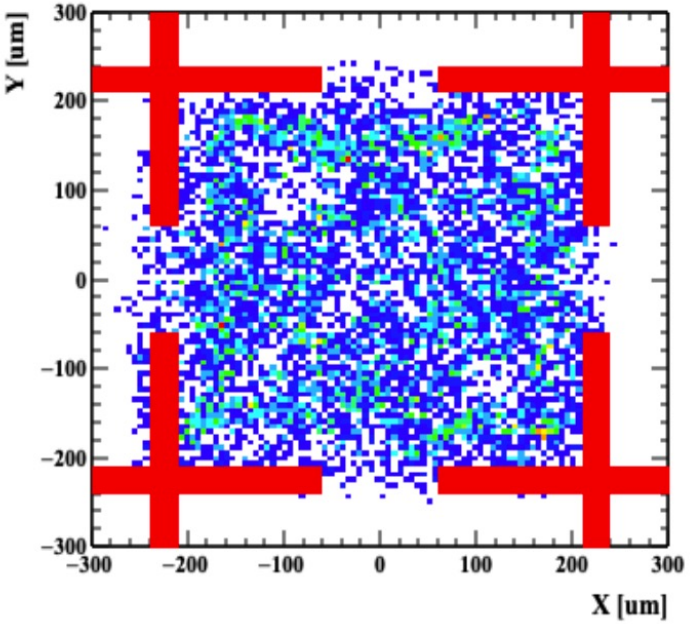
charge-weighted position centroid

Migration map



imbalance compensation algorithm

Corrected reconstruction map



centroid + compensation

Possible implementations are: look-up tables (depend on the sensor under test) or run-time correction (no pre-calibration required - any device)