

Overview and Status of the AGORA Electronics System

Ye, Jingbo

On behalf of the Agora electronics study team

中国科学院高能物理研究所
Institute of High Energy Physics
Chinese Academy of Sciences

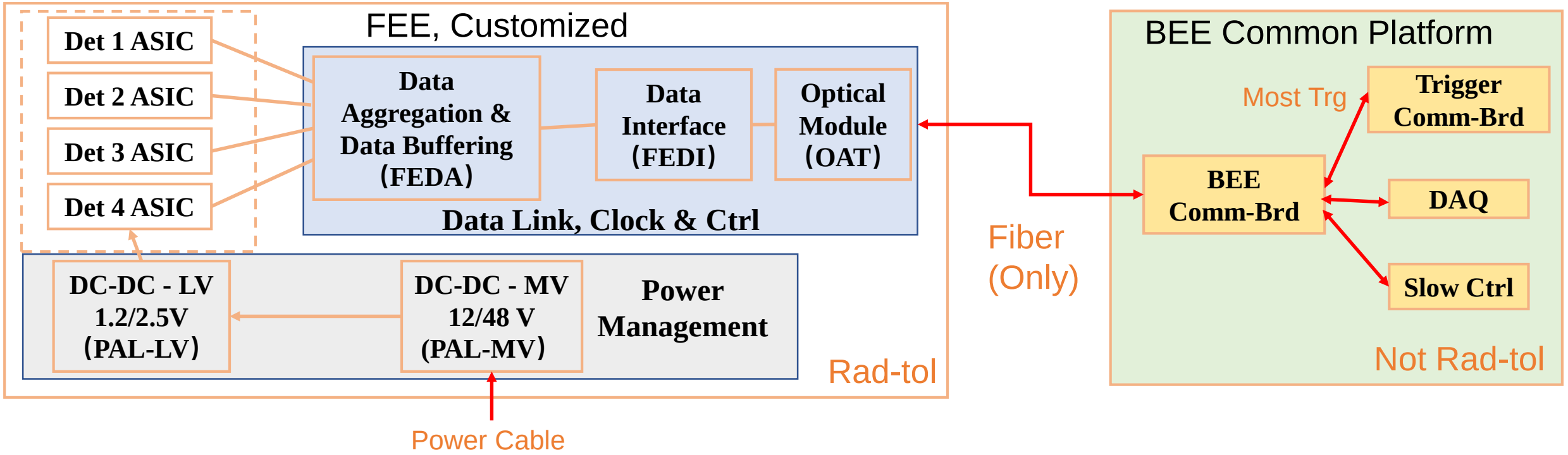
Content

- From the CEPC Reference Detector to AGORA
- The unchanged top-level electronics block diagram
- The progressing and changing details
  - TEPIX for the TPC
  - LATRIC for the OTK
  - SIPAC3 for the full glass calorimeter
  - Progress in the detector data interface: FEDI
  - The powering, GaN based BUCK, and a novel serial powering scheme
  - Although not in the AGORA readout baseline, wireless data & clock transmission is pressing ahead
- To be continued/expected

From Ref.Det to AGORA

- CEPC Ref.Det TDR has been published in RDTM: Advance online publication. DOI: 10.3724/rdtm-2026-0001.
- Detector R&D, electronics included, continue, with a name of the detector now chosen to be the Advanced Glass Optimized Research Apparatus, or AGORA.
- The top-level AGORA readout diagram is the same as in the Ref.Det TDR for the moment, with details in subsystems start to improve or to change.

The top-level electronics block diagram



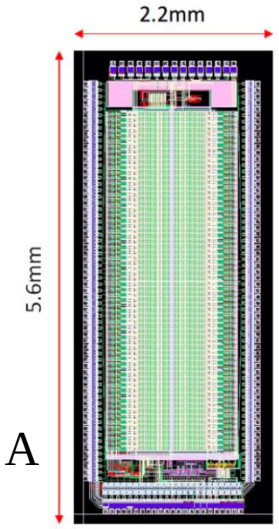
- Common detector data interface: FEDA, FEDI, OAT, and powering
- Rad-tol ASICs for the on-det electronics
- A common BEE hardware, configurable for individual subsystems ← not much progress since the last CEPCWS
- TDAQ interface is (probably) only on BEE

The progressing and changed details

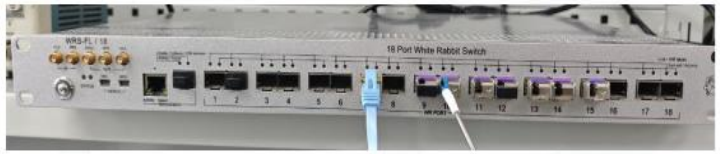
- TEPIX for the TPC
- LATRIC for the OTK
- SIPAC3 for the full glass calorimeter
- Progress in the detector data interface: FEDI
- The powering, GaN based BUCK, and a novel serial powering scheme
- Progress in wireless data & clock transmission

Prototype of the high granularity readout ASIC: TEPIX v1

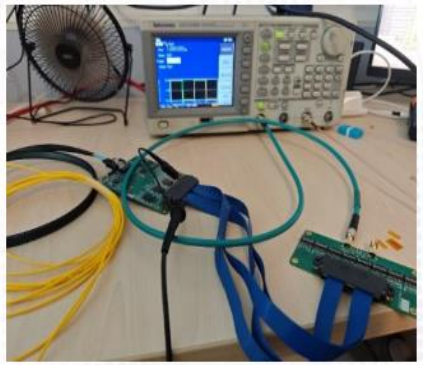
- High granularity readout Electronics: TEPIX v1
  - Charge-sensitive preamplifier
  - Correlated double sampling shaper
  - 4-channel sample/hold circuits and 10 bit ADC
  - 128 channels using 180 nm process
  - Chip size: 2.2 mm × 5.6 mm
- A total of 40 chip-in-package devices were commissioned. A full-readout Micromegas detector has been developed.



Total number of channels	30 Million per endplate
Pixel size	500 μm × 500 μm
Equivalent Noise Charge (ENC)	100 e^-
Dynamic range	20 fC
Charge buffer dynamic range	8-10 bit
Event rate	12 kHz/cm^2 max. in low-lumi. Z mode
Event size	64 bit
Readout bandwidth	<10 Gbps per module with compression
Power consumption	<100 mW/cm^2



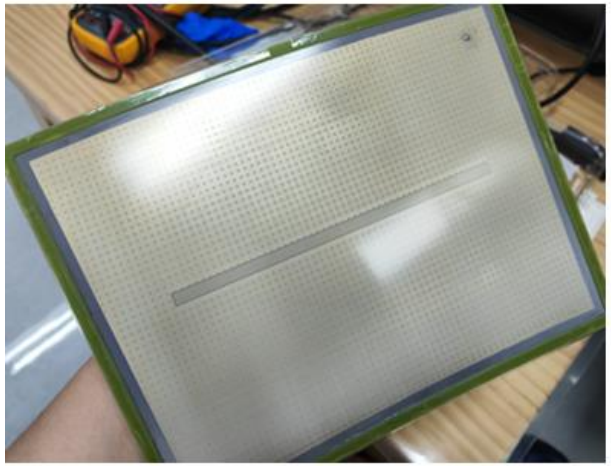


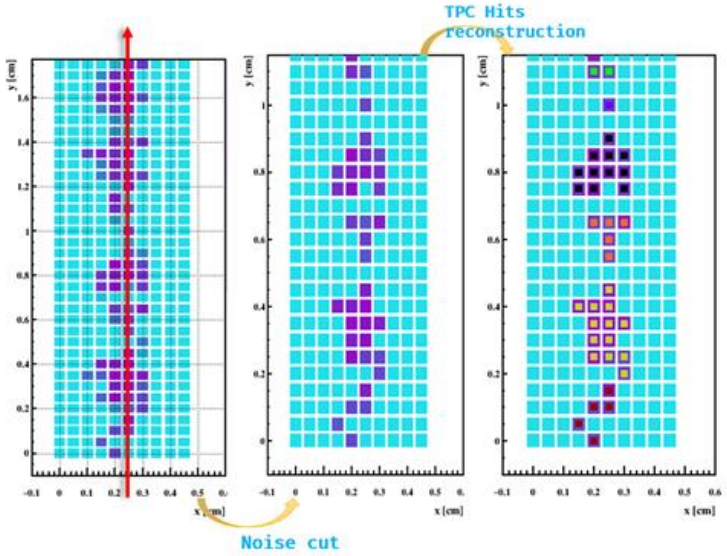




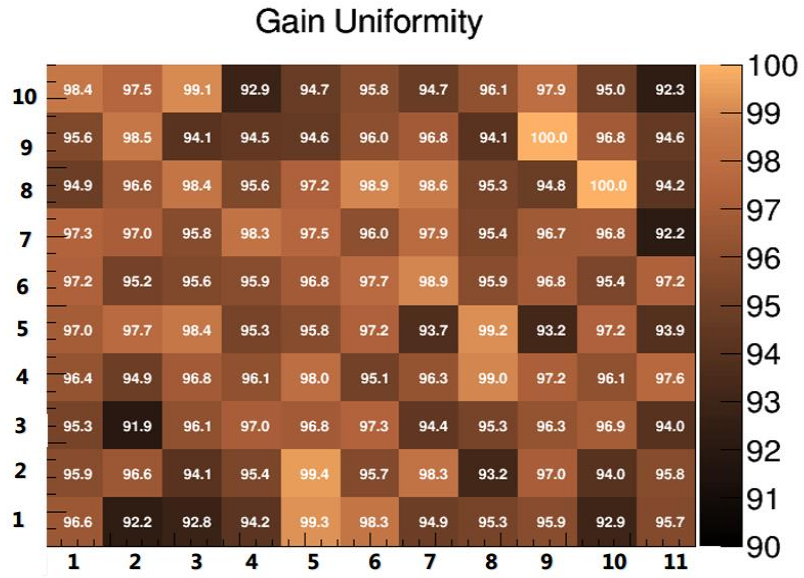
Progress of the high granularity readout detector R&D

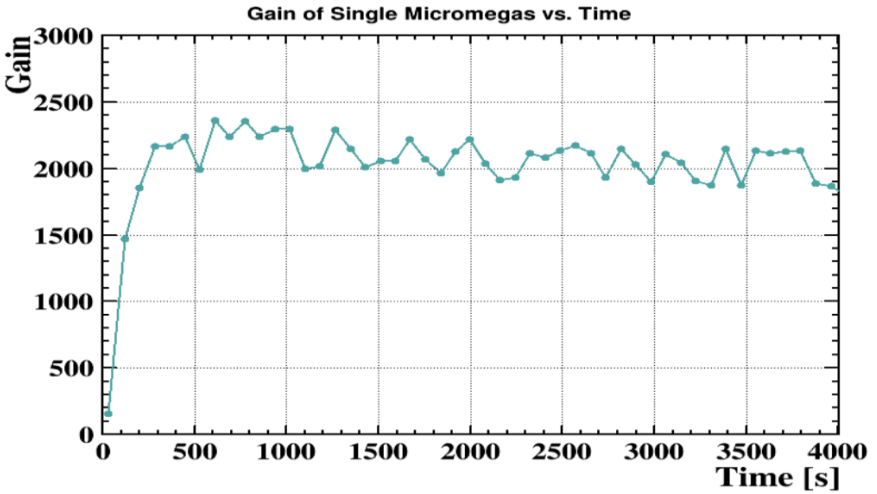
- **The Micromegas detector integrated with the readout chip has been successfully developed.**
- The detector operates at a gain of 2000–3000, exhibiting good gain uniformity Detector with the DAQ system is currently under joint commissioning.
- Based on Garfield++, KalTest and a pixel-type TPC simulation framework
  - Offline data-processing code developed
  - Time-stamp misalignment across multiple channels





Detector integrated with the high granularity readout with event displayer (simulate data)





Gain and gain uniformity of the detector

The progressing details

- LATRIC for the OTK

  The tests of LATRIC1 (the 4-channel prototype ASIC) with LGAD-strip are on-going, identifying a few issues that are being worked on, for example a noise level increase only when the ASIC is wire-bonded to the LGAD-strip.

  With this I would like to point out that although the R&D on ASICs has been slowing down a bit, people profit from it by carrying out very careful evaluations of the prototypes in hand.

The changing details

- SIPAC3 for the full glass calorimeter – please see Huaishen's talk in the morning for previous versions.
  - This is the ASIC that is recently putting back on fast track thanks to the progress in the glass scintillators.
  - The current thinking is a full-glass calorimeter (ECAL & HCAL). To be in-line with the very aggressive detector R&D schedule, we floor the gas-pedal again on SIPAC, a SIPAC3 focusing on the glass ECAL and HCAL.
  - We plan to tape out SIPAC3 (MPW) January 2027, with an engineering run in mind end of 2027 to produce enough chips for the module0 ECAL and HCAL for beam tests.

The progressing details

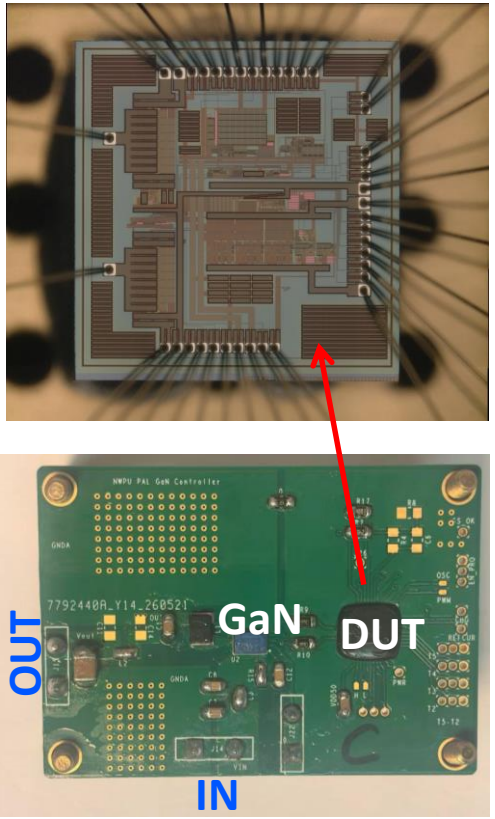
- Progress in the detector data interface: FEDA, FEDI and OAT
  - The 1st prototype of data aggregator FEDA has been successfully tested and reported in the last CEPCWS. It is awaiting FEDI to be tested in the full chain.
  - The 1st prototype with most of the circuit blocks of FEDI was taped out in July 2026. The chips are coming back in about 3 weeks. People are active in preparing for the tests.
  - OAT, the optical module with the driver and receiver ASICs, is under development. The plan is to test it with FEDI, once its electric functions are verified.

The progressing and changing details

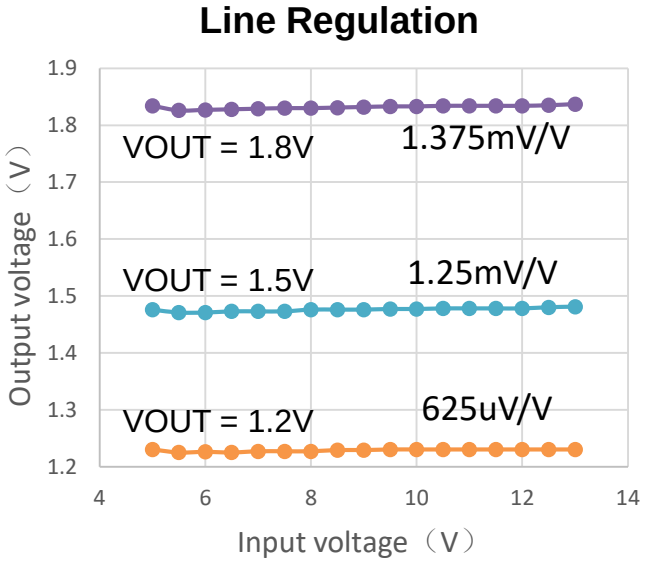
- The powering, GaN based BUCK, and a novel serial powering scheme. The later was reported in details this morning. I will not repeat that here. The former, the GaN based BUCK, is also making progress.
- For the progress in wireless data & clock transmission, please see Hu Jun’s talk this afternoon.

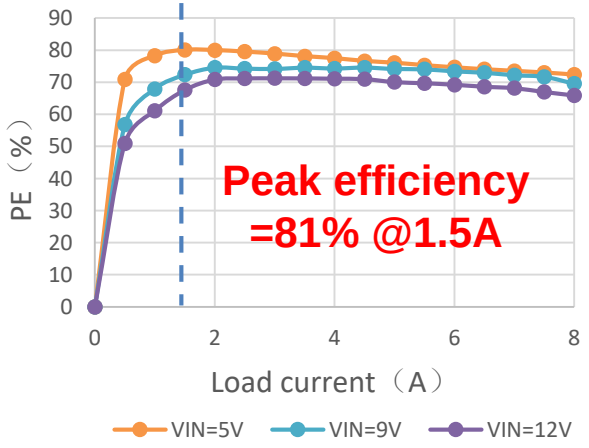
GaN DC DC Converter

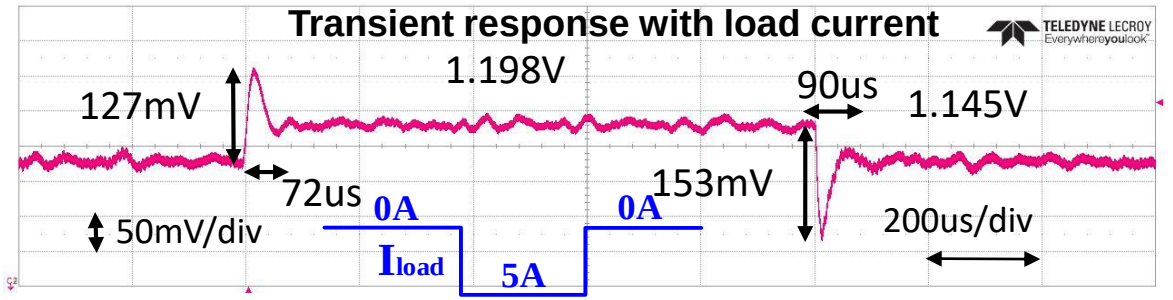
Measurement Results

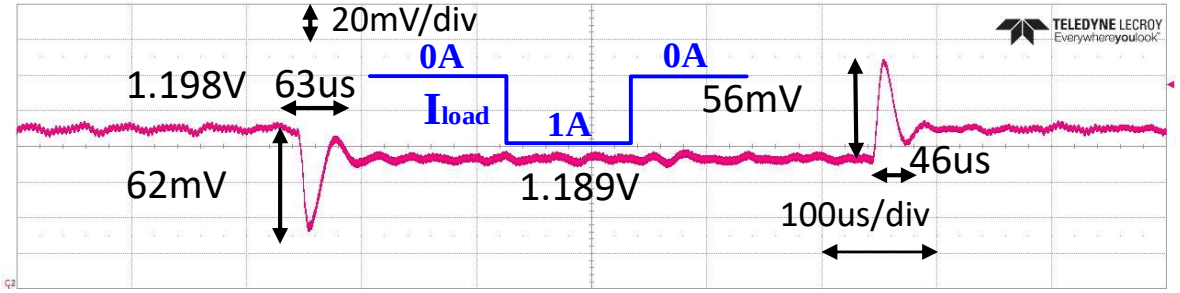


The tests were performed on a commercial GaN power stage paired with the designed controller. The system works well.









Measured Performance Parameters Summary

Parameter	Value
Process	180 nm
Input voltage	5-12 V
Output voltage	1.2-1.8 V
Power efficiency	70%@2A
Overshoot (SR=1A/us)	127 mV @5A
Undershoot (SR=1A/us)	153 mV @5A

To be continued/expected

- On the ASIC side: SIPAC3 and its performance in the beam tests.
- On the testing side: LATRIC with LGAD-strip, FEDI
- On the system side: TEPIX in the TPC, the FEDI based data interface, powering the modules
- Disclaimer: sensor developments for the VTX and the ITK, to me, belong to detector R&D, so I did not include them here. If I missed out any other things, that only demonstrates my ignorance, and I apologize.

Thank you!

We invite you to publish in RDTM:

Radiation detection Technology and Methods

Springer Nature

Founded By

Institute of High Energy Physics, Chinese Academy of Sciences

Chinese Nuclear Society (Nuclear Electronics & Detection Techniques Div.)

Publication

Published by **Springer Nature** • Frequency: **Bi-monthly**

Journal Scope

- Detection technology & methods
- Electronics & system design
- Computer technology applications
- Synchrotron-radiation techniques
- Particle acceleration technology
- Astroparticle technology
- Imaging and radiology



INDEXED BY

ESCI | Scopus | INSPEC

CONTACT

RDTM@ihep.ac.cn

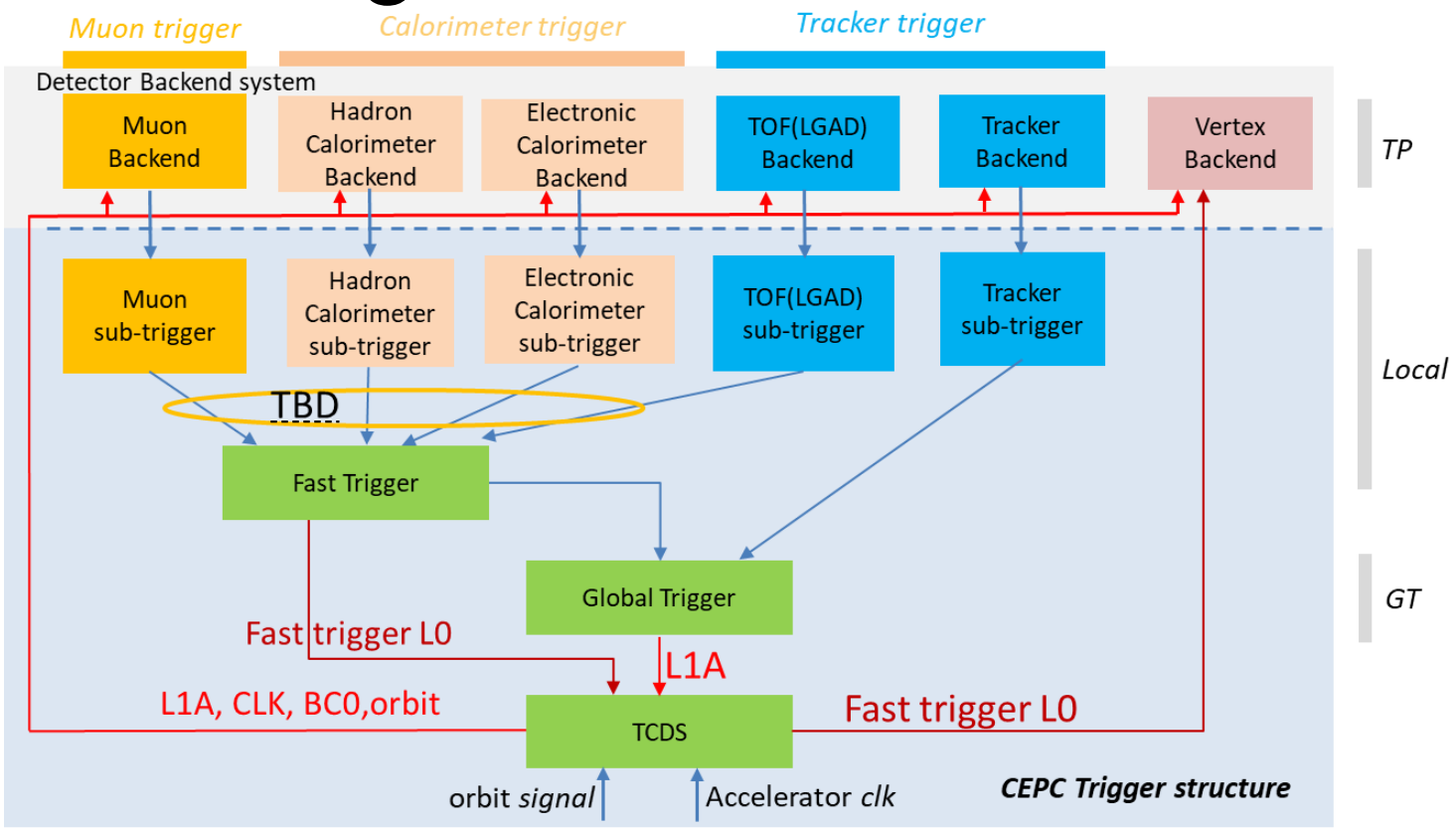
springer.com/journal/41605 | rdtm.ihep.ac.cn

To submit your manuscript: https://www.editorialmanager.com/rdtm/default.aspx

Backup Slide

The unchanged top-level electronics block diagram

- The proposed framework was based on the estimated background rate of all sub-det.
- Background rate indicated the data link capability can manage the Phase I operation of Higgs & Low LumiZ in the first ten years
  - Shielding optimization ongoing to suppress the background
  - High LumiZ situation is still not fully understood, but in the 2nd ten years
    - Replaceable detectors e.g. VTX, ITK.. can be upgraded with new chips with intel-compression and advanced trigger in case
    - Unreplaceable detectors e.g. ECAL, HCAL can be upgraded with more fiber channels



The conventional trigger scheme can serve as a backup plan, with sufficient on-detector data buffering and reasonable trigger latency, the overall data transmission rate can be controlled.