Front-end Readout Electronics of the Belle II TOP Detector: Firmware Status and Future Development

V. Shebalin on behalf of the Belle II TOP group

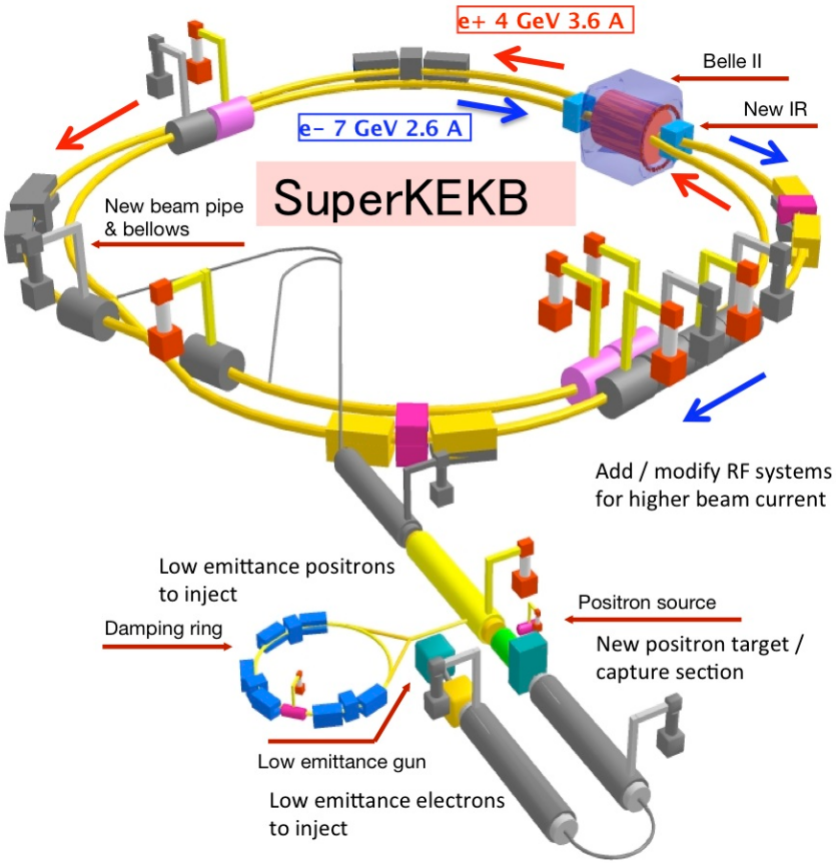
University of Hawaii at Manoa
2505 Correa Road Honolulu, HI 96822

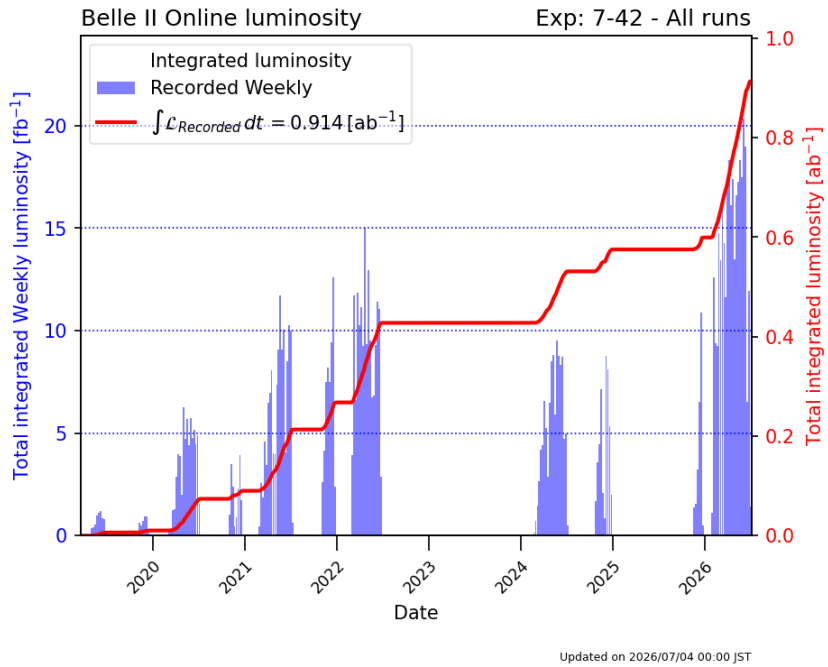
CEPC2026, Shanghai, China
24 October 2026





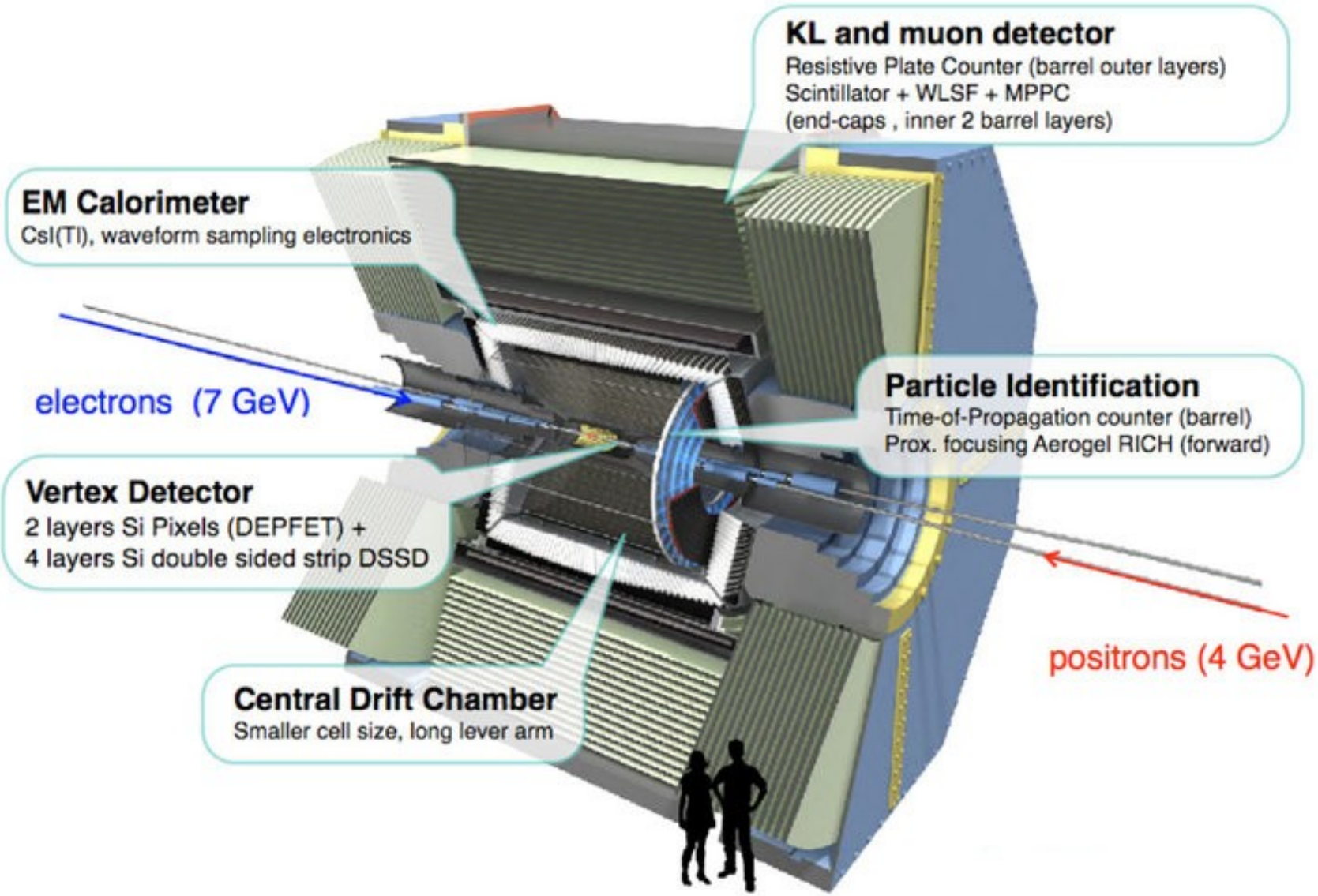
SuperKEKB: Assymetric e^+e^- collider





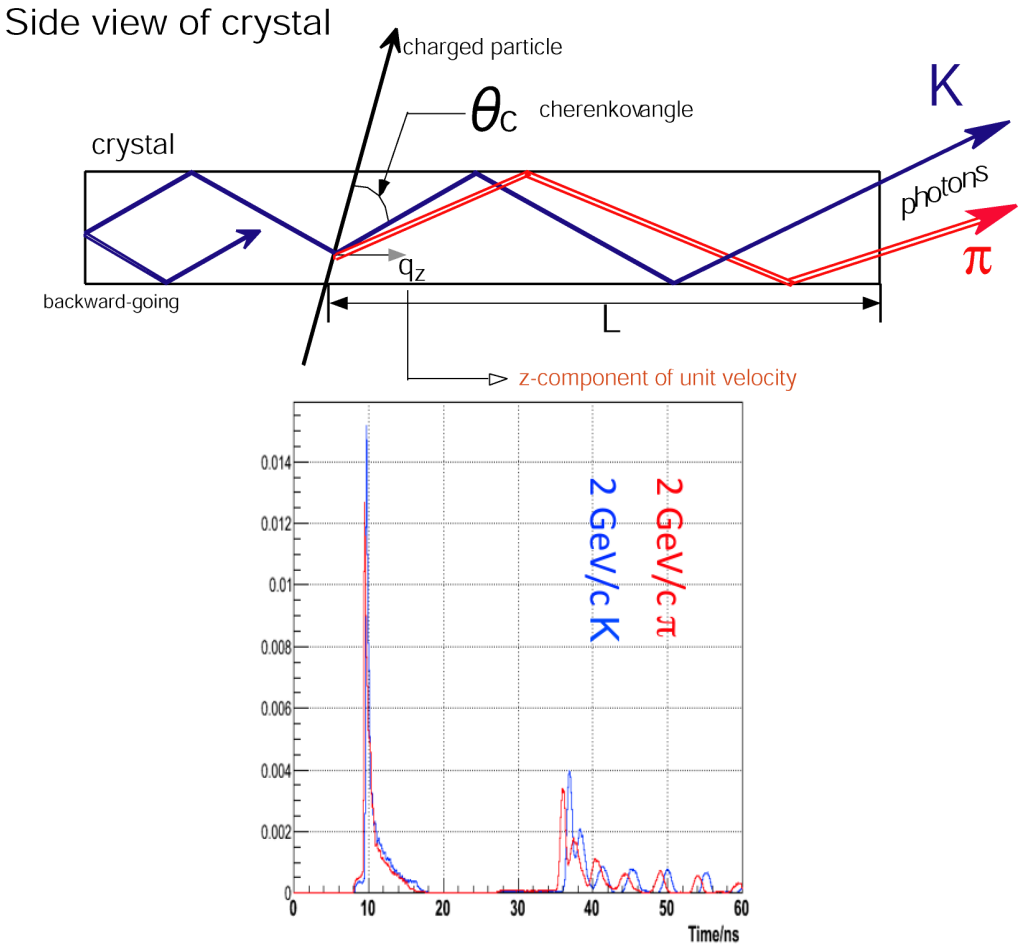
- $E_{e^-} = 7\,GeV$ $E_{e^+} = 4\,GeV$, $E_{cm} = 10.58\,GeV$
- Peak luminosity of $5.319 \times 10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$ (achieved on June 30, 2026)
- Integrated luminosity: over $914\,\mathrm{fb}^{-1}$
- Target peak luminosity: $6.0 \times 10^{35}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$

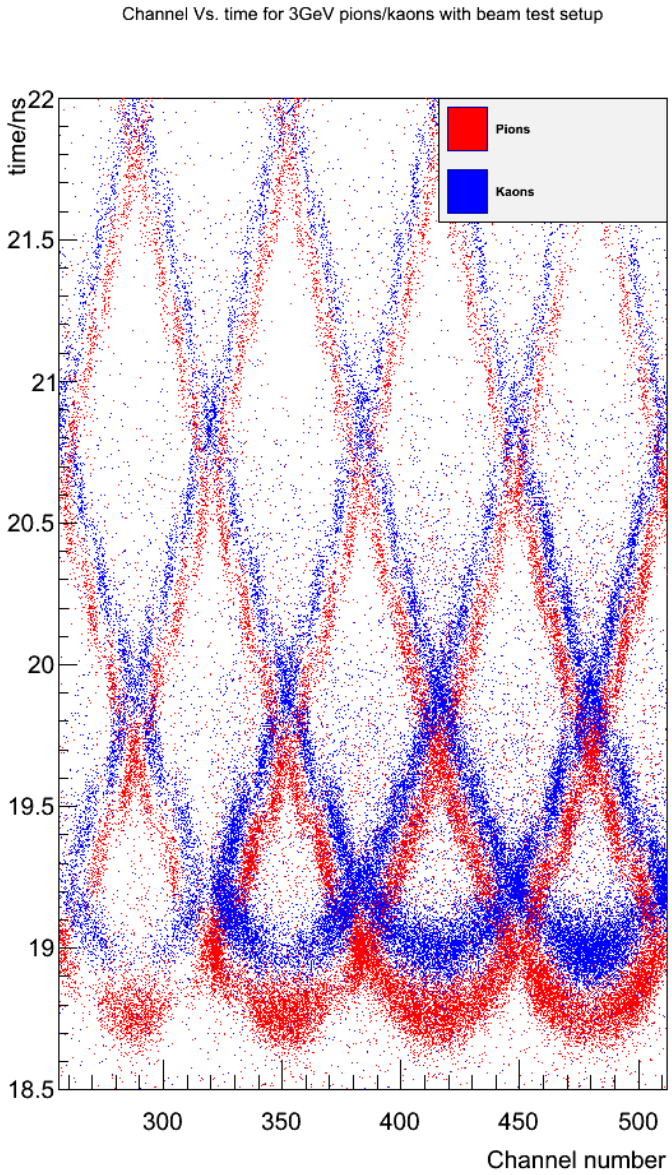
Belle II detector



TOP detector: principle of operation

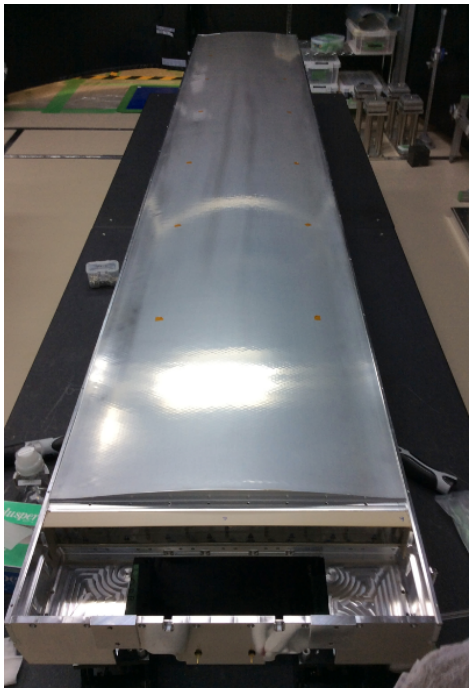
- Particle identification in the barrel region
- Time-of-flight + Cherenkov angle

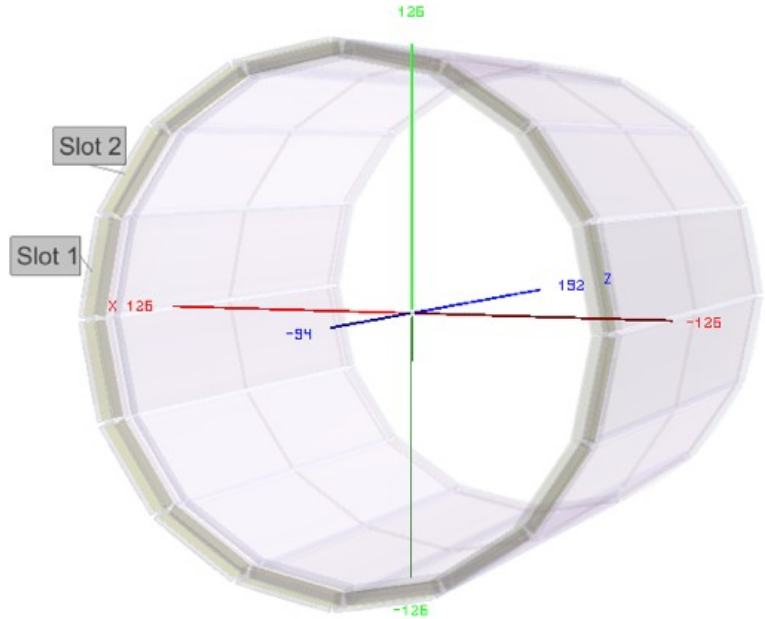


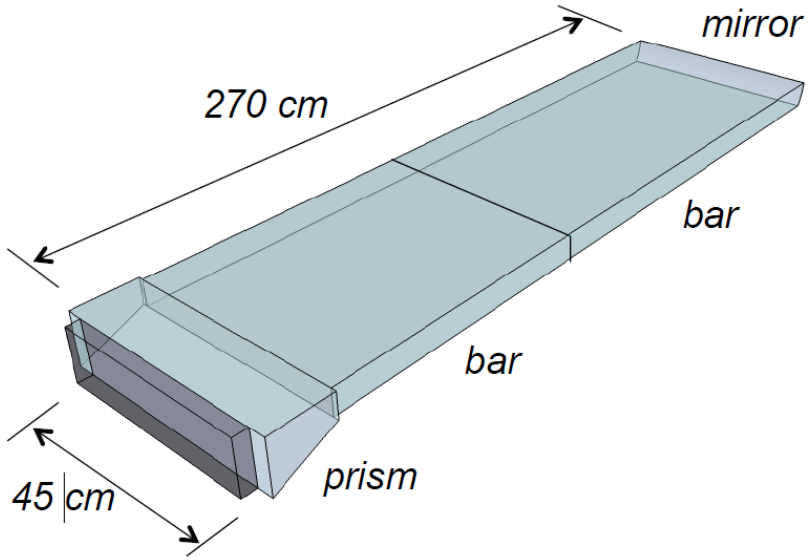


TOP detector: geometry

- 16 quartz Cherenkov radiator bars
- Bar size: $270 \times 45 \times 2\ \mathrm{cm}^3$
- Surface flatness better than $6\,\mu$m
- Cherenkov light is read out by 32 MCP-PMTs (16 pixels each) attached to the prism surface

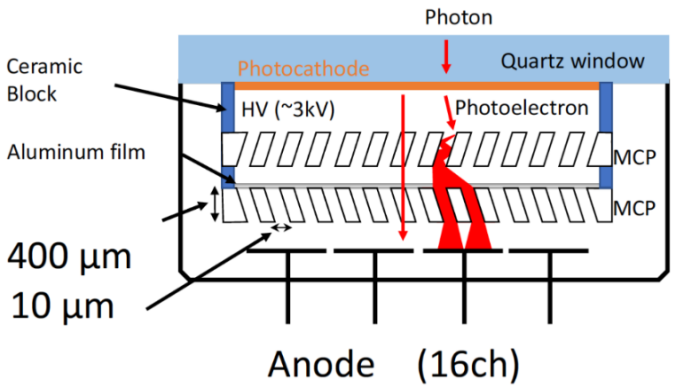






Microchannel Plate (MCP) PMTs

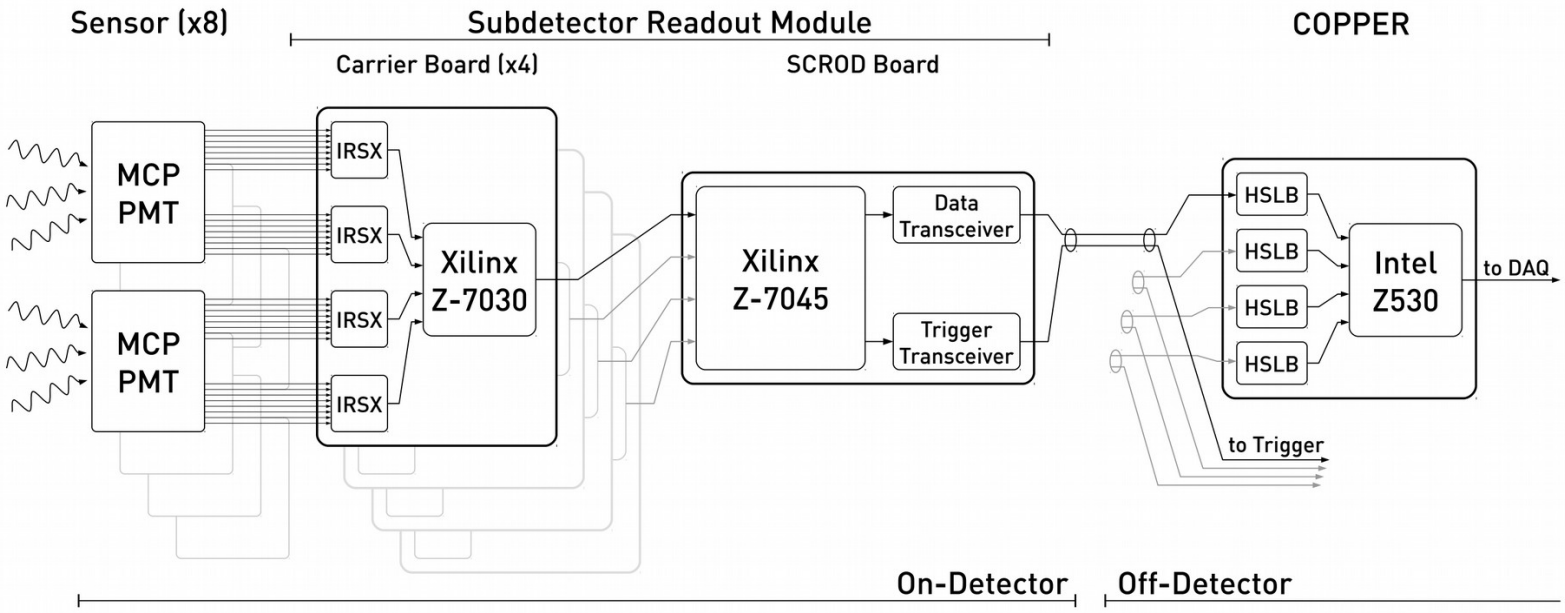




Properties

- Hamamatsu R10754-07-M16(N), developed for TOP
- Photocathode area: $23 \times 23\ \mathrm{mm}^2$
- 16 channels
- Average measured peak quantum efficiency: 29.3%
- Time resolution of about 34 ps
- Operates in a 1.5 T magnetic field
- Can operate at MHz-range hit rates

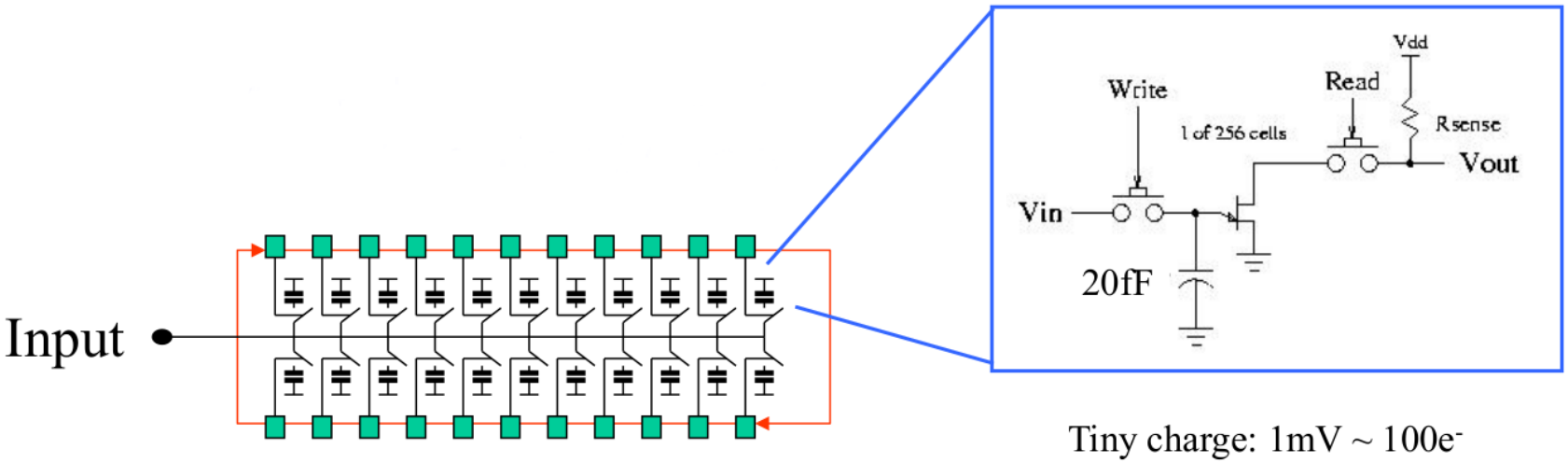
Readout Electronics

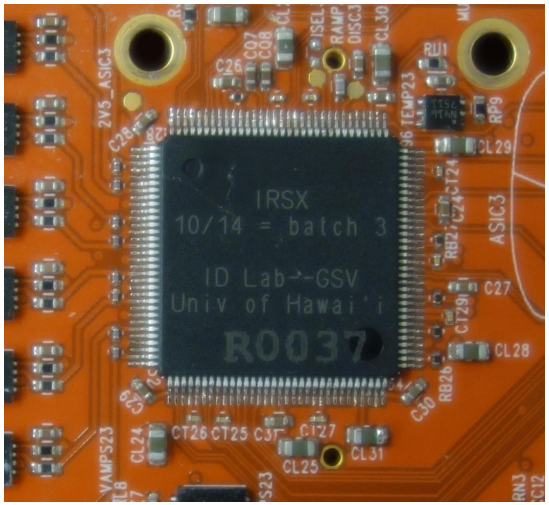


Requirements

- 8192 readout channels in total
- Trigger rate up to 30 kHz
- Time resolution better than 100 ps
- Must operate in a radiation environment

Readout Electronics: IRSX ASICs

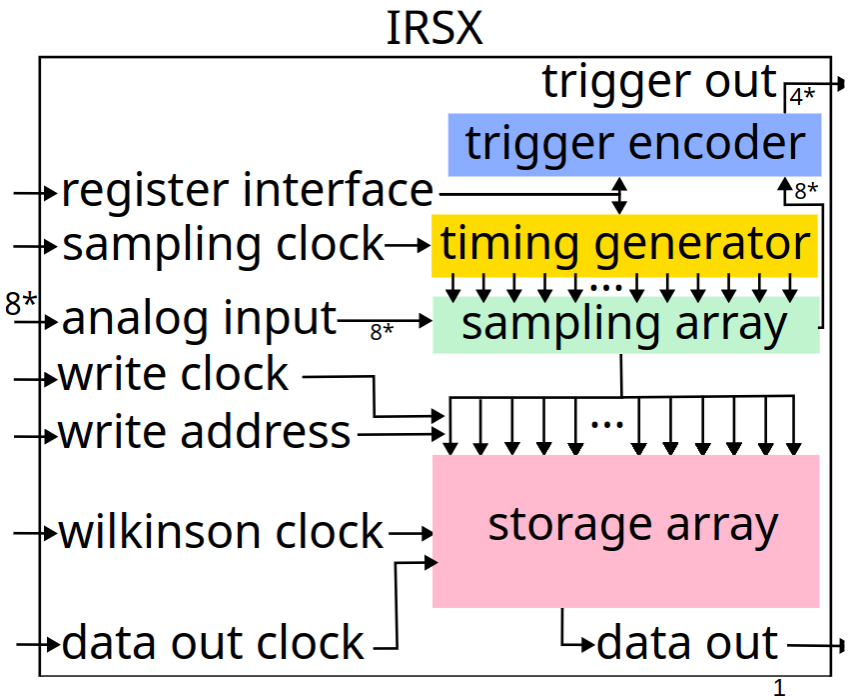


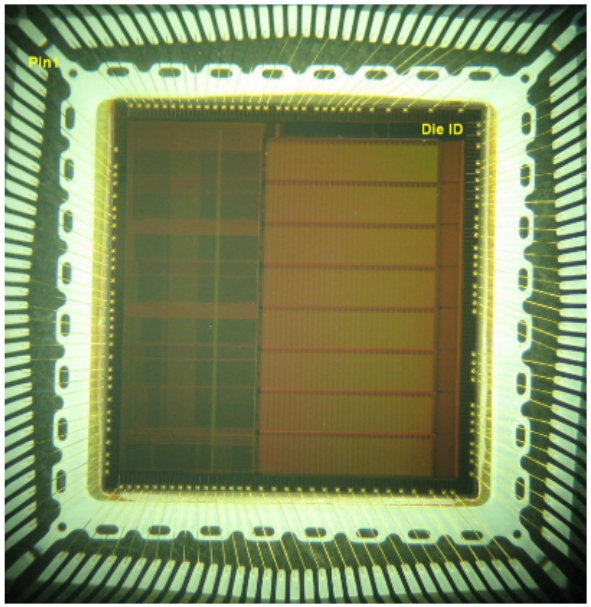


IRSX

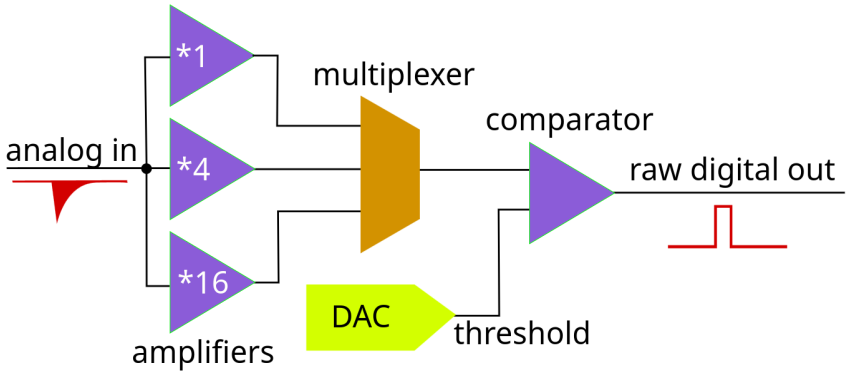
- Waveform-sampling ASIC
- 8 input channels
- Sampling rate of 2–4 GSa/s (2.7 GSa/s in TOP)
- 12-bit Wilkinson ADC
- ~600 MHz analog bandwidth
- 32k analog storage cells (about 10 μs)
- Power consumption of ~100 mW per channel

IRSX ASIC structure

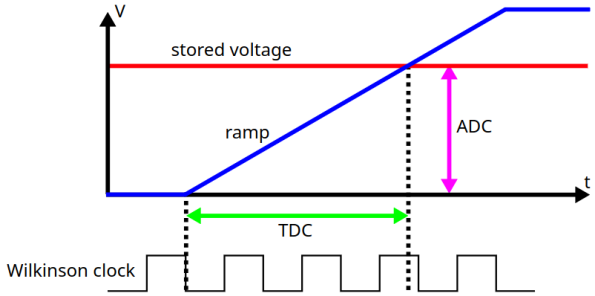




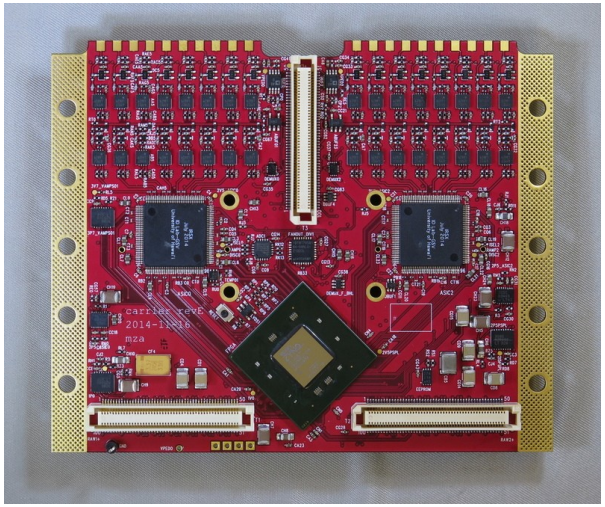
IRSX channel trigger

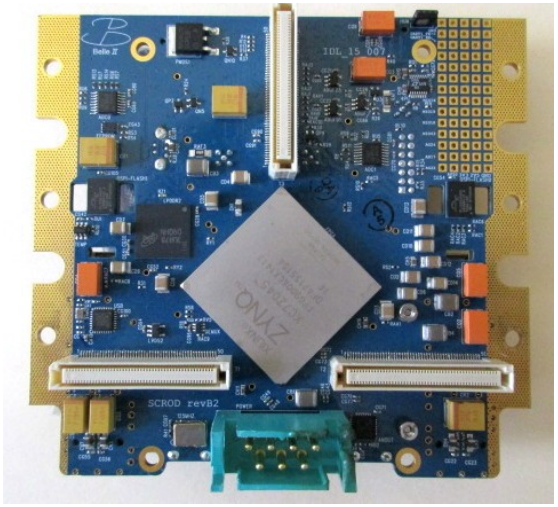


Wilkinson ADC



Carrier and SCROD boards





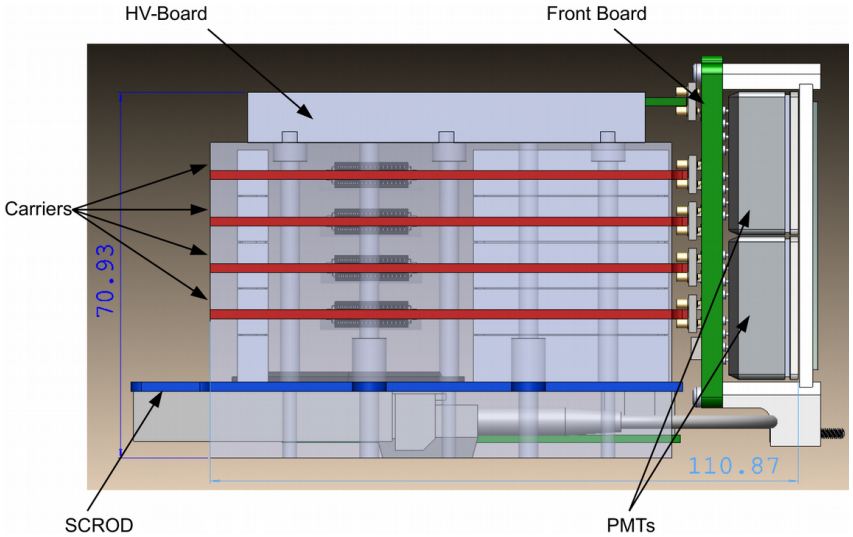
Carrier board

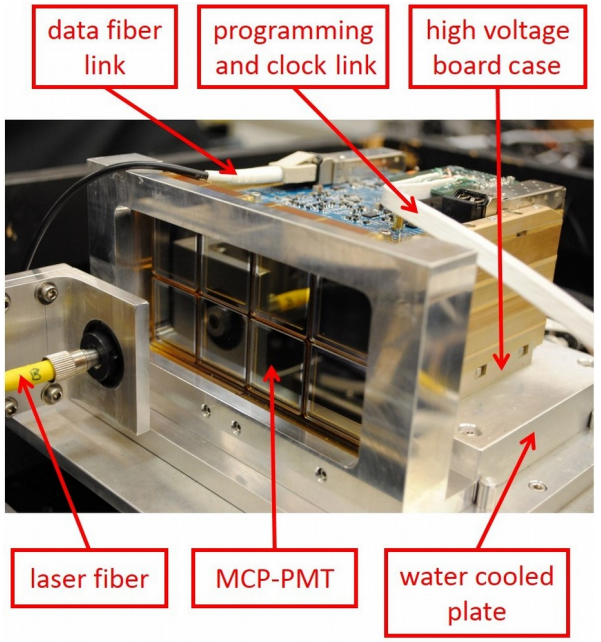
- Hosts PMT preamplifiers and 4 IRSX ASICs
- Xilinx Zynq-7030 SoC: FPGA (PL) + ARM CPU (PS)
- FPGA collects data from the ASICs and streams it to the SCROD board
- ARM: housekeeping only, but could be used for data processing

SCROD board

- Xilinx Zynq-7045 SoC
- Receives ASIC data streams from the Carrier boards
- Builds DAQ packets and sends them via optical transceivers
- ARM processor is used for online data processing

Readout Electronics: Boardstack

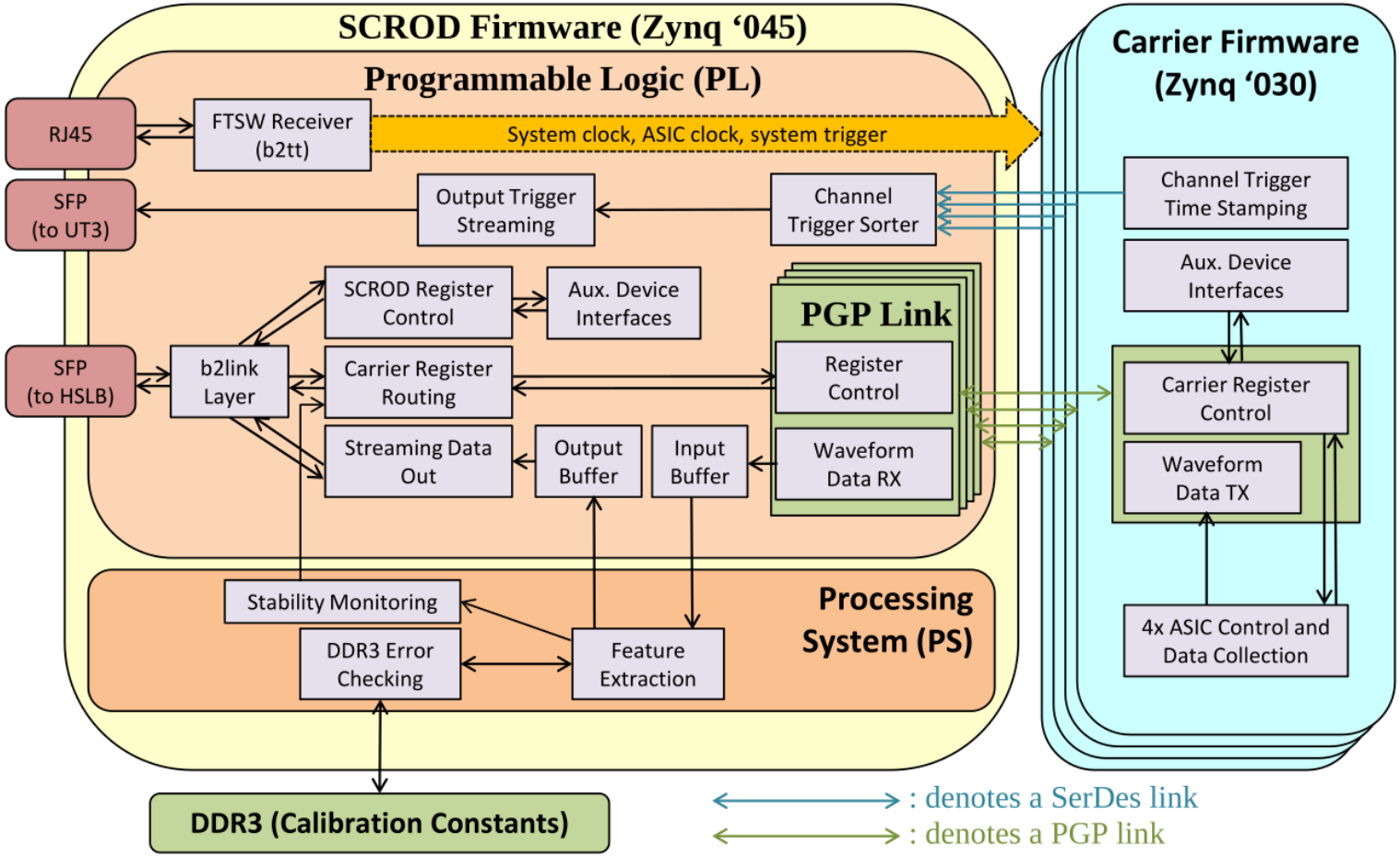




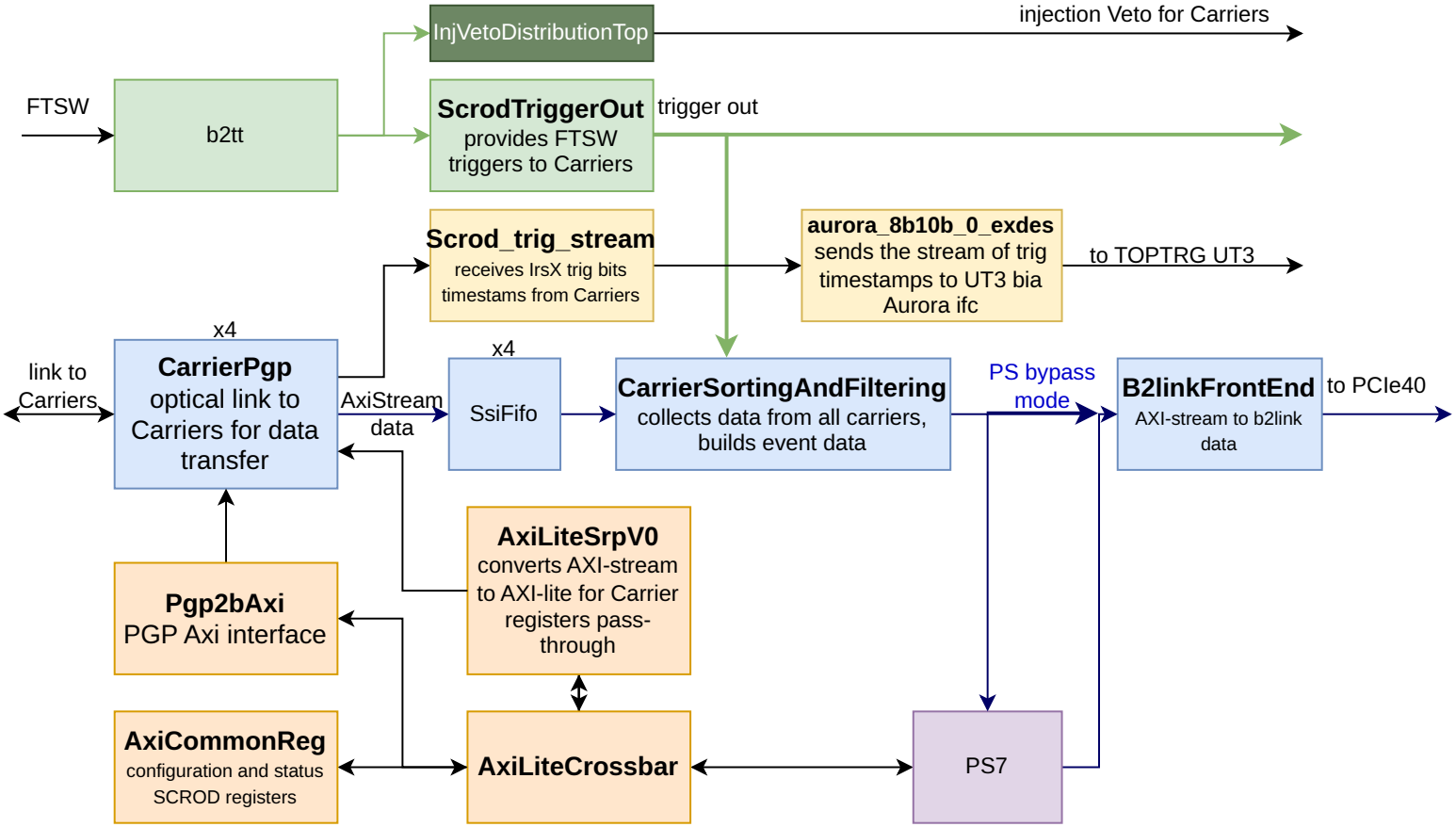
TOP boardstack

- 1 SCROD + 4 Carrier boards + HV control board
- Serves 8 MCP-PMTs
- 4 boardstacks per TOP module (bar)
- Sealed inside the module cover → electronics must operate in a radiation environment

Firmware overview



SCROD firmware in more detail

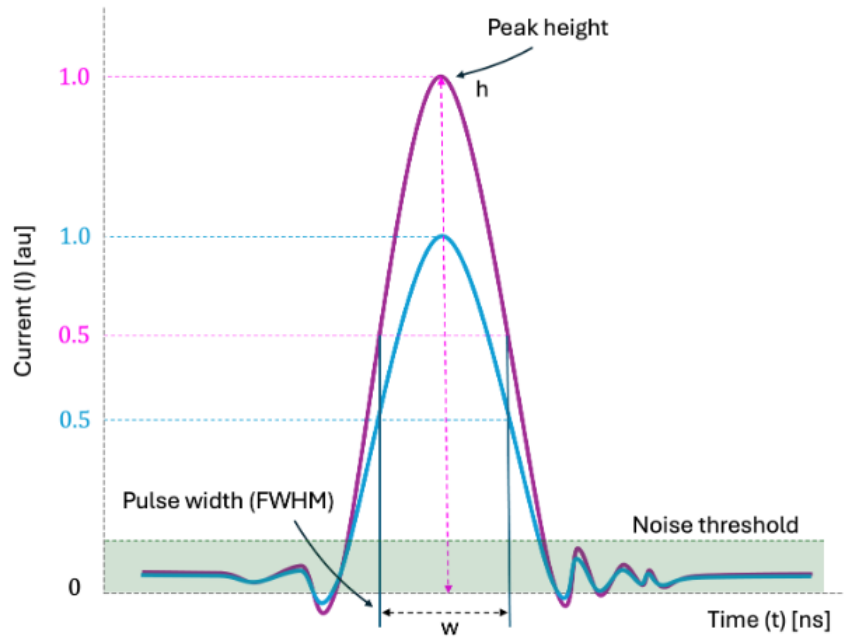


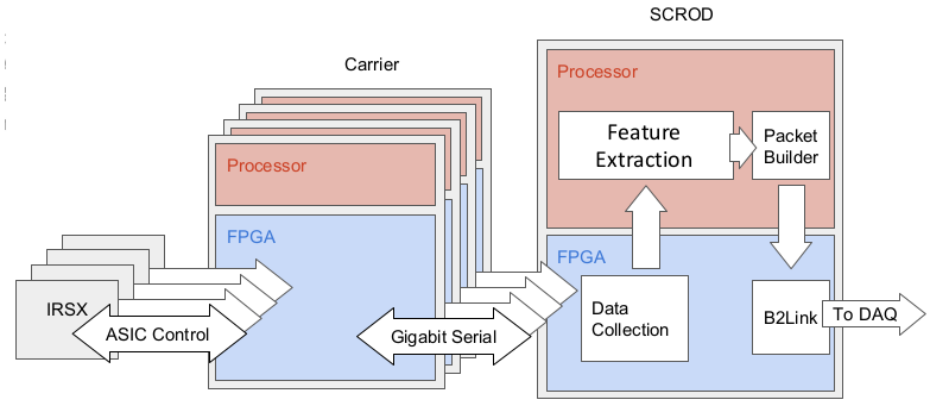
Feature extraction

- Constant fraction discriminator (CFD)
- Simple, fast, and resource-efficient algorithm
- Determines peak height and rise/fall times
- Implemented in the PS embedded software

Issues

- SCROD PS lock-ups due to radiation-induced single event upsets (SEUs), while the PL remained operational. This caused about 10 min/day of detector downtime.
- Dead time introduced by PS data processing

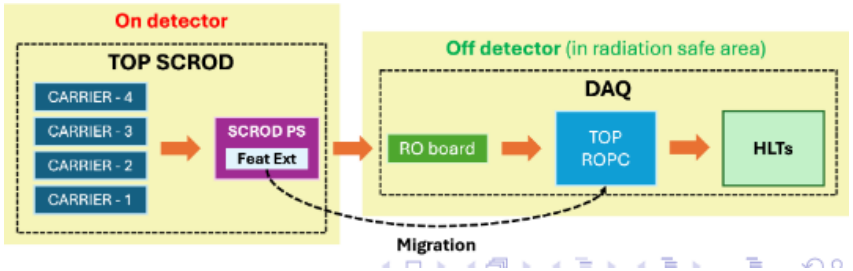


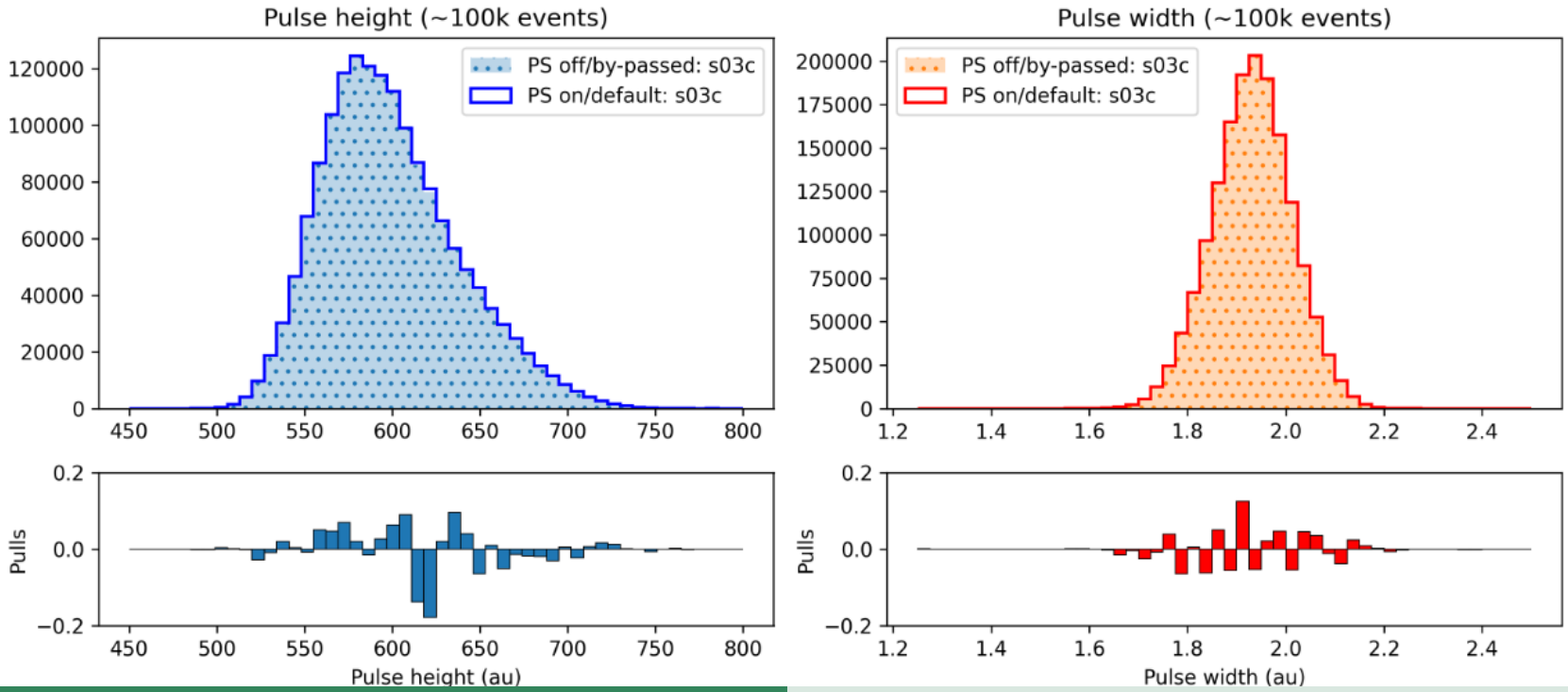


Migrating feature extraction to the readout PC

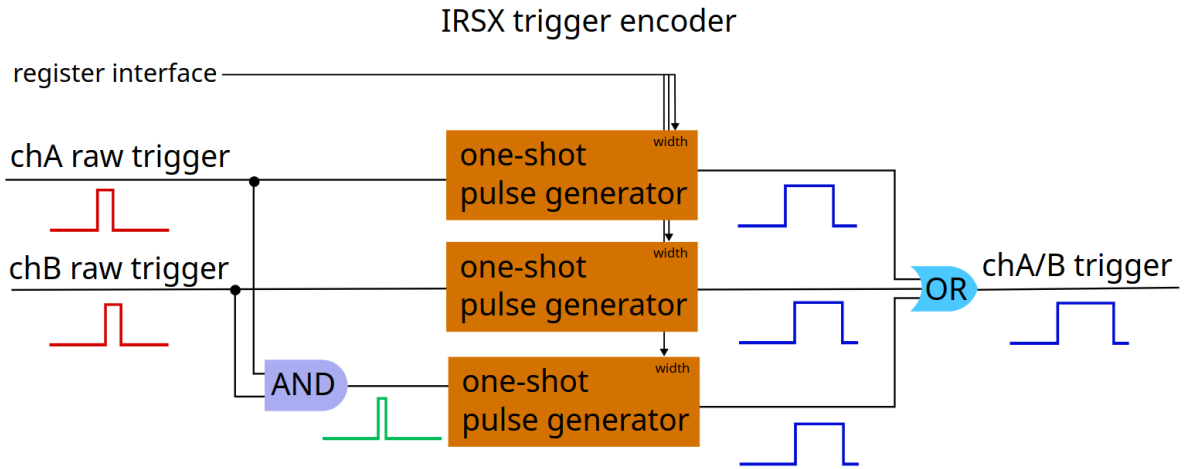
PS bypass mode

- Raw waveforms are sent directly to DAQ
- Stable operation without lock-ups
- Zero dead time
- Downside: data rate to the readout PC increases by a factor of ∼5





Reducing the data rate



Further development focuses mainly on:

- Improving overall system stability
- Reducing the data rate by optimizing the data format
- Studying online pedestal subtraction (for every sample)
- Zero suppression of waveforms without a signal, by identifying which channel in the trigger group fired. The fired channel can be decoded from the width of the IRSX trigger signal.

Conclusion

- The TOP detector has been operating stably since physics runs began in 2018
- Excellent time resolution achieved in high-rate runs without dead time
- TOP PID is successfully used in ongoing Belle II analyses
- Further improvements are mainly related to migrating feature extraction to the readout PC