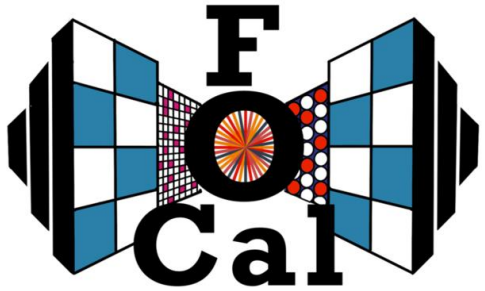
# Readout Electronics for the FoCal-E Pixel Layer in ALICE




**Shoulong Lin (CIAE)**

**On behalf of the ALICE FoCal Collaboration**

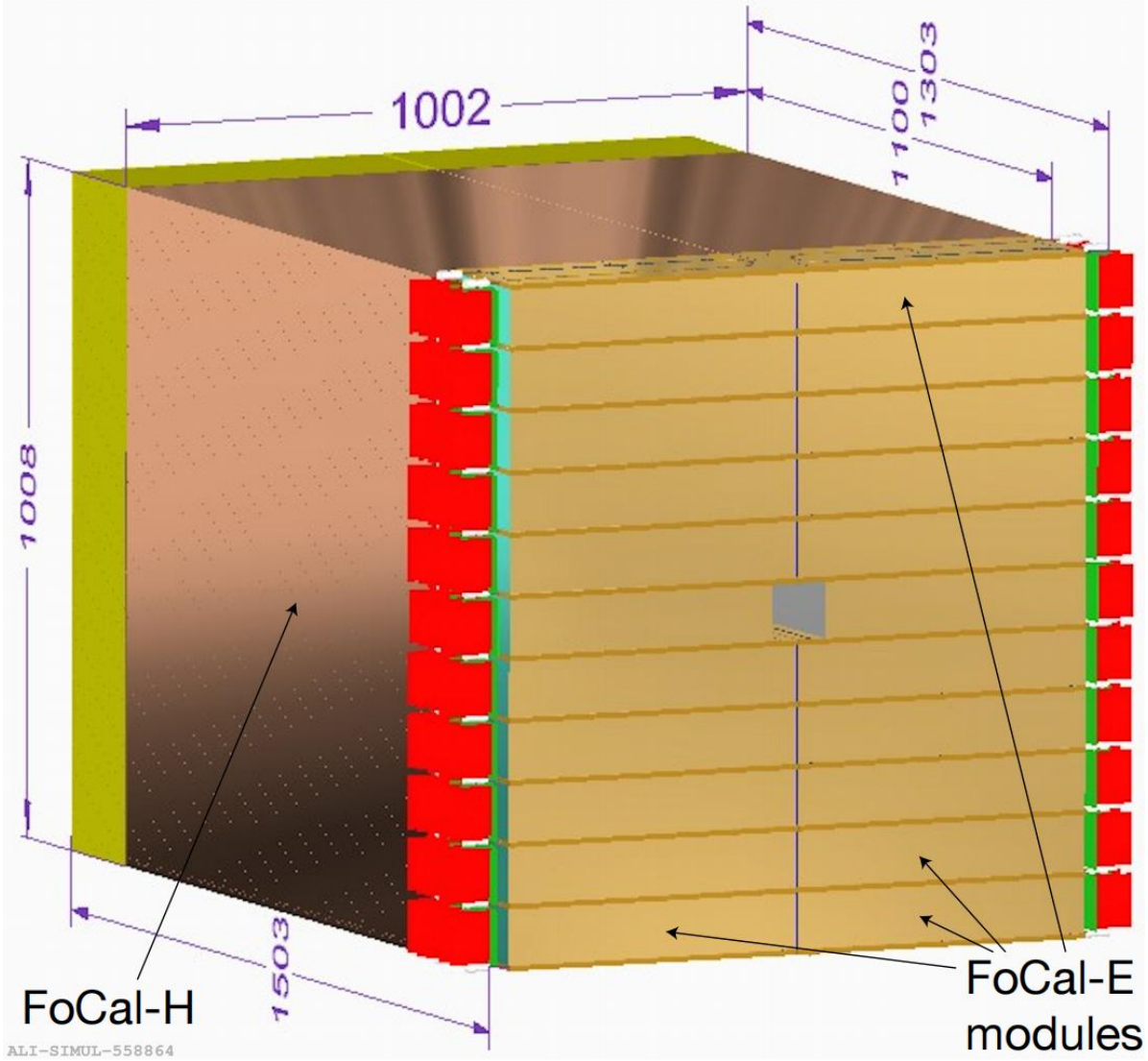
2026 International Workshop on the High-Energy Circular Electron-Positron Collider (CEPC2026)
21-26 October, Shanghai, China

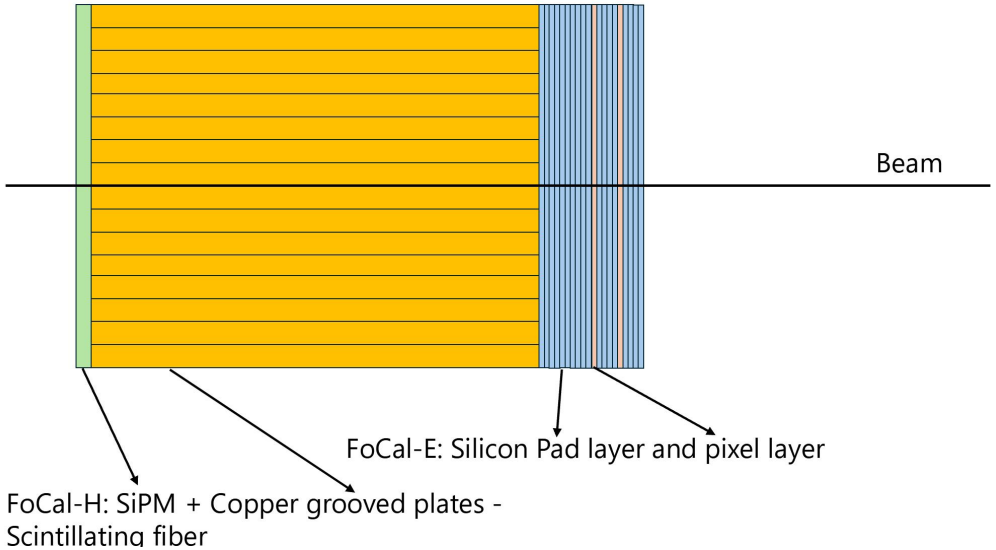
# Outline

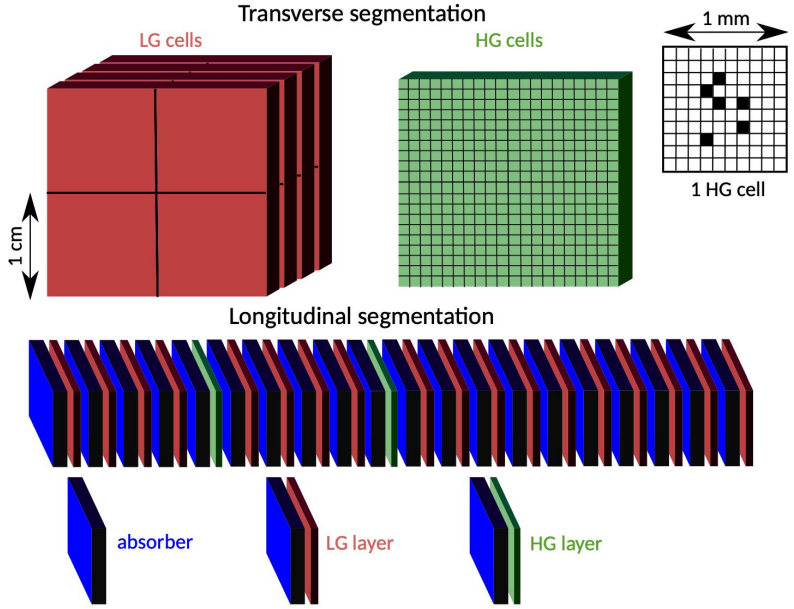
1. FoCal-E pixel layer
2. Readout system
3. Readout unit and firmware design
4. Summary

# FoCal-E pixel layer

## FoCal detector

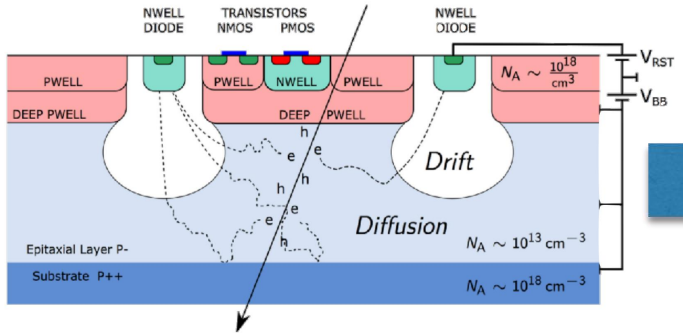


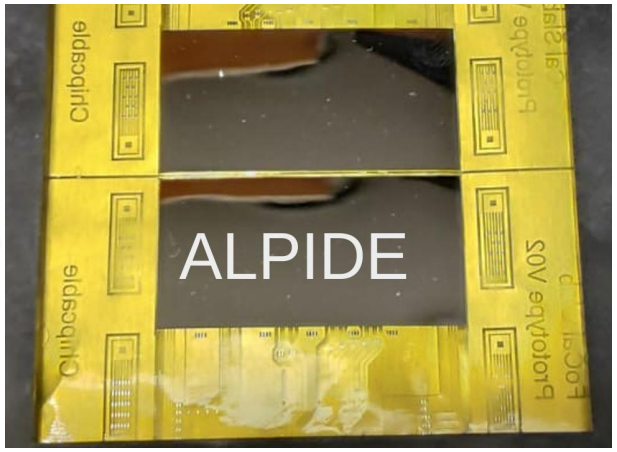



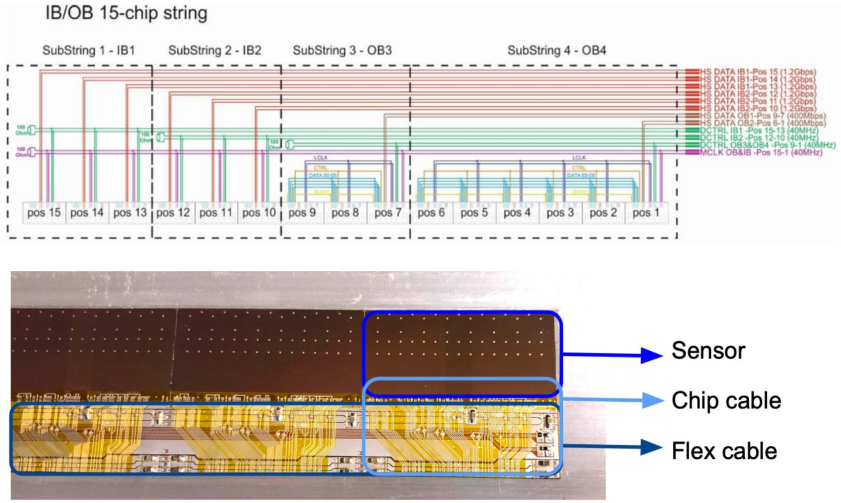



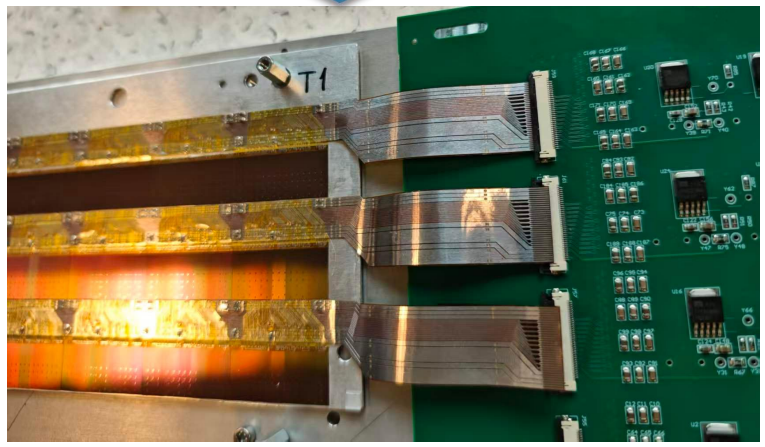
# FoCal-E pixel layer

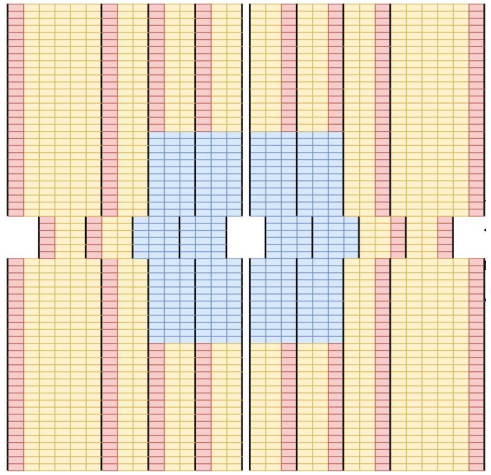
## Sensors to pixel layer



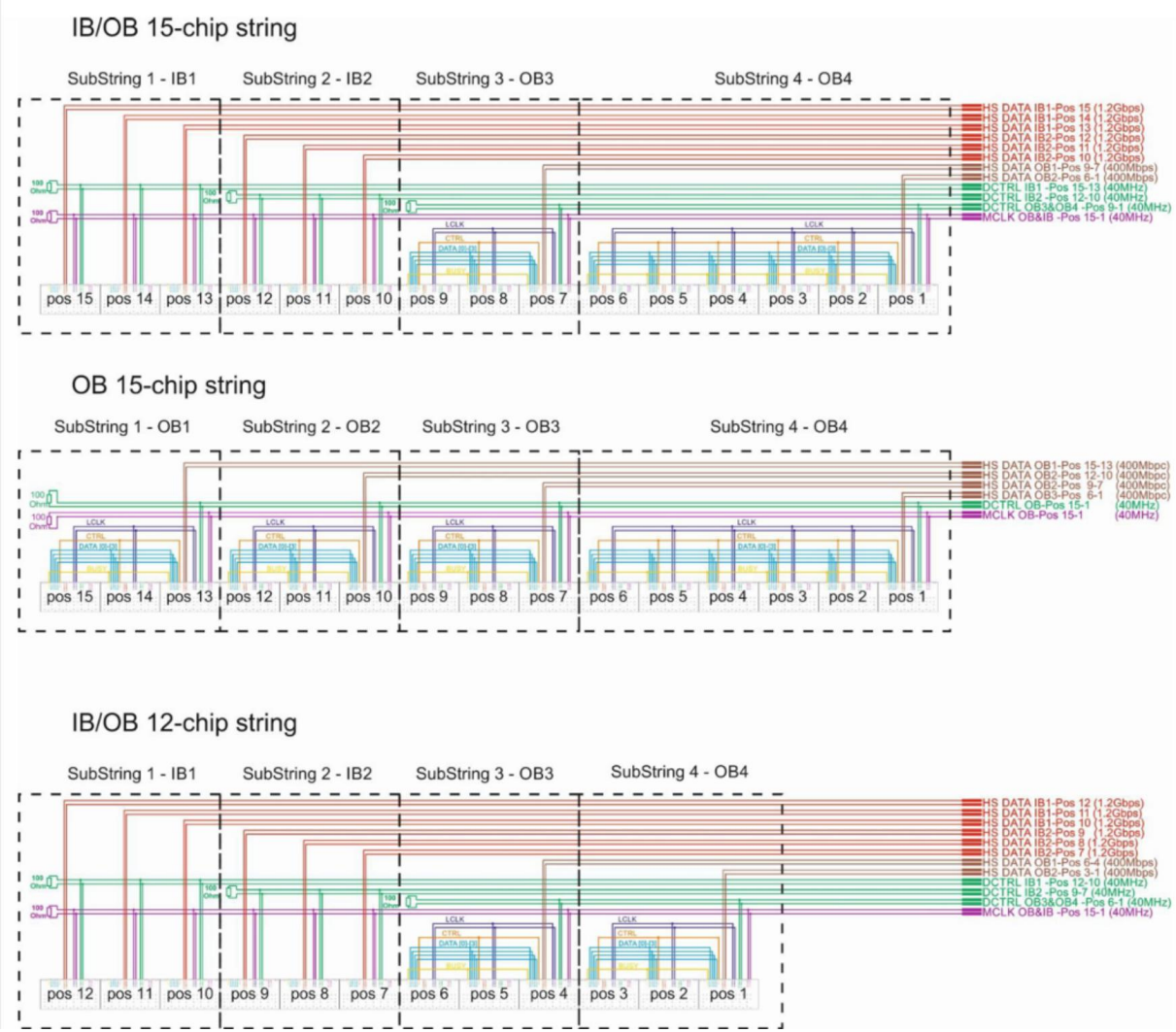
*Note: Represents one pixel layer but there are two in the final design. Drawing is not to scale.*

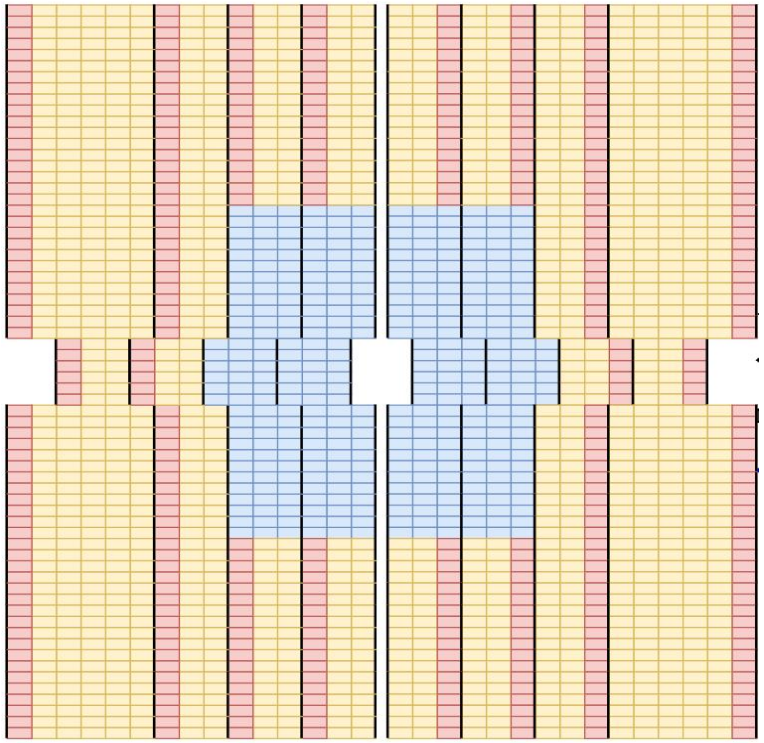
Detector layout:

- ALPIDE:
  - 3 x 1.5 $cm^2$ 1024 x 512 pixels
  - ~ 30x30 $\mu m^2$
- Sensor, string, module, detector
- Sensors work in different modes (IB/OB)

# FoCal-E pixel layer

## Strings



*Note: Represents one pixel layer but there are two in the final design.*
*Drawing is not to scale.*

Two flavors of modules

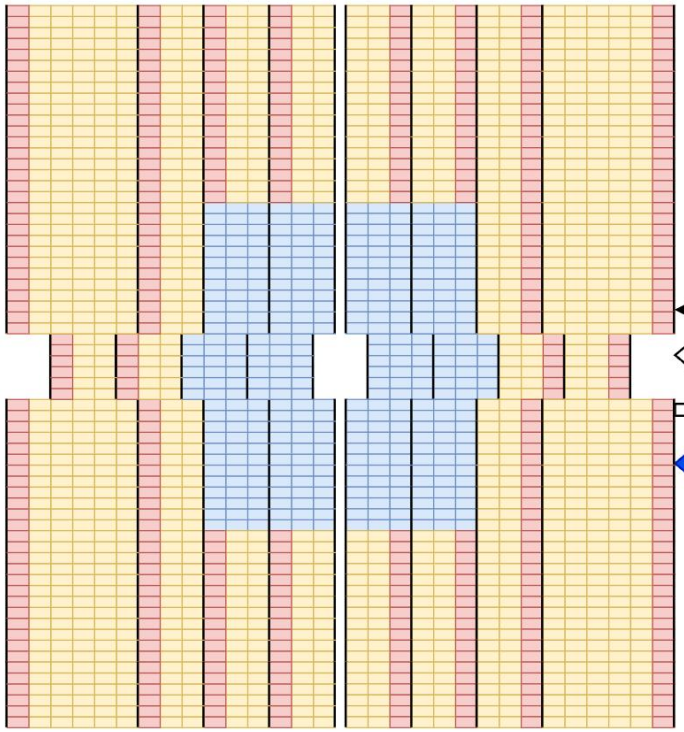
- IB/OB strings/modules
- OB only modules

Two flavors of readout chain

- 72 OB master chips (3 OB modules)
- 36 IB chips and 12 OB master chips (1 IBOB )

# Readout system

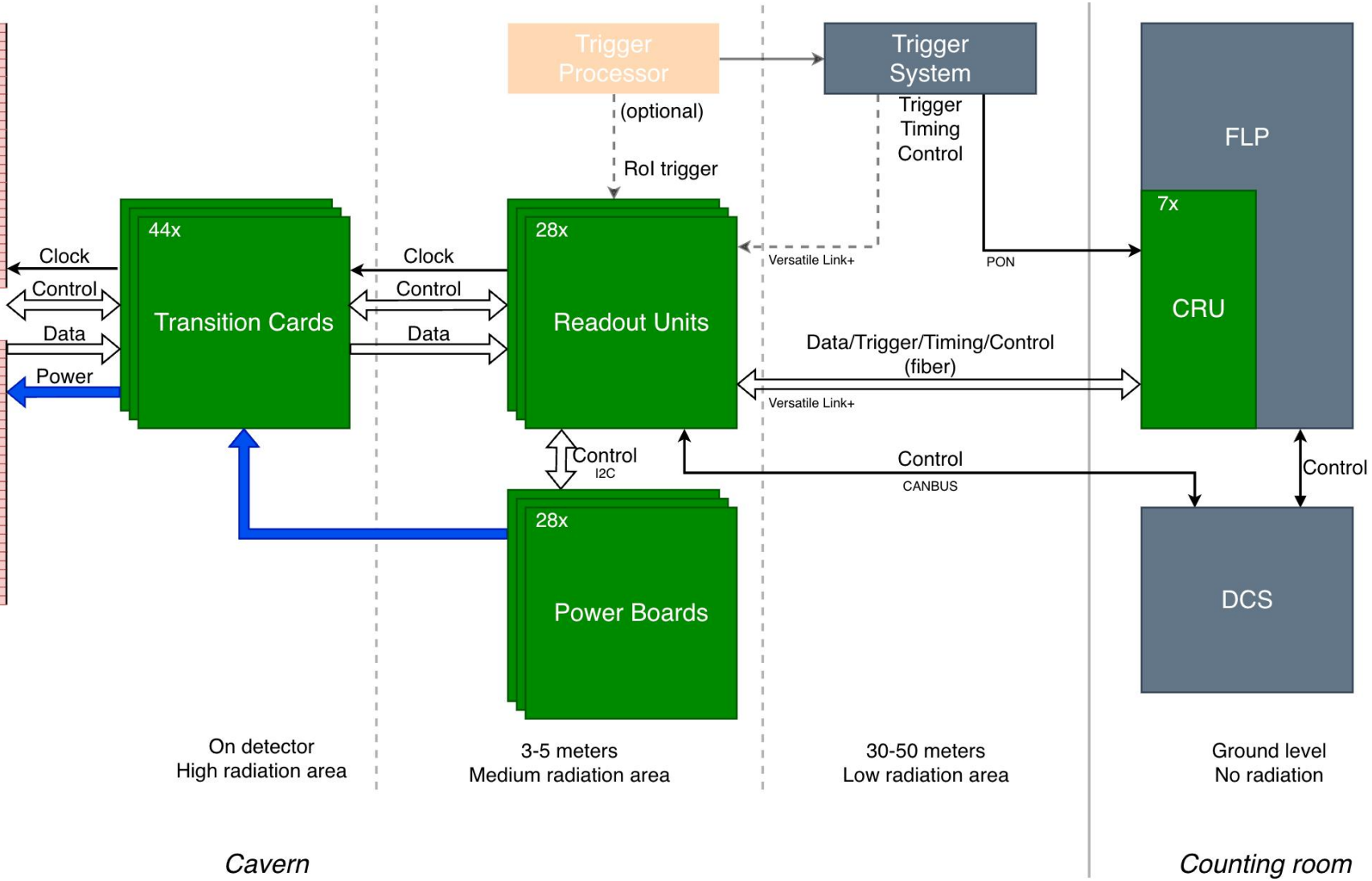
## System overview



*Note: Represents one pixel layer but there are two in the final design.*
*Drawing is not to scale.*

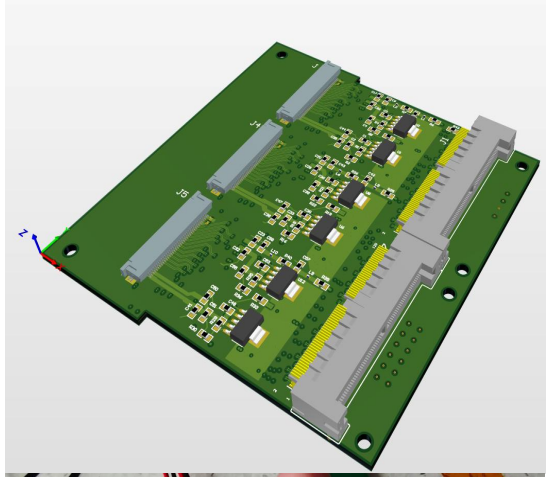
**ALPIDE modes:**

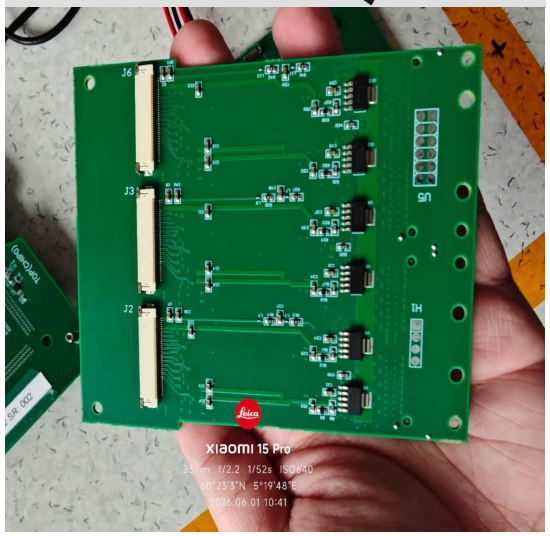
- Inner Barrel
- Outer Barrel Master
- Outer Barrel Slave



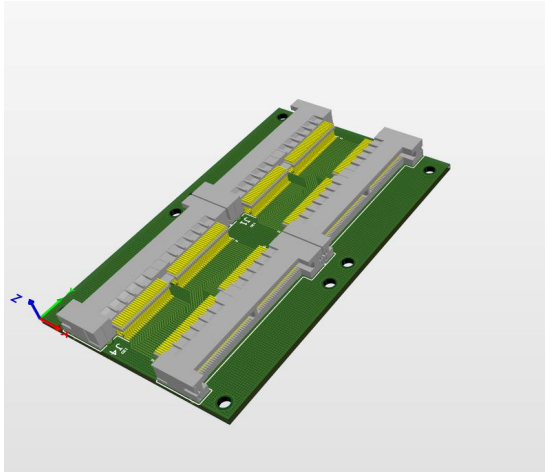
# Readout system

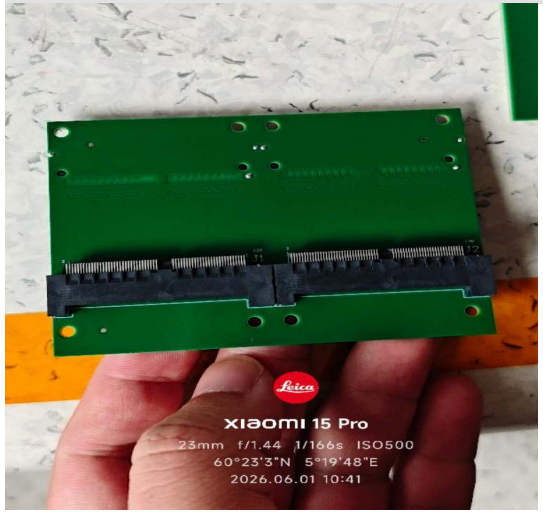
## Transition card and patch panel board





Transition Card






Patch panel board

Transition card

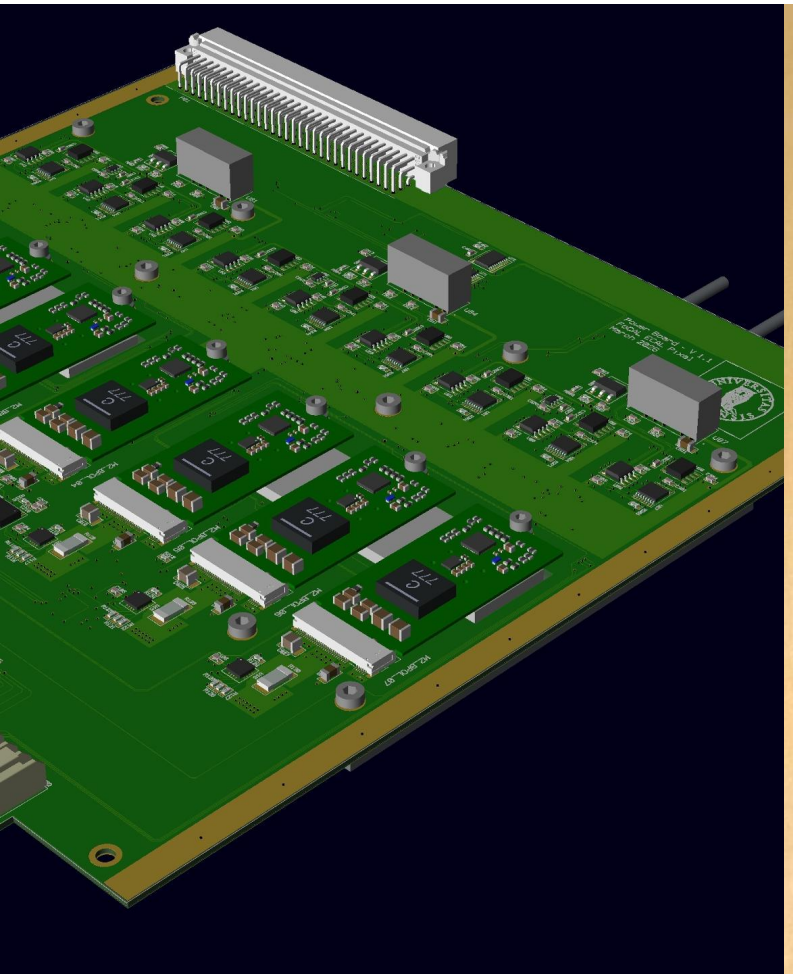
- Voltage regulators close to sensors make the sensor voltage stable (experience from ITS2)

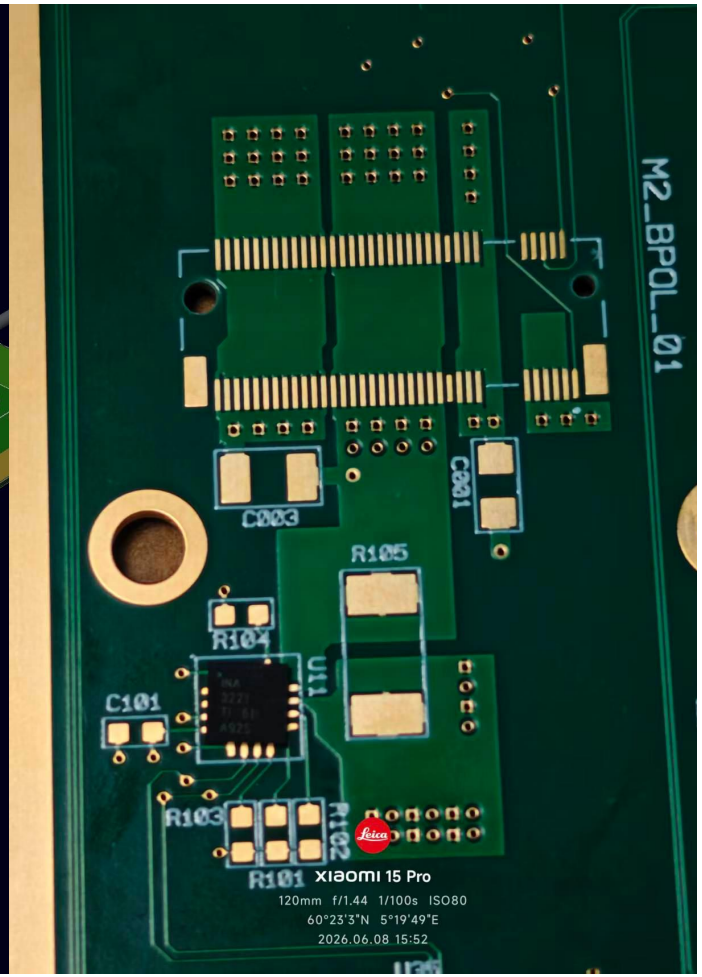
Patch panel board

- Located between detector modules and readout unit
- Disconnect the cables from patch panel board to make life easy :-)

# Readout system

## Power board






Power board

- Main power to the TC (transition card) via bPOL48V modules
- Negative voltage (PWELL) to the TC
- Current measurement of each bPOL48V
- Temperature measurement
- Two I2C buses connected to the RU
- Two different configurations:
  - One IB/OB TC is connected
  - Three OB TCs are connected

# Readout system

## FoCal vs ITS2

### Data and control links per RU

| FW mode | IB data links 1.2Gbps | OB data links 400Mbps | Control links |
|---|---|---|---|
| ITS-IB | 9 | 0 | 1 |
| ITS-OB | 0 | 16 middle/28 outer | 4 |
| FoCal-OB | 0 | 72 | 18 |
| FoCal-IBOB | 36 | 12 | 18 |

### GBTx and lpGBT

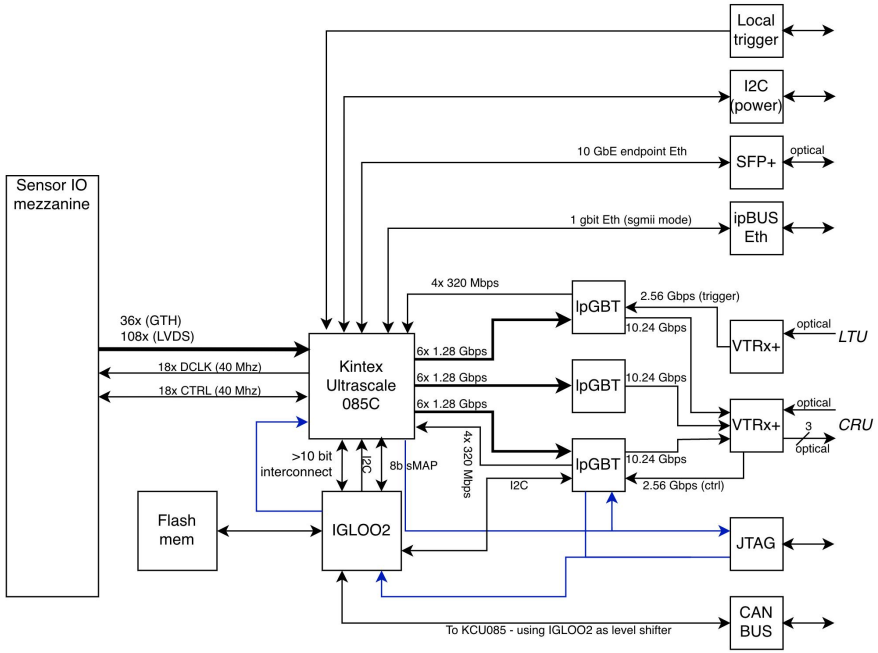
| Chip | Down-link | Up-link | Up-E-links | Down-link |
|---|---|---|---|---|
| GBTx-ITS2 | 3.2-4.48 Gb/s | 10*320 Mb/s | 10*320 Mb/s | |
| lpGBT | 2.56 Gb/s | 5.12/10.24 Gb/s | 6*1.28 Gb/s | 4*320Mb/s |

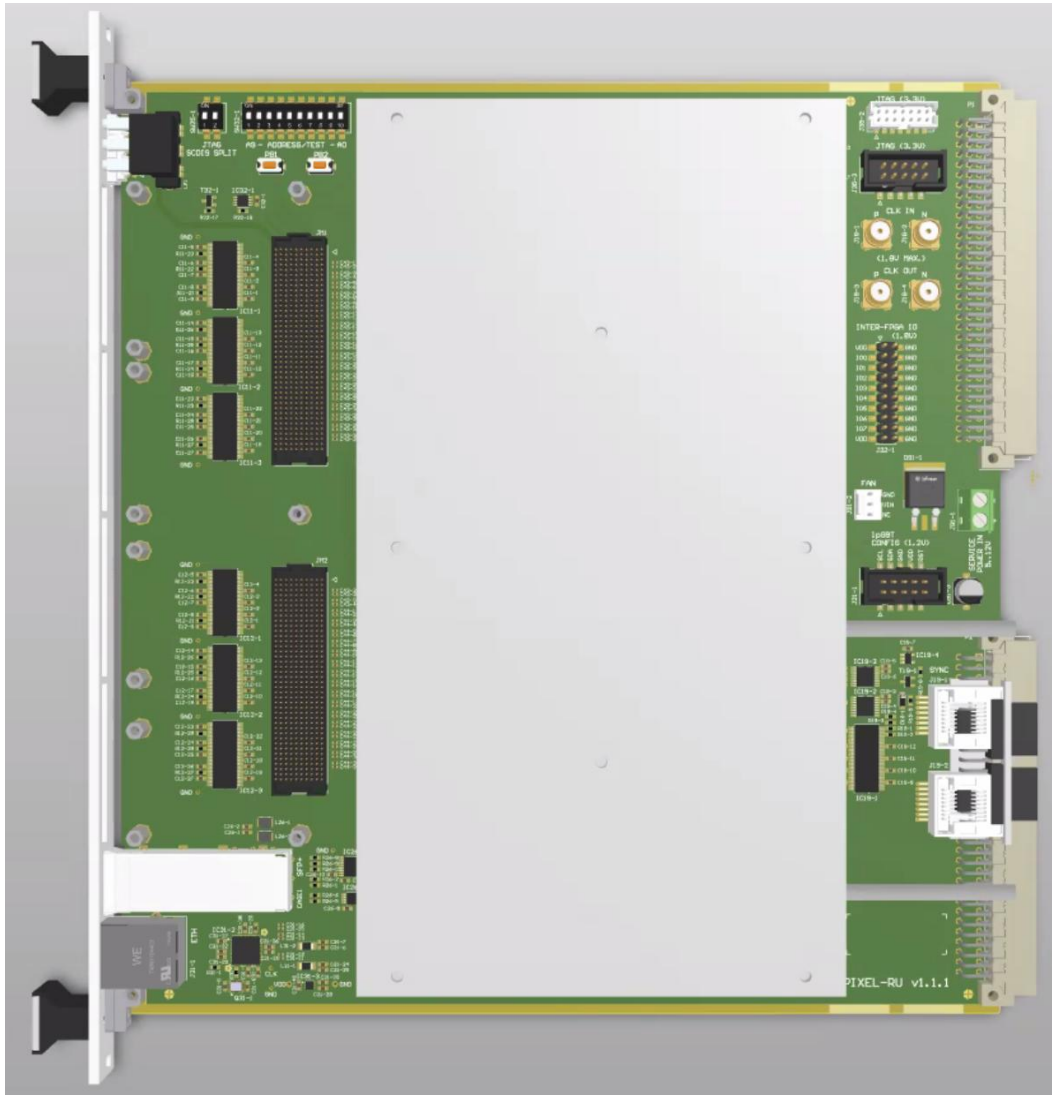
**Challenge:**

- More data links, more control links, readout IB and OB in one RU (never done in ITS)
- New uplink and downlink speed and protocol, new data format need to be design

# Readout unit and firmware design

## Readout unit hardware

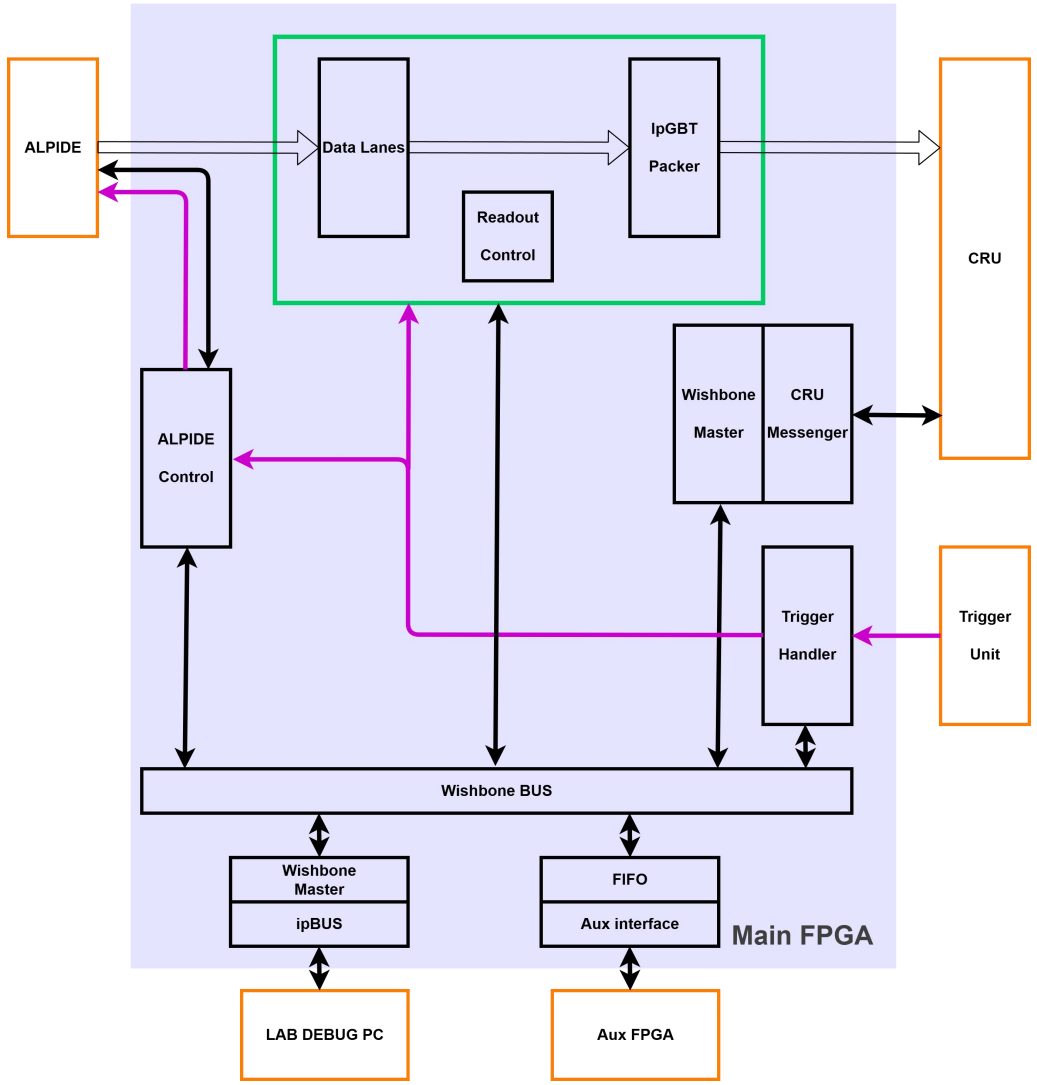


- Based on ITS2 experience
- Different MEZZ for IBOB or OB module
- SRAM-based main Xilinx FPGA for readout
- FLASH-based aux IGLOO2 FPGA for radiation mitigation
- lpGBT & VTRX+ for communication

# Readout unit and firmware design

## Firmware functional design




**ALPIDE Control, Trigger handler**

- Configure
- Control
- Send trigger to ALPIDE

**Data lanes, lpGBT Packer, Readout master**

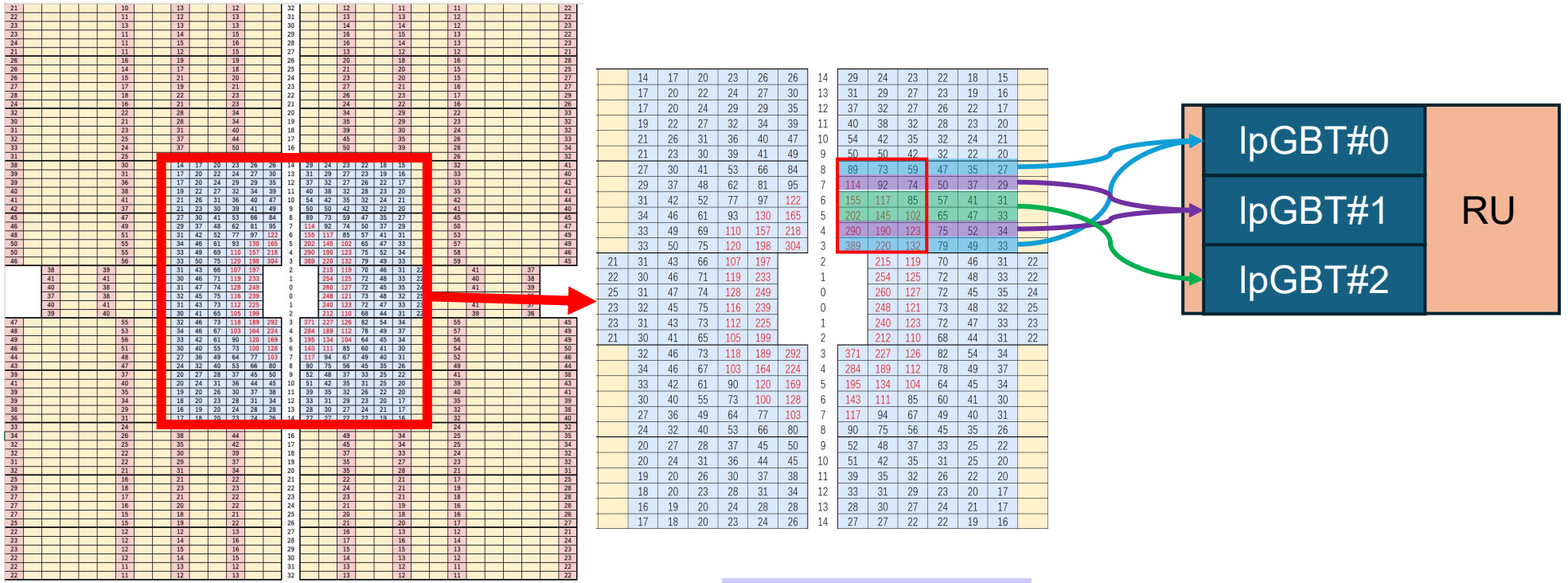
- Get ALPIDE data, deserializing
- Pack data to lpGBT payload, FoCal data format
- Transmit data to CRU

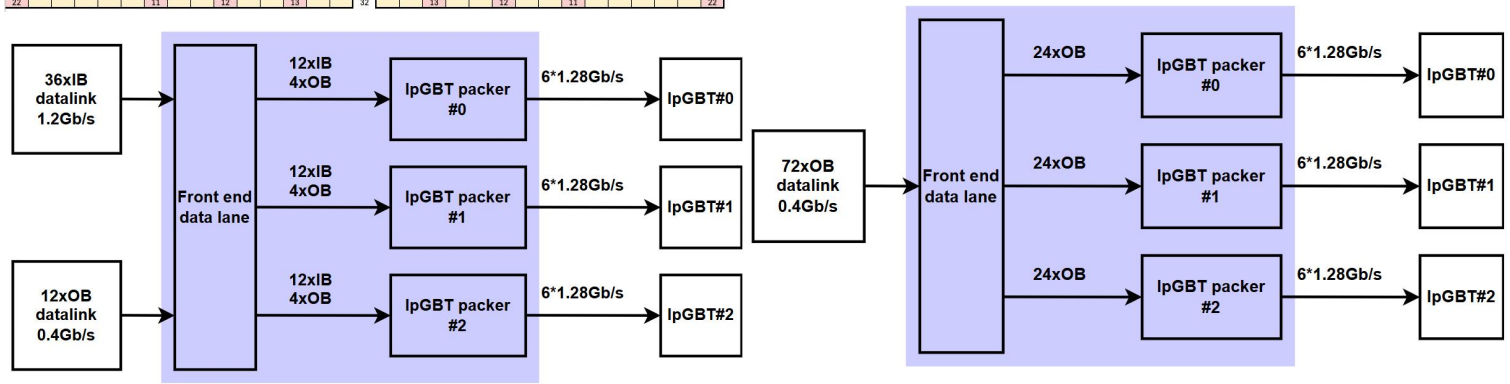
**Wishbone interfaces**

- Report FW status to CRU
- Listen to CRU to do proper adjustment on FW

# Readout unit and firmware design

## Data rate balancing



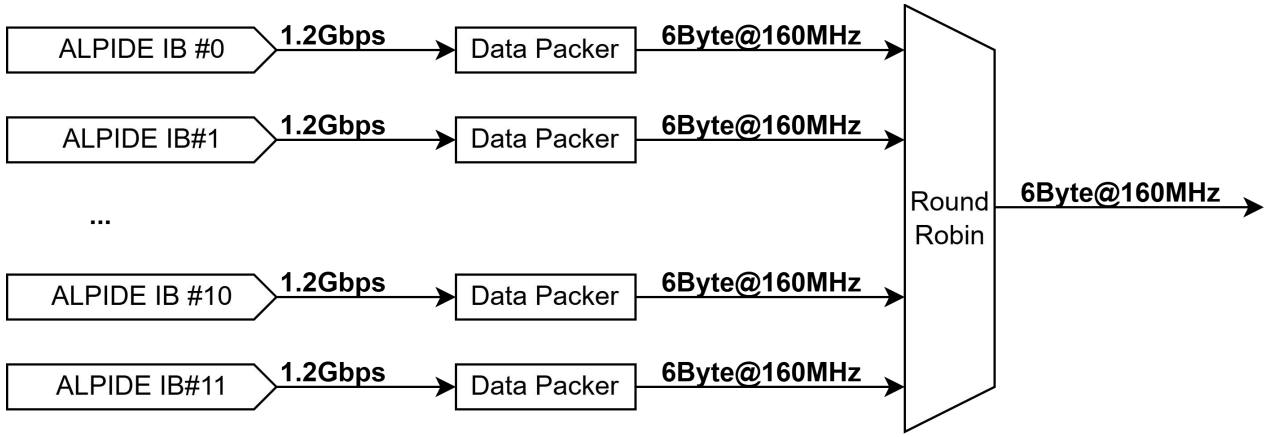

- In IBOB RU, group 12 IB and 4 OB to one lpGBT to balance the bandwidth
- Group the high and low data rate sensors links to balance the bandwidth

# Readout unit and firmware design

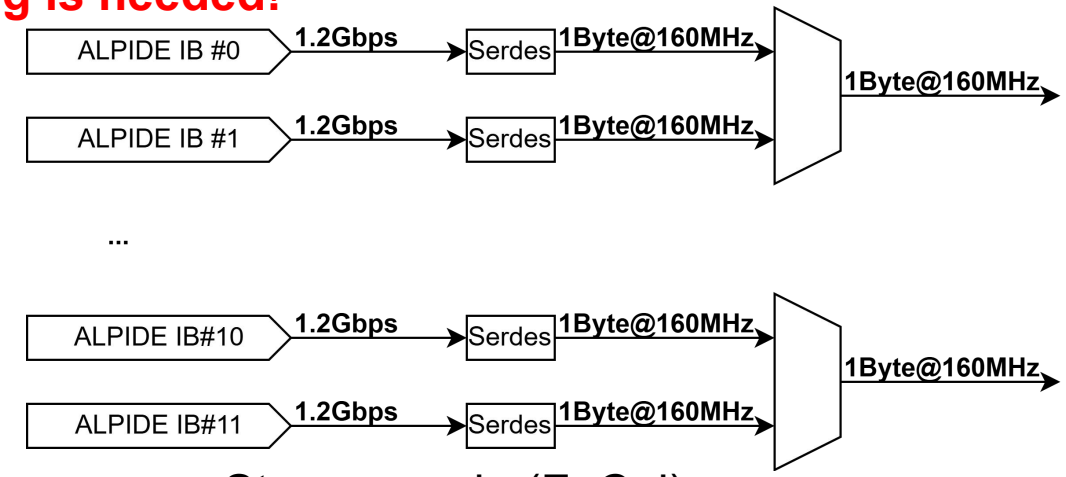
## Packing method simulation

- IBOB RU have 1.2Gbps * 36 + 400Mbps * 12 input elinks, OB RU have 400Mbps * 72 input e-links
- They have 3 * 6 * 1.28Gbps e-links uplink (to CRU)

**Packing and buffering is needed!**




Round Robin (ITS2)
"Pack and readout one by one"

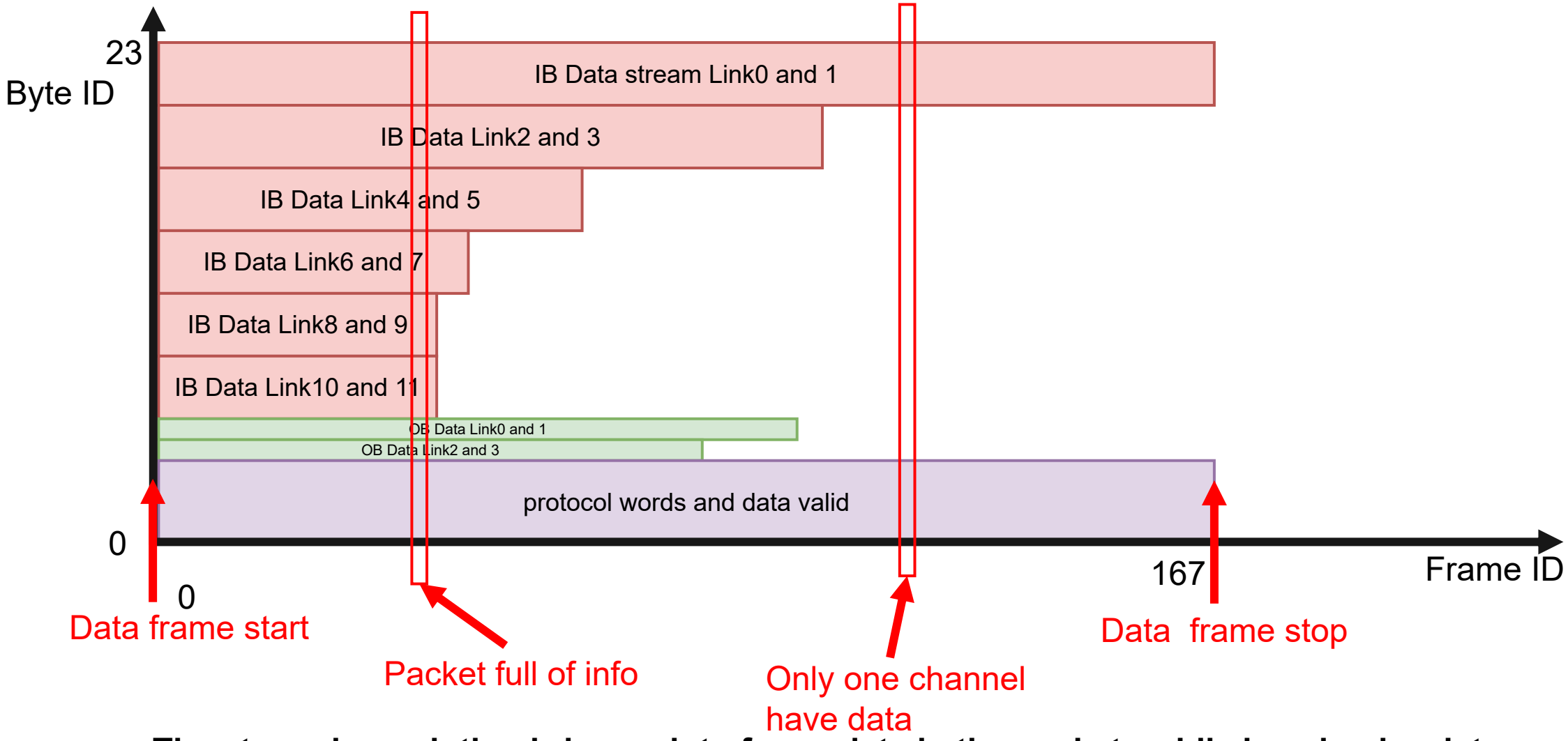



Stream mode (FoCal)
"Merge channels and readout directly"

| | Round Robin | Stream mode |
|---|---|---|
| clock cycle * bits | 2904k | 335k |
| FIFO depth | 11640 | 2117 |

# Readout unit and firmware design

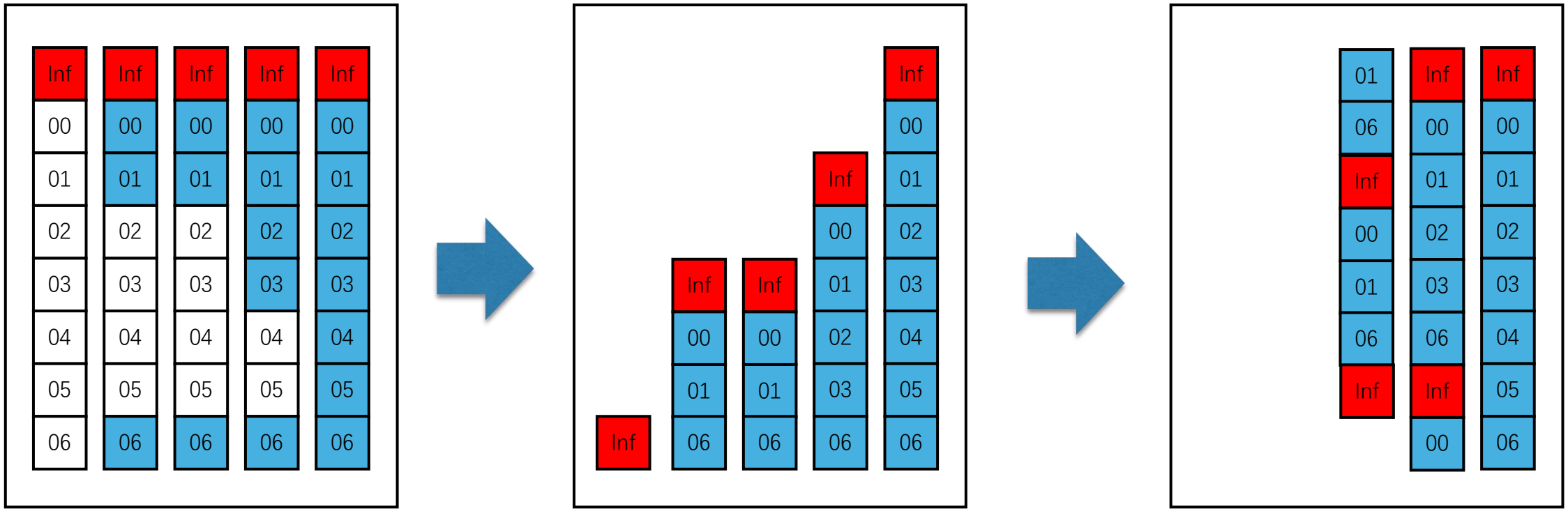
## Typical event packet in stream mode




**The streaming solution brings a lot of zero data in the packets while keeping low latency**

# Readout unit and firmware design

## Zero suppression




Inf **Address of data**

00 **Valid data**

00 **Zeros**

- Uplink data will contain valid channel map which will help zero suppression
- Zero suppression is implemented in CRU
- Software can use address map decode the data

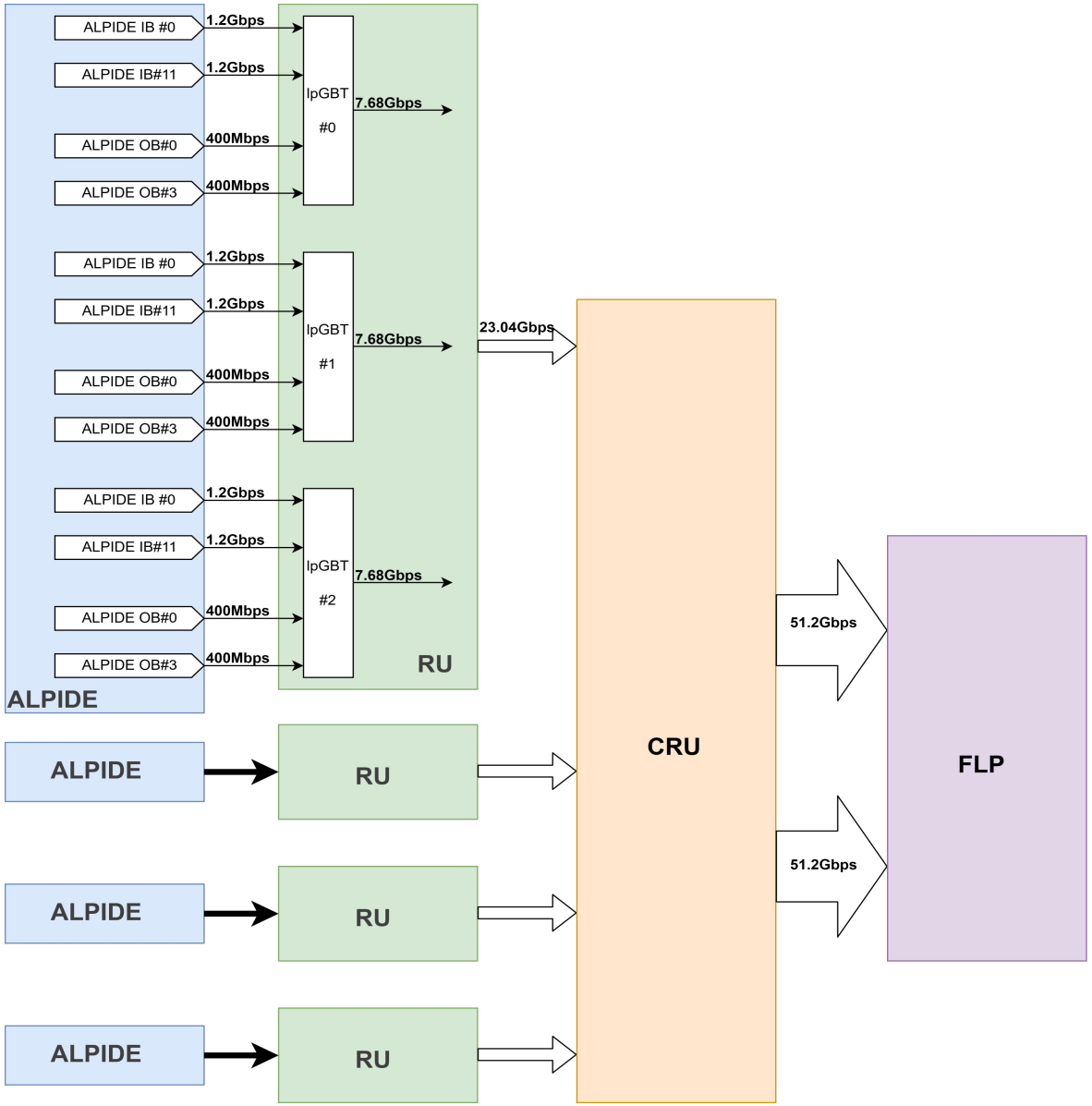
# Summary

- The FoCal-E pixel layer will employ the **ALPIDE** as high granularity component
- ALPIDE will work in **IB or OB mode** depending on their position on detector
- The readout electronics comprise **ALPIDE modules, Transition Cards (TCs), Readout Units (RUs), a Common Readout Unit (CRU), and power boards (PBs)**
- The readout system is similar to ITS2 but uses **different FPGAs, Transceivers and firmware**
- New low latency readout packing method was simulated and show advantage over **latency and resource cost**
- Zero suppression method is introduced to CRU to reduce bandwidth waste

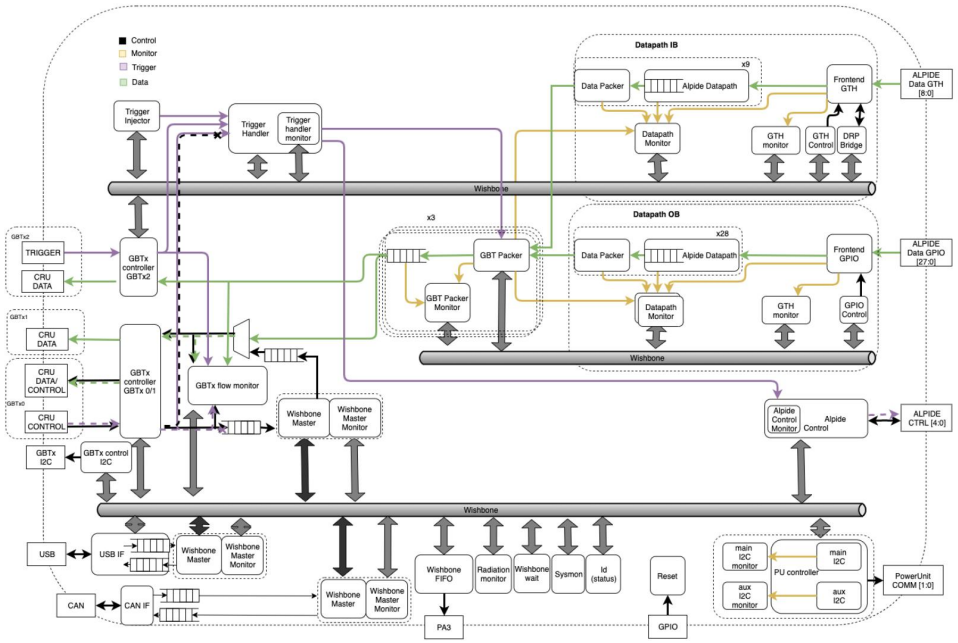
# Thanks for your attention!

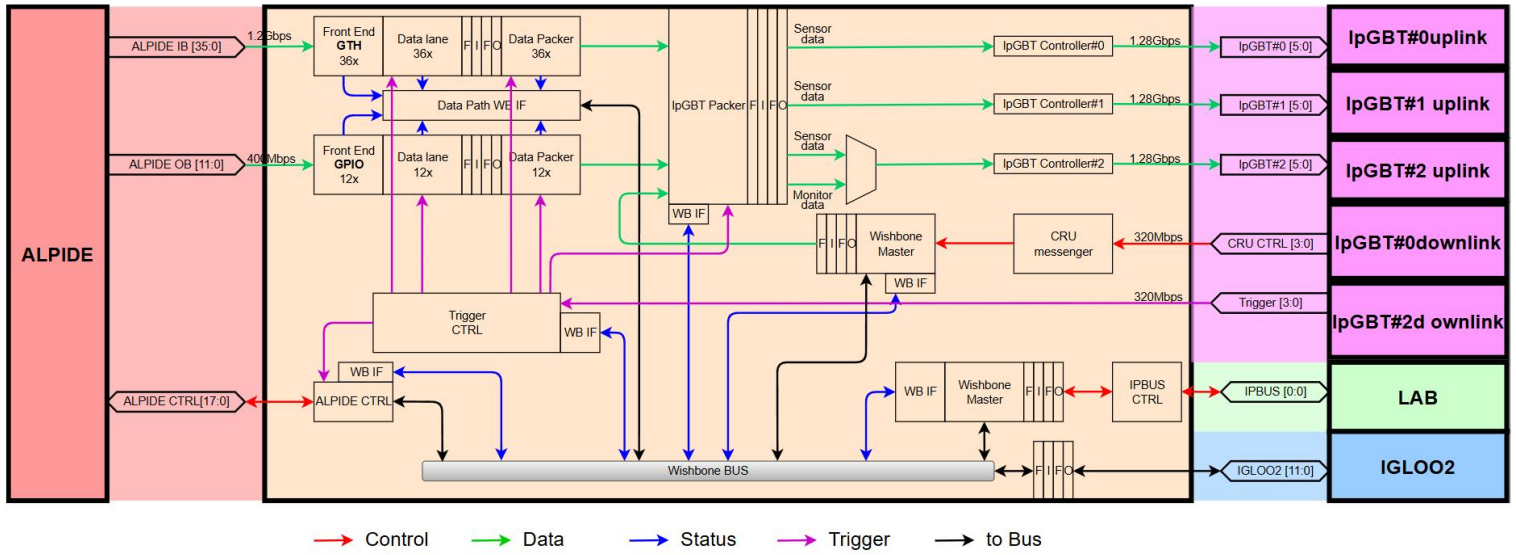
# Backup

# Readout data path



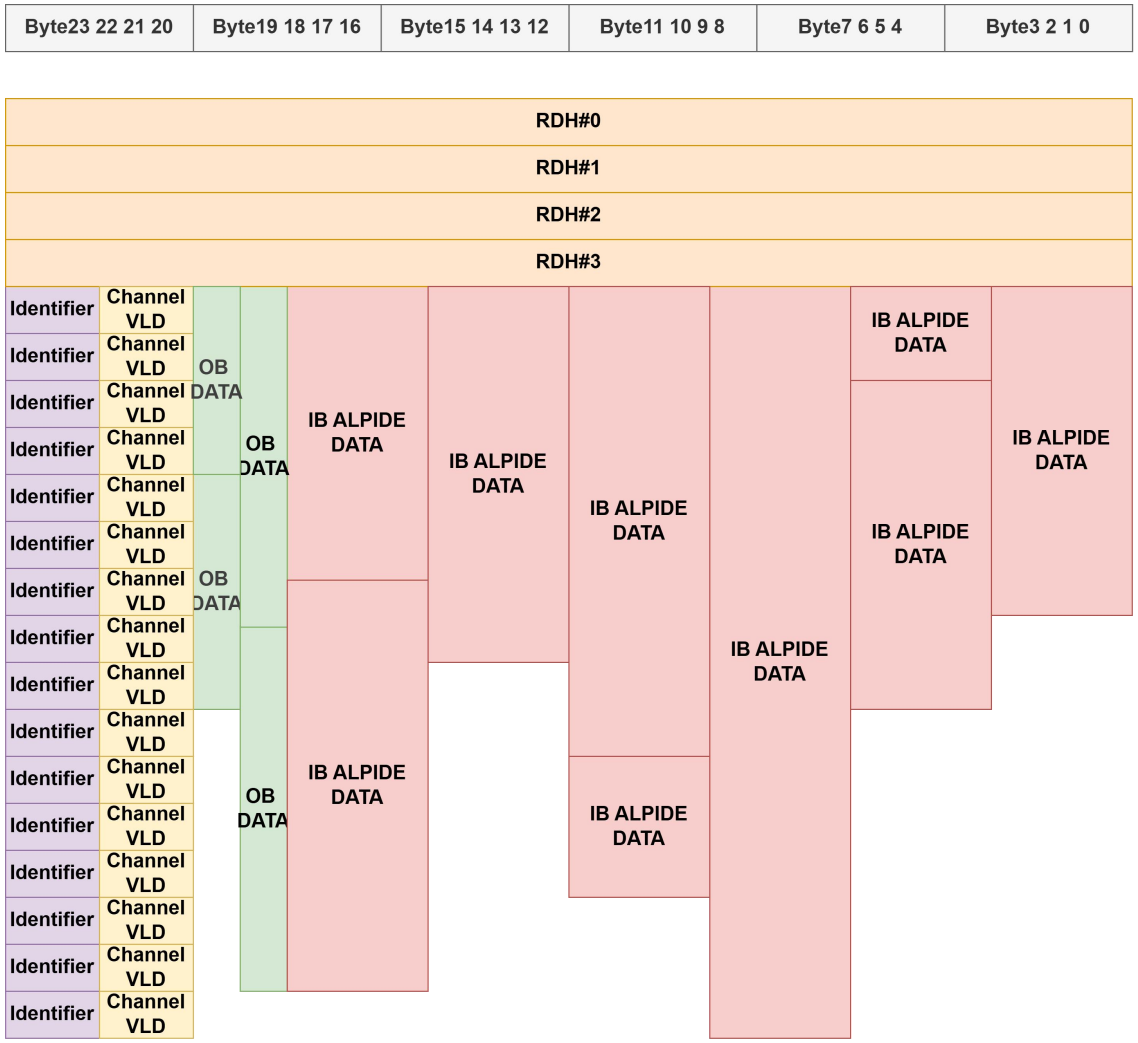
# Firmware




- Move Power board control, CAN BUS to Aux FPGA
- Remove USB interface, add IPBUS for lab debug
- Update GBT packer to lpGBT packer, GBT controller to lpGBT controller (HPIO interface)
- Simplify FW design
- Make the project easy to read and reuse

# Data format




| | NEW 32-BITS | OLD 80-BITS GBT |
|---|---|---|
| Outside of run | 0 00000000 | 0 000000010DEA00000000 |
| | 0 00000000 | 0 000000010DEB00000000 |
| | 1 00000009 | 1 0000000200000004883 |
| "BC" Prefix for payload readability | 0 BC000100 | 0 0000002000100004000 |
| | 0 BC000200 | 0 0000002000200004000 |
| | 0 BC000300 | 0 0000002000300004000 |
| | 0 BC000400 | 0 0000002000400004000 |
| | 0 BC000500 | 0 0000002000500004000 |
| | 0 BC000600 | 0 0000002000600004000 |
| | 0 BC000700 | 0 0000002000700004000 |
| Physics Trigger | 1 BC000802 | 1 0000002000880004010 |
| | 0 BC000900 | 0 0000002000900004000 |
| | 0 BC000A00 | 0 0000002000A00004000 |
| | 0 BC000B00 | 0 0000002000B00004000 |
| | 0 BC000C00 | 0 0000002000C00004000 |
| | 0 BC000D00 | 0 0000002000D00004000 |
| | 0 BC000E00 | 0 0000002000E00004000 |
| | 0 BC000F00 | 0 0000002000F00004000 |
| | 0 BC001000 | 0 0000002001000004000 |
| | 0 BC001100 | 0 0000002001100004000 |
| | 0 BC001200 | 0 0000002001200004000 |

# Simulation math

- **Packing(from 8bit to 48bit)**

$$W_{assem,full} = 8\sum_{j=0}^{P_b-1} j = 8 \cdot \frac{P_b(P_b-1)}{2} \quad W_{assem,rem} = 8\sum_{j=0}^{rem-1} j = 8 \cdot \frac{rem(rem-1)}{2}$$

$$W_{accum,i} = full_i \cdot 8 \cdot \frac{P_b(P_b-1)}{2} + 8 \cdot \frac{rem_i(rem_i-1)}{2}$$

- **Waiting for readout(RR)**

$$W_{tx,i} = 8P_b \sum_{k=0}^{P_i-1} (pos_i + N \cdot k)$$

$$W_{tx,i} = 8P_b \left( P_i \cdot pos_i + N \cdot \frac{P_i(P_i-1)}{2} \right)$$

- **Sum**

$$W_i = W_{accum,i} + W_{tx,i}$$

$$W_i = 8\left[ full_i \cdot \frac{P_b(P_b-1)}{2} + \frac{rem_i(rem_i-1)}{2} + P_b\left(P_i \cdot pos_i + N \cdot \frac{P_i(P_i-1)}{2}\right)\right]$$

$$W_{total} = \sum_{i=0}^{N-1} W_i$$

Round Robin

- **Waiting for readout (one of the links occupy the path)**

$$W_{pair} = 8 \cdot B_{long} \cdot B_{short}$$

$$W_{total} = 8\sum_{i=0}^{N/2-1} B_{(i)} \cdot B_{(N-1-i)}$$

Sequential Merge

# Simulation framework

10us between trigger
Each link generate data

ALPIDE Speed from simulation

Data generate

Based on average rate and poisson random

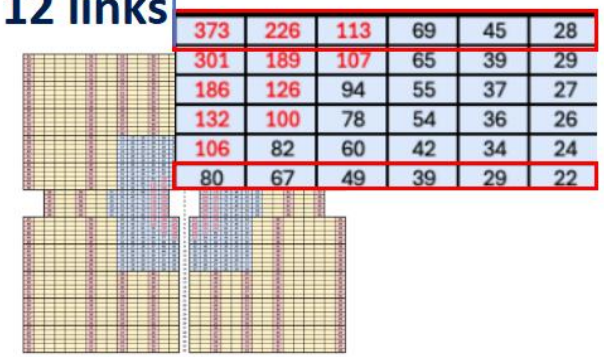
Method#1 RR sorted

Method#2 Sequential Merge

Method#3 RR fixed order

Report&Plot

12 links

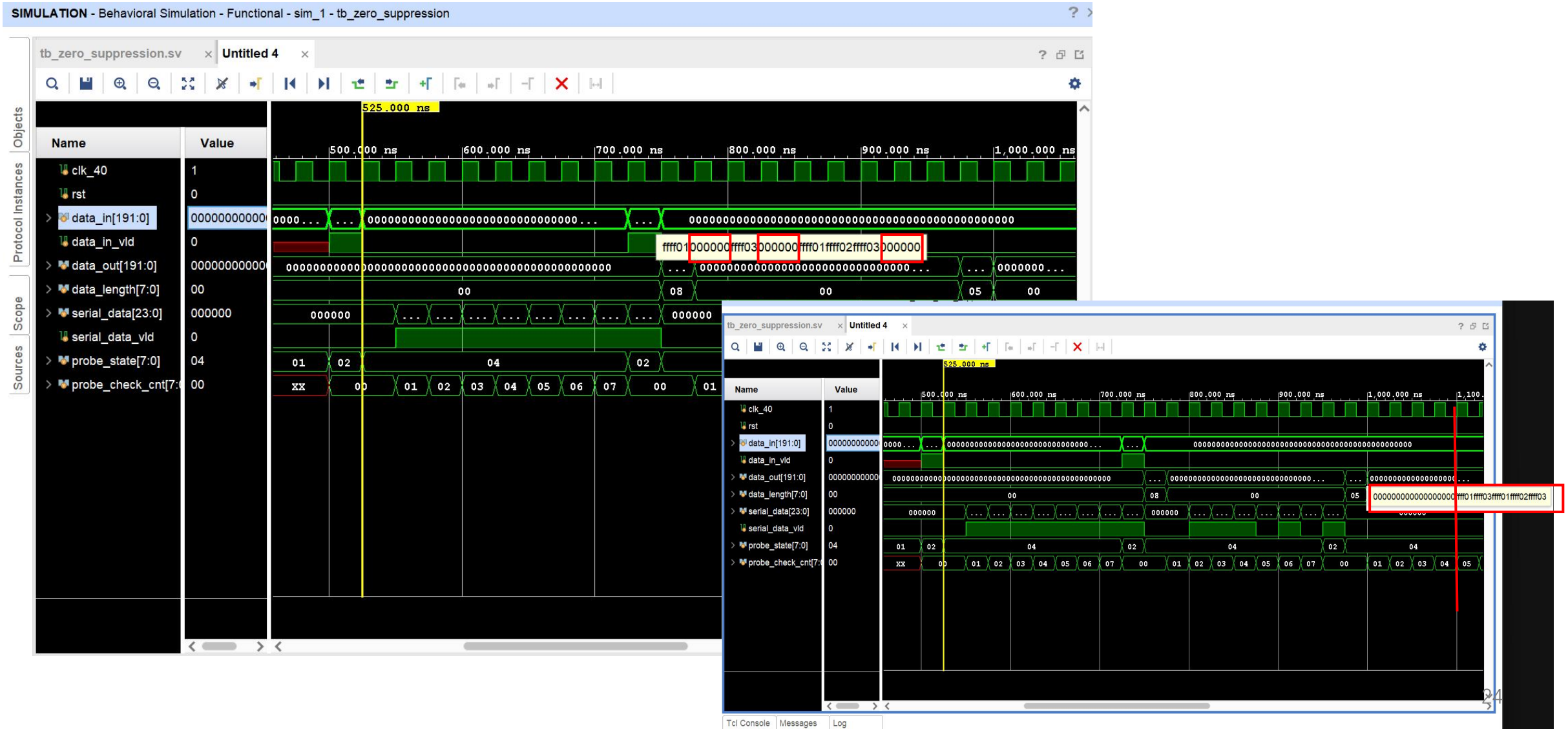


| | | | | | |
|---|---|---|---|---|---|
| 373 | 226 | 113 | 69 | 45 | 28 |
| 301 | 189 | 107 | 65 | 39 | 29 |
| 186 | 126 | 94 | 55 | 37 | 27 |
| 132 | 100 | 78 | 54 | 36 | 26 |
| 106 | 82 | 60 | 42 | 34 | 24 |
| 80 | 67 | 49 | 39 | 29 | 22 |

M1 is impossible in HW design

FIFO depth
bits*cycle
...

# Zero suppression



# Estimation

| Device | LUTs | Cost | GTH | Cost |
|---|---|---|---|---|
| ITS2 KCU060 | 331,680 | 166,866 | 32 | 9 |
| FoCal KCU085 | 497,520 | 311,416 | 56 | 36 |

# Estimation

| | | ITS | FoCal-IBOB | FoCal-OB |
|---|---|---|---|---|
| GTH | | 1.435W<br>9GTH for IB | 5.6W<br>36GTH for IB | 0W |
| Dynamic | Clock | 0.399W | 0.734W | 0.734W |
| | Signal | 0.596W | | |
| | Logic | 0.679W | 1.699W | 1.699W |
| | BRAM | 1.356W | 0.568W | 0.568W |
| | MMCM | 0.228W | | |
| | IO | 0.814W<br>453 IOs | 1.486W | 1.486W |
| | Sysmon | 0.003W | | |
| Static | | 0.768W(KU060) | 1.895W(KU085) | 1.895W(KU085) |
| Total | | 6.28W | 11.98W | 6.38W |