Study of On-chip Data Compression in Readout Logic for High-flux MAPS

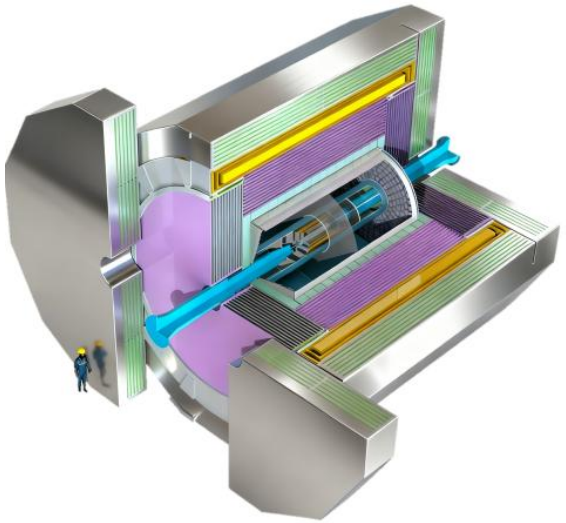
CEPC Vertex MAPS group and ITK MAPS group

Xiaomin WEI Northwestern Polytechnical University (NPU)

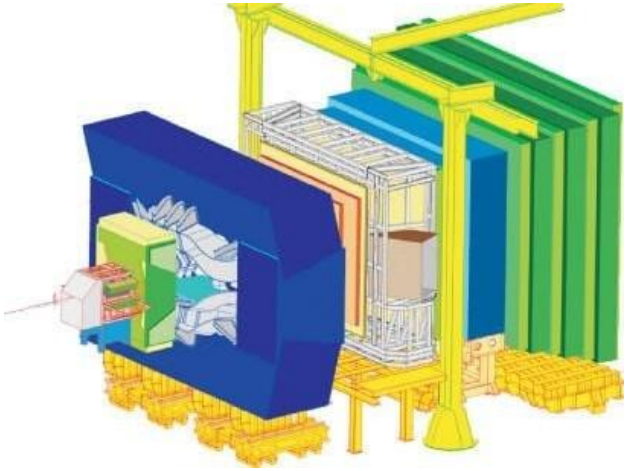
Content

- Motivation
- Data compression for vertex detector
- Data compression for tracker
- Future Work

Motivation



CEPC



LHCb

MAPS is a good candidate for particle detection in both the vertex detector and the inner tracker.

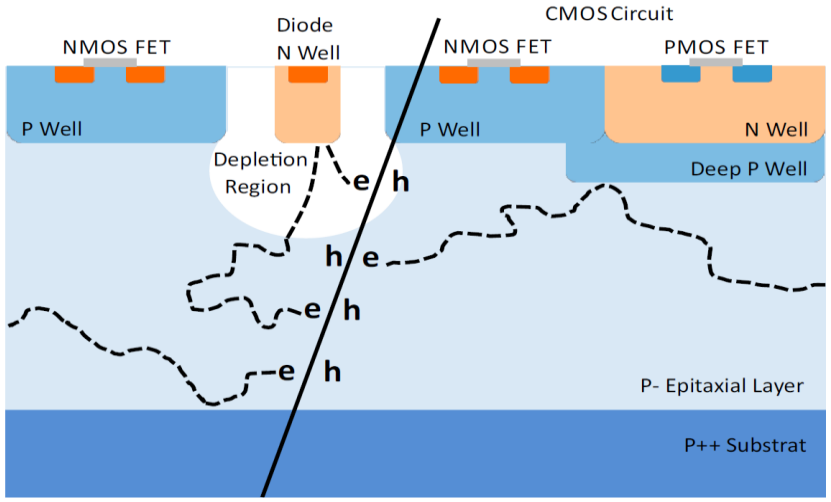
- In some cases, the data flux is high. Eg.
  - CEPC vertex detector 39M/s.cm^2 => ~10Gbps/chip
  - LHCb inner tracker 100M/s.cm^2 => ~12.8Gbps/chip
  - FCC-ee IDEA/AGORA 200M/s.cm^2

=> High data bandwidth and high power consumption!

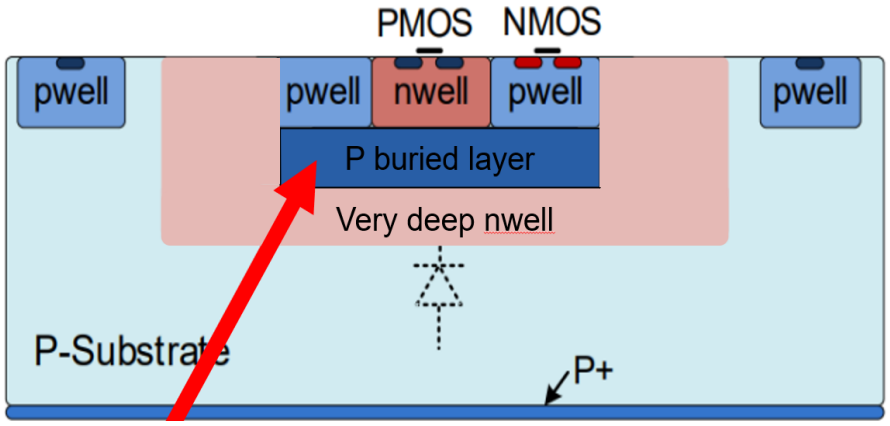
- Possibility of data reduction
  - The occupancy is small, the data is still sparse.
  - The data are clustered.
  - BXID, part of address can be shared.
  - Some information can be used inside the chip without output.
  - …

Vertex detector and Inner Tracker

According to the different requirements, the sensor technology and the readout logic are different.



LV-MAPS



HV-MAPS

Table 2.3: Parameters and layout of the CEPC tracker including VTX, ITK, TPC, and OTK. The column labeled $\pm z$ shows the half-length of the barrel layers, and the z position of the endcap disks. The column labeled σ_ϕ and σ_t represent the spatial resolution in the bending direction and time resolution, respectively.

Components		Radius R [mm]	$\pm z$ [mm]	Material [X_0]	σ_ϕ [μm]	σ_t [ns]
Beam pipe		10.55	85.0	0.454%	—	—
VTX	Layer 1	11.1	80.7	0.067%	5	100
	Layer 2	16.6	121.1	0.059%	5	100
	Layer 3	22.1	161.5	0.058%	5	100
	Layer 4	27.6	201.9	0.061%	5	100
	Layer 5	39.5	341.0	0.280%	5	100
	Layer 6	47.9	341.0	0.280%	5	100
Beam pipe protective cylinder		66.3	462.0	0.19%	—	—
ITK Barrel	Layer 1 (ITKB1)	235.0	493.3	0.68%	8	3–5
	Layer 2 (ITKB2)	345.0	704.8	0.68%	8	3–5
	Layer 3 (ITKB3)	555.6	986.6	0.68%	8	3–5
OTK Barrel	Layer 4 (OTKB)	1,800.0	2,840.0	1.58%	10	0.05
TPC	Inner wall	600.0	2,900.0	0.45%	—	—
	Gas	605.4–1,779.6	2,750.0	1.00%	110–144	—
	Outer wall	1,800.0	2,900.0	0.69%	—	—
		R_{in}	R_{out}			
ITK Endcap	Disk 1 (ITKE1)	82.5	244.7	505.0	0.76%	8	3–5
	Disk 2 (ITKE2)	110.5	353.7	718.5	0.76%	8	3–5
	Disk 3 (ITKE3)	160.5	564.0	1,000.0	0.76%	8	3–5
	Disk 4 (ITKE4)	220.3	564.0	1,489.0	0.76%	8	3–5
OTK Endcap	Disk 5 (OTKE)	406.0	1,816.0	2,910.0	1.37%	10	0.05

Ref. CEPC Ref-TDR

Vertex detector and Inner Tracker

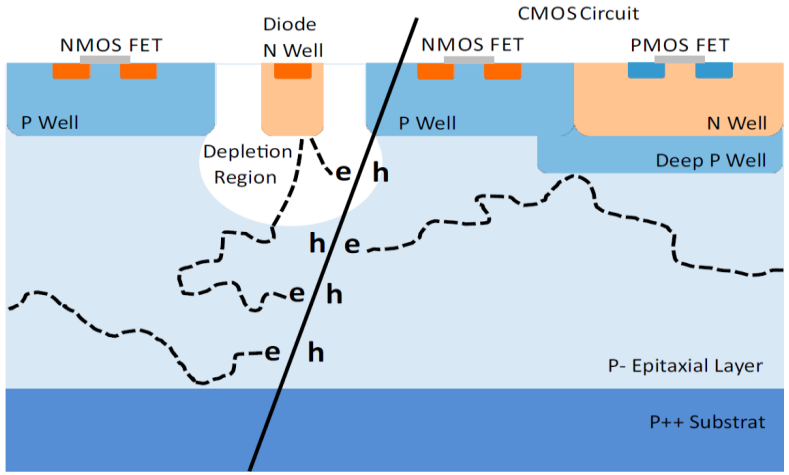
Vertex detector

- High spatial resolution
- LV MAPS ： low material and small noise
- Cluster size： ~ 2-4 pixels

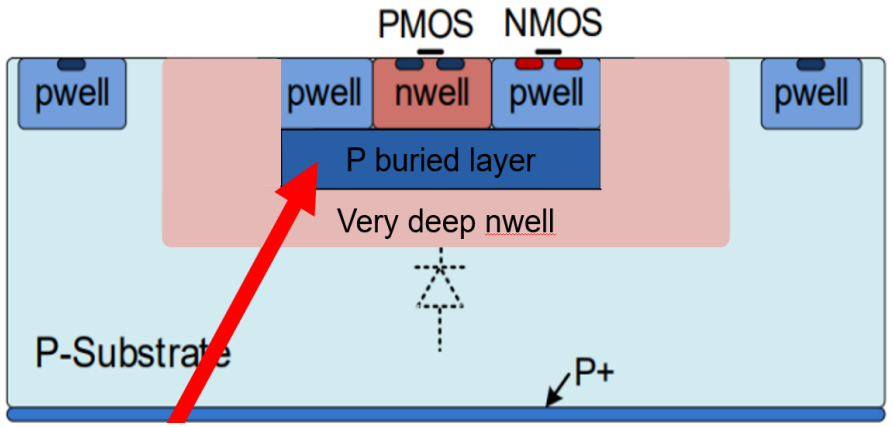
Inner Tracker

- High time resolution
- HV MAPS : fast charge collection and high radiation tolerance
- Cluster size： ~1-2 pixels

Different data compression methods can be adopted in the readout logic circuits.



LV-MAPS



HV-MAPS

Content

- Background
- Data compression for vertex detector
- Data compression for tracker
- Future Work

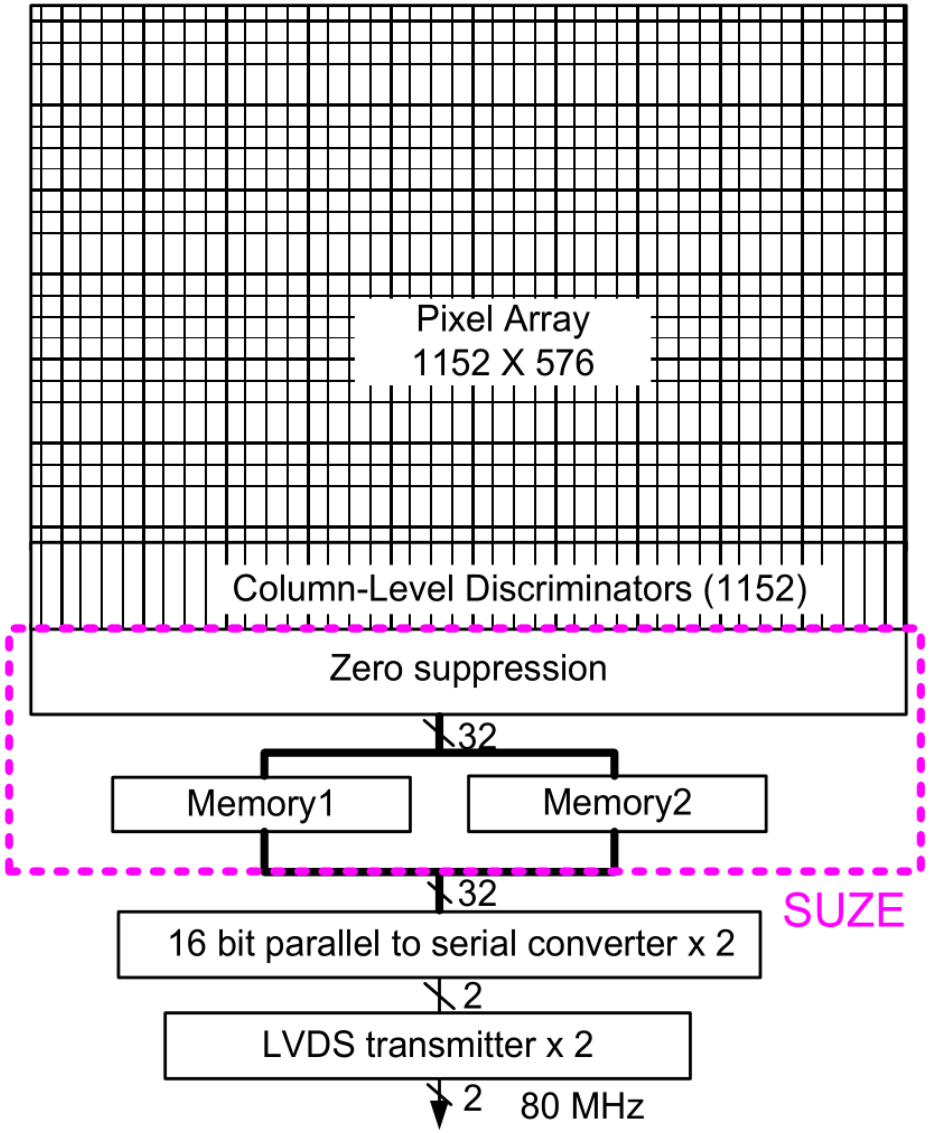
Current data compression of MAPS for vertex detector

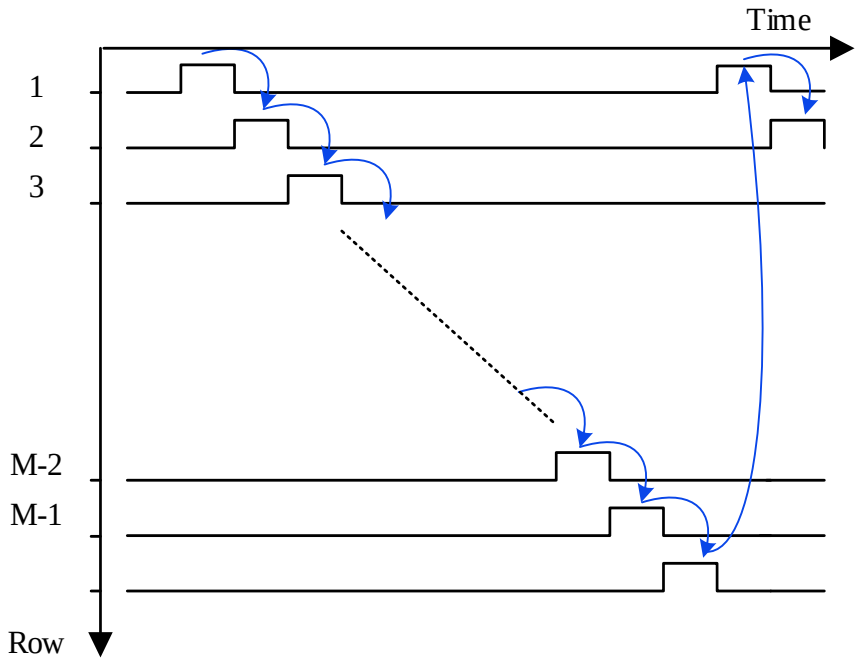
For the application of particle detection, the occupancy is low, so zero suppression is popular.

The realization is related to the readout architecture.

- Rolling shutter (MIMOSA26)
- Data driver readout (ALPIDE)

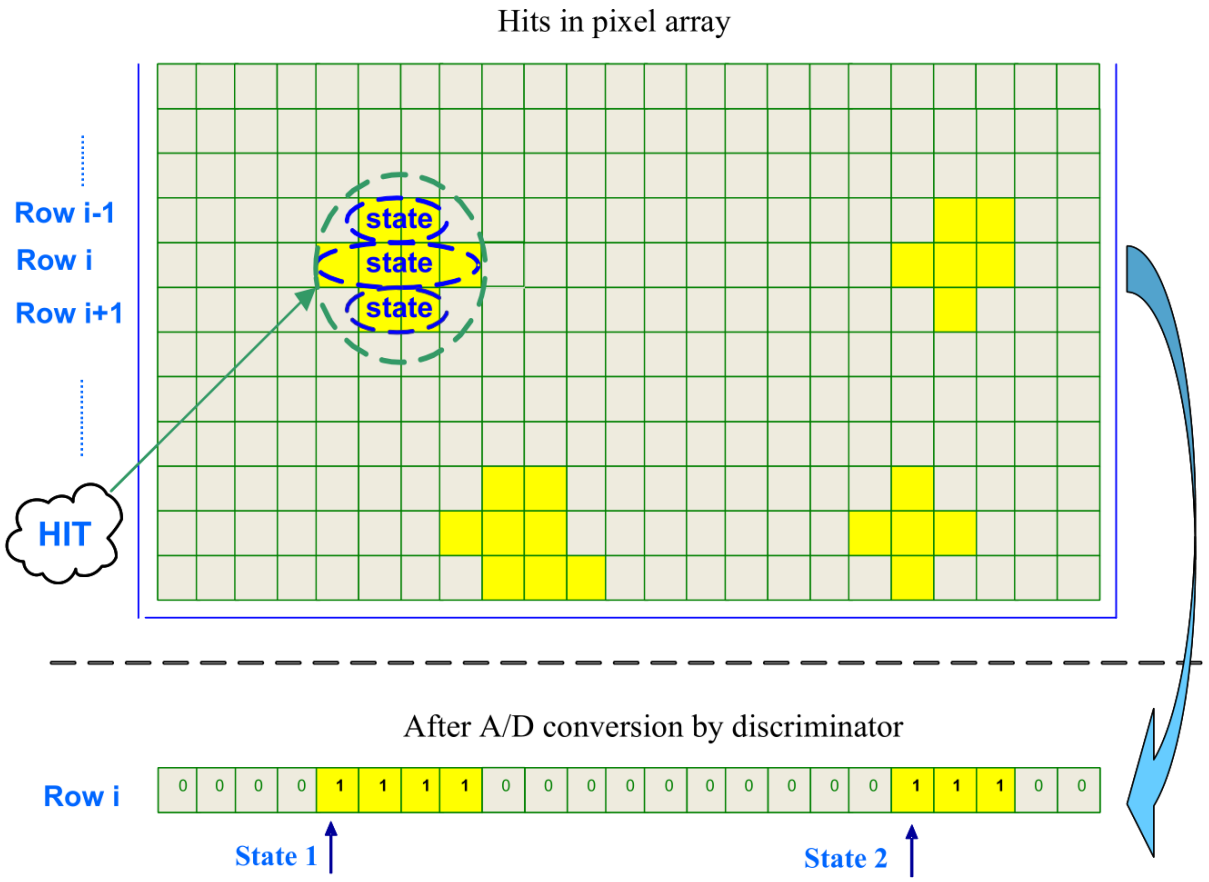
Rolling shutter readout (MIMOSA26)

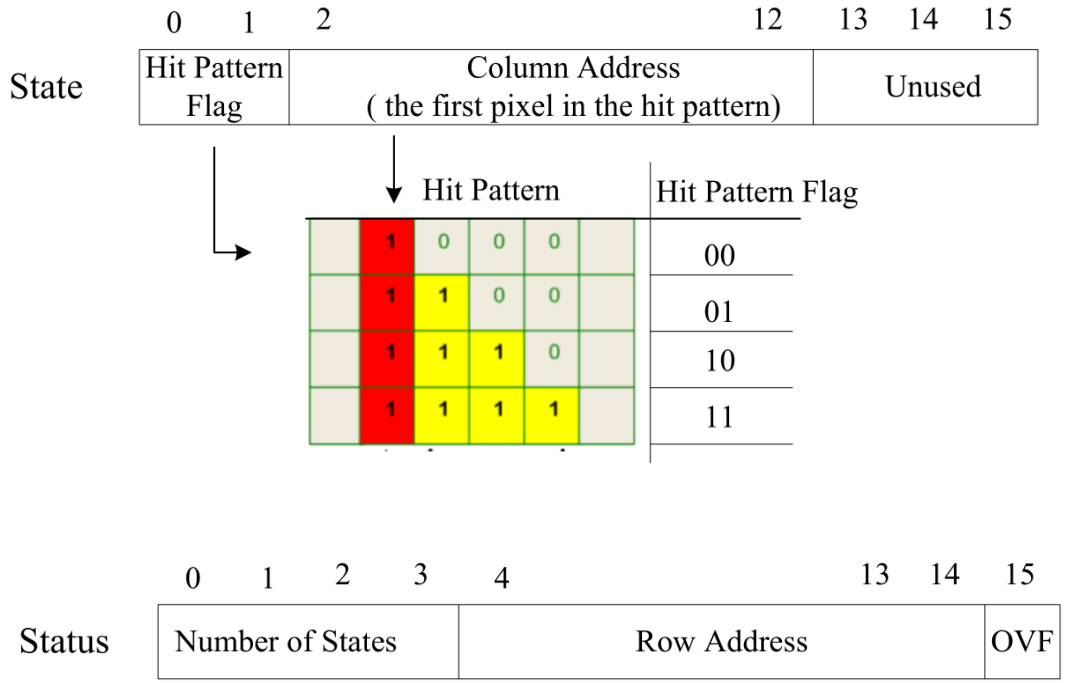




- Pixels are read out row by row
- The information is digitized at column level
- Data are compressed before entering the FIFO.

Data compression in MIMOSA26





Compression method：

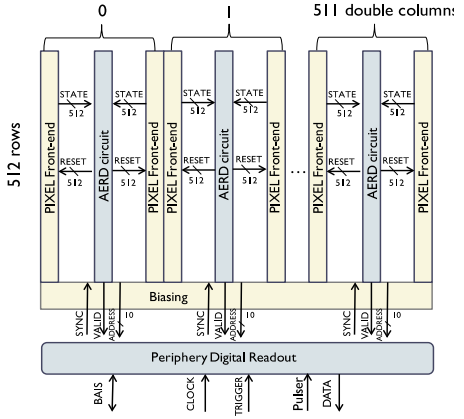
- Remove zeros
- Adjacent data compressed

Reference： A. Himmi, G.Doziere, O. Torheim, C.Hu-Guo M.Winter. Zero Suppression Micro-Circuit for Binary Readout CMOS Monolithic Sensors. TWEEP. Paris; 2009.

Data Driven （ ALPIDE ）

Only the non-zero data are read out .

Reference： P. Yang,…, et al, Low-power priority Address-Encoder and Reset-Decoder data-driven readout for Monolithic Active Pixel Sensors for tracker system, NIMA, 785(2015)



The first non-zero address is read out, and then is reset to read the next one.

Address	Data in pixels		Address
0000000000	0	0	0000000001
0000000010	0	0	0000000011
0000000100	1	1	0000000101
0000000110	1	1	0000000111
0000001000	0	1	0000001001
0000001010	0	0	0000001011
0000001100	0	0	0000001101
0000001110	0	1	0000001111
0000010000	0	0	0000010001
0000010010	0	0	0000010011

“0000000100”

Output of the priority encoding

Address	Data in pixels		Address
0000000000	0	0	0000000001
0000000010	0	0	0000000011
0000000100	0	1	0000000101
0000000110	1	1	0000000111
0000001000	0	1	0000001001
0000001010	0	0	0000001011
0000001100	0	0	0000001101
0000001110	0	1	0000001111
0000010000	0	0	0000010001
0000010010	0	0	0000010011

“0000000101”

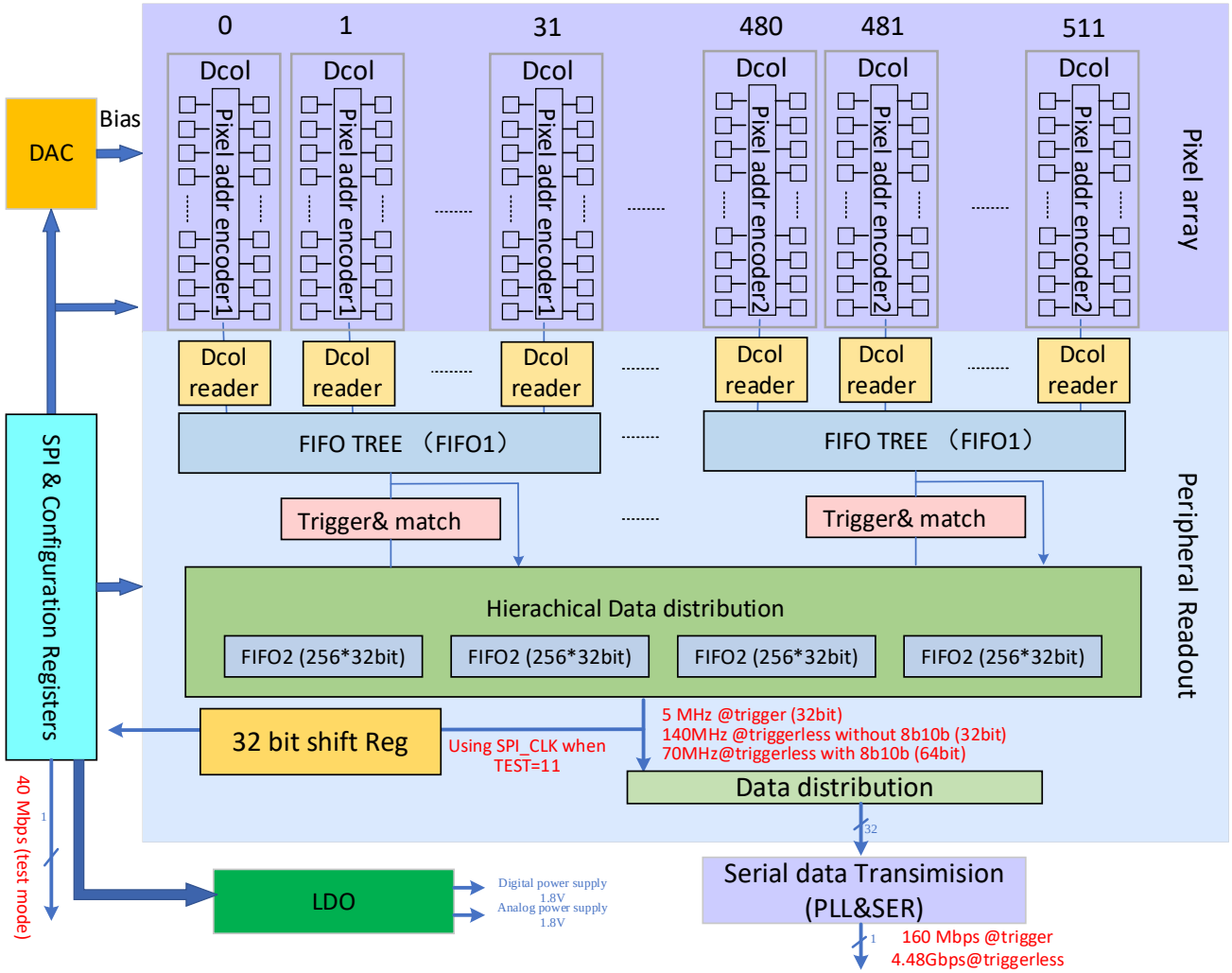
Output of the priority encoding

Address	Data in pixels		Address
0000000000	0	0	0000000001
0000000010	0	0	0000000011
0000000100	0	0	0000000101
0000000110	1	1	0000000111
0000001000	0	1	0000001001
0000001010	0	0	0000001011
0000001100	0	0	0000001101
0000001110	0	1	0000001111
0000010000	0	0	0000010001
0000010010	0	0	0000010011

“0000000111”

Output of the priority encoding

Our design of TaichuPix chip for CEPC

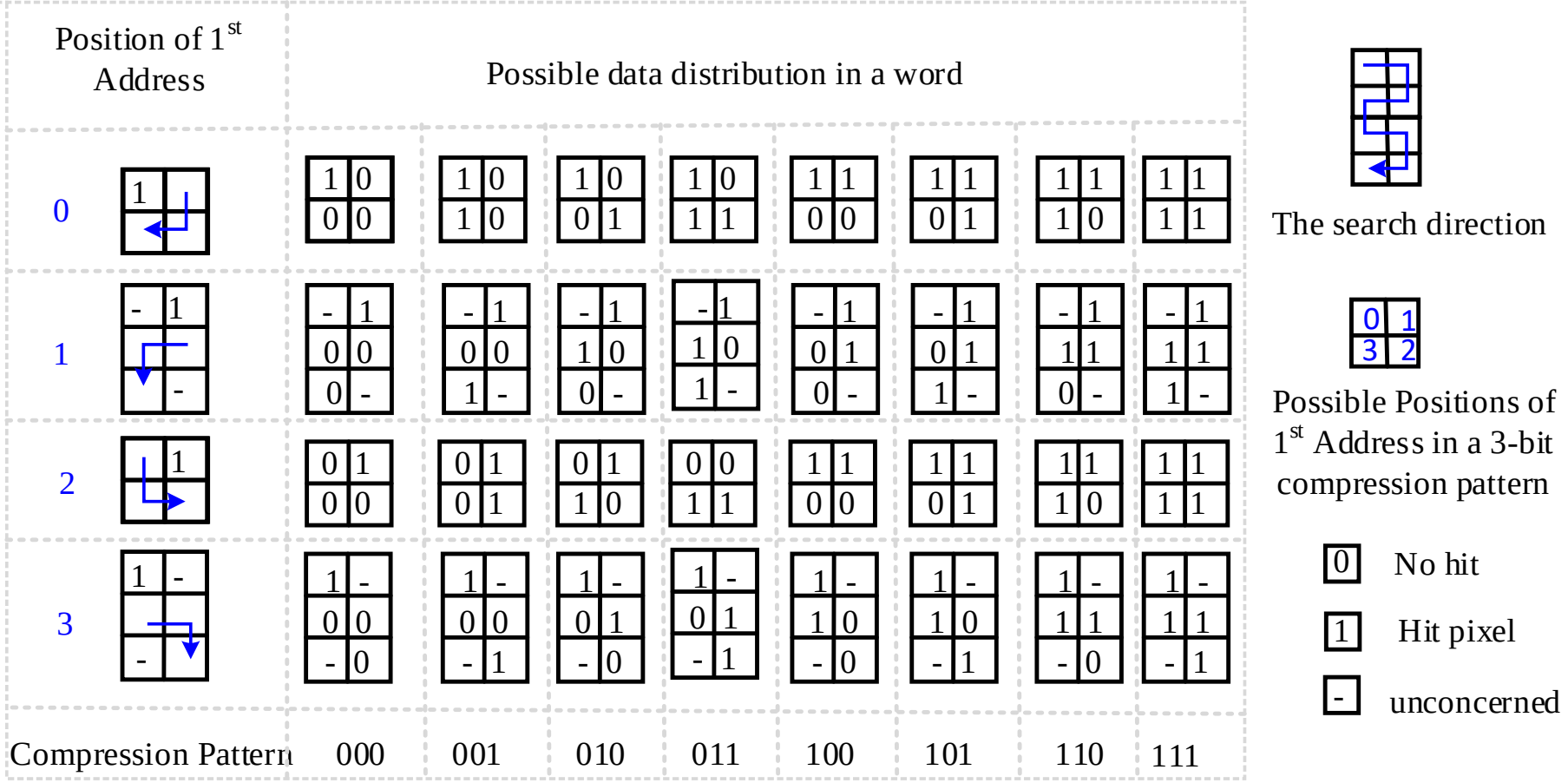


We combined the data suppression in ALPIDE/FEI3 and MIMOSA26.

- Zero suppression: Data driven readout in column level (like ALPIDE/FEI3)
- Data compression: packaging the adjacent addresses (similar with MIMOSA26)

Column level data compression (TaichuPix)

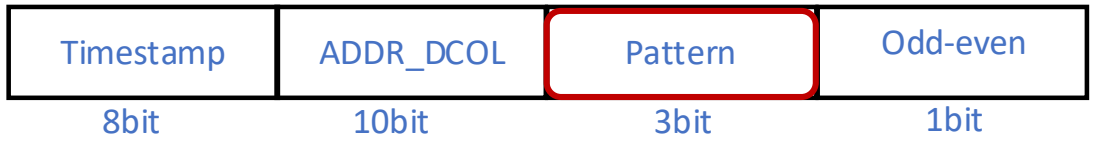
- Eg: Recording the address of the first pixels in a package, the following three pixels are indicated by a three-bit code, where “0” indicates no hit in the pixel and “1” indicates a hit pixel.
- The addresses can be recovered from the first address and the following compression pattern.



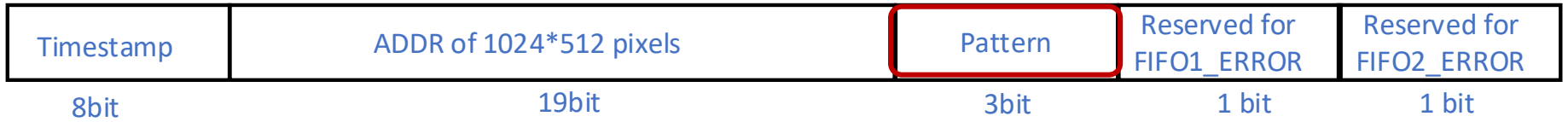
Example of Data compression in peripheral logic

Compression ratio

- Save the FIFO volume, reduce the required readout data rate



Data format of FIFO1



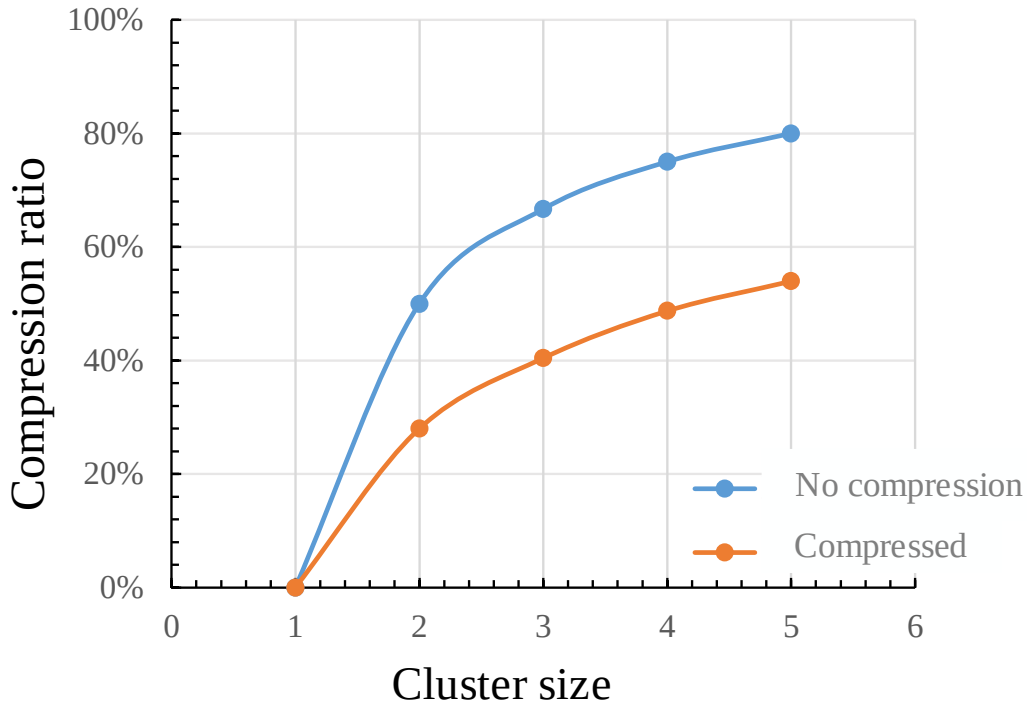
Data format of FIFO2 and output data

Number of Pixels in a package	FIFO1 No	FIFO1 YES	FIFO1 Compression ratio	FIFO2 No	FIFO2 YES	FIFO2 Compression ratio
One	19	22	1.16	29	32	1.10
Two	38	22	0.58	58	32	0.55
Three	57	22	0.38	87	32	0.37
Four	76	22	0.29	116	32	0.28

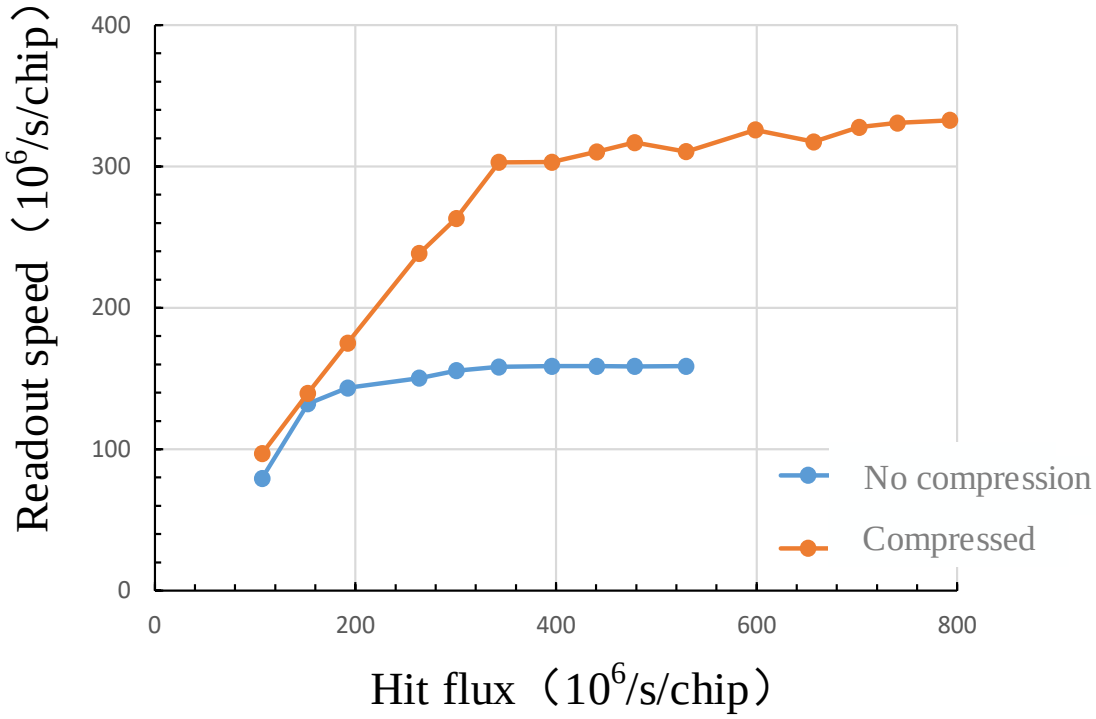
Compression ratio in TaichuPix

Simulation results of compression ratio

A 50 % data reduction can be achieved for an average cluster size of 3



(a)

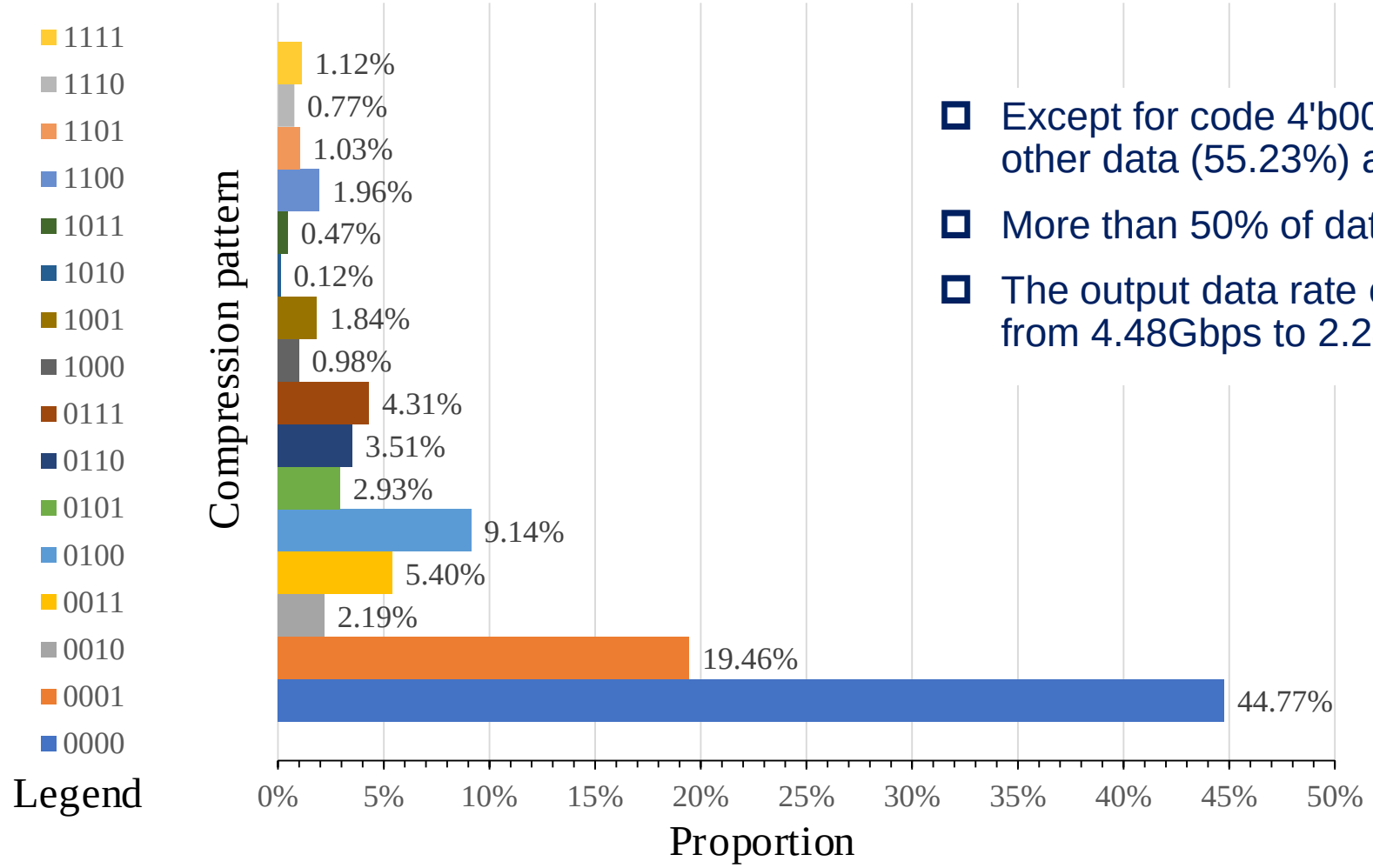


(b)

Simulation of TaichuPix3

(a) Compression ratio vs cluster size (b) Readout speed vs hit flux (the cluster size is 3)

Test Results with TaichuPix3



- Except for code 4'b0000 (44.77%), all other data (55.23%) are compressed.
- More than 50% of data is reduced.
- The output data rate can be reduced from 4.48Gbps to 2.24Gbps.

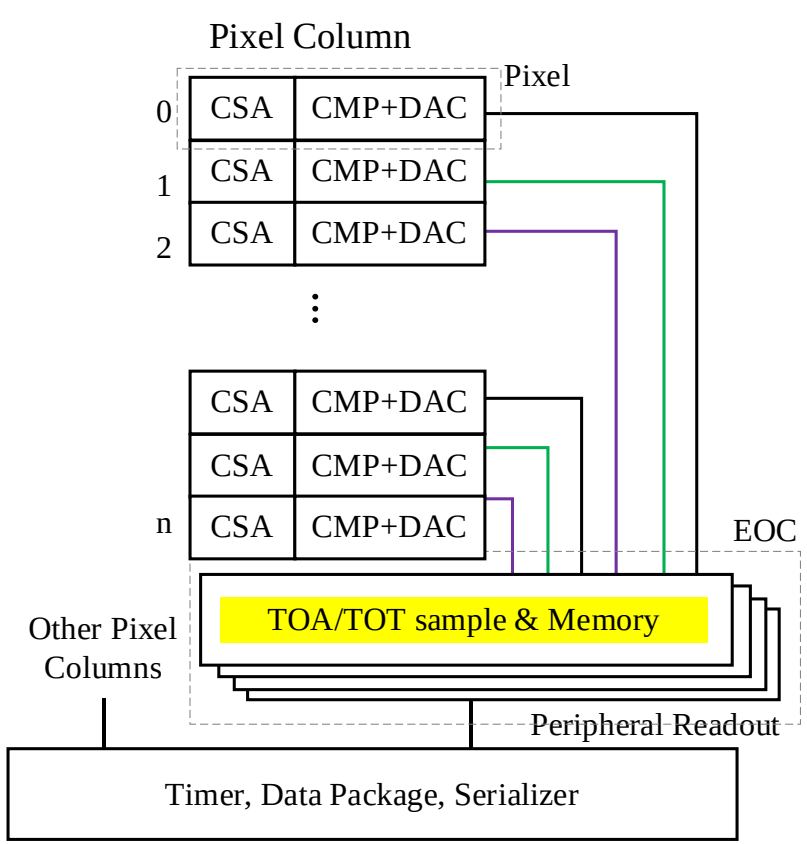
Statistics of each compressed code appearing under Strotium-90 source irradiation with TaichuPix3

Content

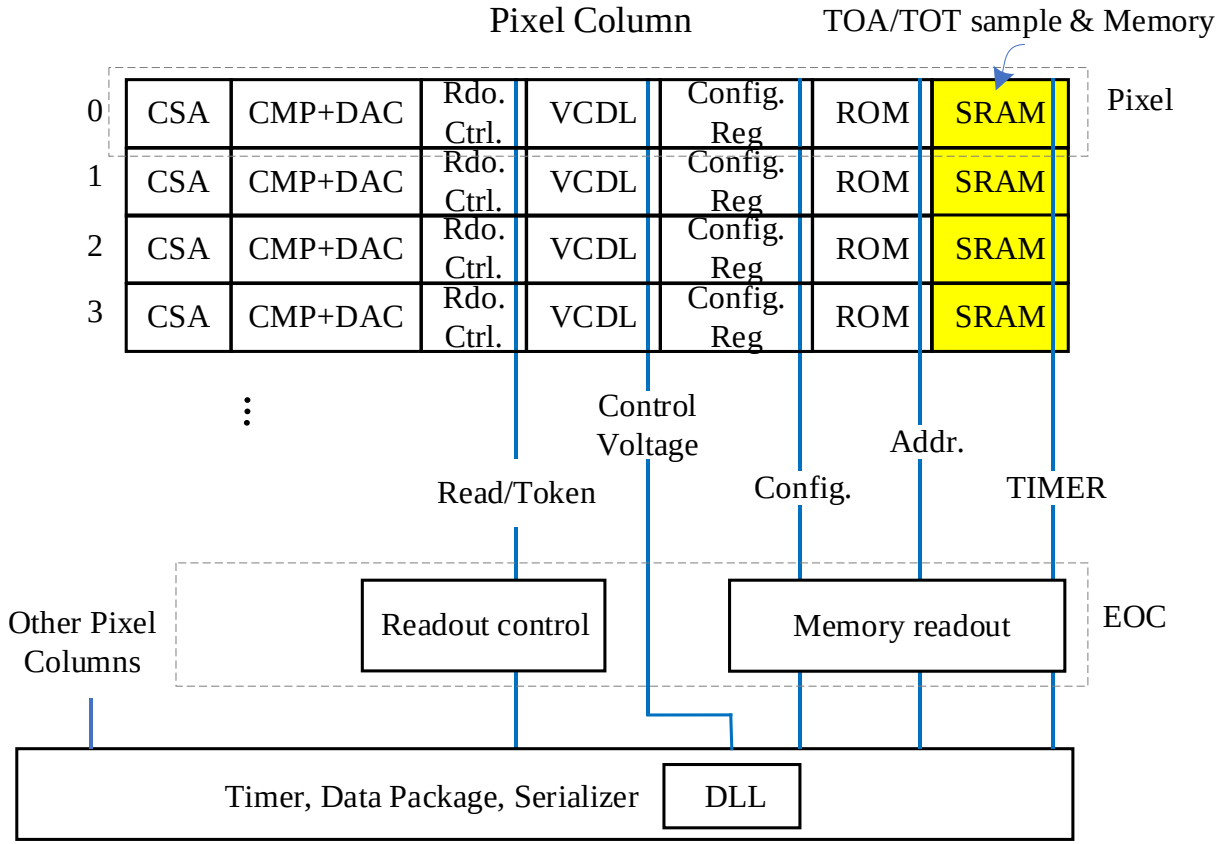
- Background
- Data compression for vertex detector
- Data compression for inner tracker
- Future Work

Readout architectures of inner tracker

Ref. Xiaomin Wei et al 2026 JINST 21 C04075



(a)

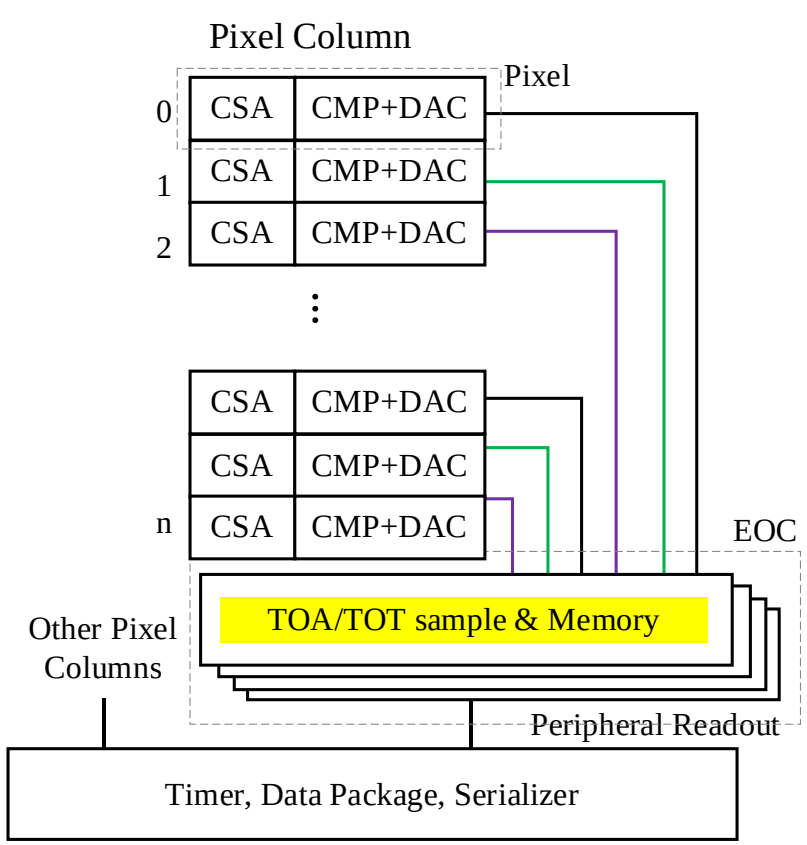


(b)

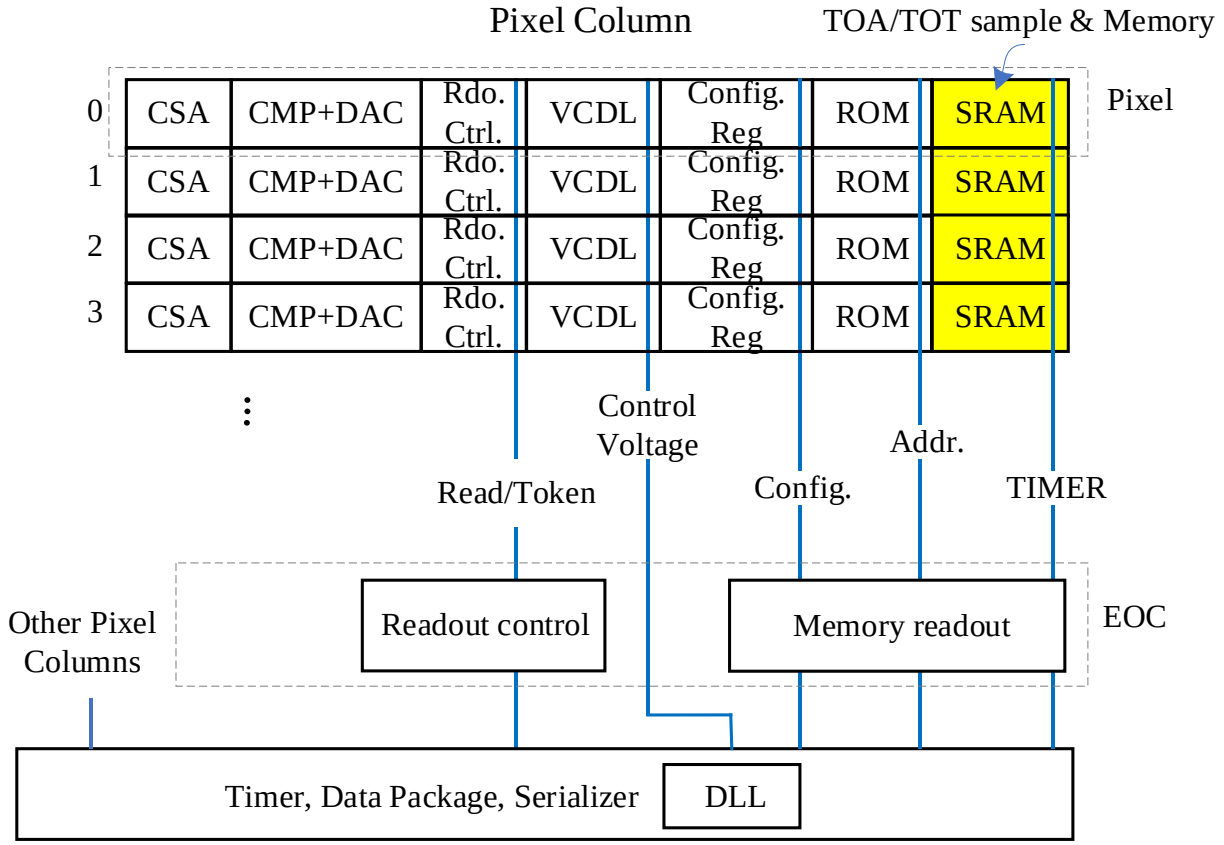
Block diagrams of COFFEE3 (a) the architecture 1 for triple well process and (b) the architecture 2 for the process with p-type buried layer isolation

Readout architectures of inner tracker

Ref. Xiaomin Wei et al 2026 JINST 21 C04075



(a)



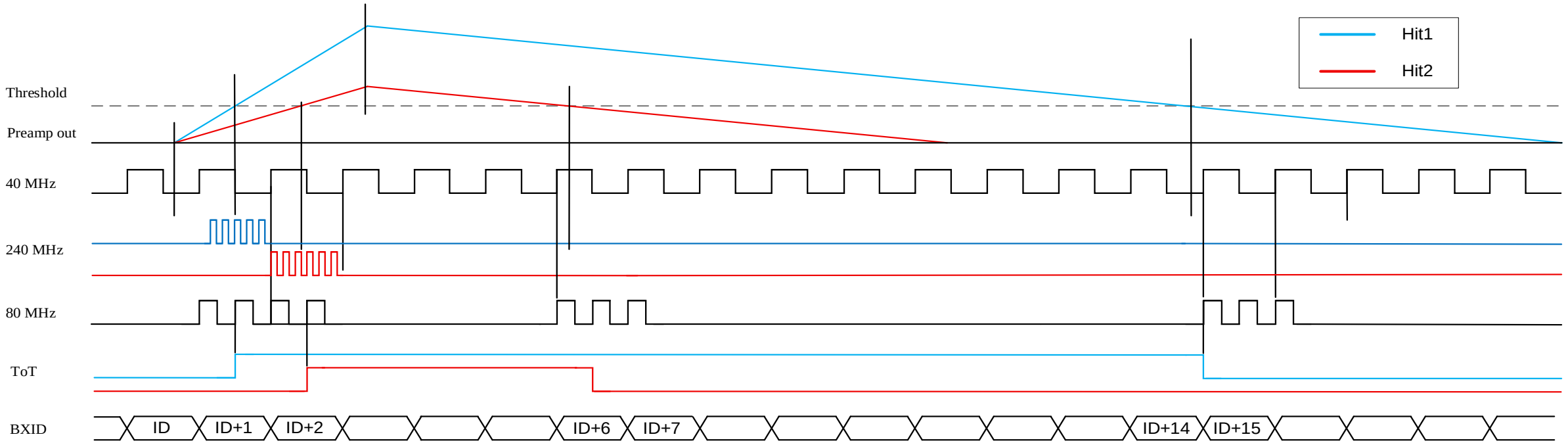
(b)

- Hit addresses and BXID are of primary concern.
- TOA, Fine TOA and TOT are measured to achieve high time resolution.

Data compression strategies

- Zero suppression by data-driven (like FEI3)
- On-chip BXID correction
  - TOA (both coarse and fine) and TOT can be processed on-chip and do not need to be output externally.
- New data format
  - A well-designed compact data format facilitates data reduction

On-chip BXID correction

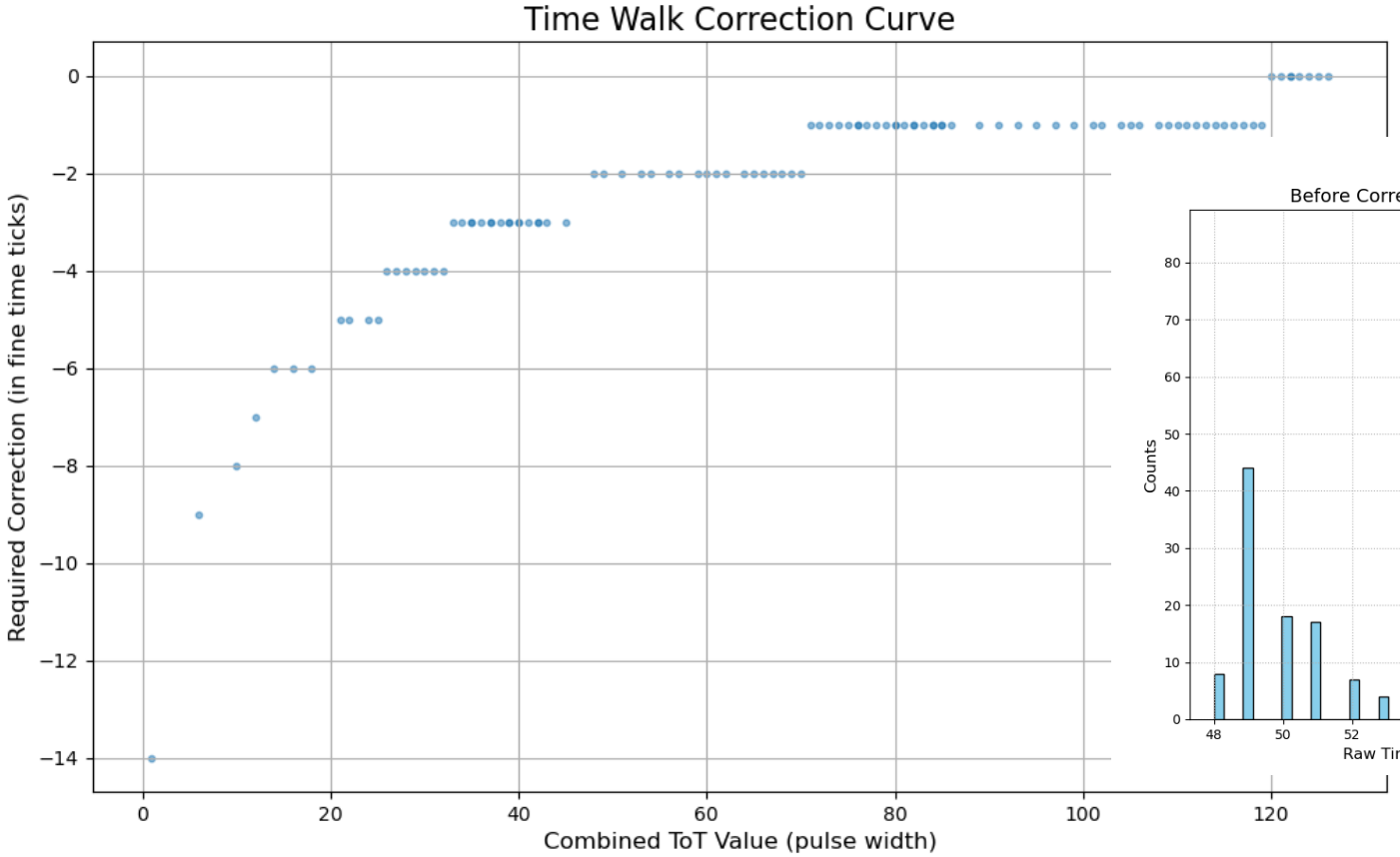


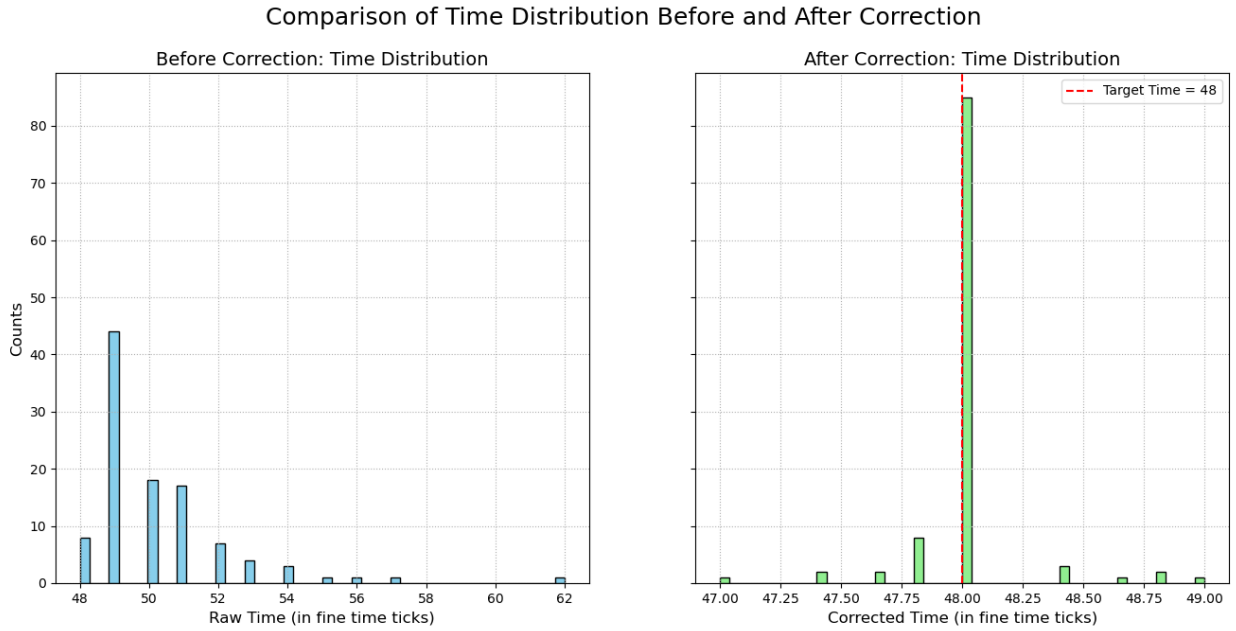
example	ToT[7:1]	ToT[0]	BXID	Fine ToA	ΔBXID	TrueToA	Qin from TOT	ΔToA	ToT
Hit1	14	1	ID+1	3	1	ID	1100e	12.5ns	362.5ns
Hit2	4	0	ID+2	3	2	ID	225e	37.5ns	100ns

TOT→ΔBXID → True BXID

On-chip BXID correction

BXID is TOA after time walk correction, which is realized by subtracting the time working according TOT from TOA.





The relation of TOT and TOA is simplified by adopting a piecewise linear function to approximate the nonlinear curve. The TOA after correction is aligned to a certain BXID without time walk.

On-chip BXID correction

- Compression ratio: 74%

  BXID:12bit

  ADDR: 16bit

  TOA:12bit

  FTOA: 3bit

  TOT: 7 bit

- Data after zero suppression and before BXID correction:

  38 bits (ADDR+TOA+FTOA+TOT)

- Data after BXID correction:

  28 bits (ADDR+BXID)

New data format with shared BXID segment (1)

- Define four kinds of data package
  - Normal compact package is used for reducing the data amount.
  - The whole information can be output in calibration package.

Compression performance degrades below 75 % when a package contains fewer than 8.

Normal	b'00	Chip	BXID	Col	Row	
Normal Compact	b'01	Chip	BXID	NumHits		
	Col 1	Row 1		Col 2	Row 2	
	•••			•••		
	Col N	Row N		(0x5555, for odd NHits)		
Calibration	b'10	Chip	BXID	Col	Row	
	0x0C	ToT	ToA	0x0C	ToT	ToA
Status	b'11	Chip	BXID	Type	0xAAA	

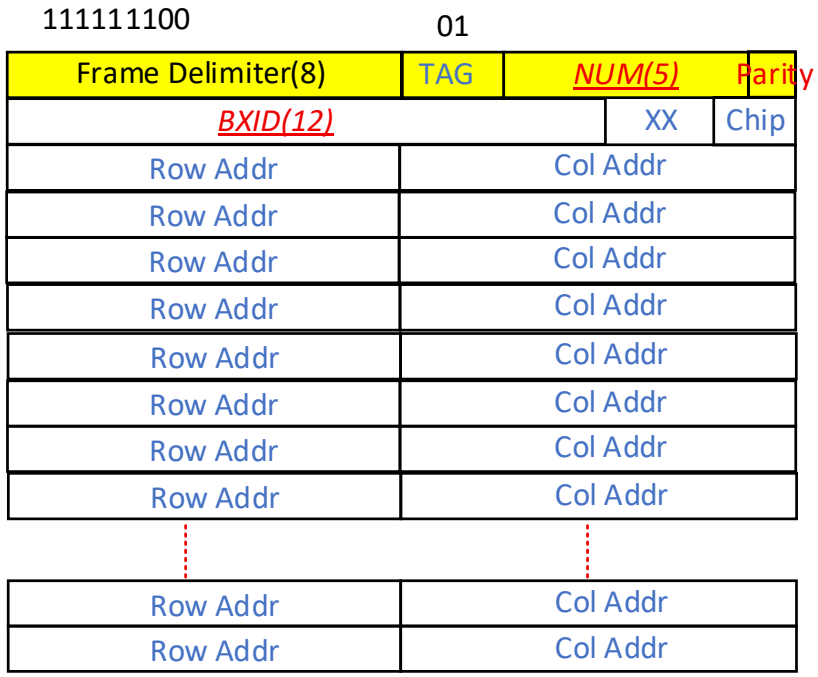
Hit Number in a BXID	words in Normal Mode	words in Normal Compact Mode	Compression ratio
1	1	2	200%
2	2	2	100%
3	3	3	100%
4	4	4	100%
5	5	5	100%
6	6	5	83%
7	7	6	85%
8	8	6	75%
9	9	7	78%
10	10	7	70%
11	11	8	73%
12	12	8	67%

Ref. https://doi.org/10.1016/j.nima.2026.171886

New data format with shared BXID segment (2)

- A new data format can improve the compression ratio. The data length is changed from 32 to16 .

The compression ratio is better than 75% when a package includes more than 4 hits.



Hit Number in a BXID	words in Normal Mode	words in Normal Compact Mode	Compression ratio
1	1	1.5	150%
2	2	2	100%
3	3	2.5	83%
4	4	3	75%
5	5	3.5	70%
6	6	4	67%
7	7	4.5	64%
8	8	5	62.5%
9	9	5.5	61%
10	10	6	60%
11	11	6.5	59%
12	12	7	58.3%

We are still searching for higher-efficiency data format…

Summary

- In future particle detection, the readout of high hit flux data takes challenge for MAPS. On-chip data compression / data-reduction techniques are therefore valuable.
- For the vertex detector, zero suppression and an adjacent address compression method is realized. An additional 50 % data reduction can be achieved after zero-suppression.
- For the inner tracker, on-chip BXID correction and BXID shared data format are proposed for advanced readout requirements.
- In future work, we will investigate new readout-logic architectures and data-reduction methods, e.g., extracting hit-cluster centroid information.

Thank for your attention!