Vertex Detector R&D for AGORA

From the CEPC Ref-TDR design to AGORA at FCC-ee

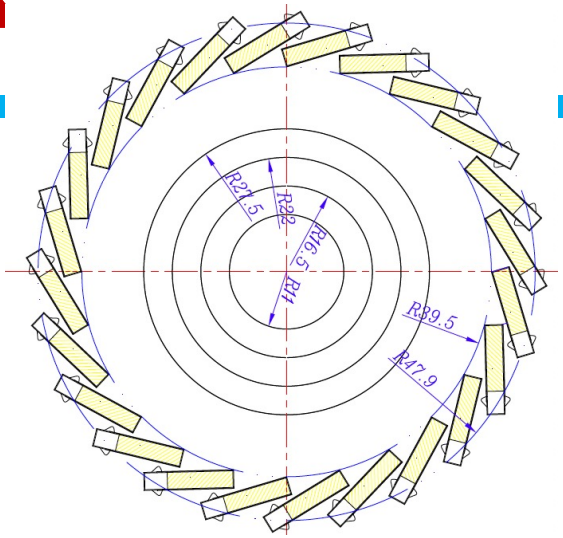
Zhijun Liang
(IHEP, Beijing)

CEPC2026 Workshop, Shanghai, 22–26 October 2026



中国科学院高能物理研究所
Institute of High Energy Physics
Chinese Academy of Sciences

Vertex detector in CEPC Ref-TDR

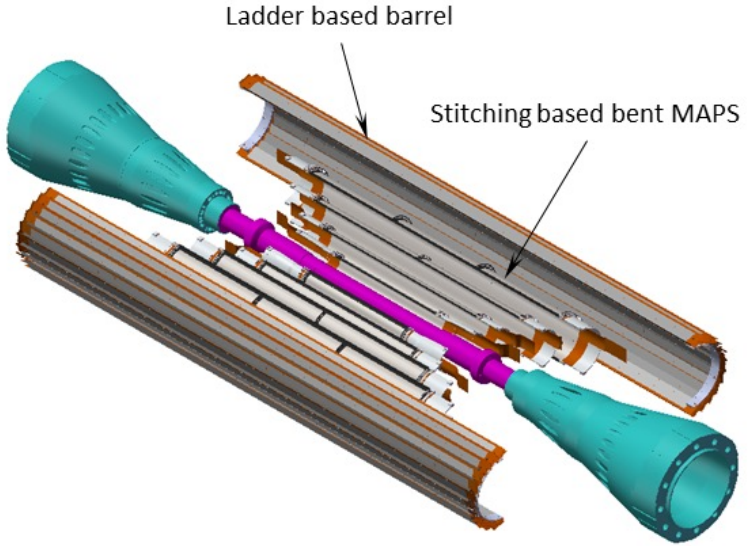


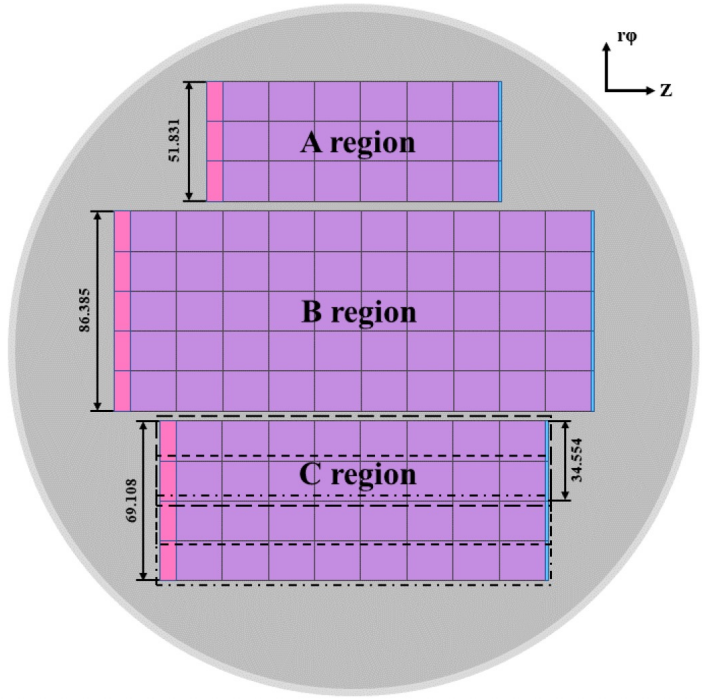
- CEPC Ref-TDR vertex = AGORA baseline
  - 4 single layer of bent MAPS + 1 double layer ladder
  - Use single bent MAPS for Inner layer (~0.15m^2)
    - Low material budget 0.06%X0 per layer
    - Designed for Higgs + low-lumi Z (2.4×10^{35} cm^{-2}s^{-1}, 3 T)

FCC-ee check: central pipe r_{out} = 11.7 mm (AlBeMet, 0.68% X_0) > layer-1 radius 11.06 mm → L1 must move out

Long barrel layout (no endcap disk) to cover cos $\underline{\theta}$<=0.991

layer/VXD X	radius .mm	length .mm
layer 1	11.06	161.4
layer 2	16.56	242.2
layer 3	22.06	323.0
layer 4	27.56	403.8
VXD 5	39.50	682.0





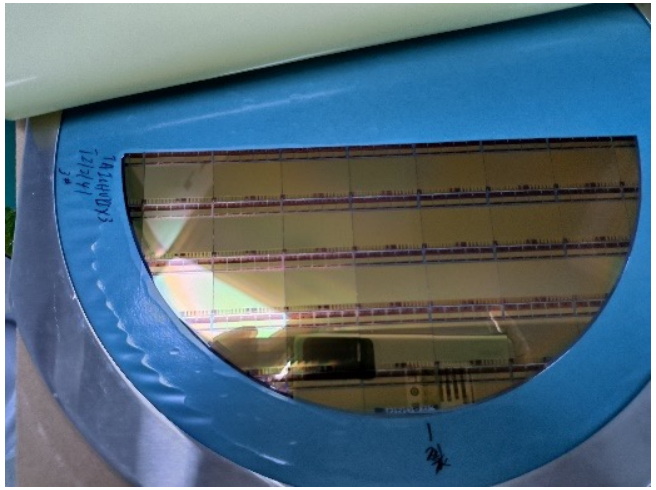
Required changes: the specifications, not the concept

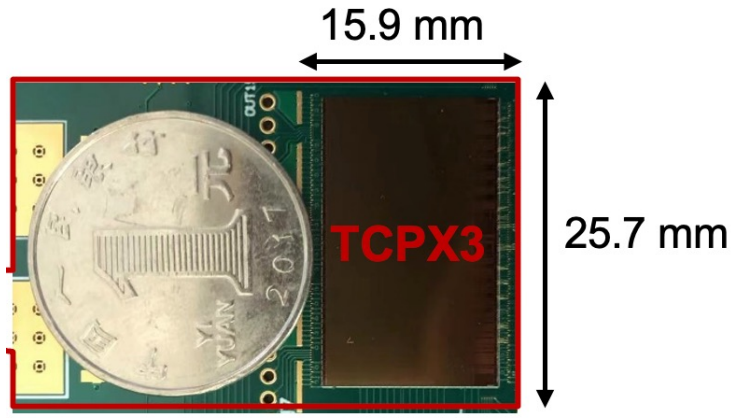
	Item	CEPC Ref-TDR	AGORA @ FCC-ee (proposed)
●	**Hit-rate capability (L1)**	~40 MHz/cm^2	≥ 150–200 MHz/cm^2 incl. safety margin
●	**Power / cooling**	< 40 mW/cm^2, air	Stay ≤ 40–50 mW/cm^2
●	**Inner radius r_{min}**	11.06 mm	≥ ~13 mm (pipe r_{out} 11.7 mm; IDEA: 13.7 mm); re-optimize L2–L4 for $\|\cos\theta\| \leq 0.99$
●	**Pixel / resolution**	25 × 25 μm^2, ~5 μm	16 × 30 μm^2, $\sigma_{r\varphi}$ < 3 μm (already in HC90L first-run plan)
●	**Radiation**	~1–2 Mrad/yr	~10 Mrad/yr; ~10^{14} n_{eq}/cm^2 over Z run

● major change / risk ● moderate: design work ● minor: largely in hand

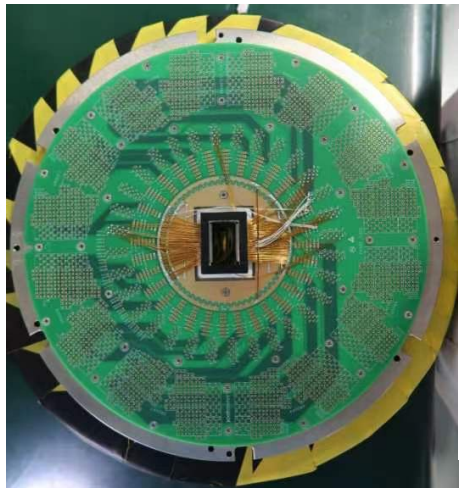
R&D efforts: Full-size TaichuPix3

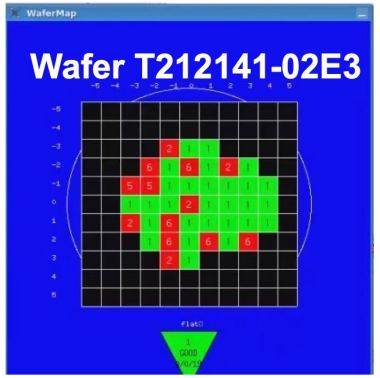
- Full size CMOS chip developed, 1st engineering run
  - 1024×512 Pixel array, Chip Size：15.9×25.7mm
  - 25μm×25μm pixel size with high spatial resolution
  - Process: Towerjazz 180nm CIS process
  - Fast digital readout to cope with ZH and Z runs (support 40MHz clock)





TaichuPix-3 chip vs. coin

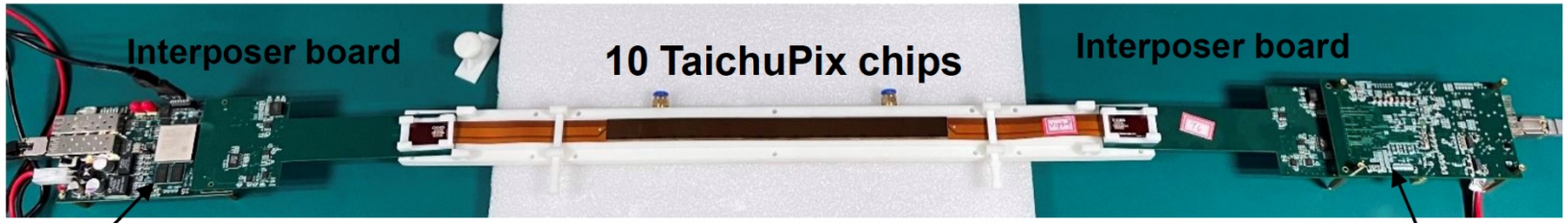




An example of wafer test result

	Status	CEPC Final goal
CMOS chip technology	Full-size chip with TJ 180nm CIS	65nm CIS

R&D effort: vertex detector prototype

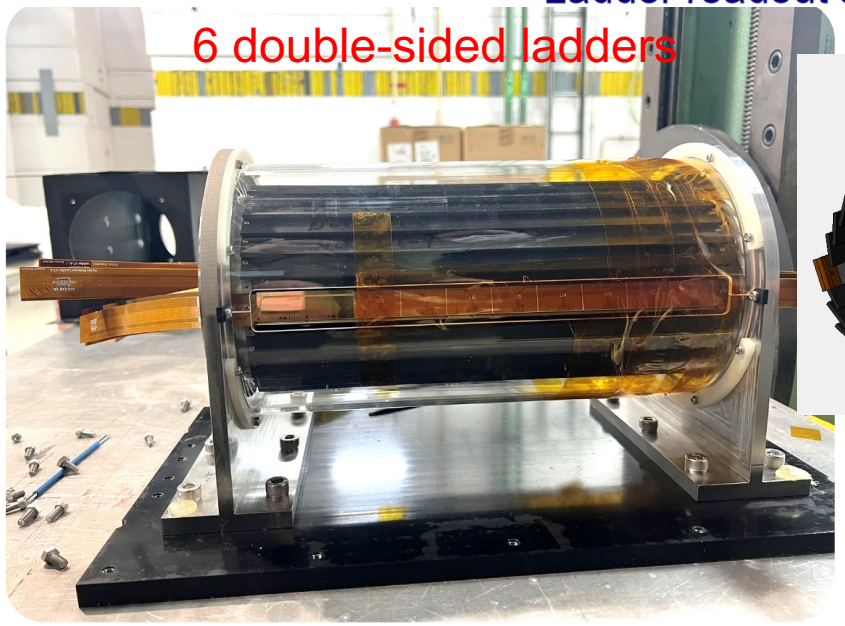


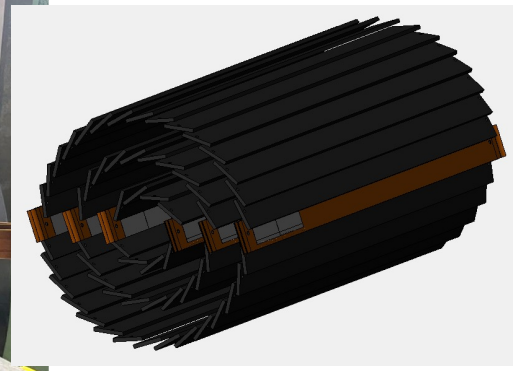
TaichuPix-based prototype detector tested at DESY in April 2023

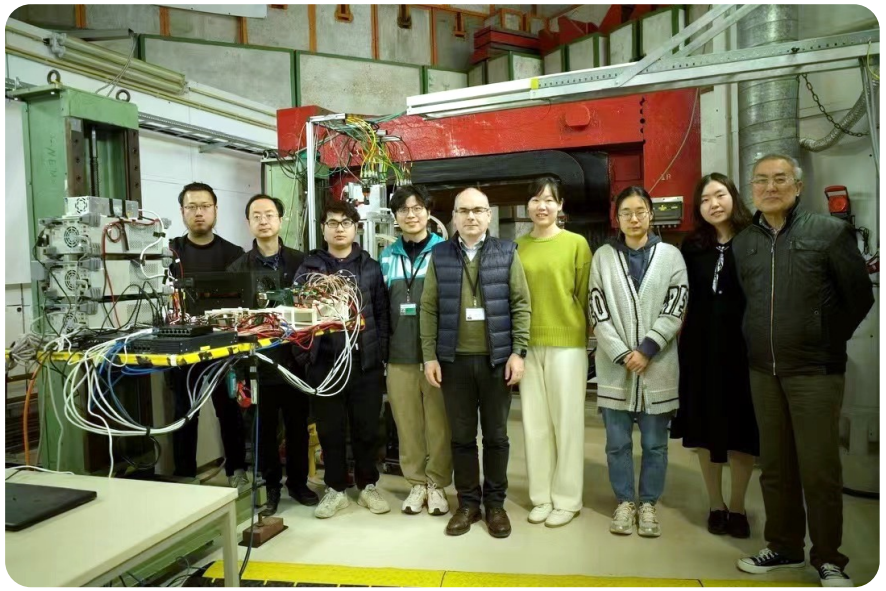
Spatial resolution ~ **4.9 μm**

Ladder readout system

6 double-sided ladders



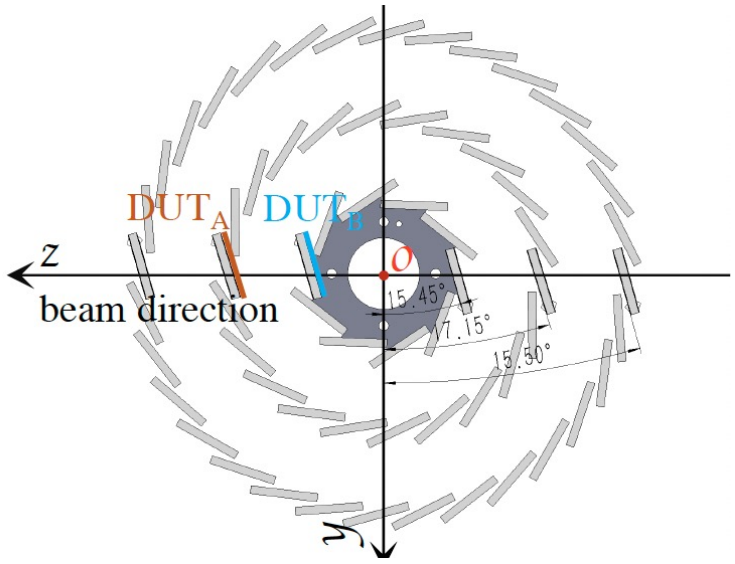


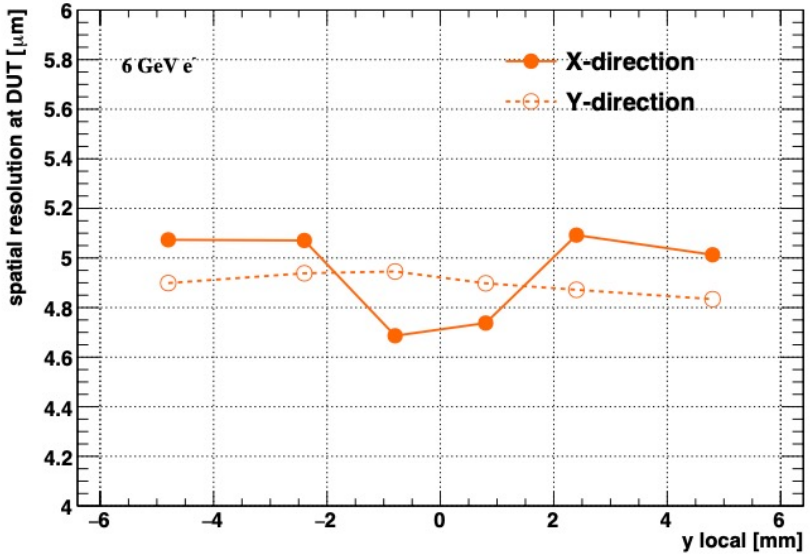


	Status	CEPC Final goal
Detector integration	Detector prototype with ladder design	Detector with bent silicon design

R&D efforts and results: vertex detector prototype beam test

Spatial resolution ~ **5 μm**

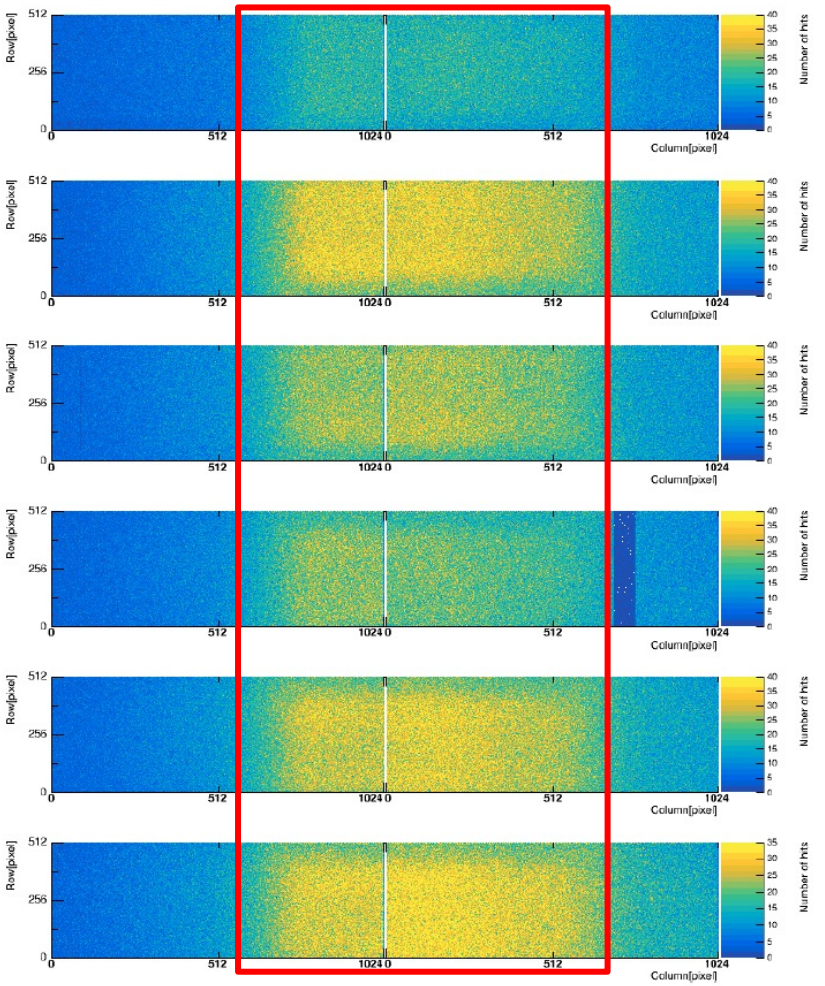




	Status	CEPC Final goal
Spatial resolution	4.9 μm	3-5 μm

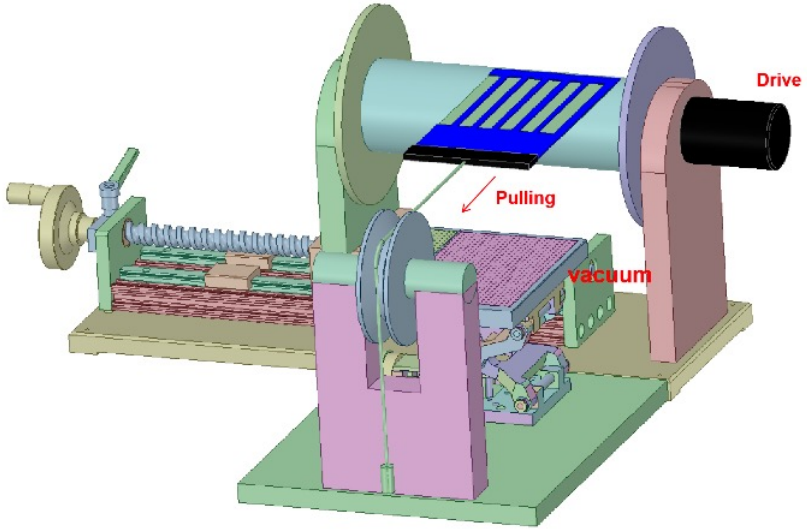
Hit maps of multiple layers of vertex detector

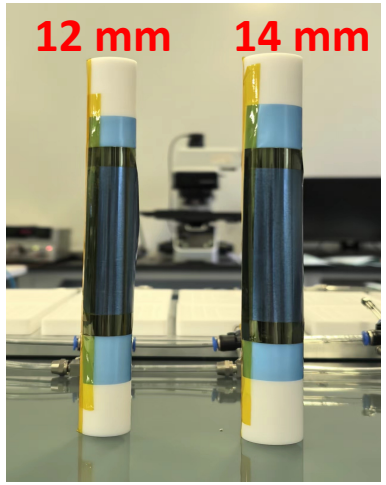
Beam spot



R&D efforts curved MAPS

- CEPC b-layer radius (11mm) smaller compared with ALICE ITS3 (radius=18mm)
- Feasibility : Mechanical prototype with dummy wafer can curved to a radius of 12mm
  - The dummy wafer has been thinned to 40μm





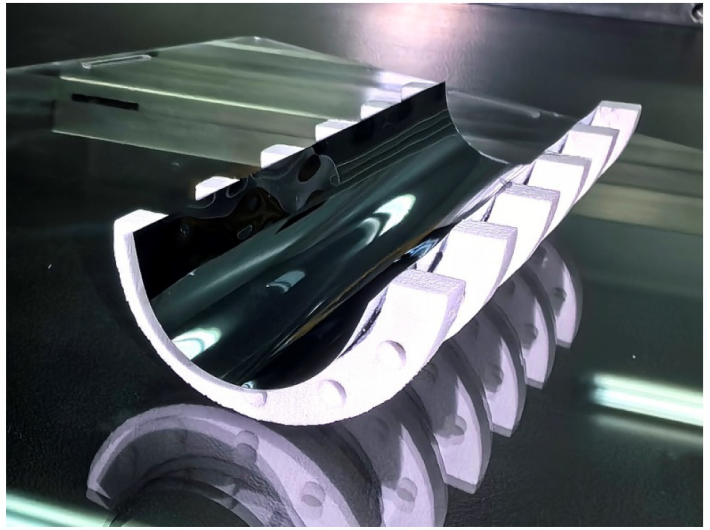


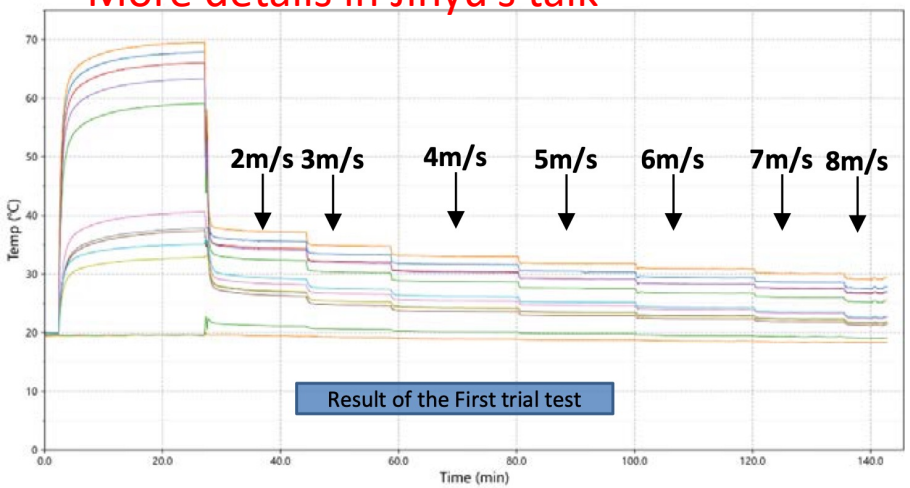
Figure 4.26: 12 mm bending radius.

	Status	CEPC Final goal
Bent silicon with radius	Bent Dummy wafer radius ~12mm	Bent final wafer with radius ~11mm

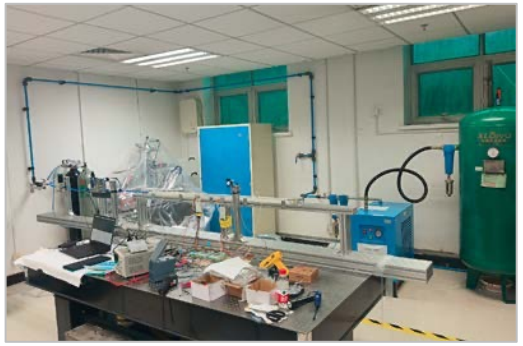
Cooling test: VTX thermal mockup

More details in Jinyu's talk

- Heat load of the stitched layers
  - 40 mW/cm² on sensors, 485 mW/cm² on the 4.1 mm left-end blocks, ~80 W in total
  - Target: every layer ≤ 30 °C with air cooling
- Phase 1: flat L1 thermal mockup
  - CF support + FPC-integrated heater + 50 μm Al spreading layer + PT100 sensors
  - Forced air 2–8 m/s, inlet 18.2–19.5 °C
- Result: temperature falls steadily with air speed
  - **Max. rise 17.7 → 10.5 °C, gradient 10.9 → 7.9 °C (2 → 8 m/s)**
- Next: cylindrical single layer, then multi-layer mockup









Air-cooling bench and L1 mockup in the test chamber · J. Fu, AGORA meeting, 2 Sep 2026

	Status	CEPC Final goal
Detector cooling	Air-cooled flat L1 thermal mockup, 2–8 m/s	Air cooling of the full VTX at full power

Motivation: R & D towards Vertex detector for future lepton collider

Aiming to vertex chip development for future lepton collider (CEPC and FCC-ee …)

	Requirement	What this means for technology
Spatial resolution	3-5 um target	**Small pitch**
Material budget	<0.15% X0/layer	**Thinning, stitching, edge services**
Operation	Higgs/Z pole	**low-power front-end and readout**
Power consumption	40 mW/cm^2	
Data rate	200 MHz/cm^2, ~10 Gbps/chip	**fast readout, high-speed data links**
Scalability	bent MAPS direction	**large-area stitching needed**
Irradiation hardness	>1E14 Neq/cm^2	Irradiation hard

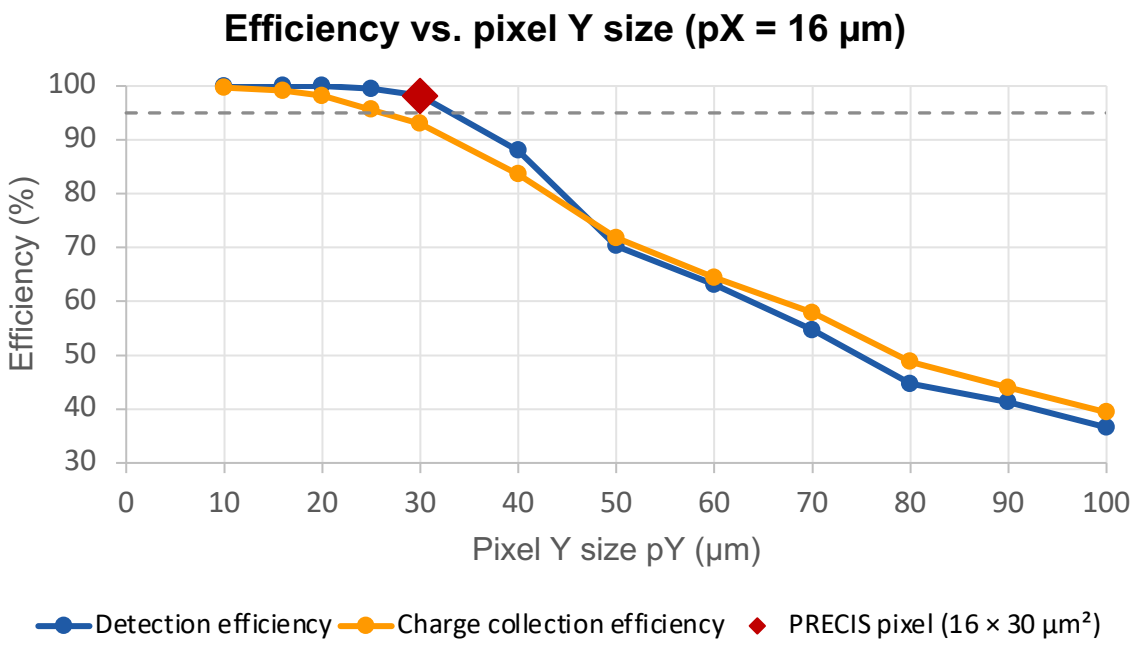
Comparison of CIS technologies

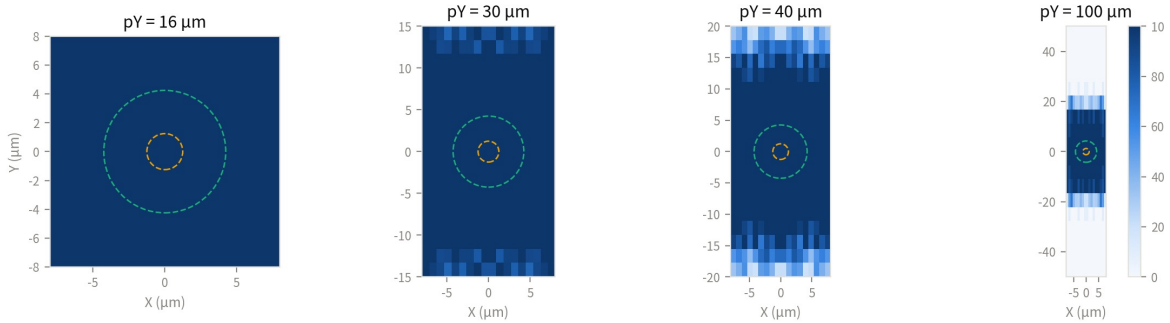
- HC90L technology is cost-effective option with stitching combability
  - Power consumption of HC90L chip is expected to be similar to 55nm technology

	Requirements	TPSCo 65 nm	HLMC 55 nm	Hynix HC90L
Feature size	55 – 90 nm	65 nm	55 nm	90 nm
Epitaxial layer thickness	10 - 25 μm	10 μm	3-5 μm	4 – 8.5 μm (default) Aiming to change to 20μm
Resistivity of epi-layer	> 1 kΩ•cm	High resistivity	Low resistivity ~10 Ω•cm	30-50 Ω•cm (default) Aiming to upgraded to 5kΩcm
Availability of deep N-well	Yes	Yes	Yes	Yes
Availability of deep P-well	Yes	Yes	Yes	Optional
Numbers of metal layers	> 6	Max. 7	Max. 5	Max. 5
Availability of stitching	Yes	Yes	Yes	Yes
Cost (NRE)		N/A	~6M RMB	2~3 M RMB

TCAD simulation: pixel size scan

3D pixel simulation: TJ180-like small-electrode CIS, SRP-measured high-resistivity epi (22.4 µm); numerical Poisson field + MC charge transport. pX = 16 µm, |Vbb| = 1.8 V, electrode Ø2.5 µm, threshold 260 e⁻, MIP at normal incidence, 1000 events per point.





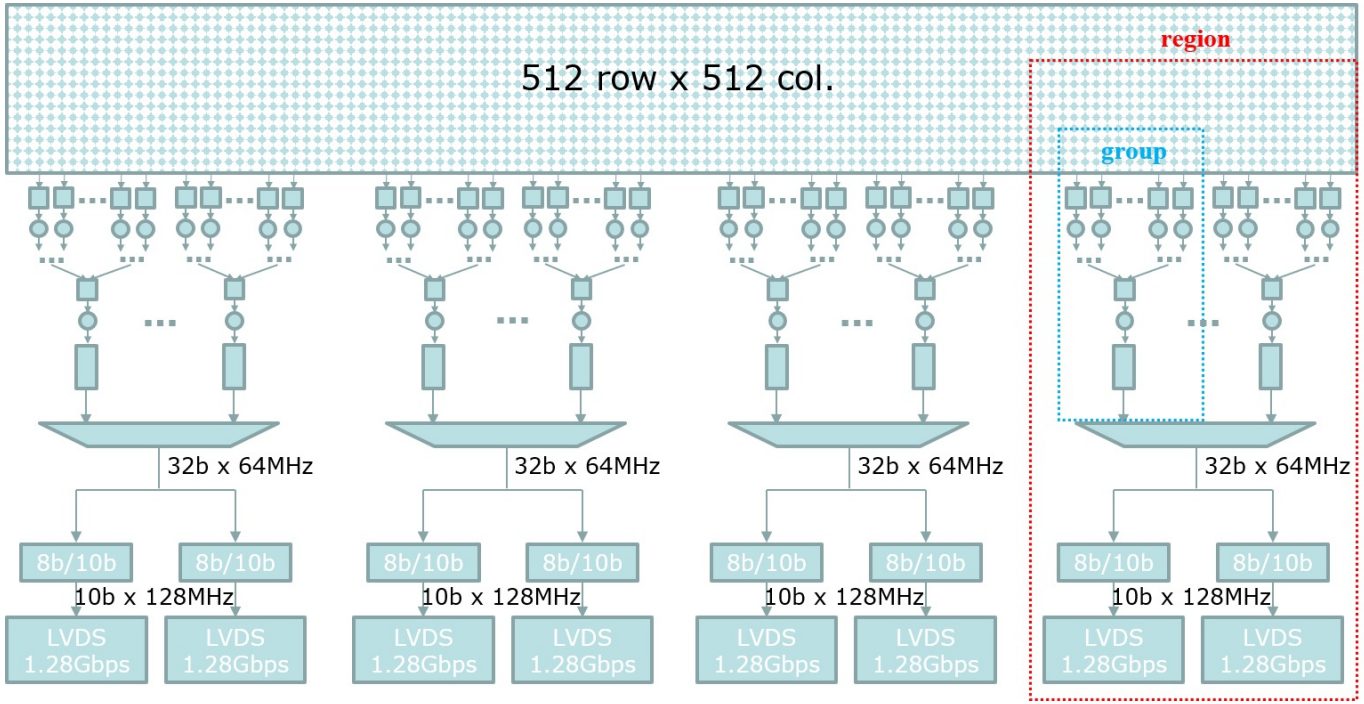
Efficiency maps (0–100%): orange = electrode, green = p-well opening

pY (µm)	16	30	40	100
Efficiency	100%	**98.2%**	88.0%	36.6%
CCE	99.1%	**93.0%**	83.6%	39.4%
⟨t_collection⟩	27 ns	**44 ns**	53 ns	63 ns
⟨cluster size in Y⟩	1.31	**1.11**	1.01	1.00

- **pY ≤ 30 µm: efficiency ≥ 98%** (95% crossing at pY ≈ 33 µm) → the 16 × 30 µm² PRECIS pixel is inside the safe window
- **pY ≥ 40 µm: efficiency collapses** (88% → 37% at 100 µm): charge diffusing from the far end falls below the 260 e⁻ threshold
- **Collection time 27 → 63 ns; no Y charge sharing above 40 µm** (⟨nY⟩ → 1), C_d ≈ 1.3–1.5 fF throughout
- **Larger electrode recovers pY = 40 µm**: Ø3.5 µm → 96.5% (C_d 1.9 fF); trend-level model, full TCAD and beam test to confirm

PRECIS design scheme

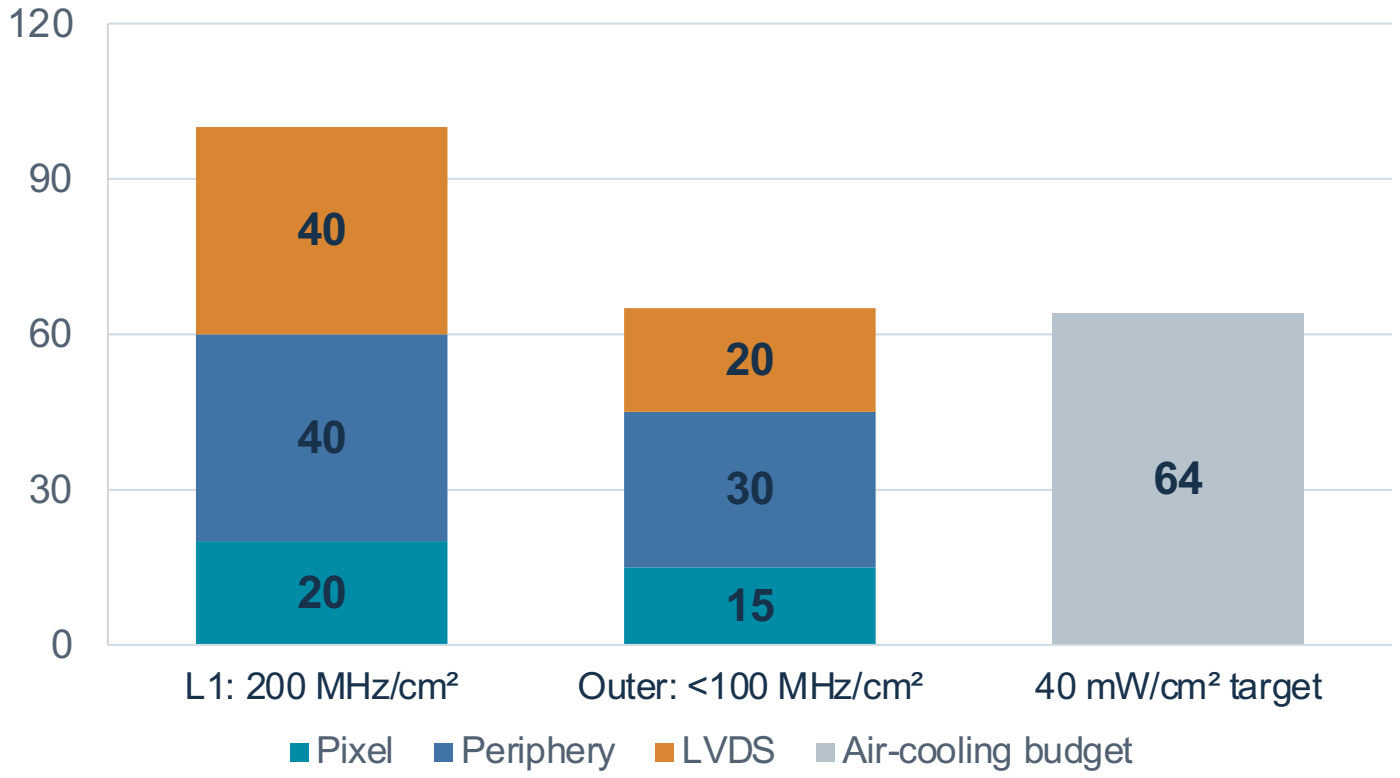
- Single chip to verify the readout architecture and the new process (HC90L)
  - 512 × 512 pixels, 16 × 30 μm²
  - Region = 4 groups + 2 × 8b/10b + 2 × LVDS transmitter
  - Group = 16 double columns + 1 shared FIFO tree
  - 140 words for each group; time stamp on each double column
- Expected data rate
  - **252 MHz pixel hits per chip (200 MHz/cm²)**
  - Also looking into fast trigger scheme



FIFO tree 32 b × 64 MHz → 8b/10b (10 b × 128 MHz) → LVDS 1.28 Gbps; one region outlined in red, one group in blue

PRECIS: operating conditions

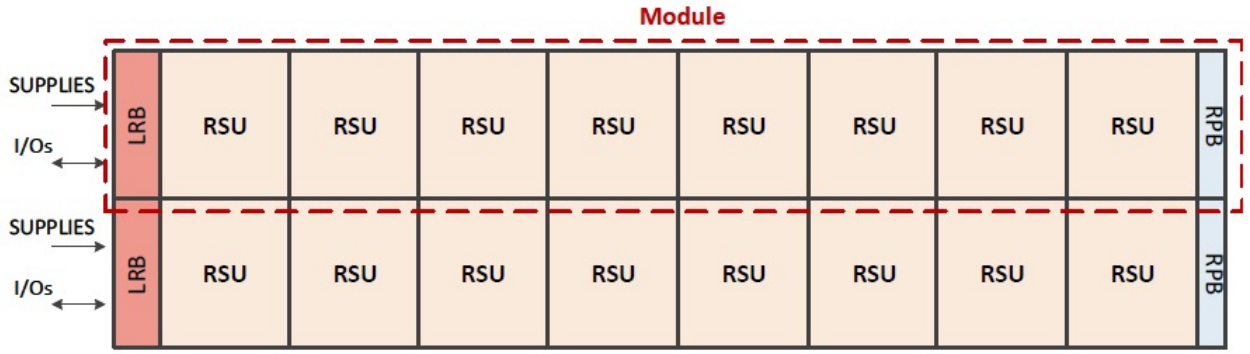
- **Innermost layer: pixel hit rate = 200 MHz/cm²**
  - Average power = 100 mW / 1.6 cm² = 62.5 mW/cm²
  - Use the beam pipe as a heat sink
- **Second and outer layers: pixel hit rate < 100 MHz/cm²**
  - Lower the system clock by 1/2
  - Power off half of the data transmitters
  - Average power = 65 mW / 1.6 cm² = 40.6 mW/cm²
  - **Very close to the air-cooling heat load (< 40 mW/cm²)**



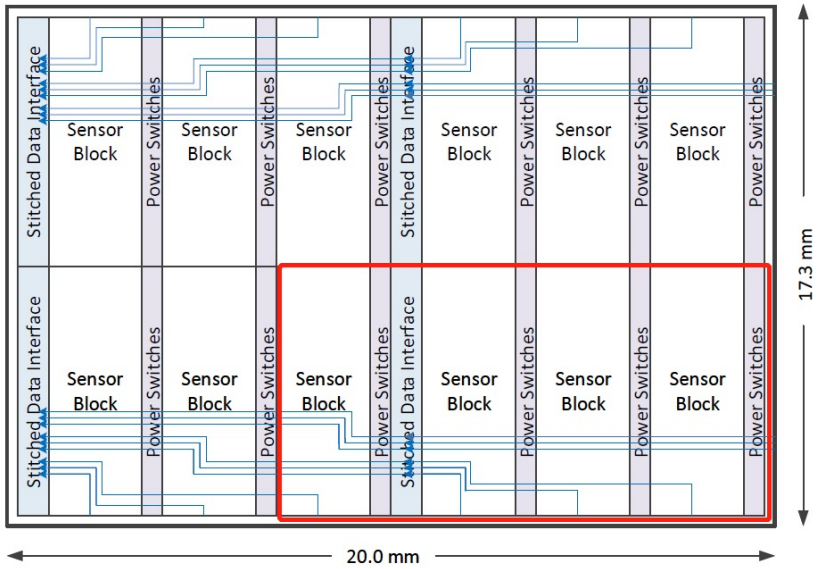
Budget: 64 mW per chip = 40 mW/cm² over 1.6 cm² (air cooling)

PRECIS: compatible with stitching

- Single chip design has 4 sensor units implemented as independent regions
  - As in the CEPC Ref-TDR repeated sensor unit (RSU)
  - Region size 8.2 mm × 15.4/4 mm; may change slightly in the final layout
  - Each region has a dedicated data buffer and data transmitter
- Standalone module design and verification
  - Power switches
  - Stitched data interface
- **1st run without stitching (2027); stitched 2nd run (2028) reuses the region**



Stitched module: RSUs between left-end (LRB) and right-end (RPB) blocks



RSU (20.0 × 17.3 mm²): red box = the part implemented in PRECIS

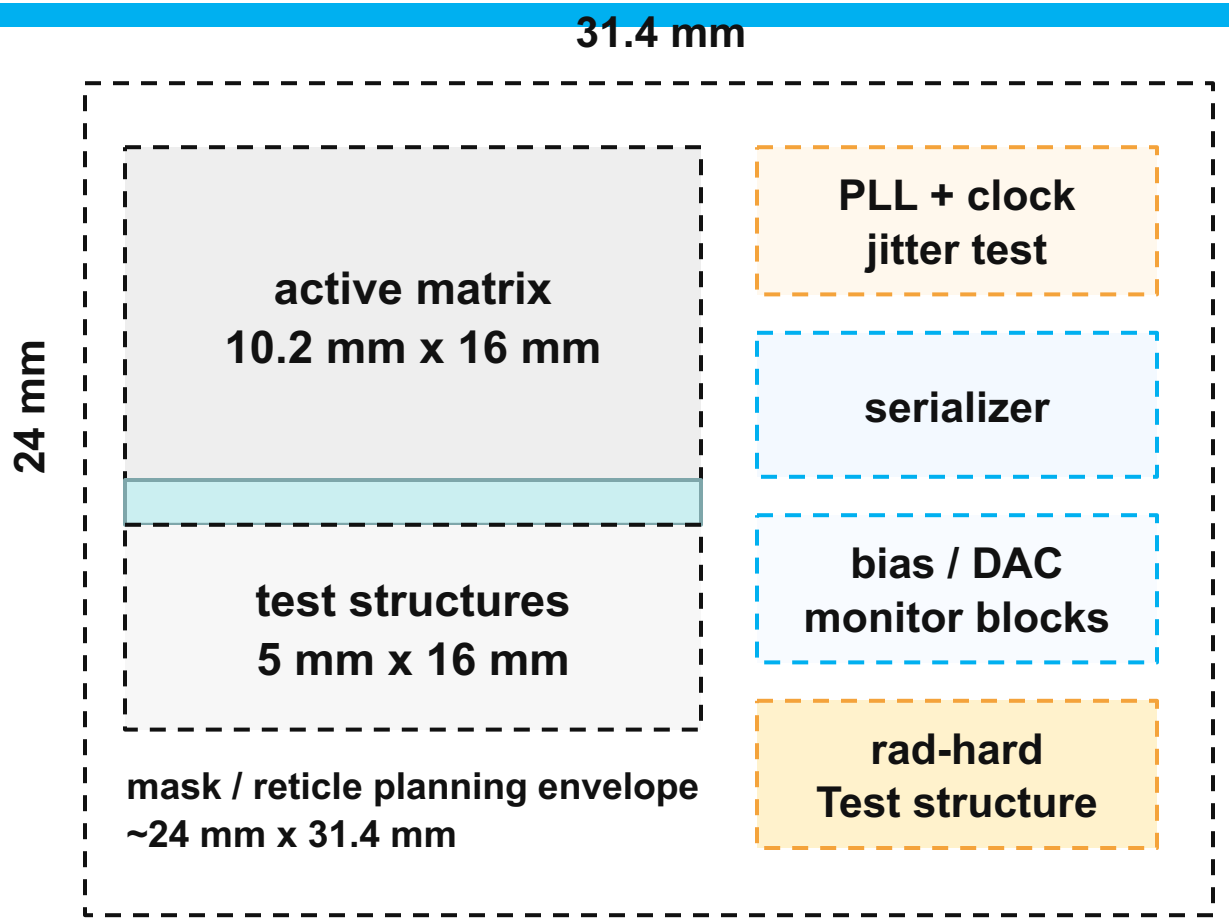
Preliminary layout for 1st engineering run

Planning envelope

- planning block: about 24 mm x 31.5 mm
- active matrix estimate: 10.2 mm x 16 mm
- test-structure area: 5 mm x 16 mm
- pixel option: 16 um x 30 um, 512 x 512 matrix

Blocks needed (missing contributions and design)

- PLL / clock generation
- Serializer, command decoder
- Rad-hard diode test structure, transistor, guard-ring, and well-isolation structures
- pixel variants for epi/resistivity/substrate-bias studies



Seeking for collaboration for R & D using HC90L CIS technology

Current Research team interested in HC90 chip R & D project

- IHEP: chip design, sensor simulation, testing
- ShanDong U.: Stitching chip design
- CCNU: chip design
- Northwestern Polytechnical U. : Readout Architecture design
- Nanchang U. : in-pixel digitation design
- Nanjing U.: Irradiation study
- NanKai U. : TCAD sensor simulation

Seeking for more collaboration for R & D using HC90L CIS technology

Summary: Propose HC90L as a complementary DRD3 MAPS technology line

Summary

- HC90L offers 90 nm CIS, epi/resistivity options, deep-well choices, stitching feasibility, and relatively low NRE cost.
- Potential candidate technology for vertex detector in future collider
- The first engineering run should validate the process before attempting stitched sensors.
- Propose 3-4 years research program should end with a clear technology-readiness decision.

Seeking for collaborations and feedback from DRD3 community

- feedback on first-run content: diode variants, pixel options, readout blocks, irradiation samples
- collaboration on TCAD, irradiation, beam tests, DAQ, and MAPS characterization

Backup: Reducing the data rate

Challenge (innermost layer, FCC-ee Z pole): 200 MHz/cm² → 252 M pixel hits/s and 10.08 Gbps per chip; the LVDS links are 40 of the 100 mW per chip. Two ways to cut the data at the source:

On-chip cluster compression

- **How:** one word per cluster (seed address + small hit map) instead of one word per pixel
- **Gain:** ⟨cluster size⟩ ≈ 1.5 for 16 × 30 μm² (TCAD) → ~1/3 fewer words, e.g. 10 → ~7 Gbps per chip; ~2 fewer LVDS links (≈ 10 mW per chip, estimate)
- **Bonus:** gain grows for inclined tracks (cluster size ≈ a·secα + b, measured)
- **Cost:** cluster logic in the FIFO tree; clusters across double-column and group edges

Fast trigger (triggered readout)

- **How:** keep hits on chip with the double-column time stamp; read out only hits matching a fast trigger
- **Gain:** data ∝ trigger rate × matching window, not the background rate: e.g. 100 kHz × 200 ns = 2% → ~50× fewer hits (illustrative)
- **Heritage:** TaichuPix-3 already has a trigger mode (time-stamp matching)
- **Cost:** buffer ≈ hit rate × latency (~60 hits per region per μs at 200 MHz/cm²); needs a low-latency trigger at the Z pole

Proposed path: keep the triggerless baseline; add cluster compression to the PRECIS readout; study a triggered mode for the innermost layers together with electronics and TDAQ.