RADPIX
PARTICLE DETECTOR

Radpix development status and plans

2026 International Workshop on the High-Energy Circular Electron-Positron Collider

Monday 22nd June 2026

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cea irfu

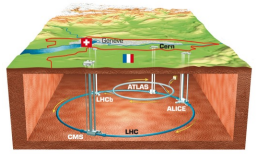
LHCb

Outlook

1. **LHCb Upgrade II**
2. **HV-CMOS pixel sensors**
3. **RADPIX 1**
4. **BIG & Serial powering chip**
5. **RADPIX2**

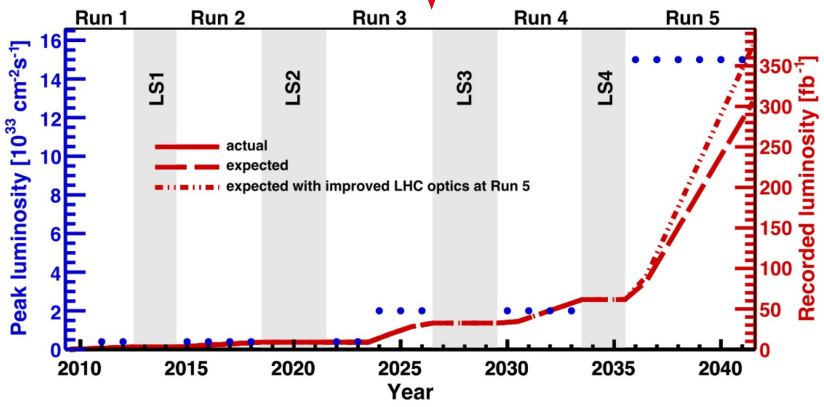
LHCb Upgrade II

High-Luminosity LHC



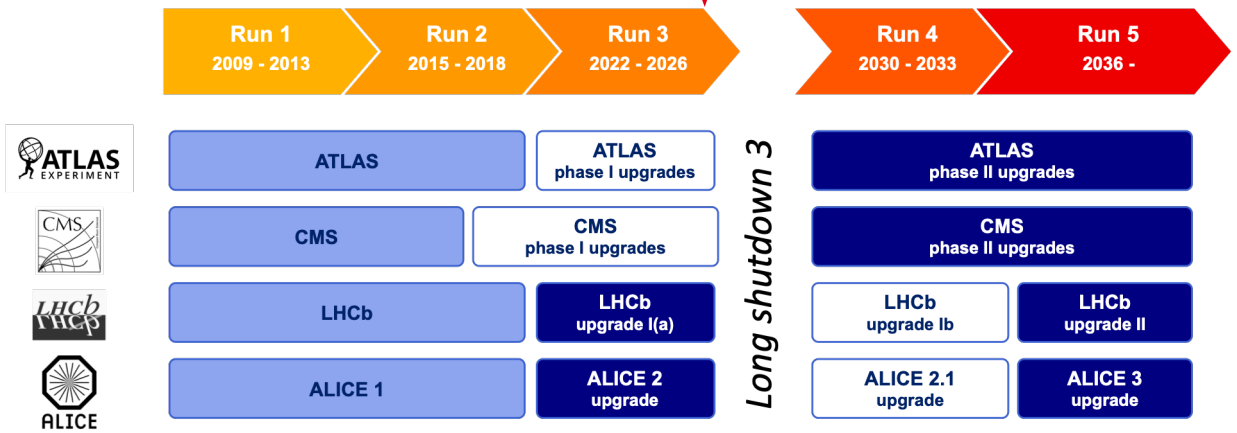
- Upgrade I : $\mathcal{L}_{peak}$ = 2 × 10^{33} $cm^{-2}{\cdot}s^{-1}$
- Upgrade II : $\mathcal{L}_{peak}$ = 1.5 × 10^{34} $cm^{-2}{\cdot}s^{-1}$

You are here



LHC Schedule

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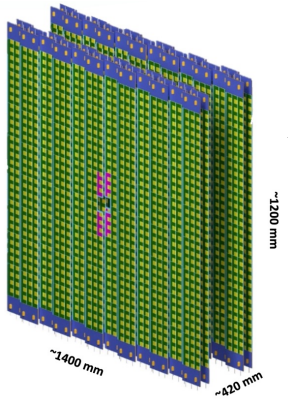


- Installation in LS 4 : **Upgrade to get the maximum physics LHC can deliver = active R&D**

LHCb Upgrade II

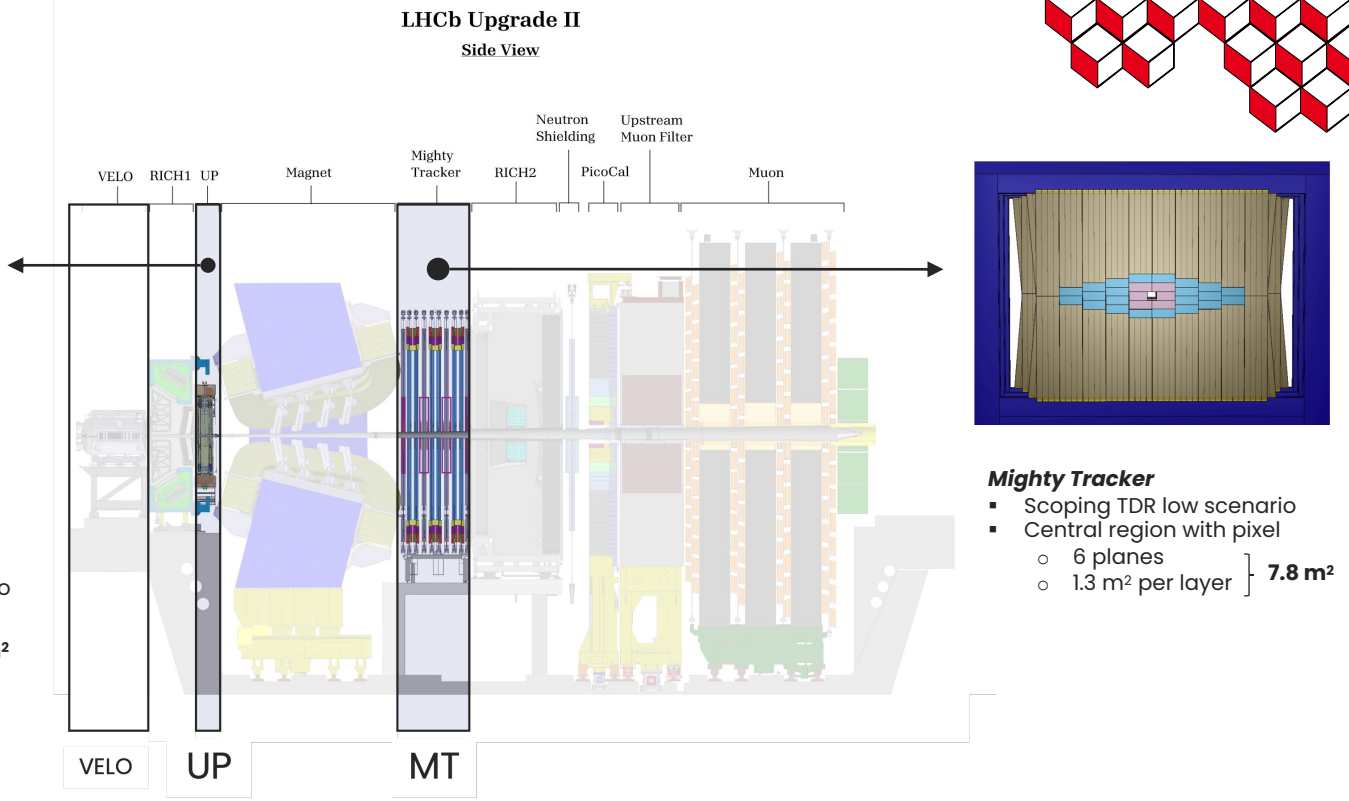
Tracking stations in LHCb

- (VELO)
- Upstream Pixel (UP)
- Mighty Tracker (MT)



Upstream Pixel
- Scoping TDR Middle scenario
- Full pixel
  - 4 planes
  - 1.7 m² per layer

6.7 m²



Mighty Tracker
- Scoping TDR low scenario
- Central region with pixel
  - 6 planes
  - 1.3 m² per layer

7.8 m²

UP & MT specifications

- Both pixel detectors with similar needs
  - Physics requirements
  - Readout architecture (LpGBT)
- Low power, high radiation tolerance

- Several m² to be equipped → monolithic

HV-CMOS pixel sensor

Parameter	UP Specification	MP specification
Pixel size (x)	≤ 100	≤ 100
Substrate thickness	$100 - 200\ \mu m$	$100 - 200\ \mu m$
Max. Particle Rate	$40\ MHz/cm^2$	$14.5\ MHz/cm^2$
Max. Hit Rate	$91.2\ Mhit/cm^2$	$37.6\ Mhit/cm^2$ n
In-time efficiency	> 99 % with in 25 ns	> 99 % with in 25 ns
Noise rate (End of life)	$\leq 400\ kHz/cm^2$	$\leq 400\ kHz/cm^2$
NIEL	$3 \times 10^{15}\ N_{eq}/cm^2$	$3.6 \times 10^{14}\ N_{eq}/cm^2$
TID	$187.5\ Mrad$	$36\ Mrad$
Power Consumption	$\leq 200mW/cm^2 + 25\%$ overhead for serial powering	$\leq 150mW/cm^2 + 30\%$ overhead for serial powering

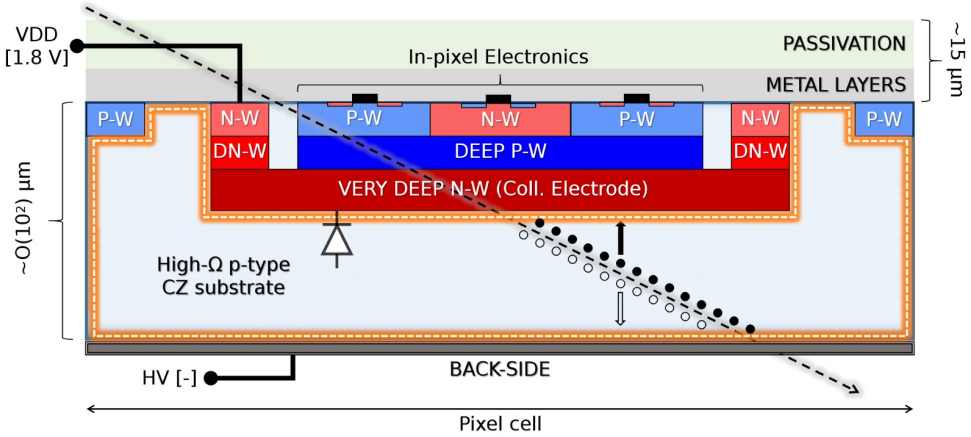
safety factor of 2 applied, safety factor of 3 applied

HV-CMOS pixel sensors

Monolithic Active Pixel Sensor with HV back bias

- Sensor + electronics in the same substrate = monolithic
- In-pixel electronics, embedded in the collection diode
  - Full depletion of the pixel volume
  - HV back bias voltage
- Need of a HV, quadruple-well technology → **LF 150nm**
  - Bonus : High-res p-type CZ substrate, standard for LF150

HV-CMOS quadruple-well pixel Cross Section

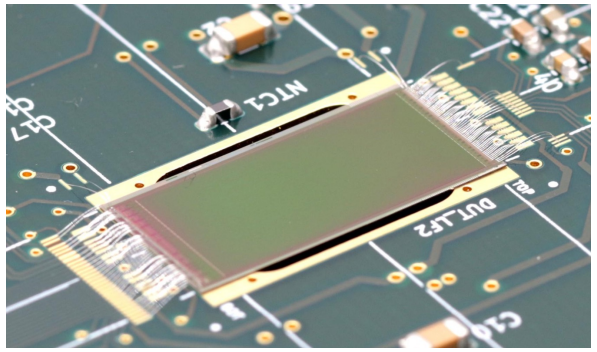


From : Improvement in the Design and Performance of the Monopix2 Reticle-Scale DMAPS

LF HV MAPS R&D

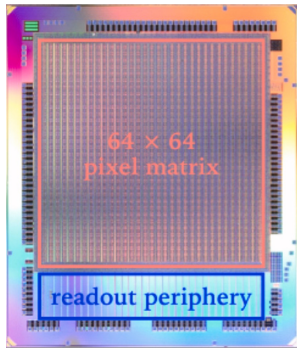
- 2017→ LF-MONOPIX 2
  - 150 × 50 µm² pixels
    - 28 µW/pixel
  - 1 × 2 cm² sensor
  - V breakdown > 480 V

LF-MONOPIX2 die



- 2019 → RD50-MPW4
  - 62 × 62 µm² pixels
  - 64 × 64 pixels matrix
  - V breakdown > 600 V

RD50-MPW4 die



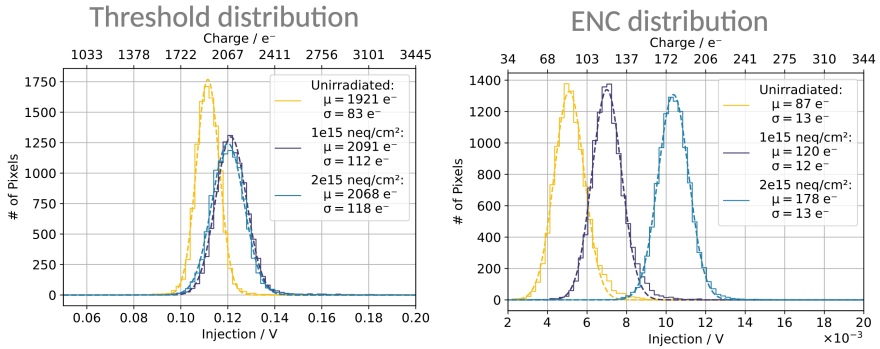
Column drain pixel architecture (FEI3-like)

LF HV-CMOS pixel sensors

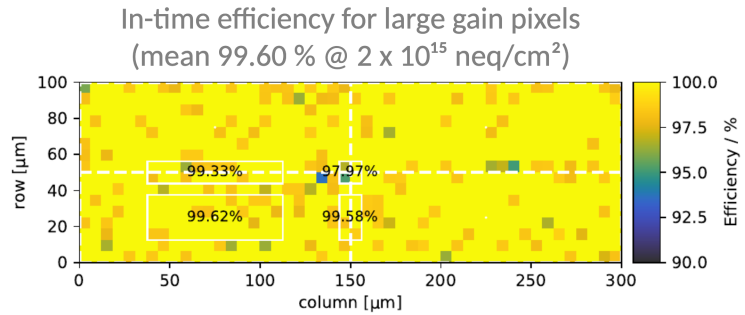
Irradiation results in a nutshell for the column drain pixel architecture

Operated in controlled environment @ -20 °C

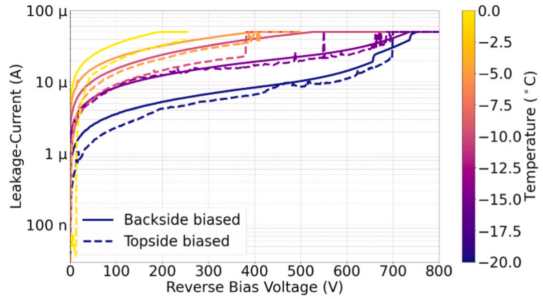
- LF-MONOPIX 2 [a]
  - Typical operational threshold of around 2.0 ± 0.1 ke⁻



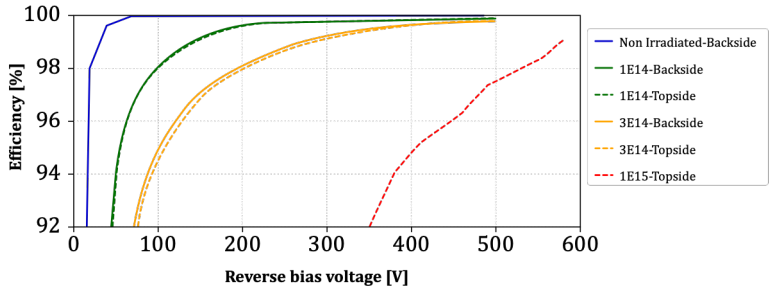
  - LF-MONOPIX2 Beam test @ Desy
    - High gain pixel (Cf = 1.5 fF) @ HV = -150V



- RD50-MPW4 [b]
  - Leakage current after 1·10¹⁵ N_{eq}/cm^2



  - RD50-MPW4 Beam test @ Desy
    - Efficiency recovered by increasing the HV



Pixel radhard architecture proven in LF 150nm

[a] Test-beam performance of proton-irradiated, large-scale depleted monolithic active pixel sensors in 150 nm CMOS technology

[b] Enhancing radiation hardness and granularity in HV-CMOS: The RD50-MPW4 sensor

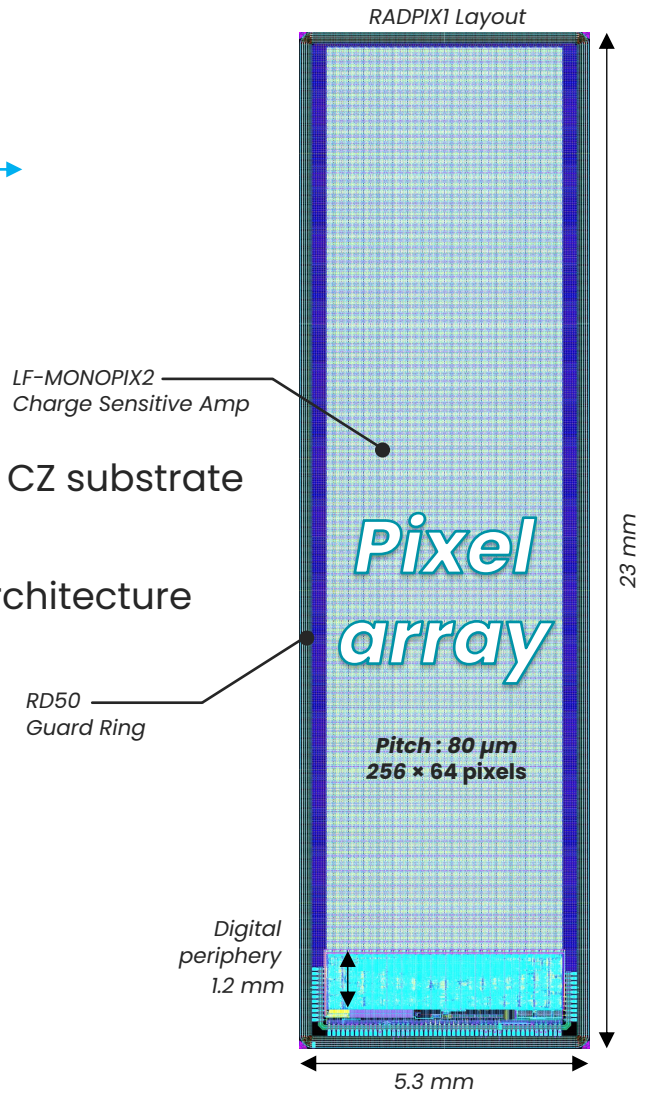
RADPIX 1

MAPS adapted to LHCb UP/MT

LF-MONOPIX 2

RD50-MPW4

- RADPIX 1 sensor
  - LF 150nm
  - High-res p-type CZ substrate
  - HV bias ~ -500V
  - Column drain architecture



RADPIX 1

Pixels array	- 256 rows × 64 columns, ¼ final sensor size - 4-pixel flavors (2 from LF-MONOPIX2), **compatible ~100MHz/cm²** - 80 µm pitch - 99% hit efficiency within 25ns - **150 mW/cm²**
Digital periphery	- Integrate **T**ime **F**ast **C**ontrol operations - Compatibility with LHCb data out protocol @1.28Gbs - Minimize power consumption
New IPs wrt RD50-MPW4	- LVDS revivers and transmitter - CMOS Band Gap - Power on Reset

- Adress LHCb UP/MT physics requirements
- Full heigh design
- Submission summer 2026 in DRD3 shared ER

RADPIX 1

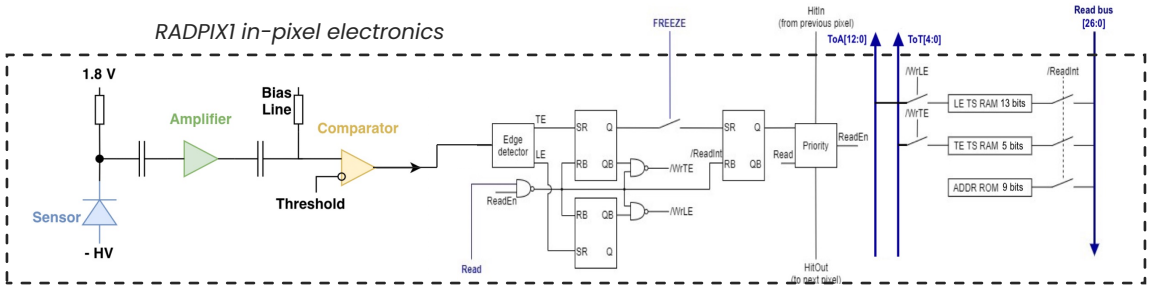
Pixel Matrix

- 3 Charge Sensitive Amp.
- 1 Transimpedance Amp.

} **ToT (MPV) ~ 500ns**

- ~ 10 µW / pixel
- Reduce time walk for in time efficiency (<< 25ns)
- In-Pixel 4-bit trimming DAC

RADPIX1 in-pixel electronics

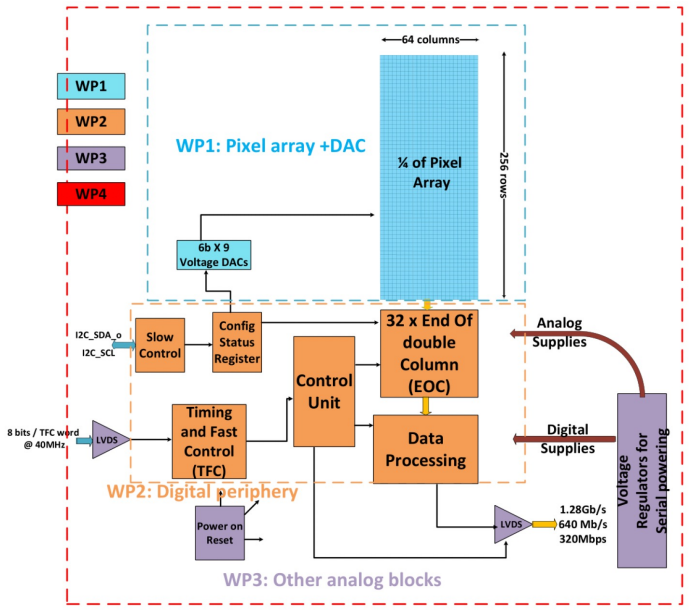


- In-pixel time stamp :
  - ToA : 12 bits + 1 overflow
  - ToT : 5 bits

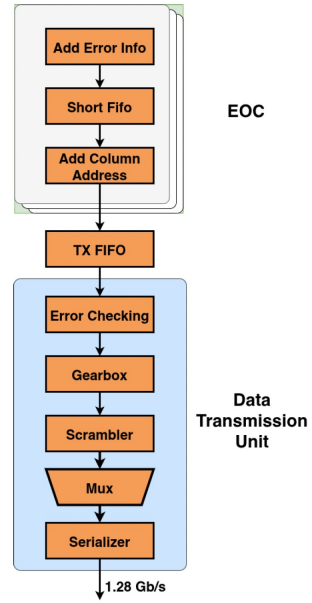
Digital periphery

- I2C Slow control
- Wishbone protocol for internal communication
- Timing and Fast Control @320MHz
- 1 hit (32bit)
  - 13bit ToA, 5bit ToT, Row address 9b, Column address 5b
- 32 Double Columns
  - FIFO, pixel configuration and data processing
- Data transmission Unit
- High speed pre-emphasis LVDS driver

RADPIX1 main functional blocks



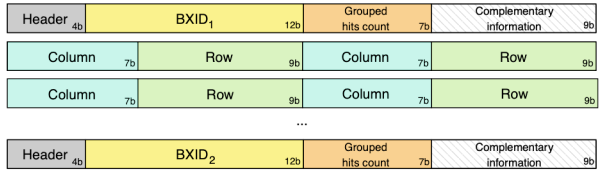
RADPIX1 Digital Data Path



Radpix 1 designed as a first step towards full UP/MT specifications

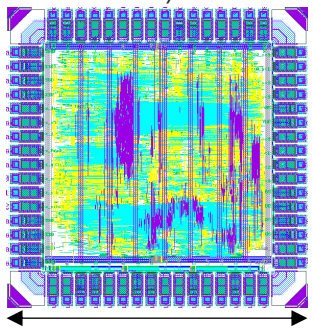
BIG & Serial Powering

- Bunch ID Grouping test chip (BIG)
  - ~ 100 MHz/cm^2 for UP. 6 e-links Max.
    - Dedicated data format to minimize overhead
    - Flexible “fix size” data format



BXID Sharing data format

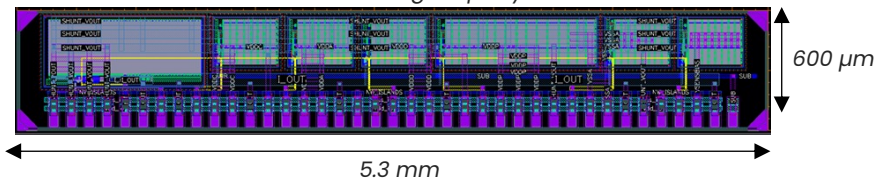
BIG Layout



- Within area and power budgets (1/4 of the final size)
- Design to be plugged to Radpix1 EoC
- Digital ASIC fully simulated with UP events
  - Expected latency from EoC + Pixel
  - Large clusters …
- Testability with digital probes and patterns injections

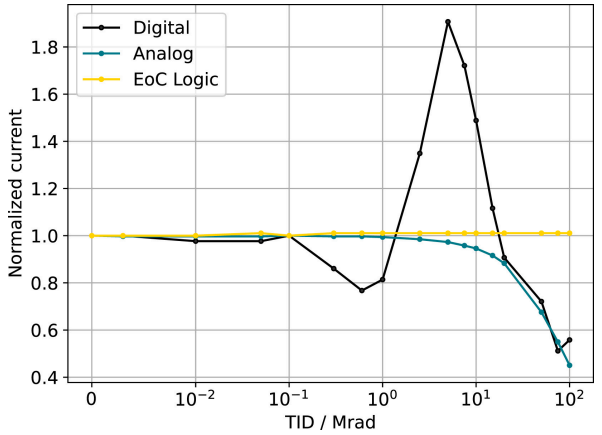
- Serial Powering Chip

Serial Powering Chip Layout



- Possibility to provide supplies directly to RadPix1 or by-pass in case of fault
  - 7 SLDO matching RADPIX1 power domains
- Possibility to test the SLDO chips independently from RadPix1
- 5 ASIC combined in parallel per hybrid, 9 in series configuration
- Designed to support different failure scenarios

Current peak @ 1 Mrad



From : X-ray irradiation studies on the Monopix DMAPS in 150 nm and 180 nm

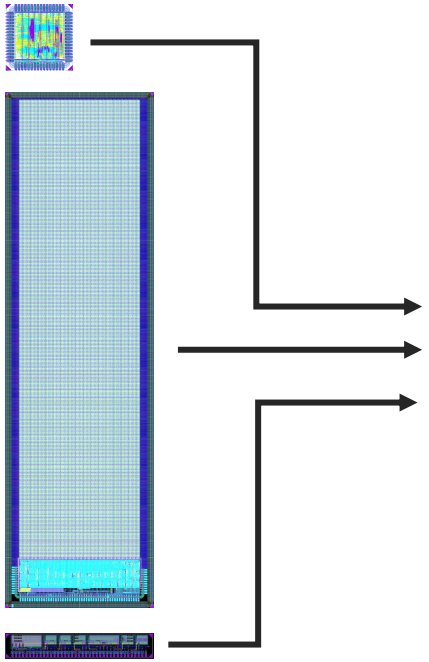
Functionalities needed for RADPIX2

RADPIX 2

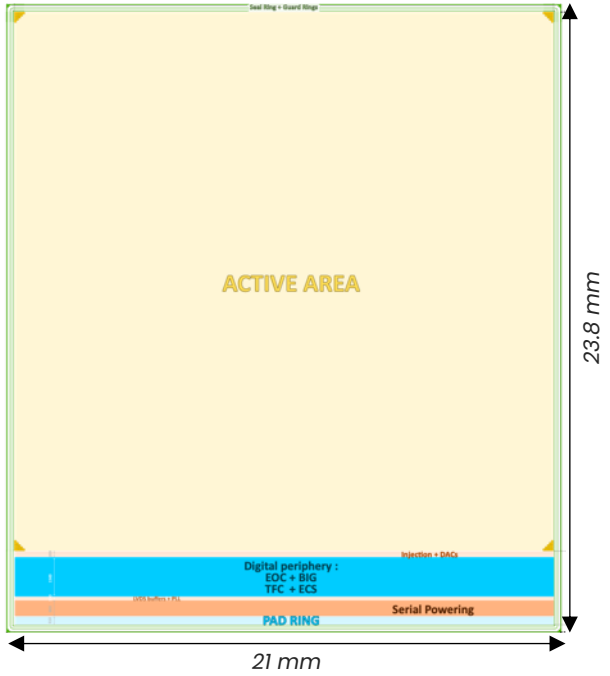
BIG : *Synthesis design for full chip exist, power optimization*

RADPIX1 : *Pixel selection and TFC optimization*
Revamp of SC (ECS) and readout

SLDO : *Current margins*



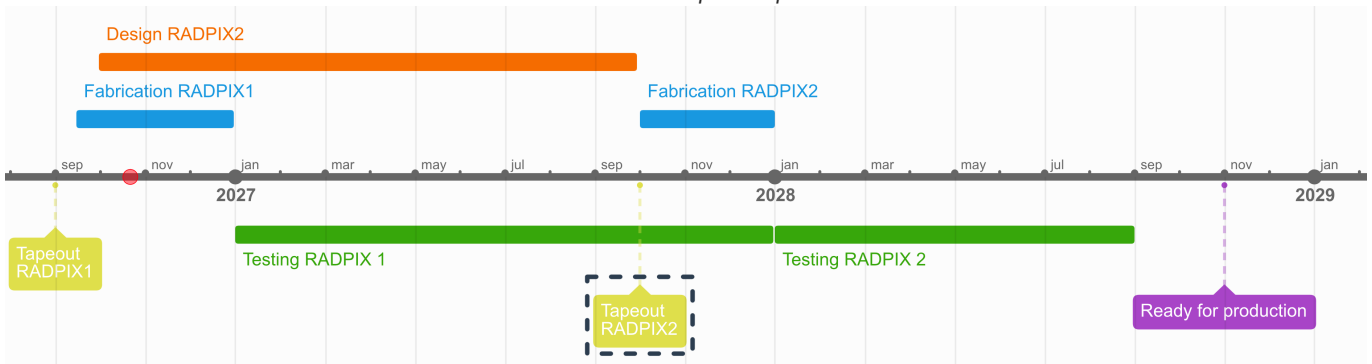
RADPIX2



- 256 × 256 pixels (~ 4 cm² active area)
- PLL from CMS HGCROC design
- Radiation hardness → digital periphery
  - Current study on DICE cells in LF
- ECS protocol ("Slow" Control)
  - Up/down links to LpGBT
  - AC coupled signals (serial powering)
  - Daisy chain up link for 5 sensors

- RADPIX R&D plan
  - Active test campaigns in Q1-Q3 2027
  - RADPIX 2 tapeout in Q4 2027

RADPIX development plan



Radpix2, full size sensor for LHCb UP/MT

Summary

Upgrade of the tracker stations (Upstream Pixel & Mighty Tracker) in LHCb foreseen for the long shutdown 4 at CERN LHC

- HV-CMOS pixel sensor in LF 150 nm technology for LHCb trackers :
  - **Column drain architecture** has been proven to be radhard in this technology (LF-MONOPIX and RD50-MPW4)
    - High-res p-type CZ substrate
    - HV bias ~ -500V
  - **RADPIX1**, ¼ final size prototype, reusing the previous design concepts → LHCb, submitted in august 2026
    - 4 pixel flavors, column drain architecture, for power and in-time efficiency optimization
    - Digital periphery with LHCb TFC control interface and AC coupled readout
- Test chips companions in the same run to anticipate RADPIX2 functionalities
  - **Bunch Id Grouping** (BIG) : full digital ASIC, with optimized signal processing for UP high hit rate physics events
  - **Serial Powering Chip** : Shunt Low Drop Output matching RADPIX1 needs
- **RADPIX2**, submission in Q4 2027
  - Included RADPIX1, BIG & SLDO
  - Additional functionalities development planned : Radhard digital cells & PLL + LHCb ECS

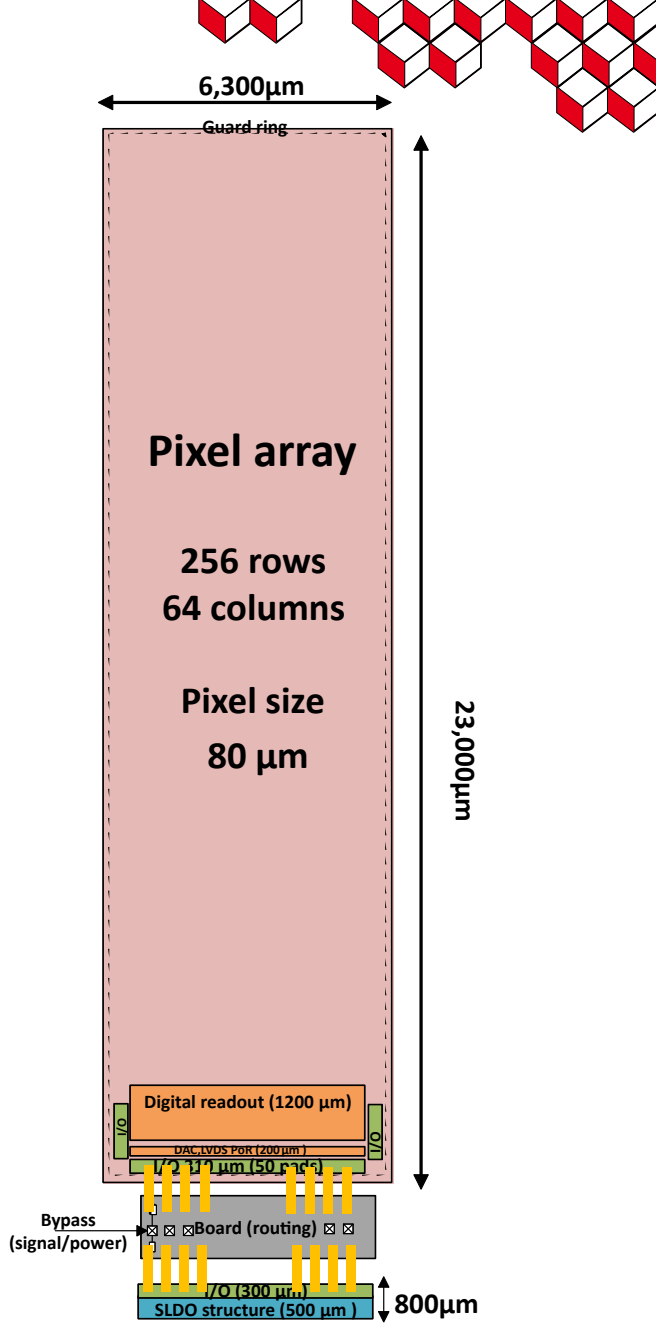

Merci

Radpix

- What's not considered in Radpix1:
  - Implementing a full radiation strategy : (Triplication, Parity checks, DICE…)
    - Test structure embedded (CRC, …) but not a full chip
  - High hit rate - data sharing strategy for UP/Mighty tracker expectations.
    - Investigation in another test chip : BIG
  - 95% sensitivity.
  - Further IPs: Daisy chaining (?) & faster slow control, PLL, ADC, DLL.

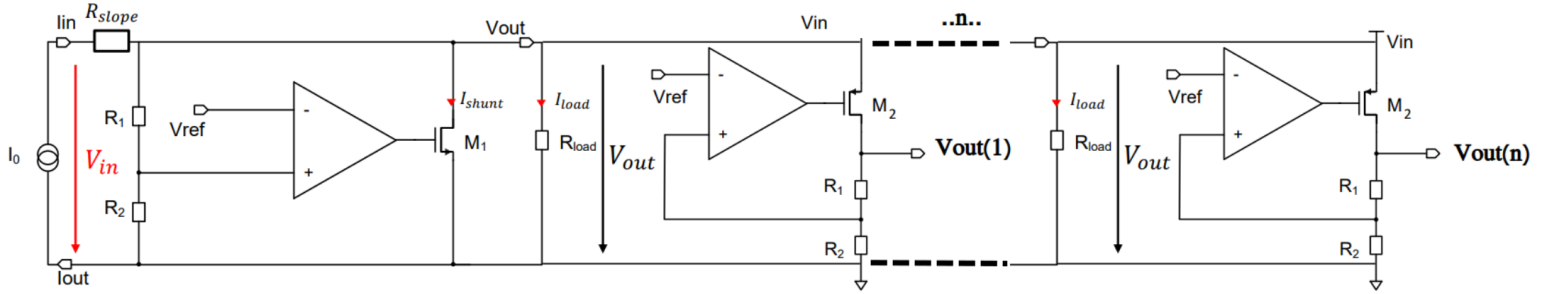
Digital periphery blocks	Level of modification from RD50 MPW4
Control unit	No modification
CLK division + system reset synchroniser	Clock division removed
BXID counters (ToT and ToA counters)	Modified from 8b/8b ->12b/5b
Periphery and top level	Same structure but many modifications
I2C_slave_Wishbone_protocol (IP)	Reused CERN IP
Config Status Registers	(small modification) added more registers
Snapshot registers	New
EOC structure	Moderate modification
TFC block (Time Fast Control)	New - provided by Velo
TX FIFO &EOC FIFO	Replaced Genus FIFO- same timings
Data transmission unit and sub blocks	Modified

LHCb & MP 2 compatibility

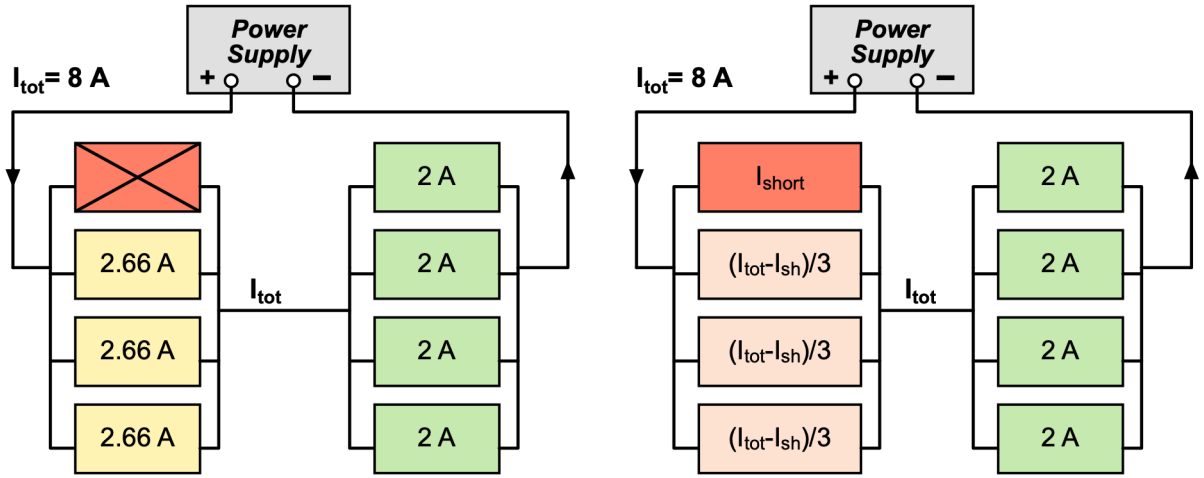


Radpix

- **SLDO**
  - Following the FE-I3 regulator approach
  - 7 SLDO
  - Verifications
    - Stability & Power Supply Rejection Ratio
    - Failures mode :
      → Open
      → Short



- **Risk mitigation**
  - Independent test chip
    - Tailor to Radpix1

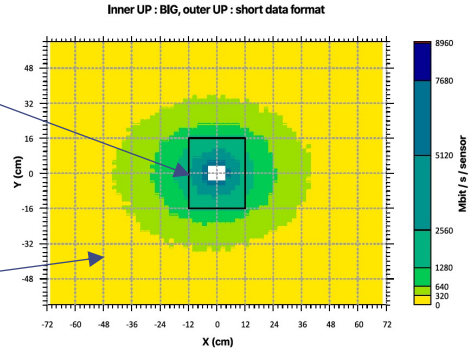


BIG

- Grouping hits by shared timestamp (BXID, bunch crossing ID) allows us to reduce redundancy without losses.
- Theoretically, we could reach a 68% compression rate at max UP's hit rate, only requiring 6 output links.

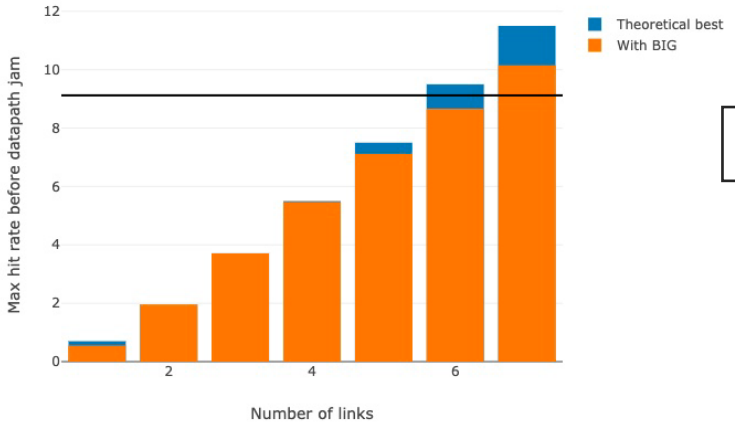
BIG data format

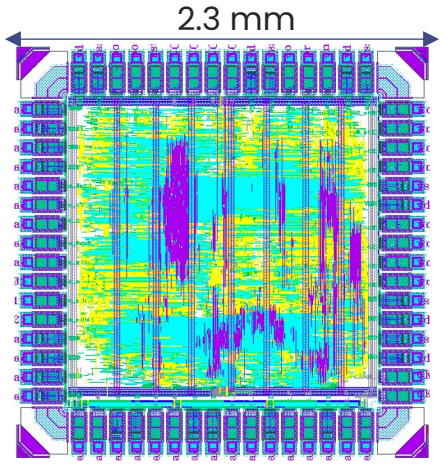
Short data format



Data Simulations → Datapath Model → RTL → Physical Implementation

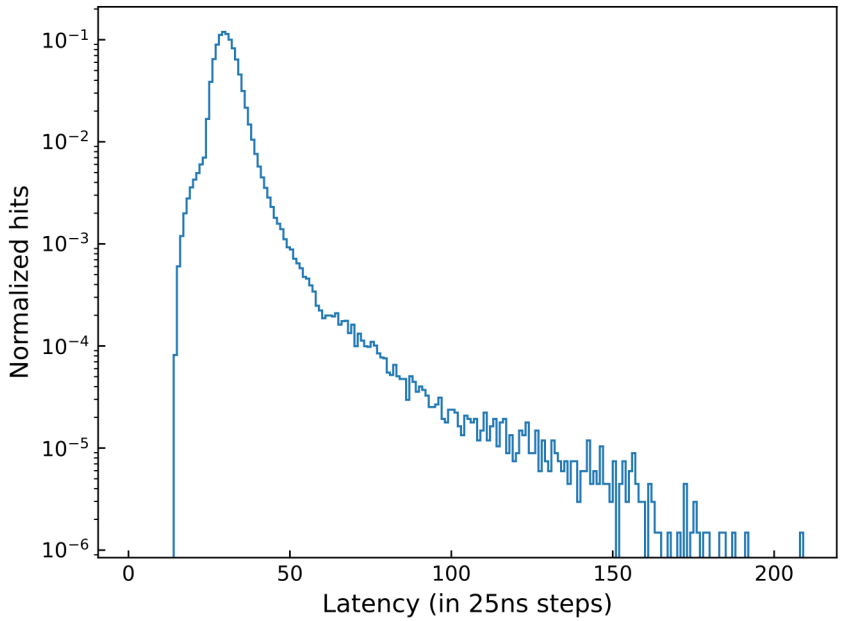
In practice, front-end delays push us to completely revamp the readout architecture

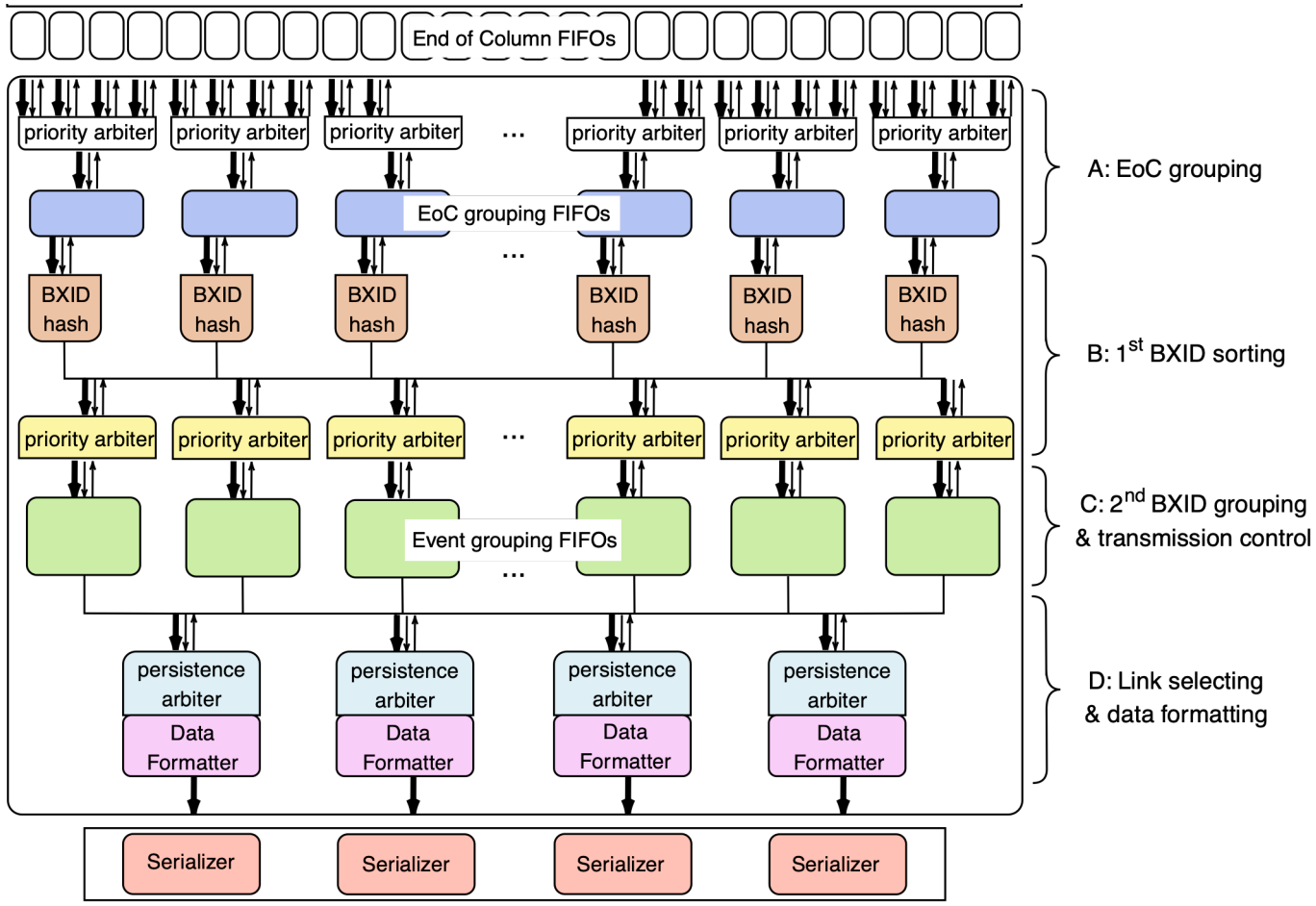




BIG

- Prototype BIG in LF 150 nm
  - 2.3 x 2.3 mm2
  - SR for testability
  - Design to be ”plugged” to Radpix EoC
  - Fifo sized optimized to Radpix FE
    - ToT ~ 500ns
    - Expected latency and hit rate in the UP



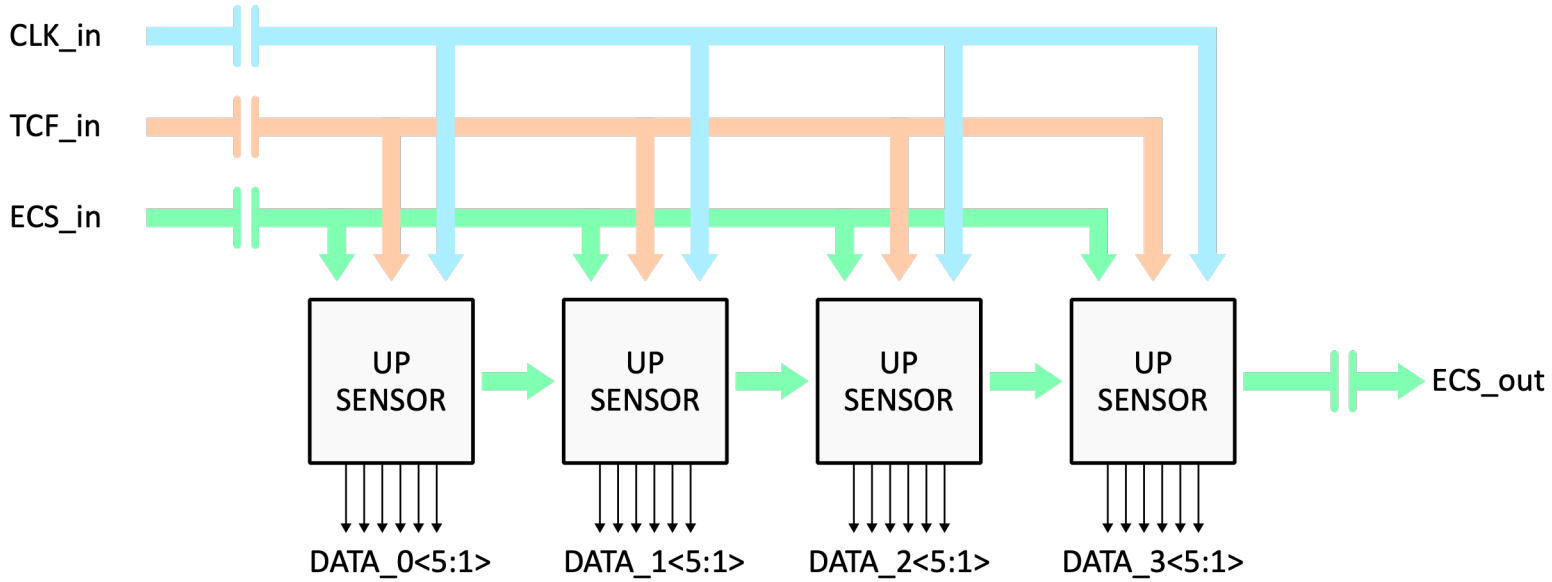


UP sensor full connectivity scheme

Assumptions :

- Multi-drop e-link will be used to the lpGBT for TFC and ECS.
- For ECS & TFC, up to 5 sensors will connect to the same e-link down-link.
- For ECS up-link requires a daisy chain.
- The TFC e-link can be fanned out to multiple sensors

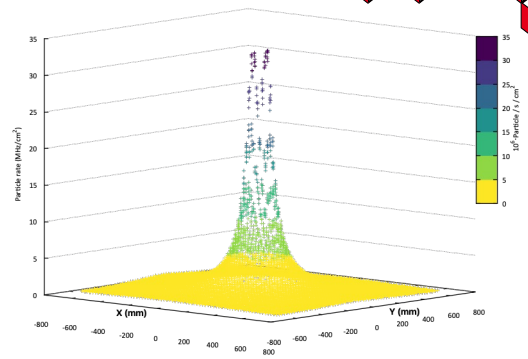
From Ch. Renard



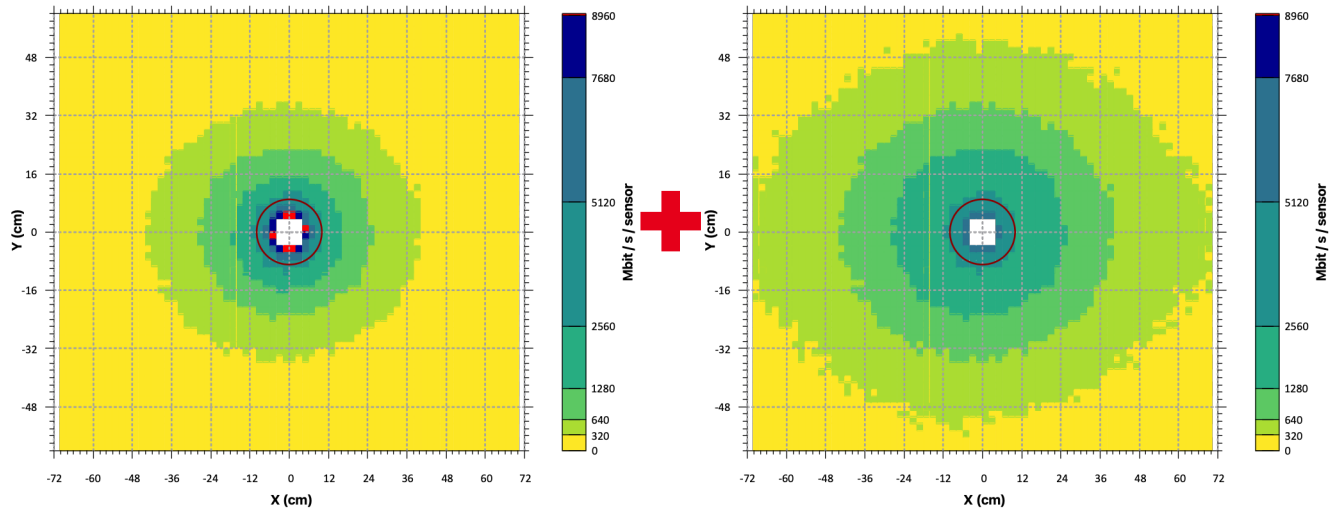
ECS AC coupled ! Scrambling protocol under study : 8b/10b alike protocol

UP DATA rate & DATA format

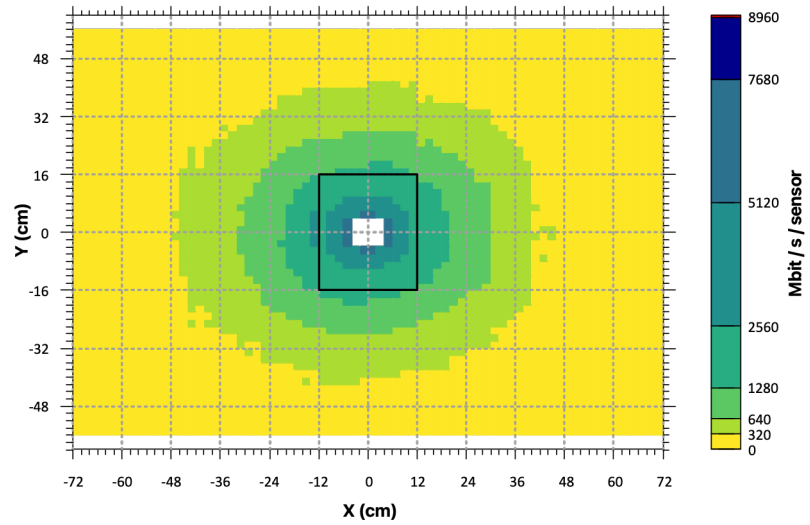
- Exponential decay of the particle rates in the UP → 2 data formats
  - Outer : 32 bits/hit, Inner : BXID sharing with 32 bits header + adaptative number of words
  - Strong assumption : ToT not needed for ToA correction (still to be fully demonstrated)
  - Worst case sensor : **6 e-links at 1.28 Gbit/s** thanks to the BXID sharing data format



Data rate for the UP0 depending of the data format @ 1.0 10^{34}



Combined Data rate



Short data format

b'00	Chip	BXID	Col	Row

BXID sharing data format

b'01	Chip	BXID	NumHits	
Col 1		Row 1	Col 2	Row 2
...			...	
Col N		Row N	(0x5555, for odd NHits)	