HV-CMOS Tracker System R&D with Serial Powering

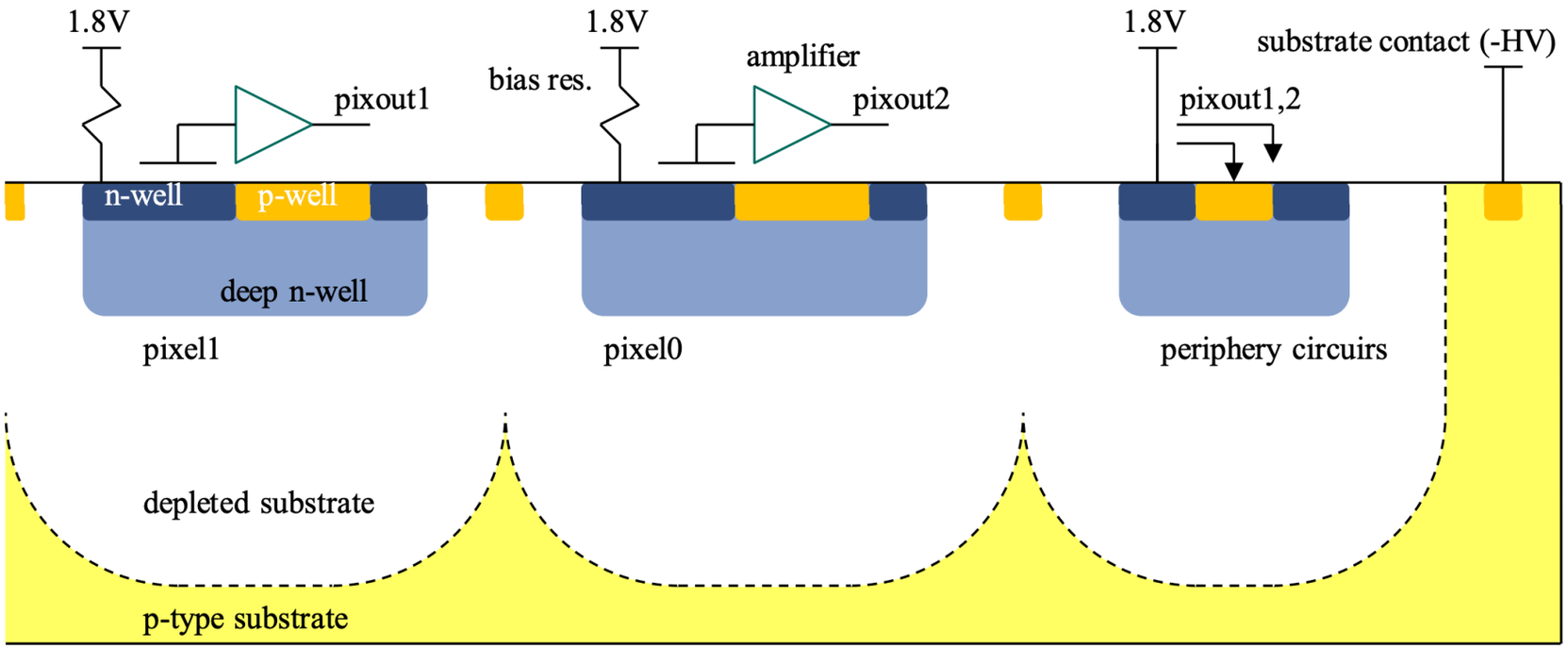
Yanyan Gao

University of Edinburgh

DRD3 and LHCb Upgrade II

The 2026 CEPC workshop in Shanghai (21-26 Oct 2026)

HV-CMOS and Serial Powering



Schematics: Ivan Peric

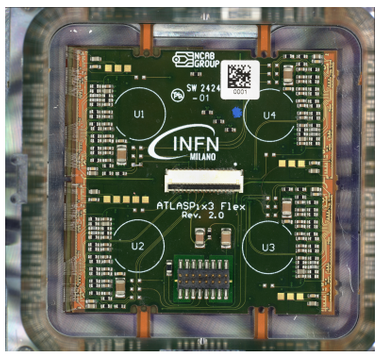
Readout electronics inside the collection diode

High radiation tolerance for HV substrate biasing

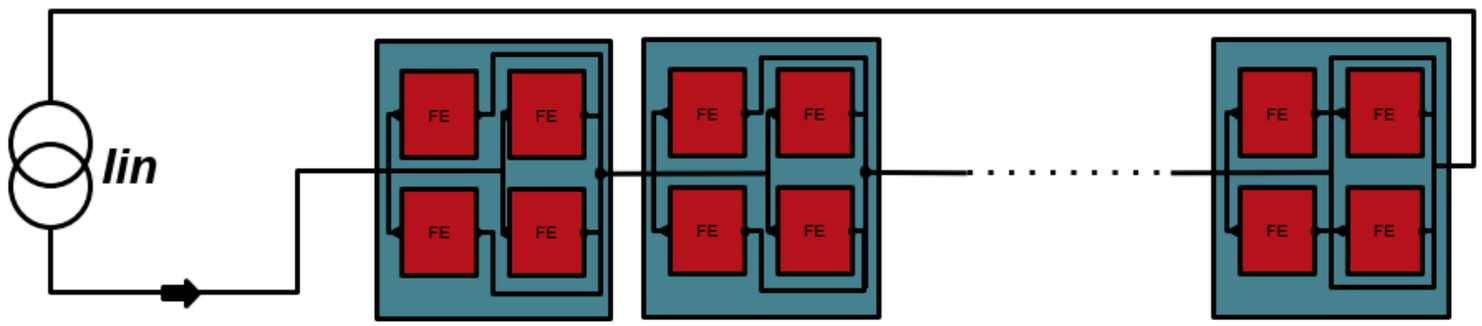
Signal collected by drift

Excellent (ns-level) timing resolution

- Large tracker system (10-100 m2), often requires, O(20k-200k) chips
  - Data aggregation, material budget, and efficient powering are key system design targets



Quad-Module: 4 sensors in parallel powering



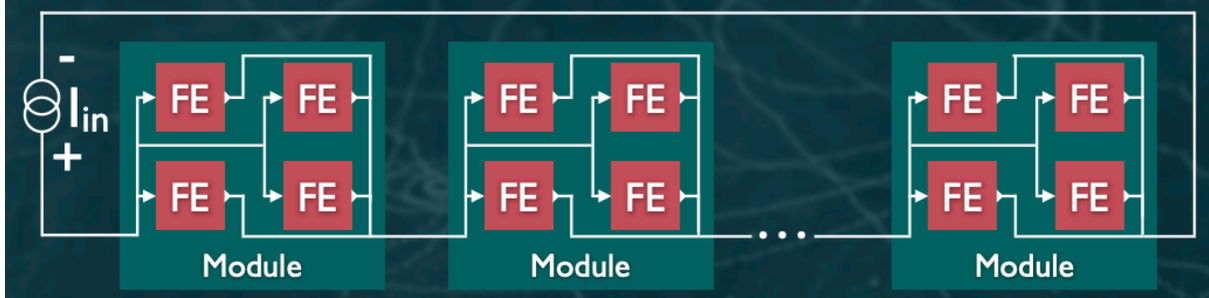
N modules powered in series with constant current

Naive ideal scaling: a factor of N reduction in the number of cables and the overall power loss in cables

ATLAS ITk (Hybrid Pixel Detector)

Timon Heim (RD53/ATLAS-ITk)

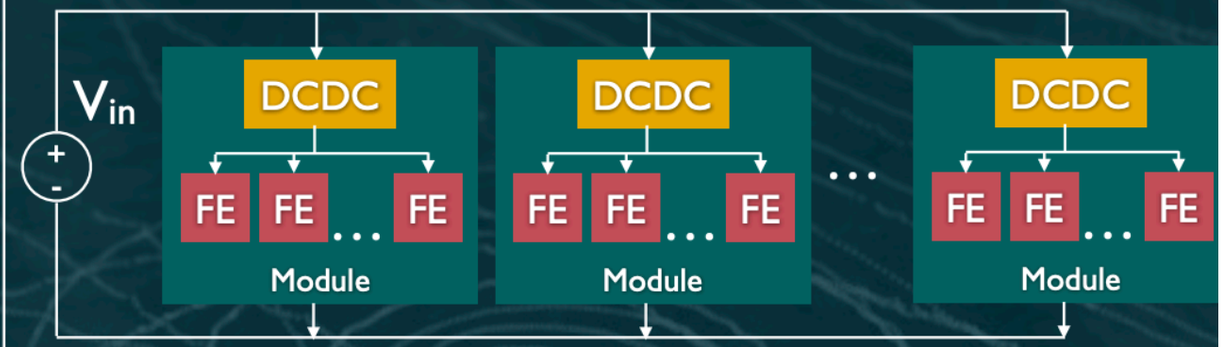
Serial Powering



Pro:
- Compact on-chip regulator design
- Robust against most common failures
- Redundancy against most severe failure
- Efficiency improves the longer the SP chain
- "Simple"
- Inherently radiation hard
- Proven to be exceptionally robust against noise

Con:
- System behavior defined during design → Need excellent knowledge of FE under operational conditions
- Regulator optimization coupled with FE chip design
- Realistic* testing requires full SP chain (N Modules)

DCDC Conversion



Pro:
- Well understood and widely used regulator design
- Efficiency independent of no. of modules
- Can be optimized independently of other components (or even developed independently e.g. CERN bPOL12V)

Con:
- DCDC converter cannot be manufactured in FE chip technology (high voltage switches)
- EMI from switch mode converter can induce noise in detector
- Requires bulky inductor
- Shielding increases mass
- Single point of failure

The radiation tolerance limit for DCDC, and constraints of cable space/material budget pushed ATLAS towards a full SP baseline for all pixel subsystems

Requires on the chip Shunt LDO circuits constant voltage, shunt excess current, low extra power overhead, and much more…

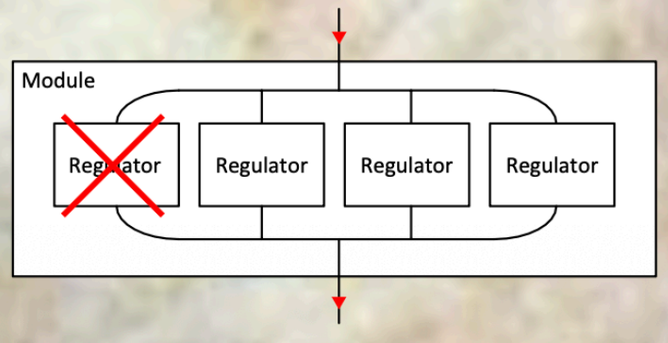
What else?

Fachhochschule Dortmund
University of Applied Sciences and Arts

The Serial Powering Commandments

- **You shall prevent the break of the serial powering chain**
- **You shall avoid hot spots**
- **You shall distribute power equally across the chips and the module**
- **You shall avoid single point of failure**
- **You shall introduce redundancy**

- **You shall operate several regulators in parallel on module level**



Michael Karagounis (RD53 SP circuit main designer): Link to his talk in LHCb SP workshop

DRD3 HV-CMOS SP Demonstrator

- DRD3 Funded Collaboration Common Fund Project (PI Attilio Anderazza)
  - A three-year (2026-28) system integration motivated project in parallel with sensor development
  - Strong synergy with LHCb Upgrade II tracker, EPIC tracker, as well as DRD7

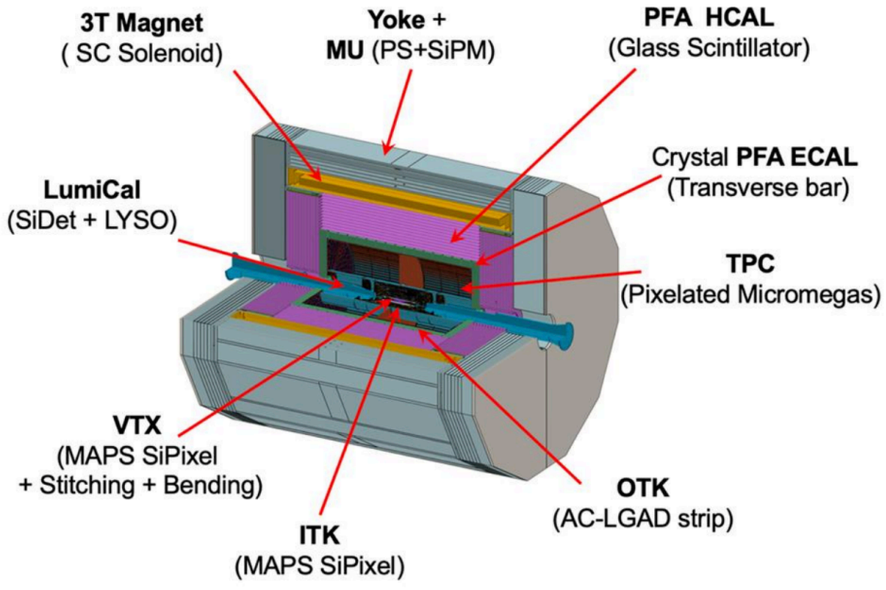
Report number	CERN-DRD3-PROJECT-2025-014
Title	**CCF: HV-CMOS Pixel Detector Demonstrator with Serial Powering and Innovative Interconnections**
Status	Draft
Author(s)	Andreazza, Attilio (Università degli Studi e INFN Milano (IT)) ; Gao, Yanyan (The University of Edinburgh (GB)) ; Peric, Ivan (KIT - Karlsruhe Institute of Technology (DE)) ; Glover, James Julian (University of Birmingham (GB)) ; Velthuis, Johannes (University of Bristol (GB)) ; Fox, Harald (Lancaster University (GB)) ; Muenstermann, Daniel (Lancaster University (GB)) ; Li, Yiming (Chinese Academy of Sciences (CN)) ; Augustin, Heiko Christian (Heidelberg University (DE)) ; Iuppa, Roberto (Universita degli Studi di Trento and INFN (IT)) ; Beole, Stefania Maria (Universita e INFN Torino (IT)) ; Novel, David (FBK Trento) *Hide*
Publication	2025
Document contact	Contact: Attilio Andreazza Email: attilio.andreazza@cern.ch
Imprint	2025-05-26
Project	DRD3
Abstract	This proposal (June 2025-June 2028) aims to develop a large area HV-CMOS pixel detector demonstrator for large-scale production in future Higgs factory experiments, based on multi-chip modules with data aggregation and serial powering. These multi-chip modules, including low-mass multilayer flexible PCBs, will then be integrated in staves, where modules will be powered in serial mode utilising the on-chip Shunt Low Drop Out (SDLO) regulators. Together with data aggregation, this will substantially reduce the number of stave data and power connections. Low-mass aluminium flex productions, innovative connection methods (e.g. single-point Tape Automated Bonding), low-mass mechanical support, and efficient cooling technologies will be explored for overall system optimization in power and material budget. The expertise gained by the participating institutes will be beneficial for the integration of future large scale devices that will be developed by the strategic DRD3 projects in the next few years.
Submitted by	yanyan.gao@cern.ch

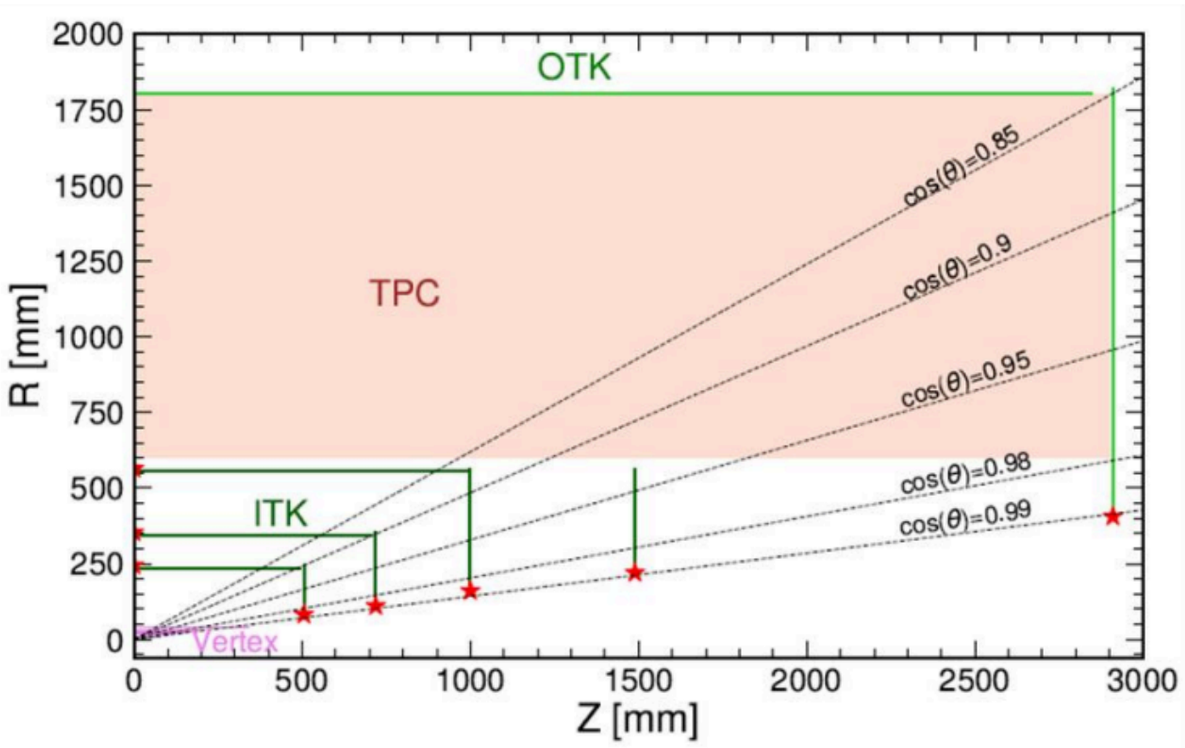
HV-SPII

Latest presentation in DRD3 (2025) - Attilio Andreazza

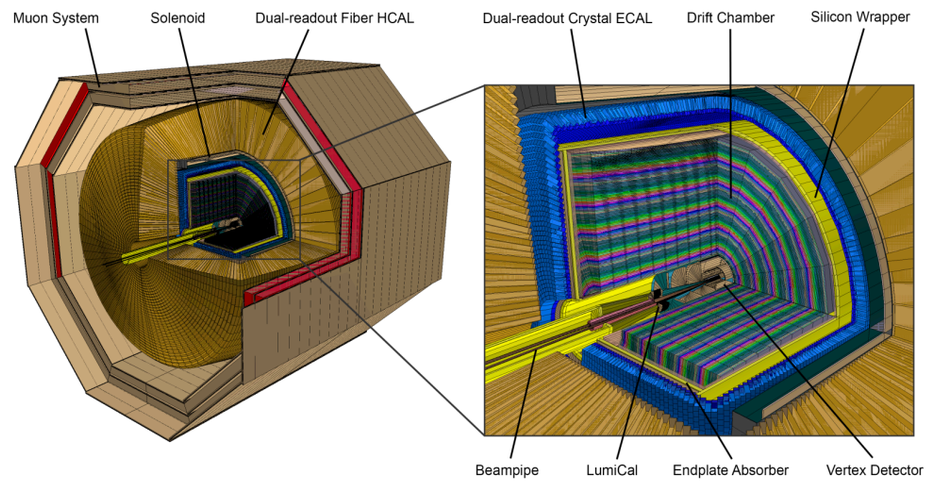
Example FCCee/CEPC Detector Applications

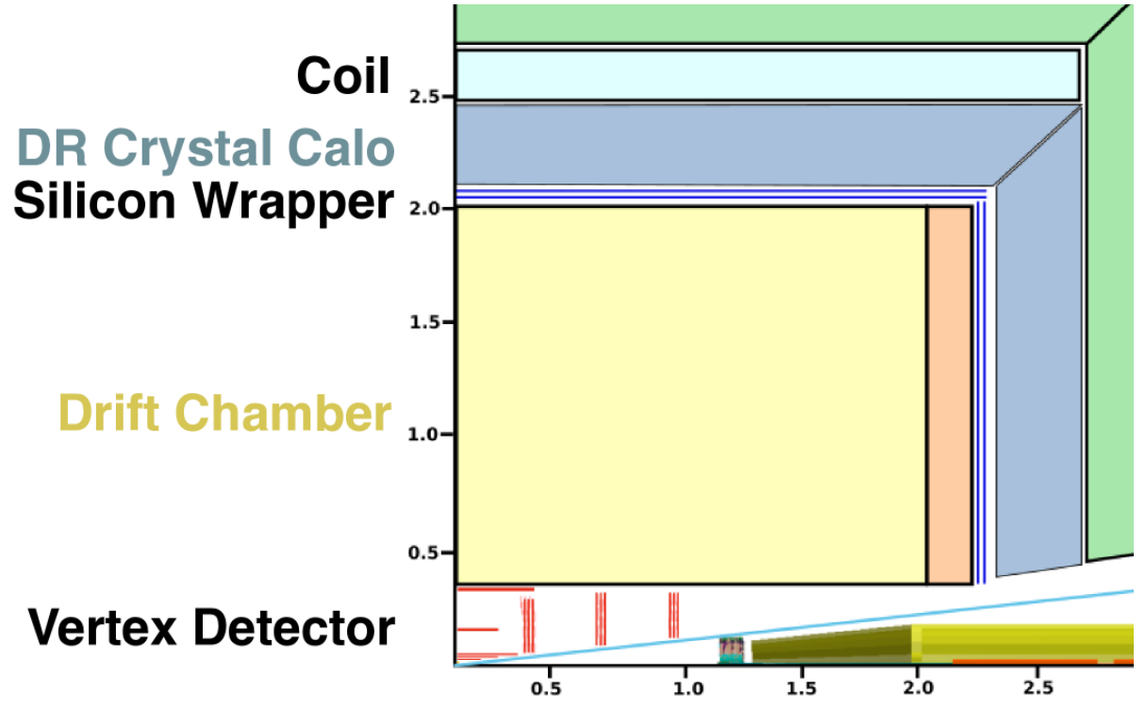
AGORA Detector: ITK subsystem





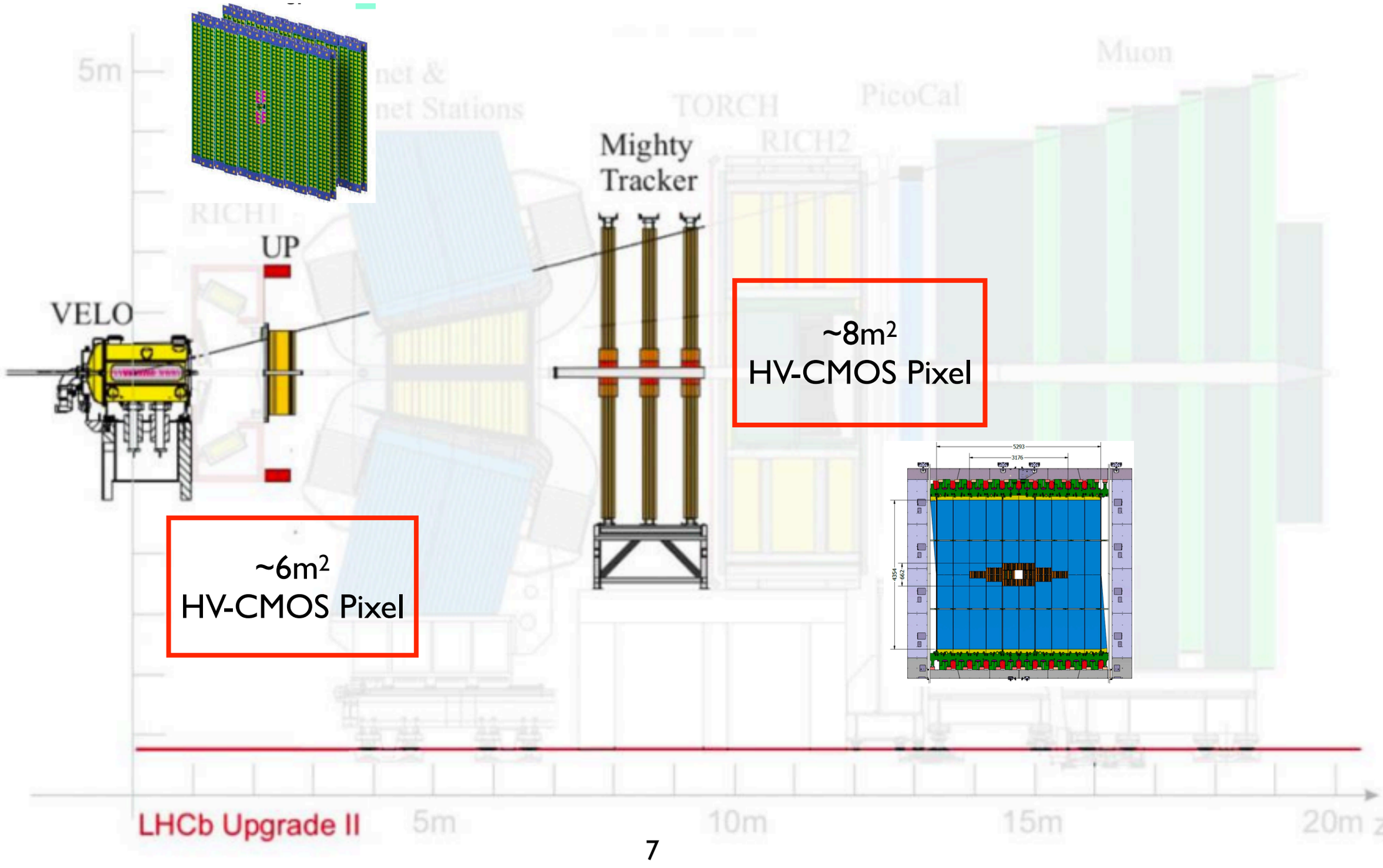
IDEA detector
Vertex Detector Silicon Wrapper





LHCb Upgrade II: Tracking Detector

- LHCb Upgrade II (2033-34): one of last major detector projects at the LHC
  - Precise vertexing and tracking, excellent PID, along with trigger and software
- Monolithic HV-CMOS technology is chosen for two main tracking detectors (similar size to ATLAS ITk pixel)



Sensor and SLDO Measurements

LHCb HV-CMOS Tracker Sensor Requirements

- In general requirements from the UP are harsher
  - Driven by the innermost region close to the beam, a factor of 3-8 higher particle rates/radiation
- Three current HV-CMOS development lines (all are co-developed with DRD3)
  - MightyPix series (180nm AMS/LF-150nm) : this talk will focus on its serial powering specs
  - RadPix series (LF-150nm): Fabrice Guilloux's talk on RadPix
  - ChiR series (55nm) : Zijun Xu's talk on AGORA ITk, and Tianyu Yang's Poster

UP

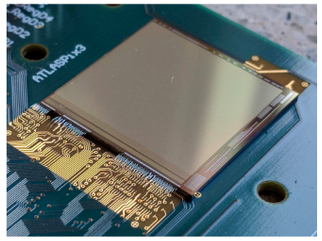
Parameter	Expected value	Safety factor	UP specification
Pixel size (bending plane)			$\leqq 100\,\mu m$
Pixel size (non-bending plane)			$\leqq 200\,\mu m$
Substrate thickness			$>100\,\mu m$ $<200\,\mu m$
Max. Particle Rate	40 MHz/ cm^2		
Max. Hit Rate	45.6 MHz/ cm^2	2	91.2 MHz/ cm^2
Max. length of data word			32
Transmission rate			N links of 1.28Gbit/s, N $\leq$ 7
In-time efficiency			>99% within 25 ns
Noise rate (end of life)			$\leq$ 400kHz/cm^2 @ max. 1% masked channels
NIEL	$1 \times 10^{15}\ n_{eq}$/cm^2	3	$3 \times 10^{15} n_{eq}$/cm^2
TID	62.5 MRad	3	187.5 MRad
Power consumption			$\leq$ 200 mW/ cm^2 + 25% overhead for serial powering

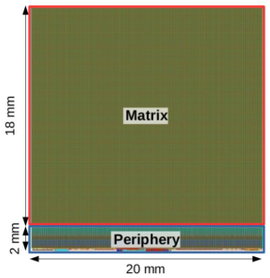
MP

Expected value	Safety factor	MP specification
		$\leqq 100\,\mu m$
		$\leqq 200\,\mu m$
		$>100\,\mu m$ $<200\,\mu m$
14.5 MHz/ cm^2		
18.8 MHz/ cm^2	2	37.6 MHz/ cm^2
		32
		4 links of 1.28Gbit/s, each multiplexed to 2 and 1 link
		>99% within 25 ns
		$\leq$ 400kHz/cm^2 @ max. 1% masked channels
$1.2 \times 10^{14} n_{eq}$/cm^2	3	$3.6 \times 10^{14} n_{eq}$/cm^2
12 MRad	3	36 MRad
		$<500\ \mu A$
		$\leq$ 150 mW/ cm^2 + 30% overhead for serial powering

MightyPix Family and Related Sensors

2019

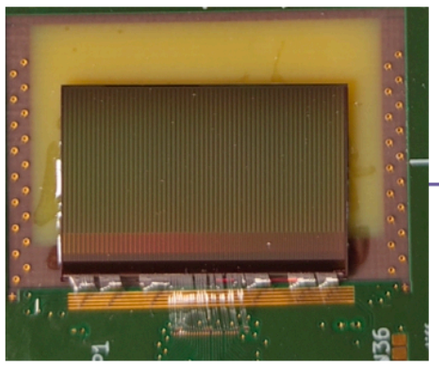




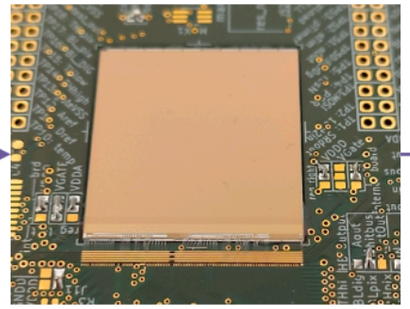
Precursor: ATLASPix3 (full reticle size)
candidate for the ATLAS ITk pixel outer layer
First full-size HV-CMOS chip with SLDO

2022 2024 2025 2026 2027

TelePix2

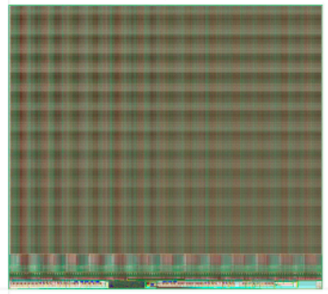


P2Pix

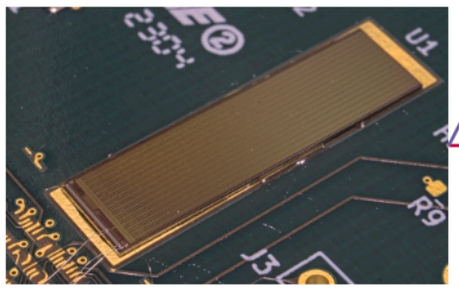


*MightyPix2
AMS

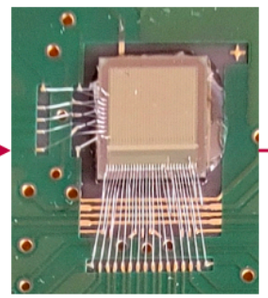
Pixel design



MightyPix3

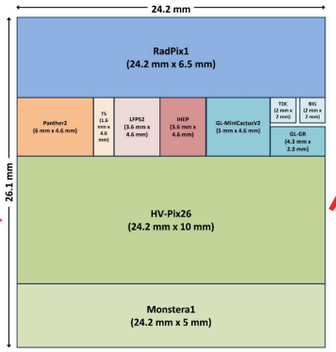


MightyPix1 TSI



LF-MightyPix

Digital design



*LF-MightyPix2
(HV-Pix26)

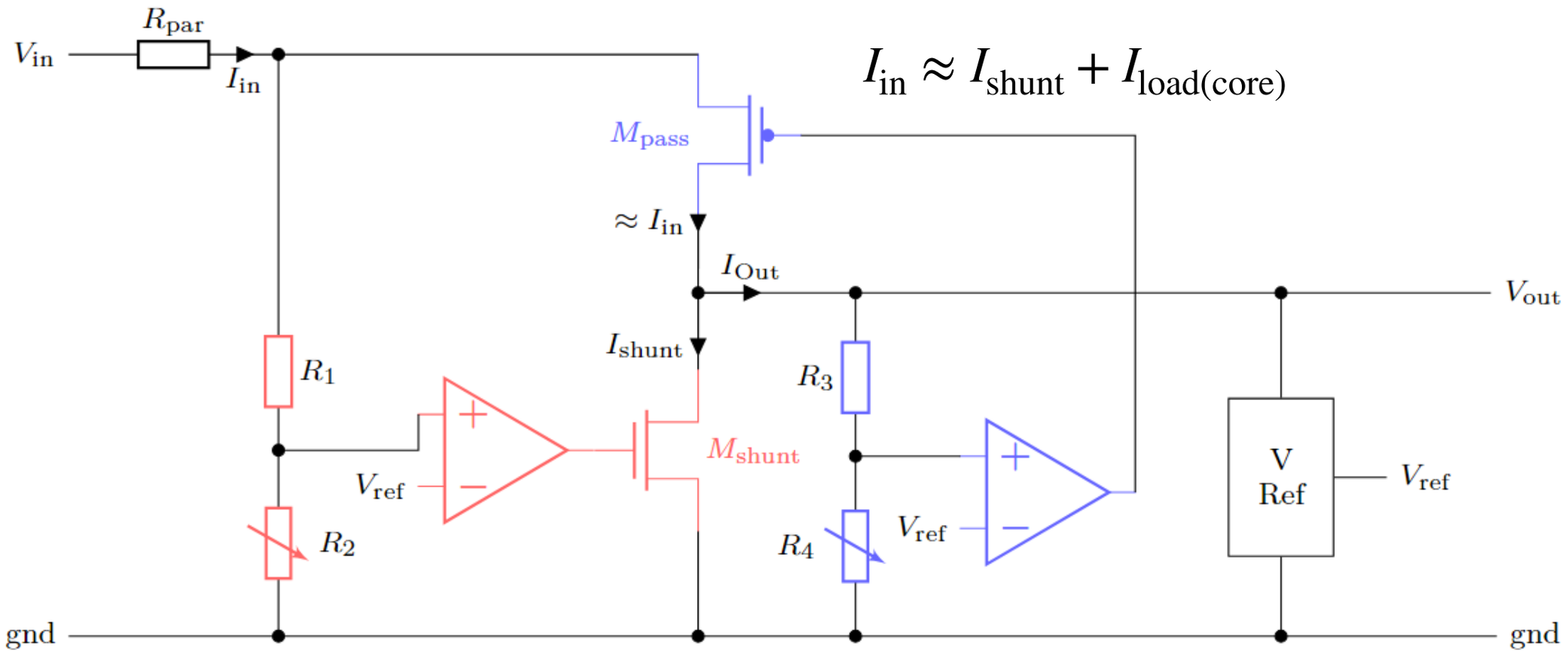
AMS (baseline)
LF (backup)

Adapted from schematic by Lucas Dittmann

Karlsruher Institut für Technologie

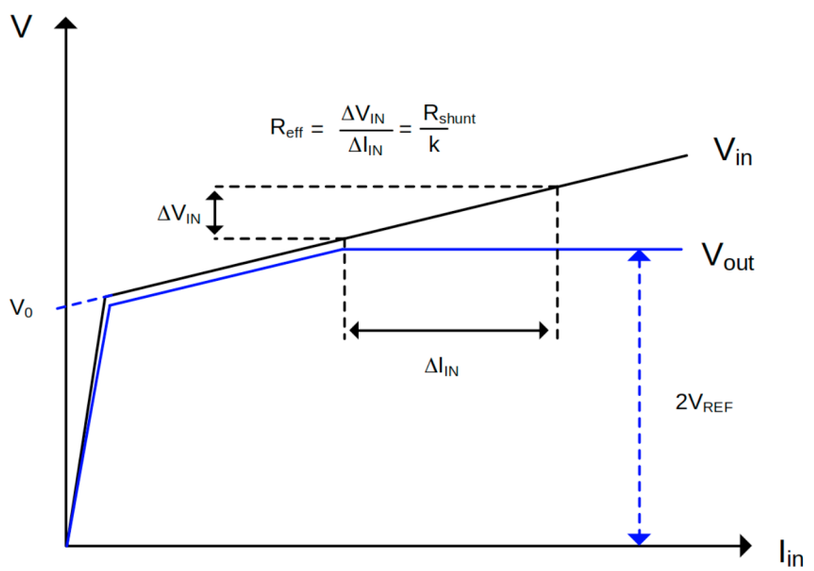
UNIVERSITÄT HEIDELBERG ZUKUNFT SEIT 1386

ATLASPix3 Shunt Low DropOut (SLDO) Design



At equilibrium: $V_{in} = V_{ref}\frac{R_1 + R_2}{R_2} + I_{in}R_{par}$ $V_{out} = \frac{R_3 + R_4}{R_4}V_{ref}$

- Shunt: Excess currents sunk through Mshunt
- LDO: provides regulated constant Vout
- Weakness: only parasitic feedback from load current on Vin



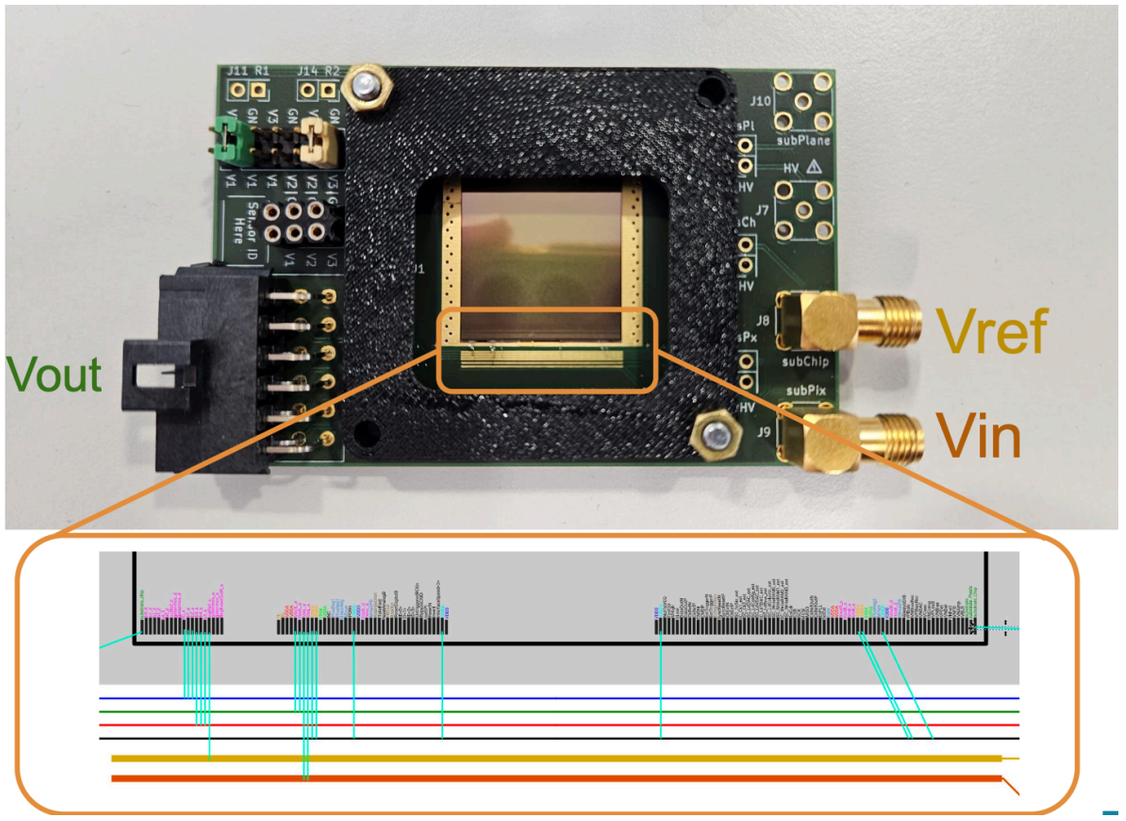
Example IV

LHCb-MT: Generic SLDO Test Stands

- A generic automated test-bench for SLDO validations from Heidelberg
  - Focus on "isolated" SLDO circuit verification, without connecting a real chip load
  - Suite of measurements are performed
    - Strongly motivated by RD53/ITk experience: Link to Michael Karagounis Talk in LHCb SP workshop

1. Static Measurements
   - Line regulation (input variation)
   - Load regulation (output variation)
   - Reference regulation (Band gap)
2. Transient Measurements
   - Startup (turn-on behavior)
   - Load & Line Transient† (regulation stability)
3. Environmental Influences
   - Temperature influence
   - Total ionizing dose (TID) effects
4. AC Measurements
   - Output Noise Spectrum
   - **P**ower **S**upply **R**ejection **R**atio

Current setup with APix3 evaluating a single SLDO
Easily adapted to other chips or standalone circuits

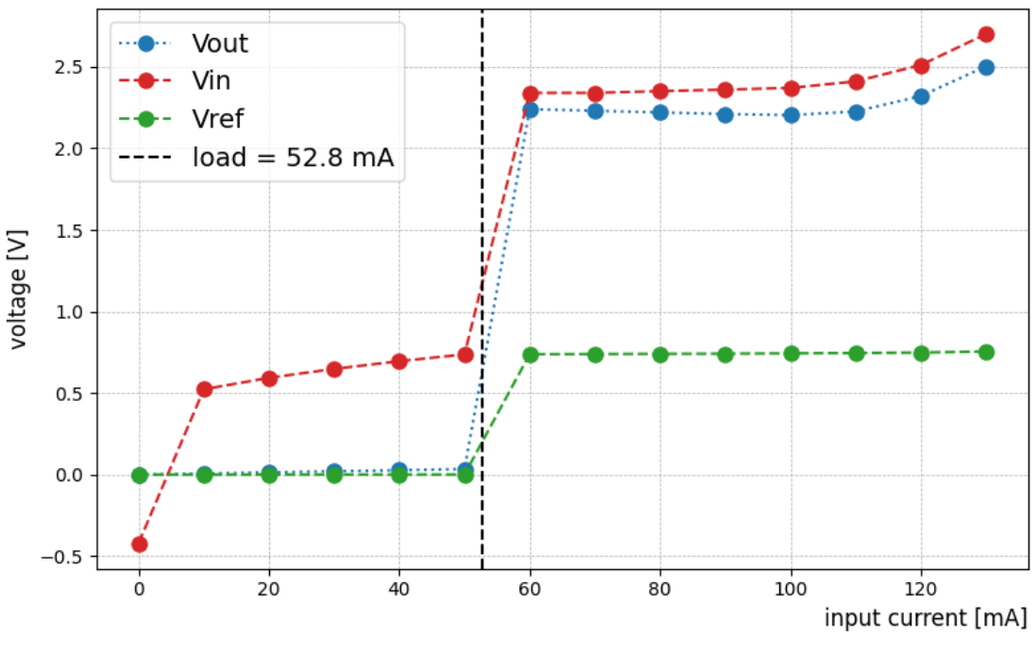


David Immig (Heidelberg)

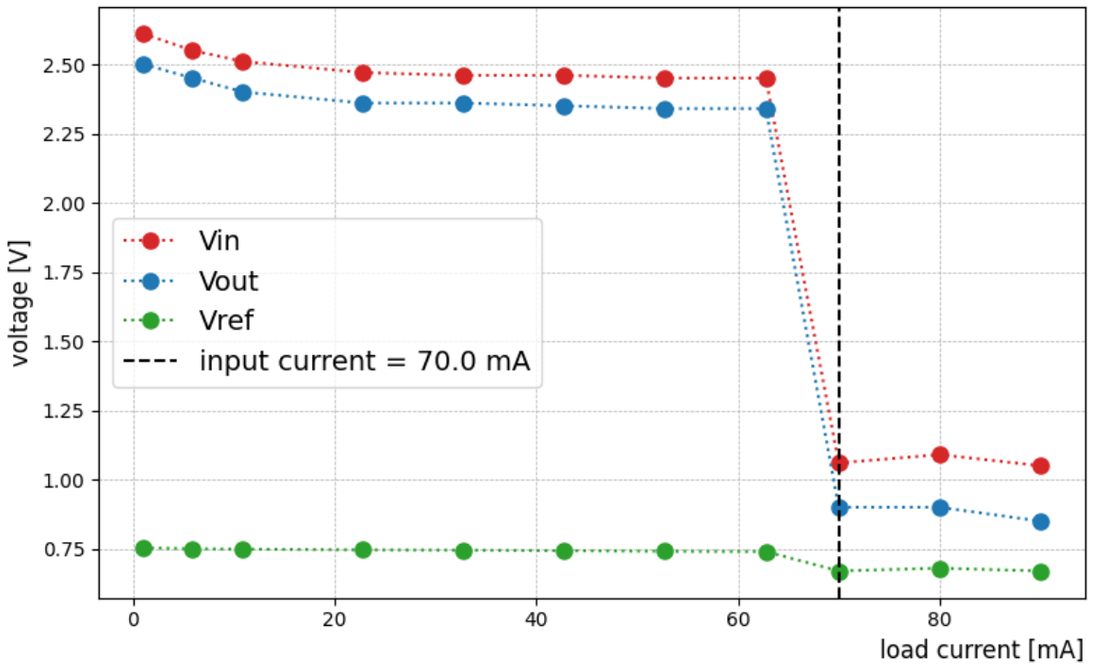
Highlight of Static Measurements - ATLASPix3

- Measurements are currently based on a single block of the power/shunt transistor

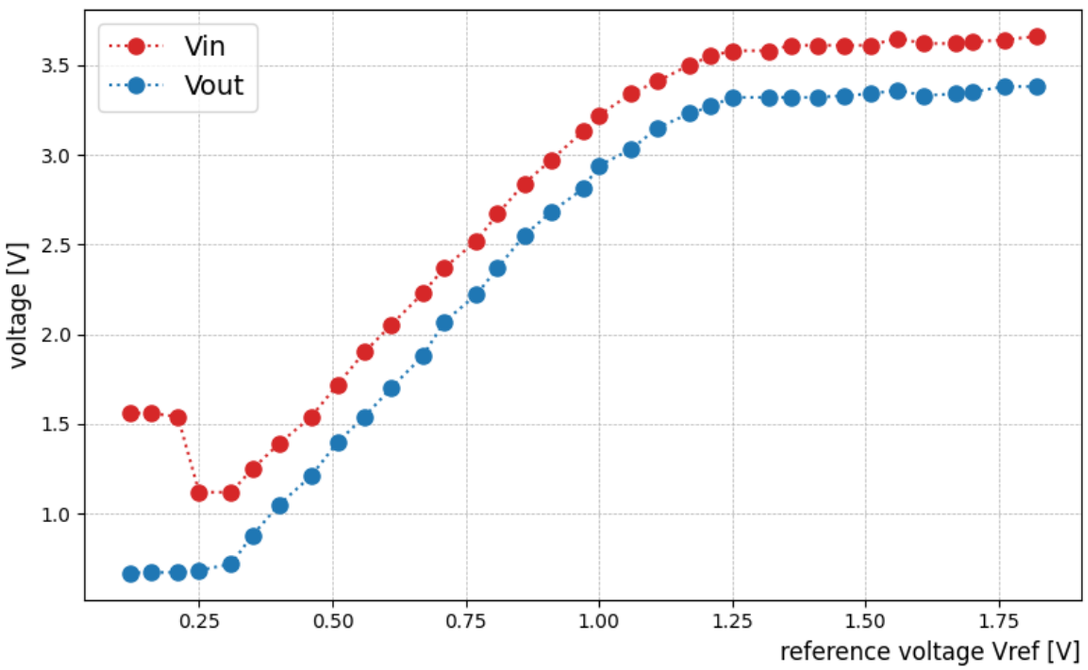
Input Line regulation



Output Load regulation



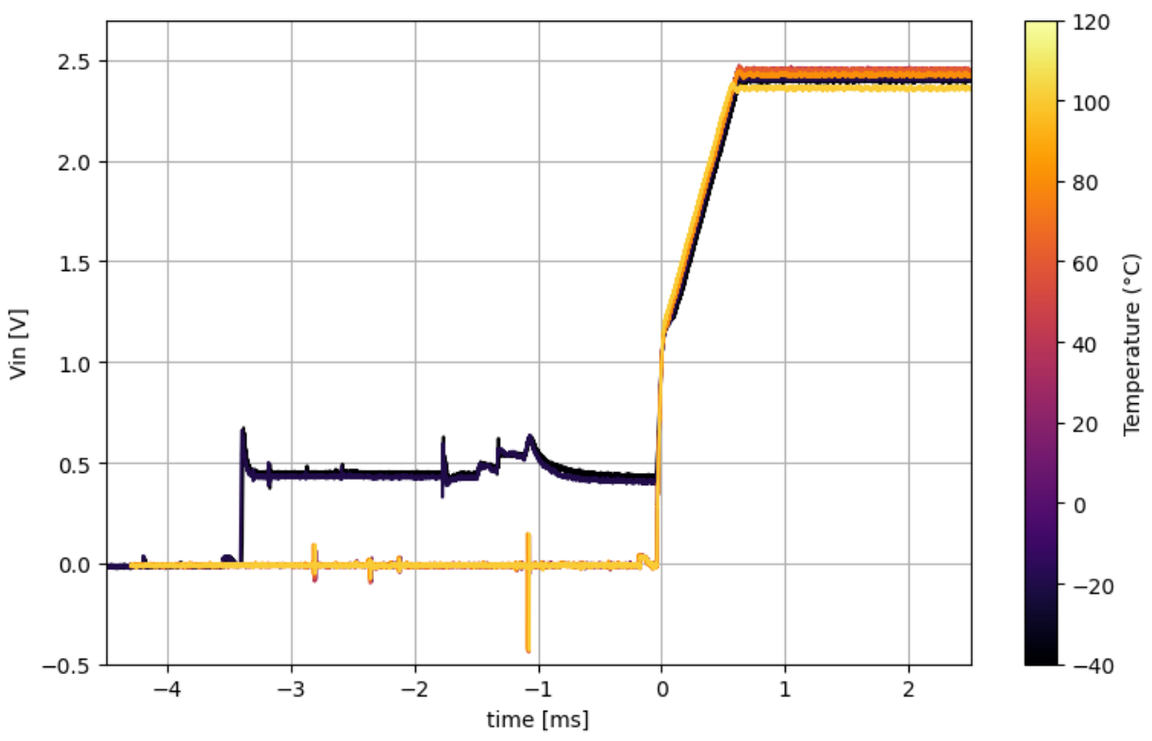
Reference Voltage Regulation (Externally supplied)

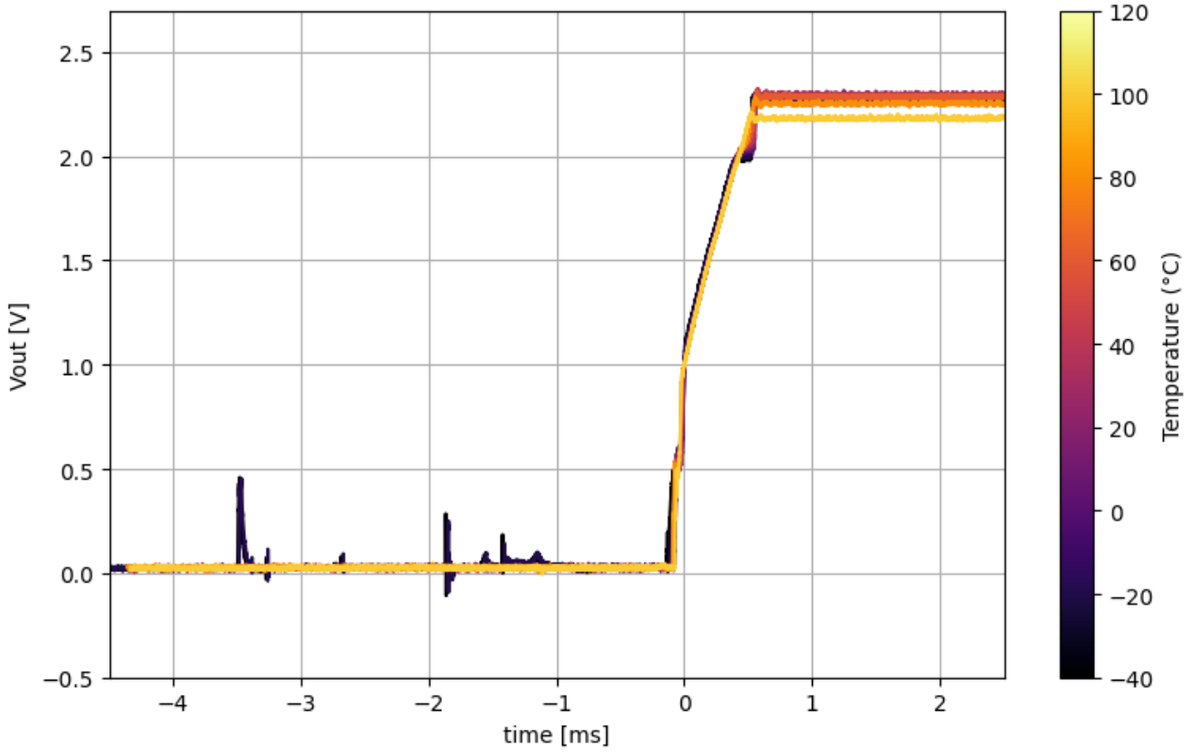


Transient Measurements: Instantaneous Startup

- Check "instantaneous" start-up for 100 mA load at different temperature (-40 °C to 100 °C)
- Startup working for all ambient temperature, but differing behaviour for sub-zero temperatures

No large unexpected pulse seen during startup and temperature impact small

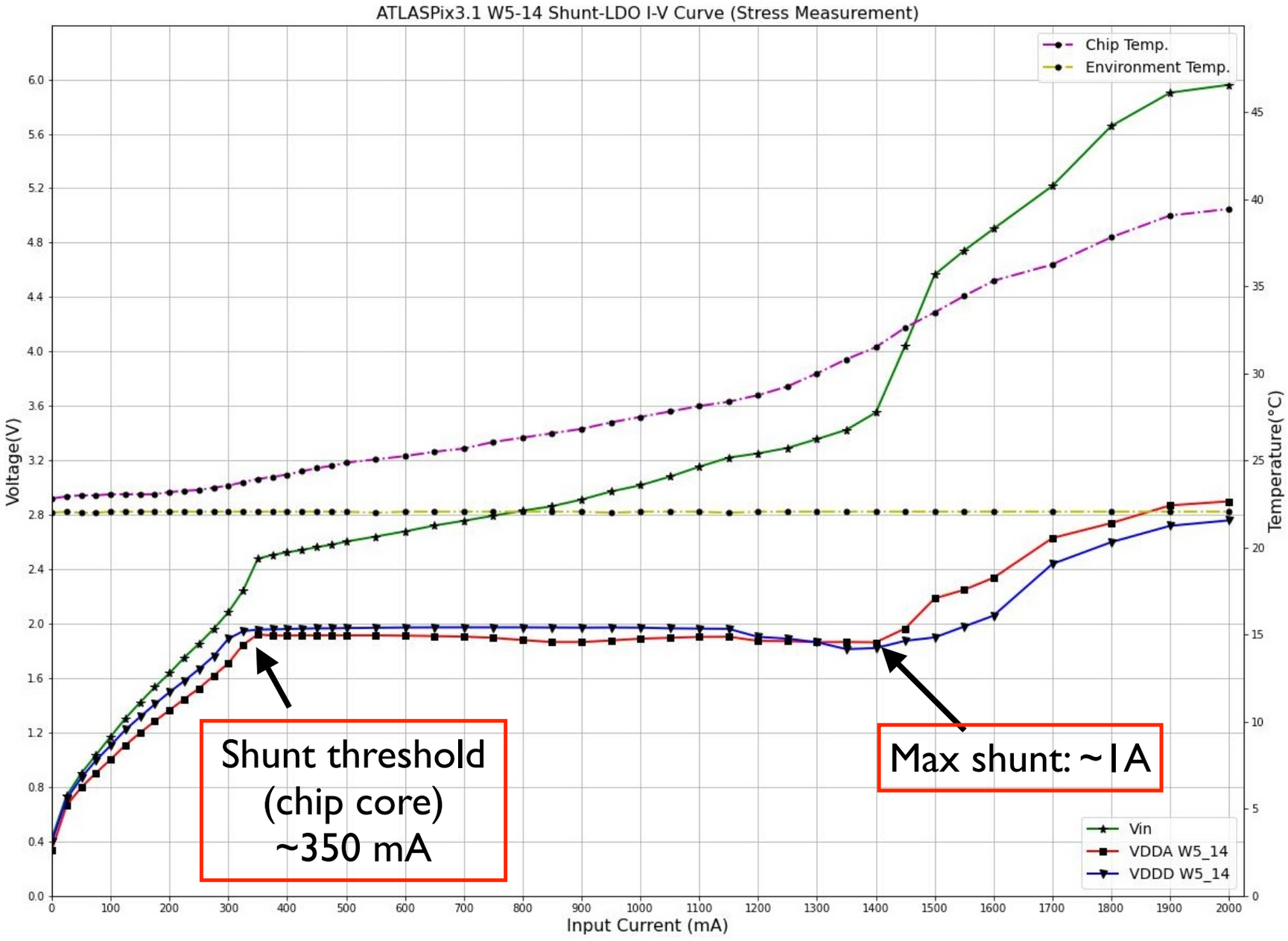


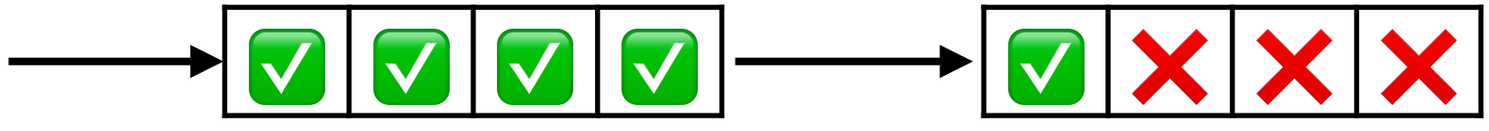


David Immig (Heidelberg)

VI characteristics with Chip Load - ATLASPix3

- All blocks in the chips are activated, including both analog and digital blocks





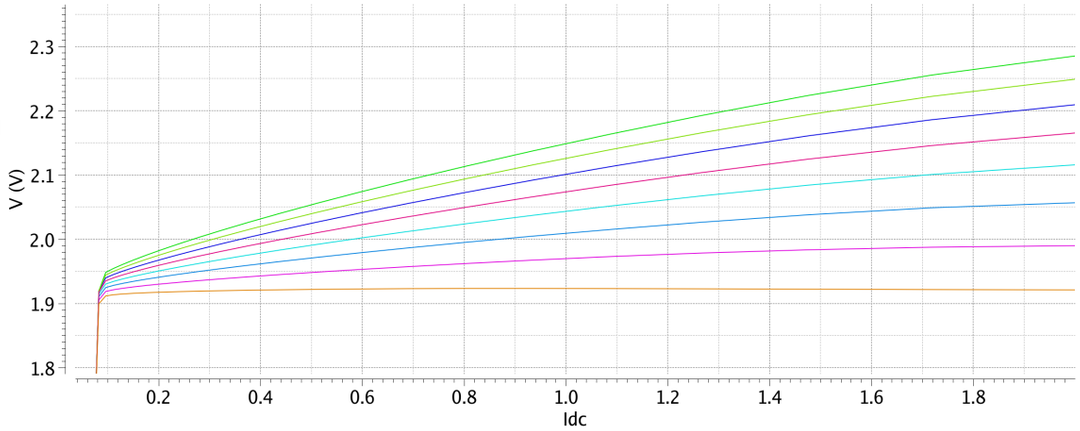
MightyPix2 SLDO Design

- Increased power FET width by factor >2 (2A max current) and improved temperature stability of reference
- Additional circuit for feedback load current Iin feedback on Vin
  - Load current is divided by N*M and subtracted from feedback divider curren
  - K is configurable 3-bit current DAC
- Additional standalone SLDO test chips

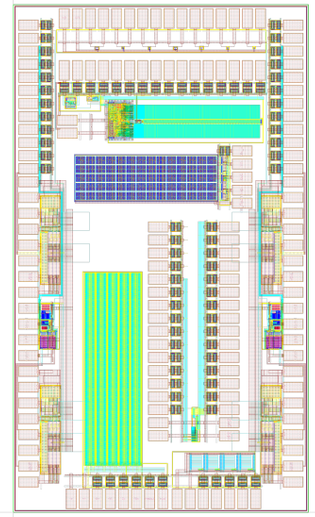
$$V_{in} = V_{ref}\frac{R_1 + R_2}{R_2} + I_{in}\left(\frac{\mathbf{K}\,\mathbf{R_1}}{\mathbf{NM}} + R_{par}\right)$$

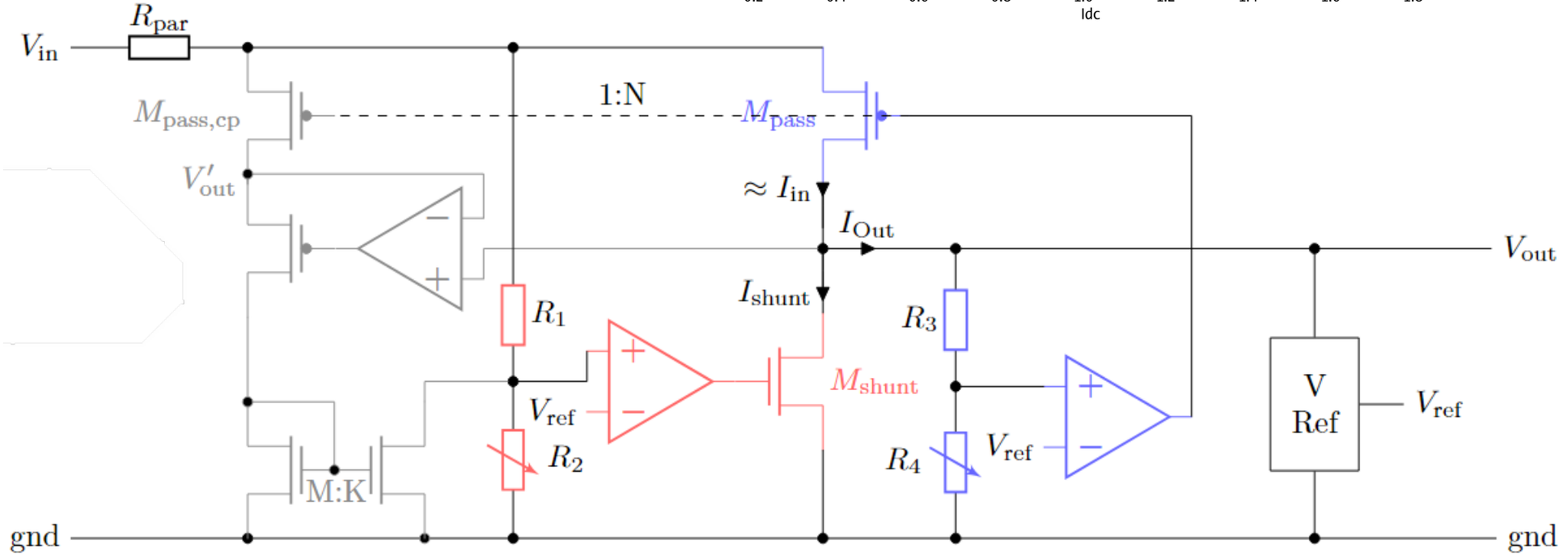
Simplified form similar to the RD53 design (Michael Karagounis)

$$V_{in} = V_{os} + \frac{R_1}{k} I_{in}$$



SLDO test chip





Layout by Bowen Xu

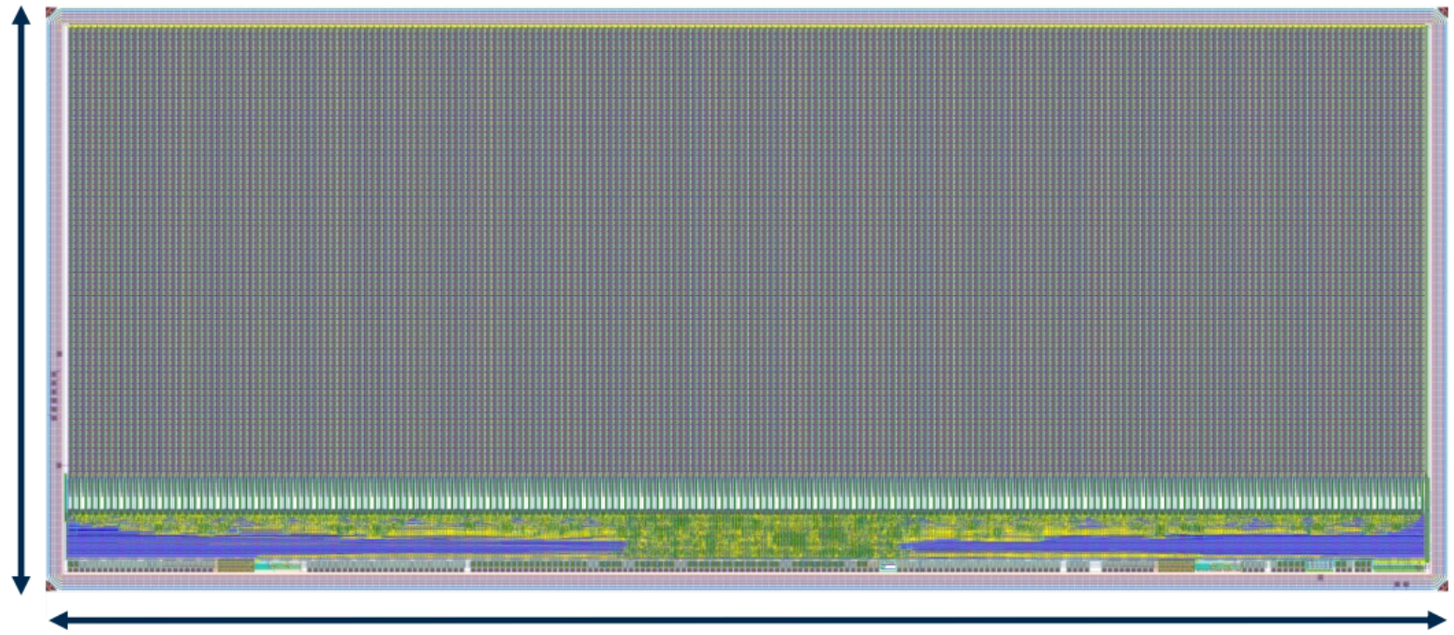
Link to Nicolas Striebig (KIT) ttalk in the DRD3 CCF meeting 15-Oct 2026

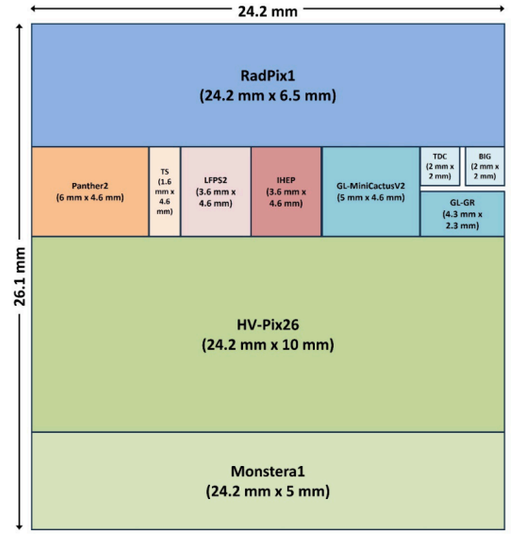
HV-Pix26/LF-MightyPix2

- High Voltage Monolithic Active Pixel Sensor (HVMAPS)
- LFoundry 150 nm process
- Recently submitted in DRD3 organized MPW
- Design based on MP2 and LF-MP design and characterization results

Features

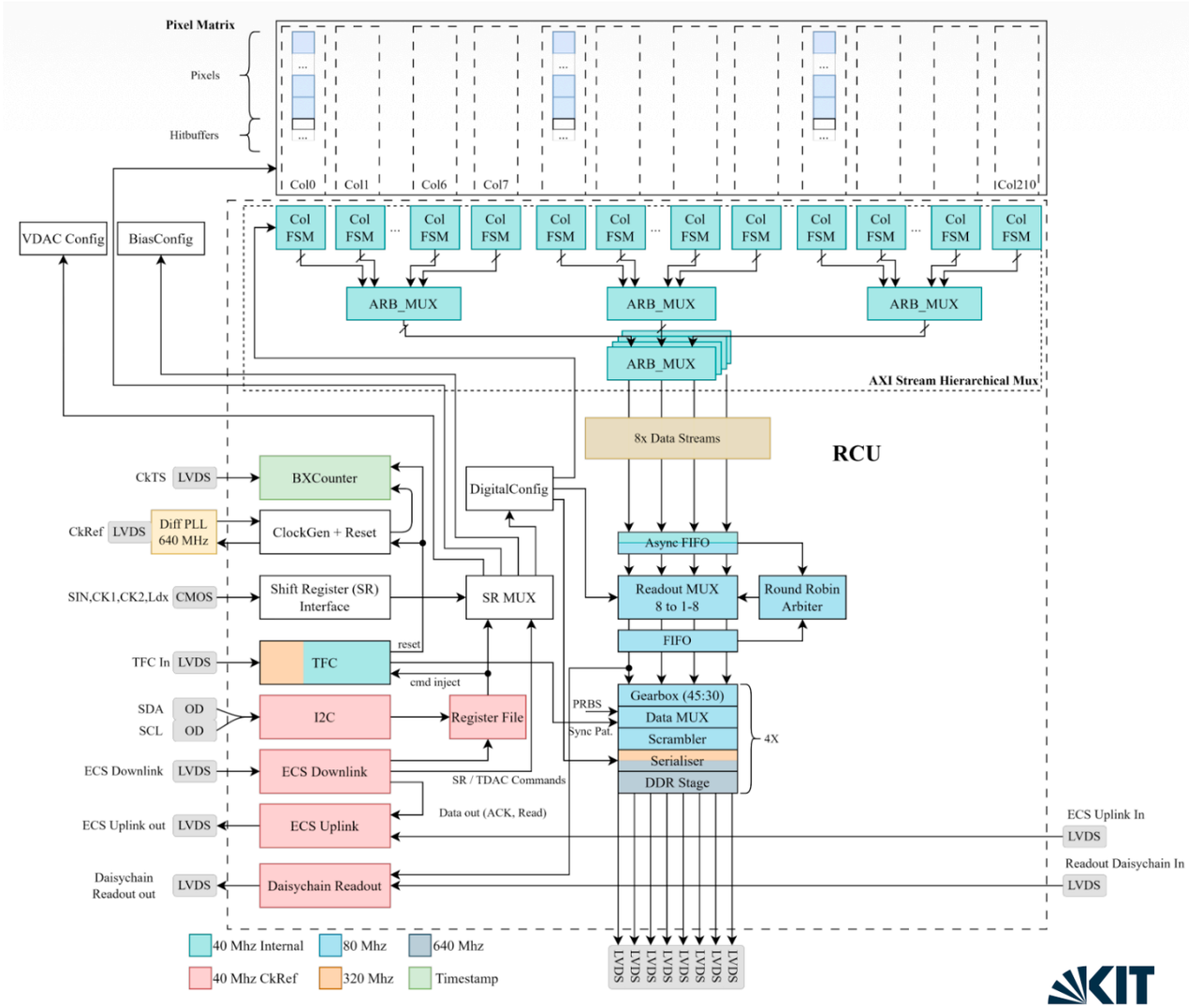
- Pixel matrix: 75 rows x 211 columns
- Pixel pitch: 100 x 110 um
- FE: NMOS input CSA, CMOS Comparator and per pixel TDC
- Timestamps: 11b ToA, 6b ToT, 6b TDC
- AXI Stream based matrix readout
- Digital Interfaces: TFC, ECS, I2C, SR
- Daisychain readout
- Data links: 8x1.28 Gbps = 10.24 Gbps
- Serial Powering





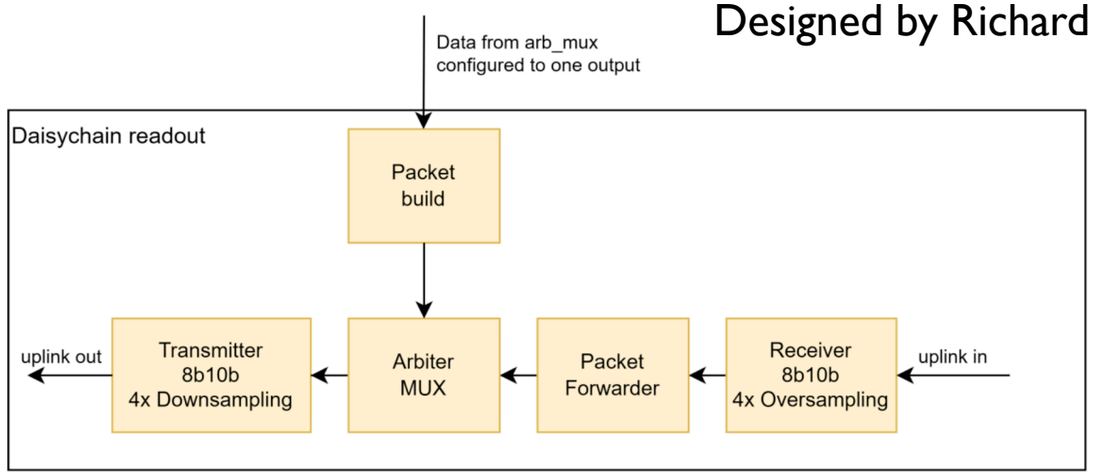
HV-Pix26: Readout Matrix and Daisychain Feature

- DRD3: first version of the data daisy chain implemented in parallel to the high speed readout
  - Further reduction in the services cables, particularly interesting for low occupancy environments (e.g. Higgs factory and outer regions of LHCb U2)
  - Significant improvement in data rate and control are envisioned for the future



- 8b10b encoding
- 10 Mbps data rate
- Packet builder gets data from arb mux configured to one output, to collect data from whole pixel matrix
- Arbiter injects data into chain, if space available in receiving FIFO

Designed by Richard Leys

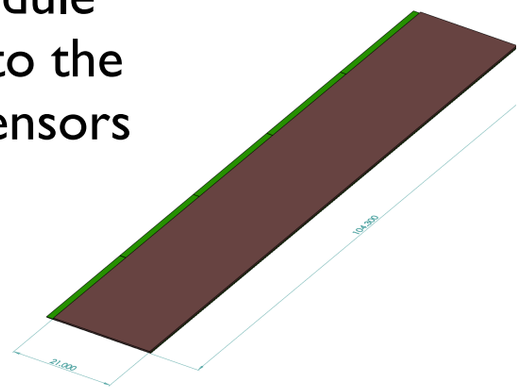


Link to Nicolas Striebig (KIT) ttalk in the DRD3 CCF meeting 15-Oct 2026

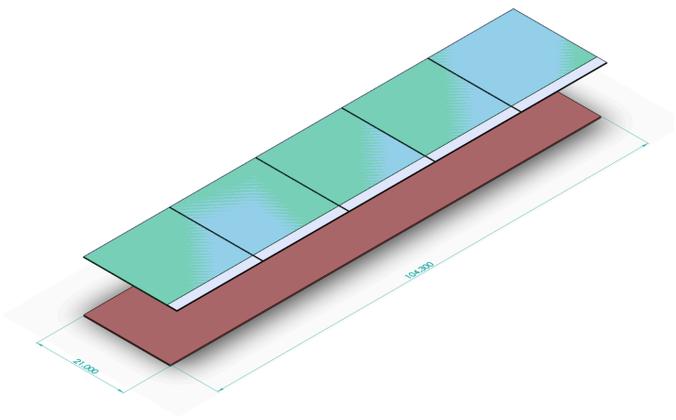
System and Powering Scheme

LHCb MT Stave Concept Design - Preliminary

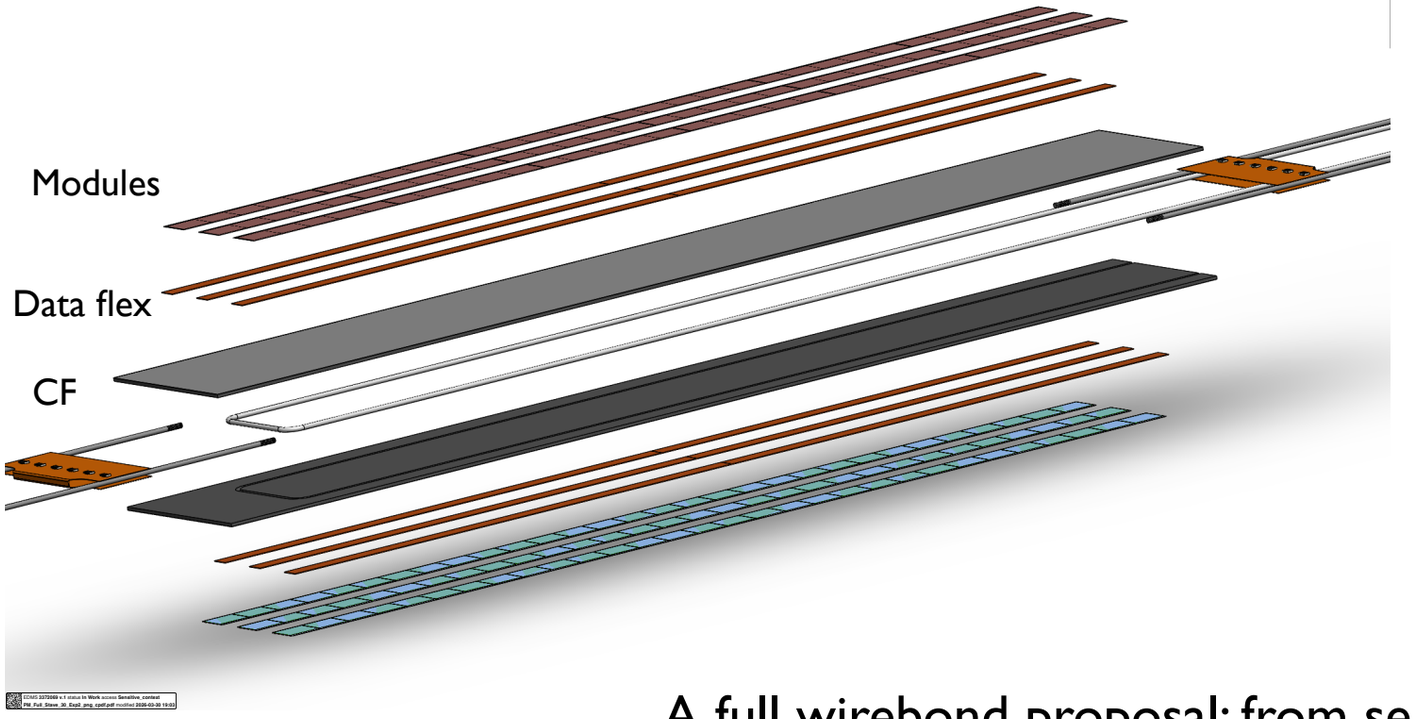
A 5-chip module
Flex bonded to the
front of the sensors

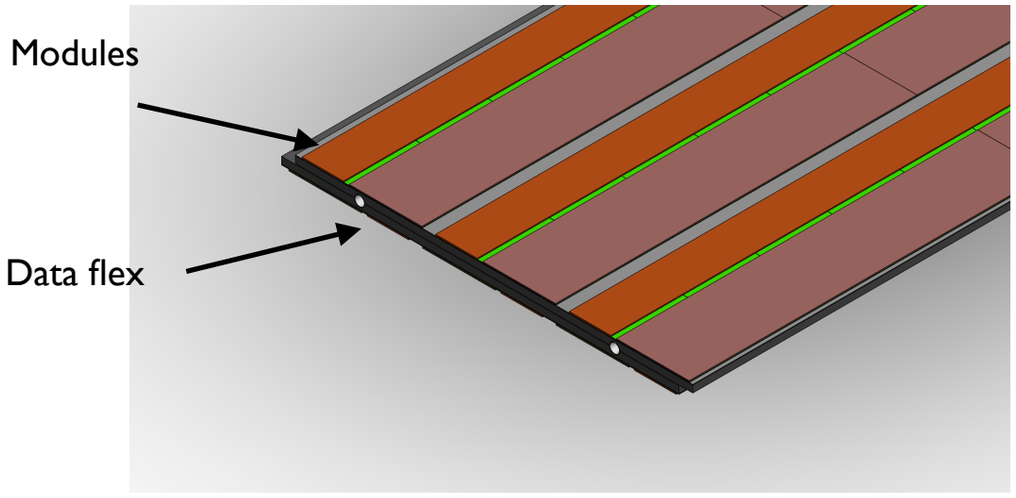


Flipped view



Double-sided Silicon modules mounted with the CF support structure



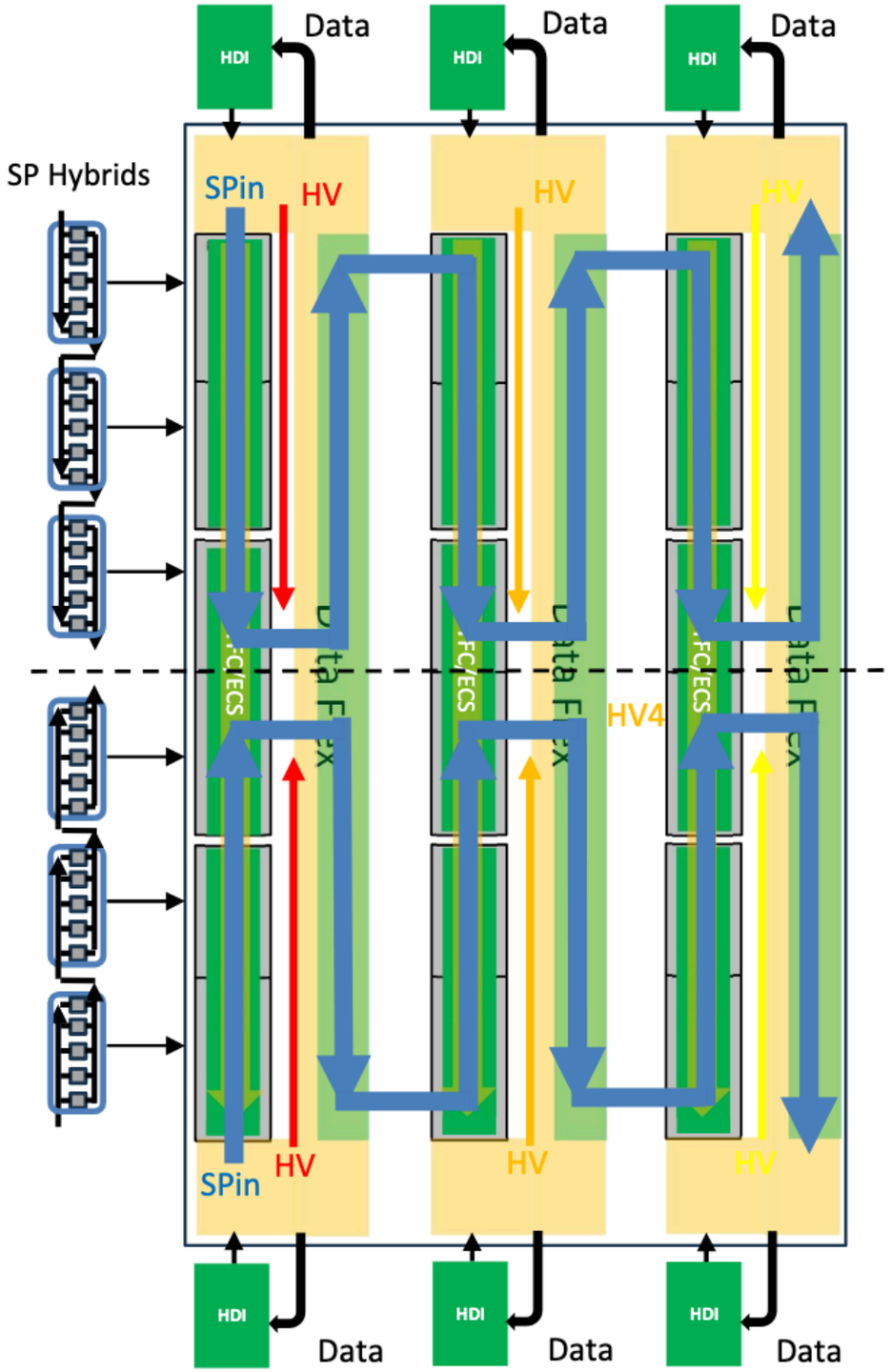


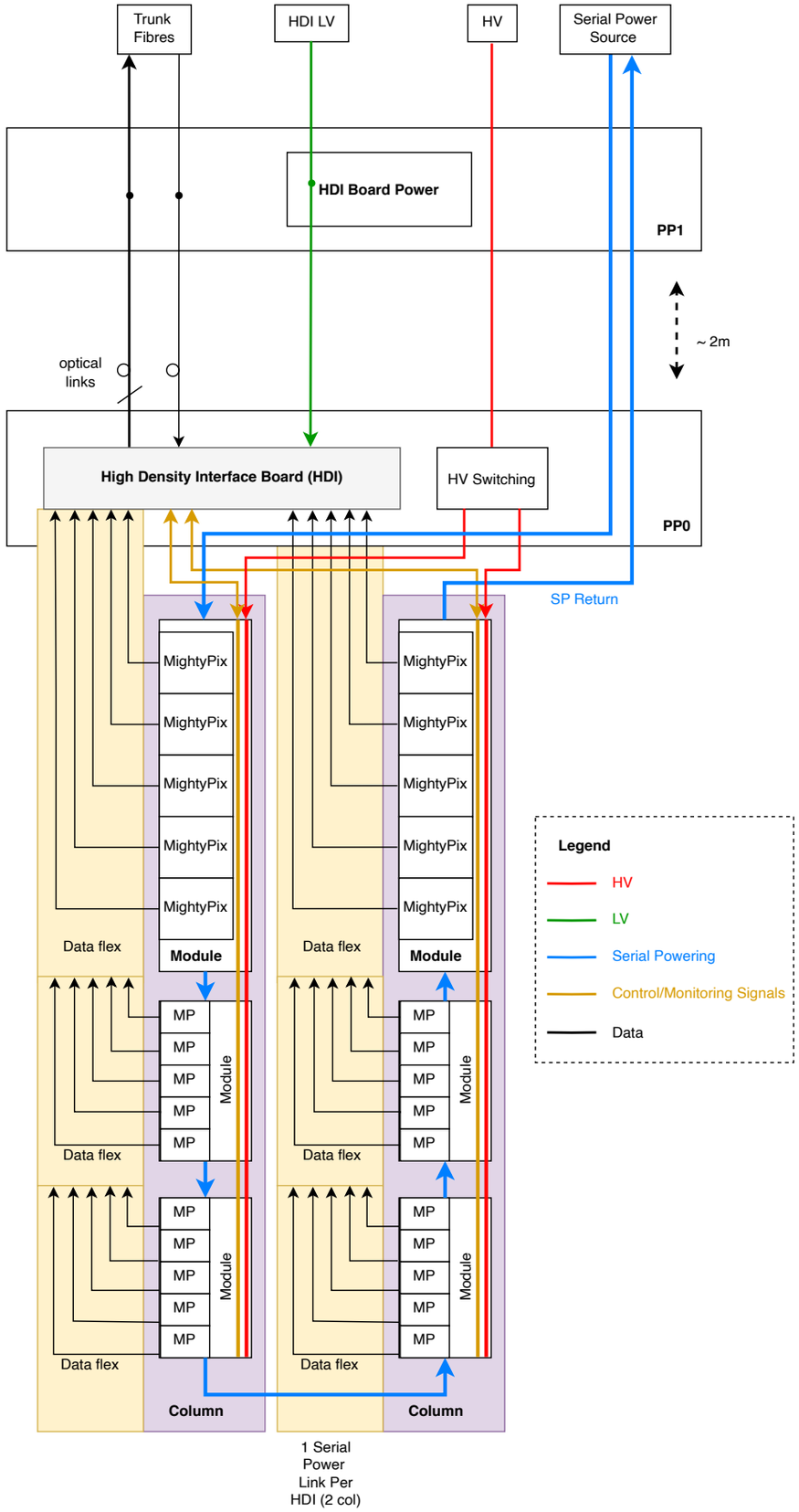
A full wirebond proposal: from sensor to end of stave card

Alex Bitadze (Manchester)

LHCb MT Serial Powering Scheme

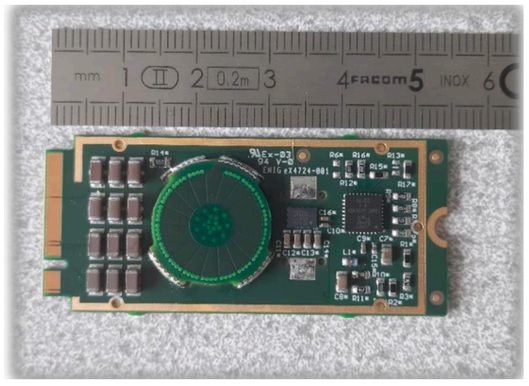
SP chain: up to 9 penta-modules → 45 sensors





Schematics: Ashley Greenall (Liverpool)

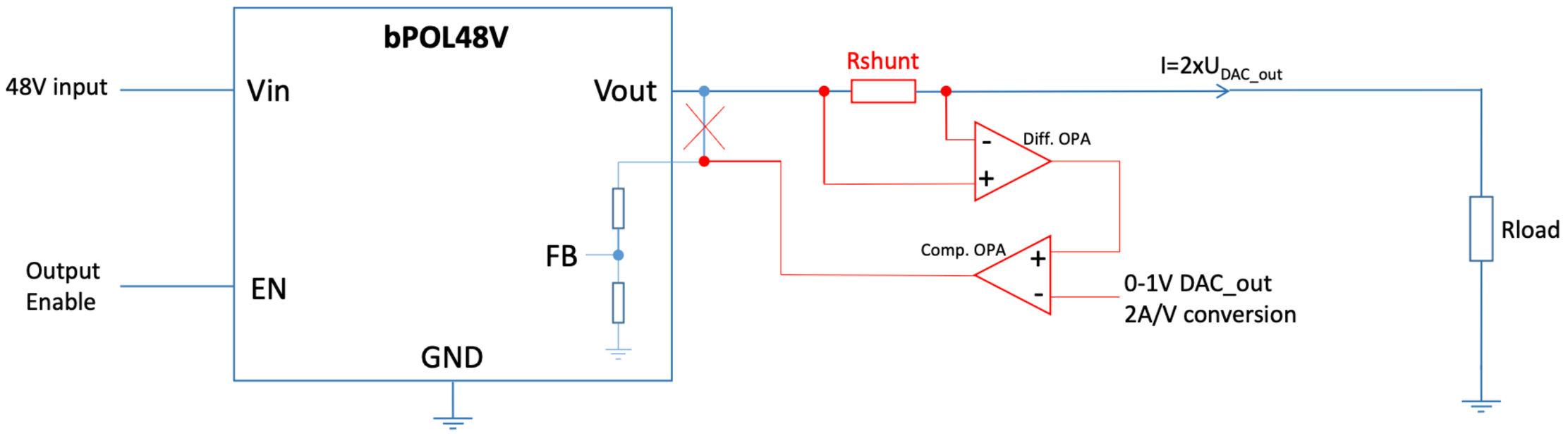
LHCb UP: Customised bPOL48 for SP



- CERN-designed rad-hard CMOS controller ASIC
- 17 to 48V input voltage range
- 0.6 to 24V output voltage range (hardware selectable)
- 10A max. output current

- bPOL48V => **Voltage regulator**
- We need **Constant current regulation** for serial powering

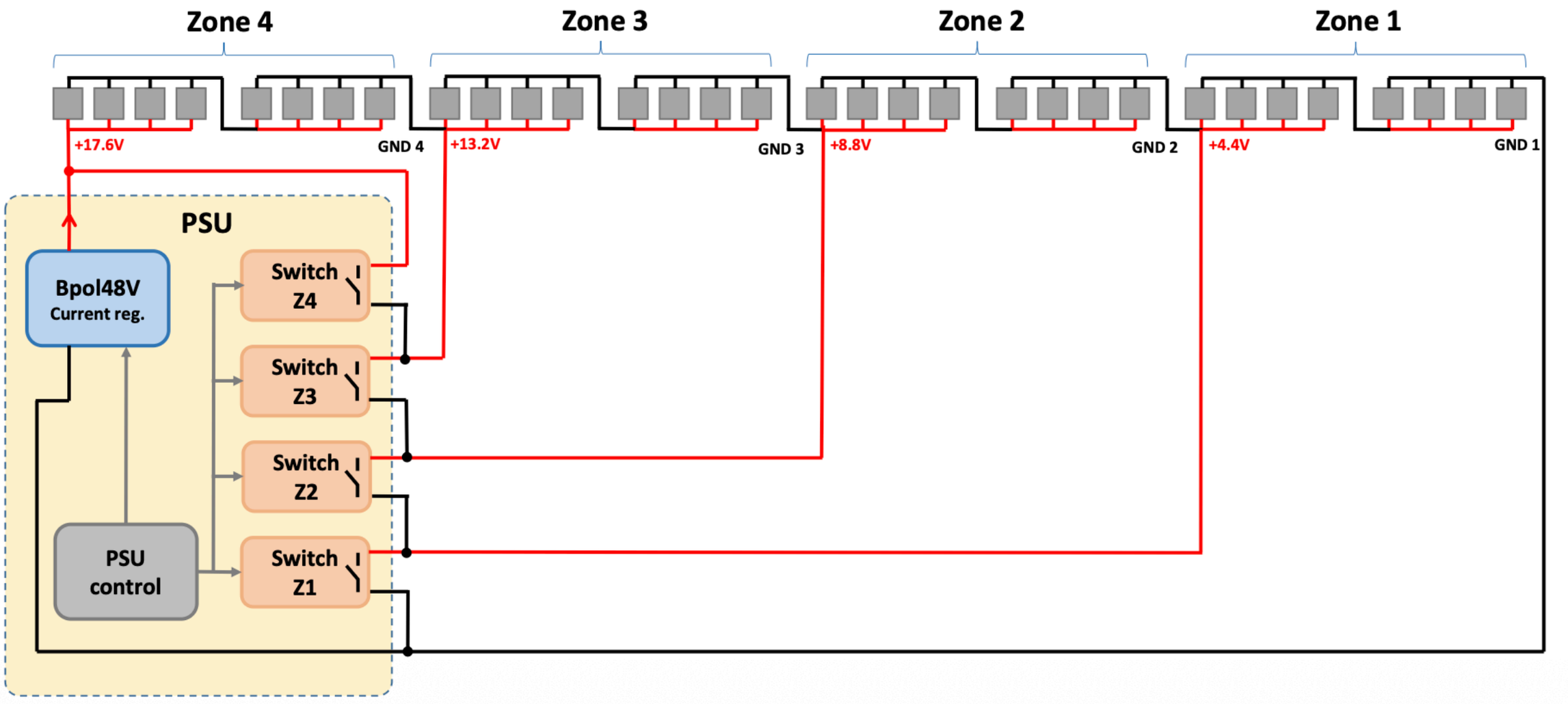
➢ **Customized bPOL48V => Current regulator (0-2A adjustable by lpGBT DAC out)**



Customized bPOL48V bloc diagram

LHCb UP: Customised bPOL48 for SP

- An alternative powering scheme: SP 4 zones (8 groups of 4 sensors in parallel)



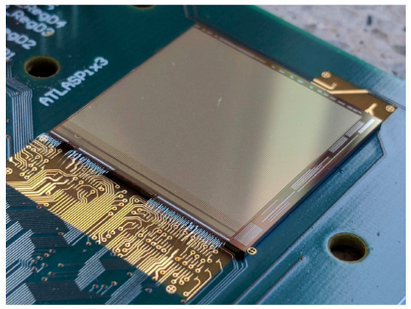
S. Martinez, C. Renard, P. Pichot, M. Guittiere (SUBATECH)

Current System level R&D

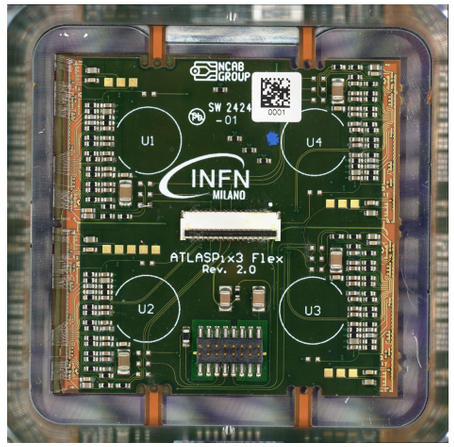
DRD3: HV-CMOS Pixel Demonstrator

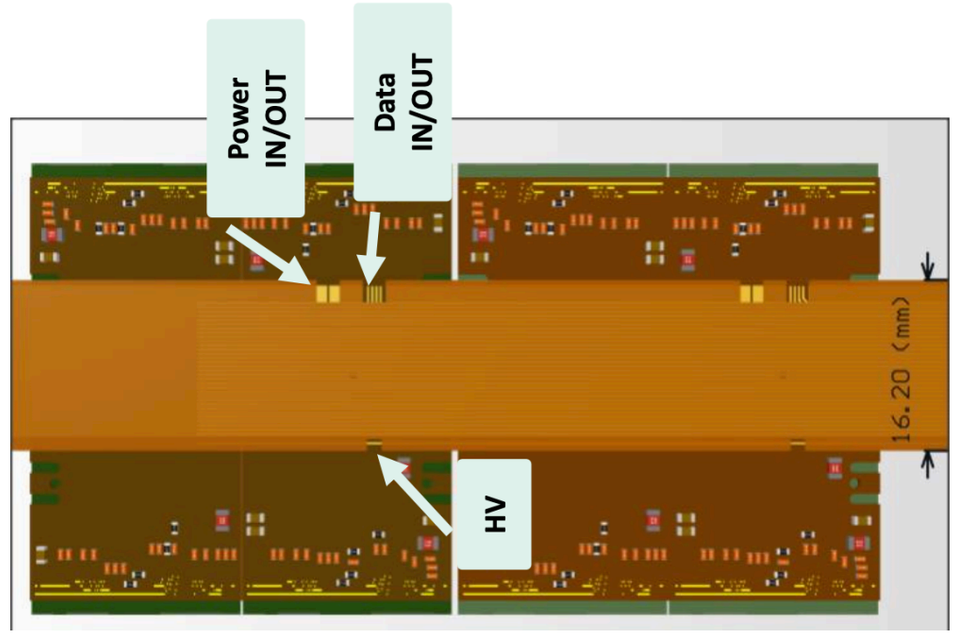
- System prototyping driven R&D activities based on HV-CMOS technology
  - Lots of synergy with the LHCb Upgrade II, exploring also knowledge from the ATLAS ITk construction

ATLAPix3



Quad-module



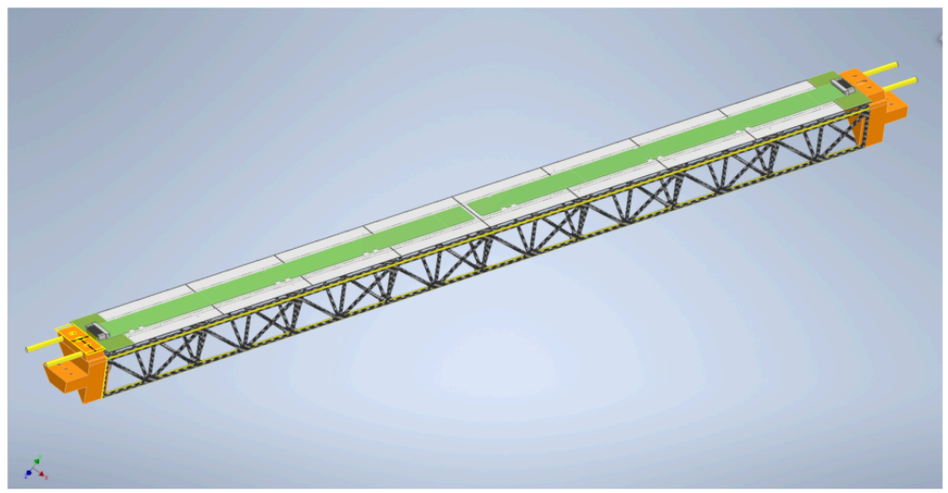


➡ SOON HV-Pix26

On-going R&D:
Al-flex (FBK)

Stave flex (data/power)
Al-flex (CERN) - produced

- Optimised **power and data signal routing** along the stave
- **Readout Unit Design**
  - **Multi-chip modules** (e.g., 2×2 quad modules)
  - **Serial Powering Architecture**:
    - Internal bias generation via **shunt-LDO regulators**
  - **Chip-to-chip data transfer** for local aggregation

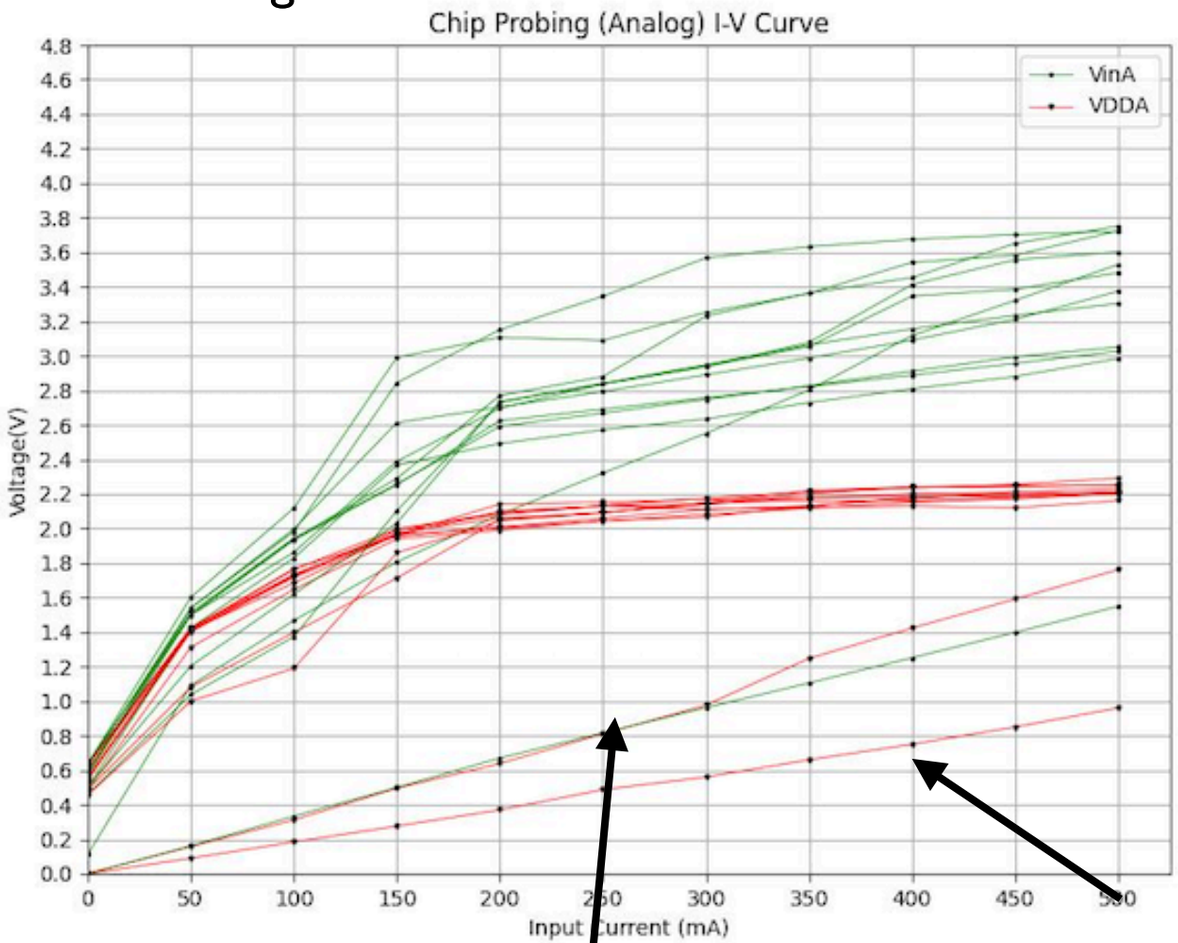


Long stave **(~1.3m)** mechanical structure (fabricated in Pisa)

ATLASPix3 SLDO Bare Chip IV Measurements

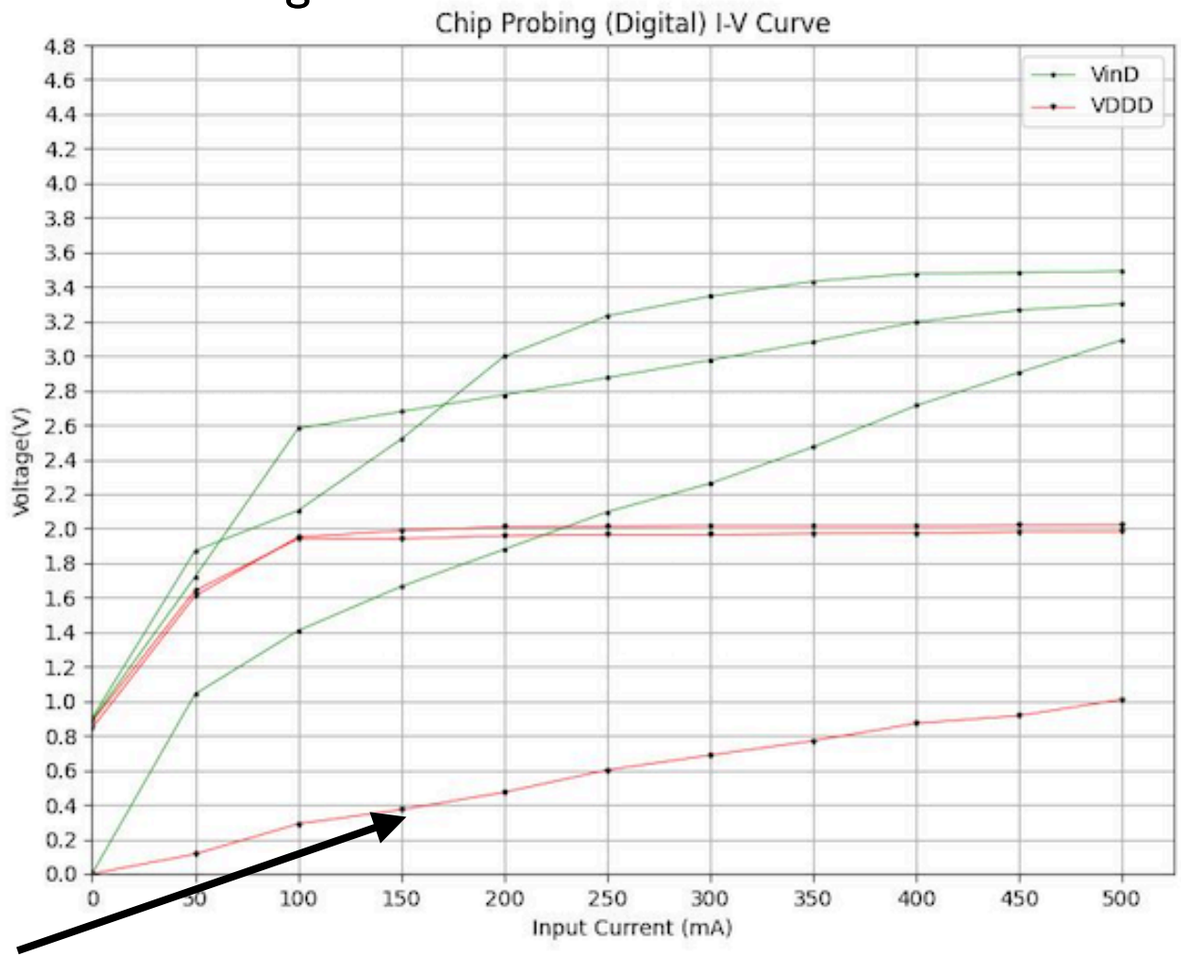
- We have manually probed around 70 chips, the analog and digital SLDO circuits using 8 contact pads
  - The "yield" based on SLDO performance is ~80% overall
  - In parallel, needle cards are being designed and tested as well in IHEP and Dortmund

Analog



Failed - chip 1
(Known handling issue)

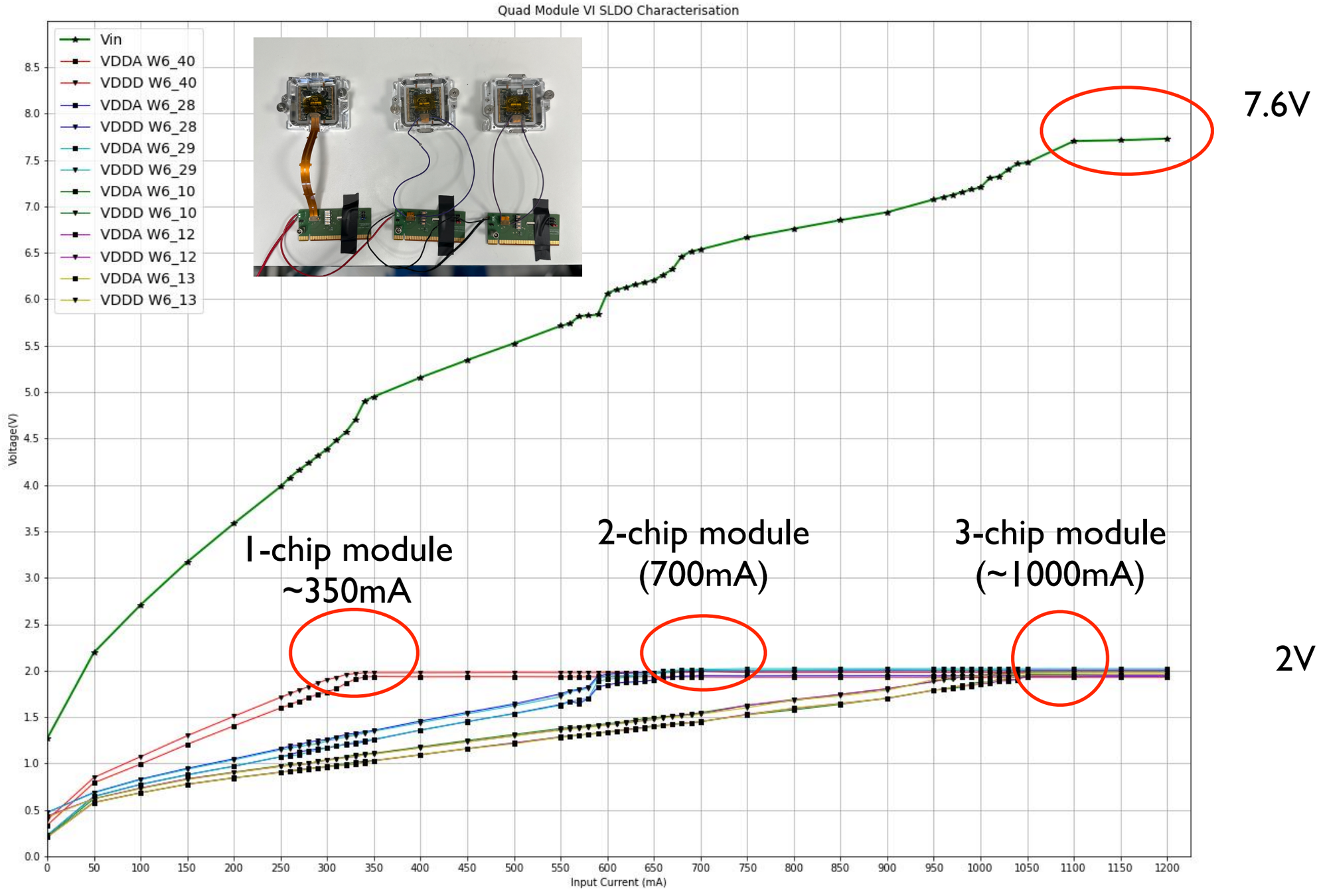
Digital



Failed - chip 5

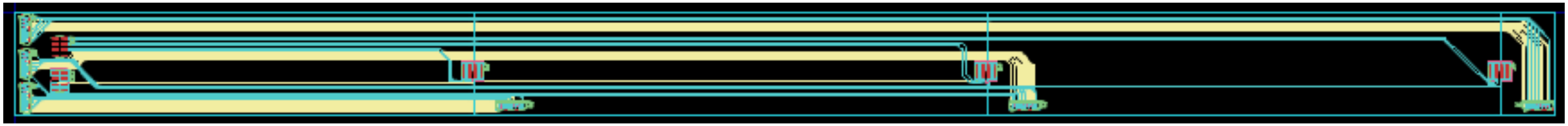
Three module (6 chips) SP Chain IV Measurements

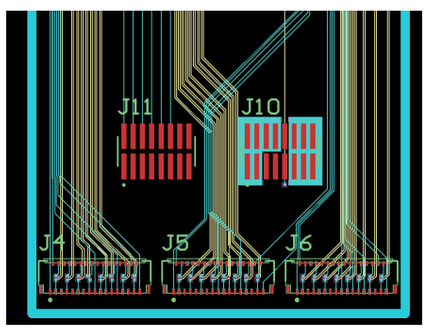
- Number of modules and chips constrains by the assembly procedures (very first trials)
  - Accidental: sequential regulation is seen due to the uneven number of chips in the modules
  - Additional electrical readout: Link to Fuat Ustuner's talk in the CEPC Workshop 2025



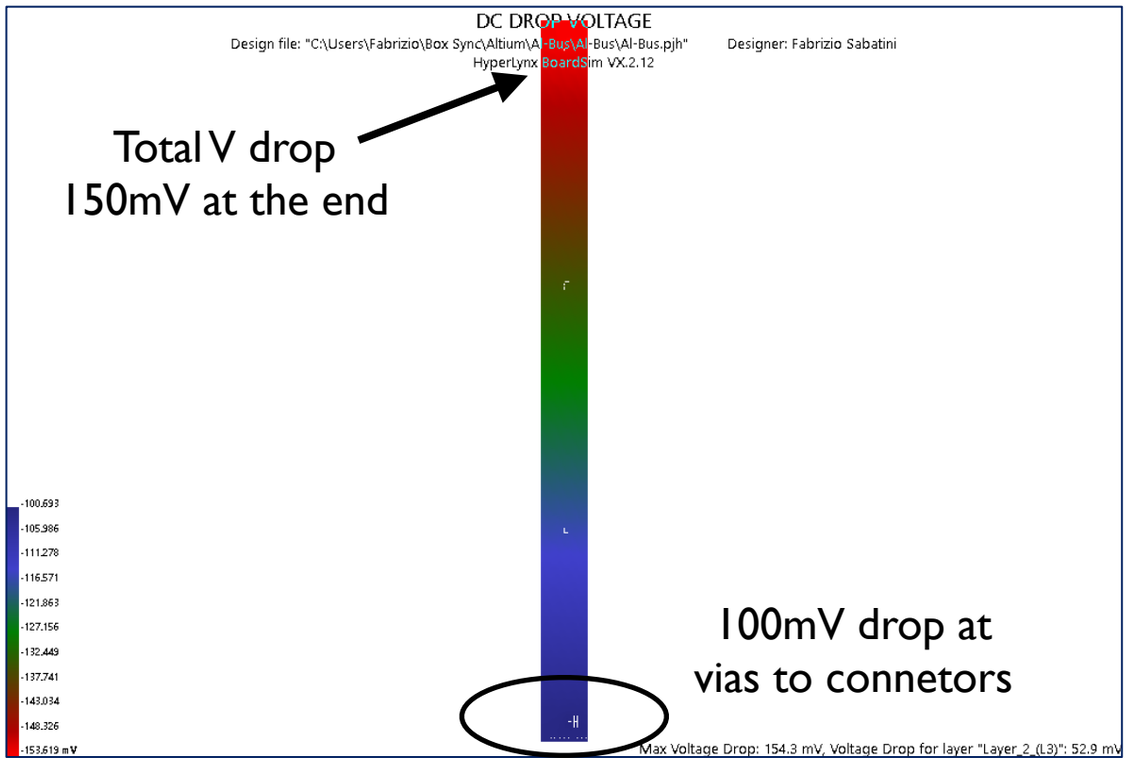
DRD3: Long Al Power/Data "Stave flex"

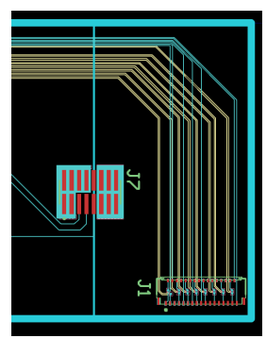
- Long PCB (60cm×4cm, 300um thick), "standard" features, with Al conductor X_0 (Al) ~ 6 X_0 (Cu)
  - 15 µm thick Al conductor layers (power lines in the central layers, data lines in top and bottom)
  - 100 µm wide lines (~200 µm gap for impedance matching, 150um pass through via
  - Designed by Milan and fabricated in the CERN Microfabrication Lab, 4/8 pieces finished the production in Oct 2026
- Preliminary plan: SP chain with 3 quad-modules, and populate the rest using dummy heaters
  - Then load to the CEPC half stave support structure fabricated in Pisa for system evaluation





EoS side



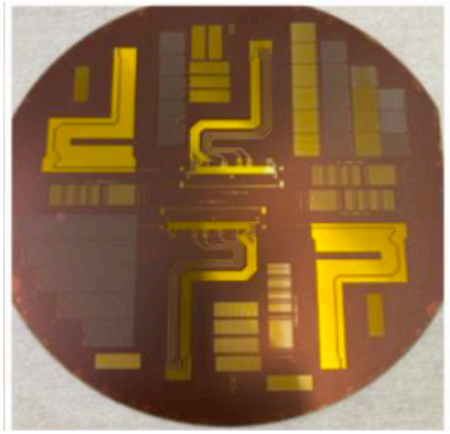


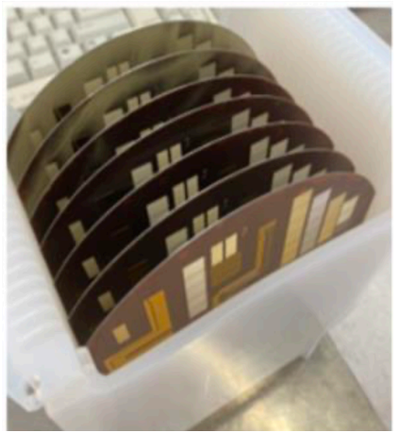
Last module

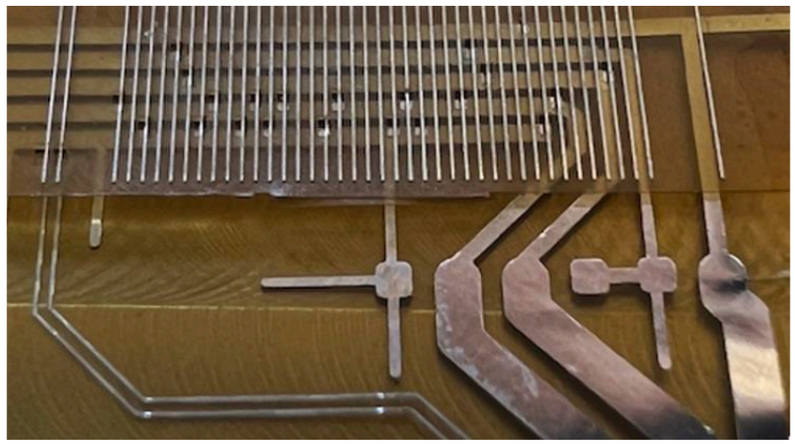
Fabrizio Sabatini (Milan)

FBK AI-flex Development

- High density low-mass flex using Polyimide/Al multilayers production at FBK
  - Interlayer and detector bondings with spTAB
  - Very low material budget, planar compact form factor
  - Link to David Novel's talk in the DRD3/7 workshop on innovative connection







Top view of stacked layers

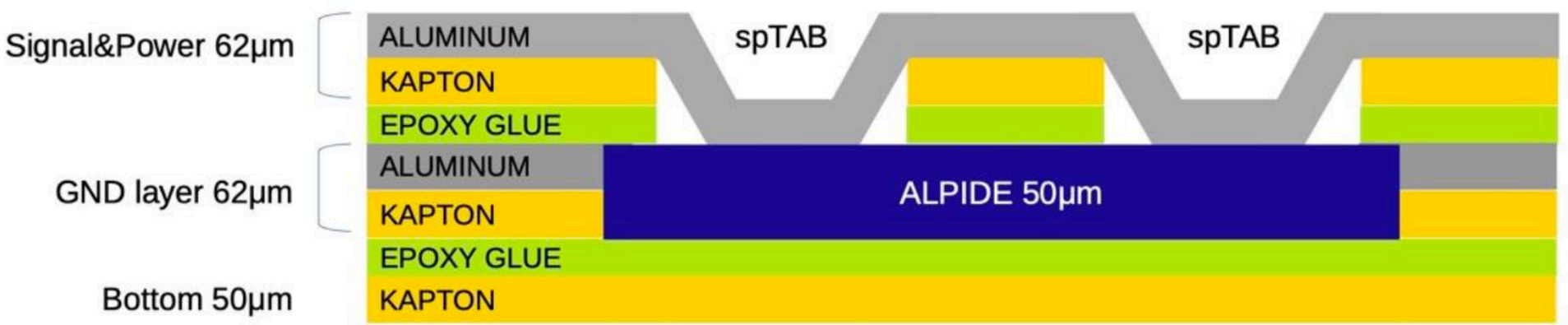


Bonds detail



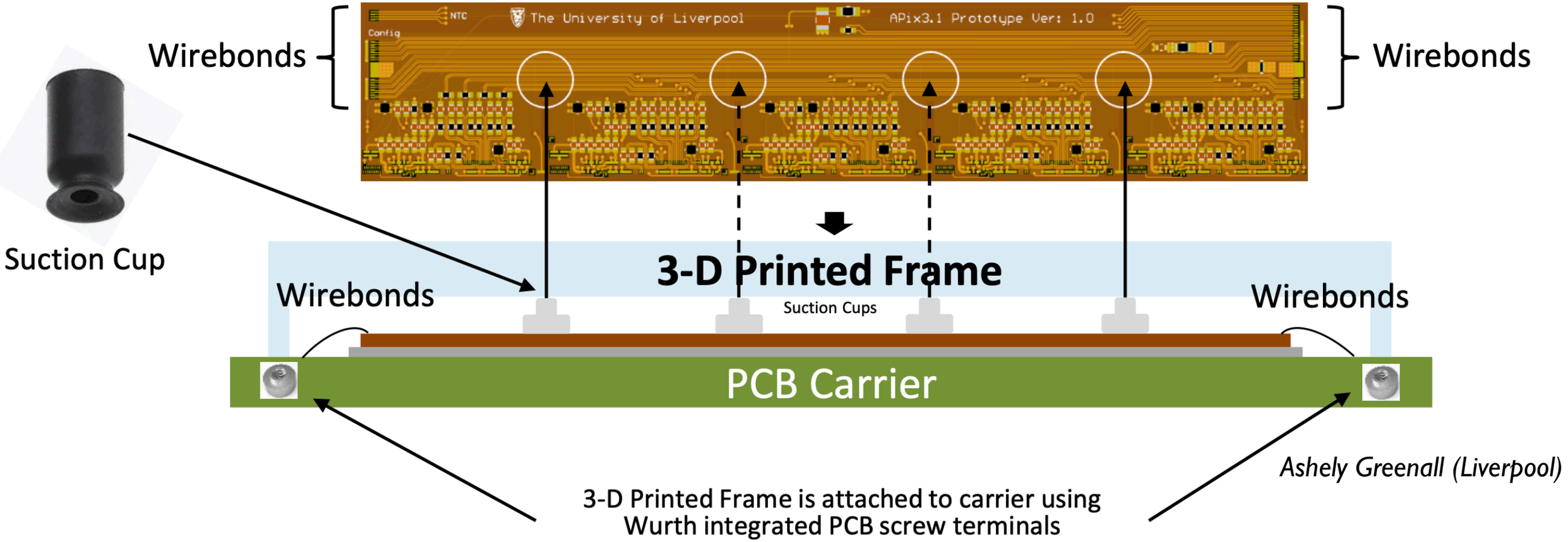
SEM image of spTABs

New concept:
Embed detector
to provide
mechanic support



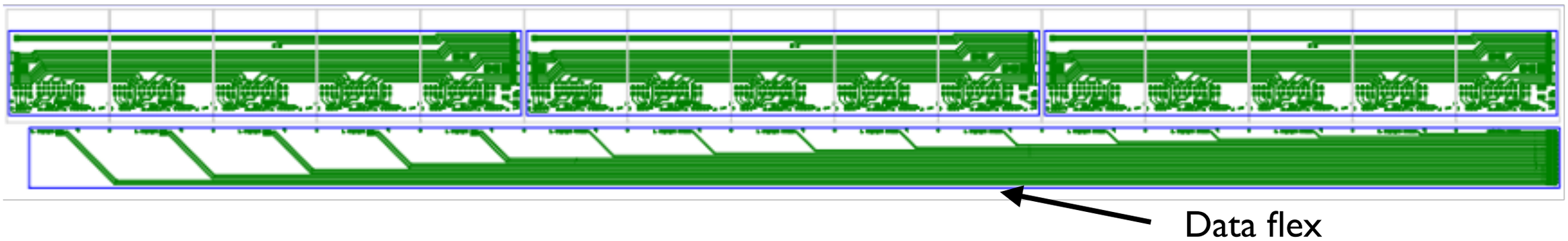
LHCb“penta-module” and 3 module SP ministave

- LHCb 5-chip flex based on the Quad-flex design from Milan, as a system R&D effort
  - Key difference is MT envision a “connector free” concept on stave
- An ITk-strip inspired carrier board is being designed at Liverpool for module testing
  - Modules are held down for wire bonding (flex->sensor) by vacuum or “suction cups”
  - Fully tested/verified modules are then permanently glued to the support structure

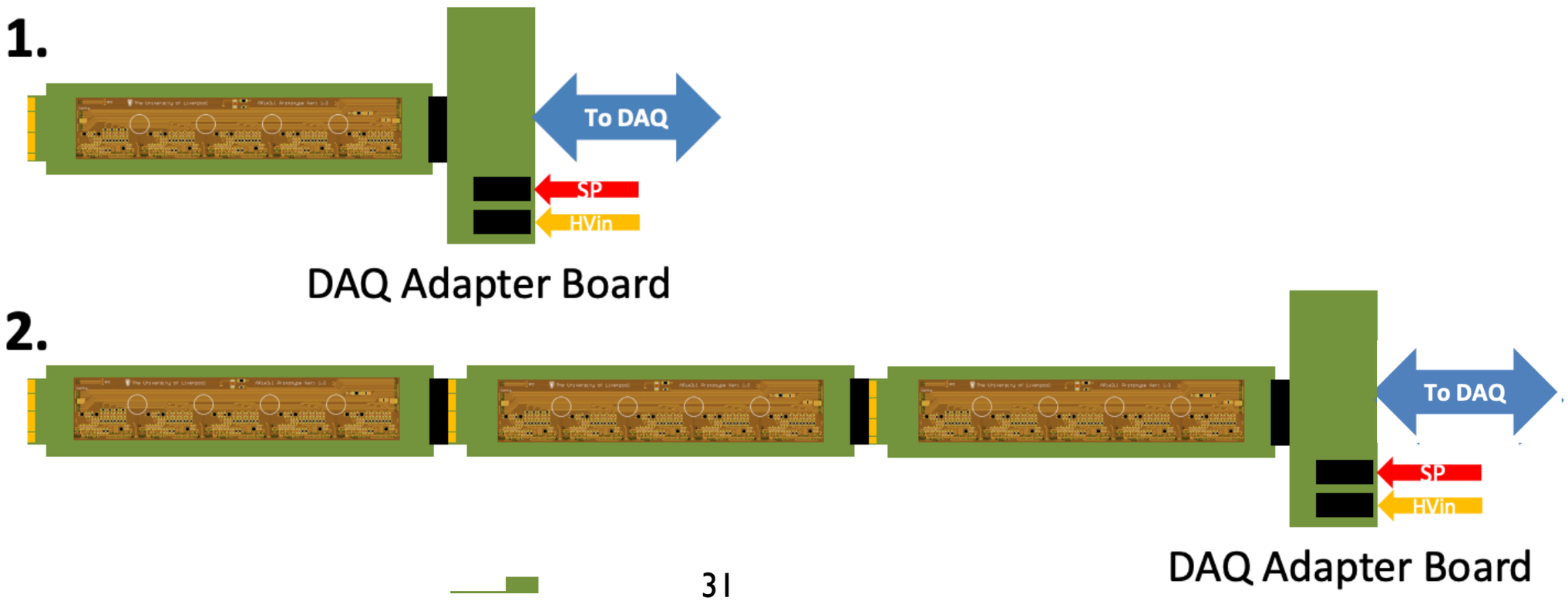


LHCb MT "mini-Stave"

- Redesign the power adaptor board to host up to 3 modules readout



- ATLASPix mini stave with three modules is a "proof of principle" prototype without data flex)
  - Data flex functionality is integrated in the carrier board with power/data lines commented module to module
    - Use high density SamTec Mini Edge Card Connector
  - A modified GECCO readout is designed to readout up to 3 modules in the chain



Summary

- HV-CMOS and Serial Powering in combination offered promising solutions for an efficient and low material tacking detectors, particularly suited for large area
  - Selected as baseline for the "near term" LHCb Upgrade II tracking detector (UP and MT)
- Serial Powering Integrated SLDO circuit in the chip have been successfully demonstrated by the RD53 in 65nm readout chips as part of the HL-LHC LS3 (2030) upgrades
- Several HV-CMOS sensors have since developed with integrated or standalone SLDO
  - MightPix2/RadPix series are expected to have devices back early 2027
- DRD3 and LHCb Upgrade II community have been working together in R&D
  - Detailed measurement plans for SLDO verifications
  - System level R&D with multi-chip modules and multi-module SP chain demonstrators
    - Assembly and readout, Al-flex development offer further reduction in material
- Not covered in this talk: a strong R&D program focusing on SP is also in the DRD7
  - Serial powering for next generation chips: SLDO implementation in the TSMC 28 nm technology node, See M. Karagounis @ DRD7 Annual Workshop