

Silicon Photomultipliers: FBK developments overview

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SiPMs for Calorimetry Applications
Outline

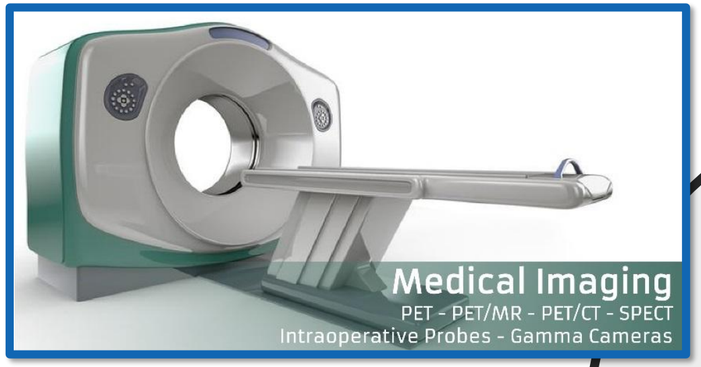
Introduction
- SiPM properties and typical applications

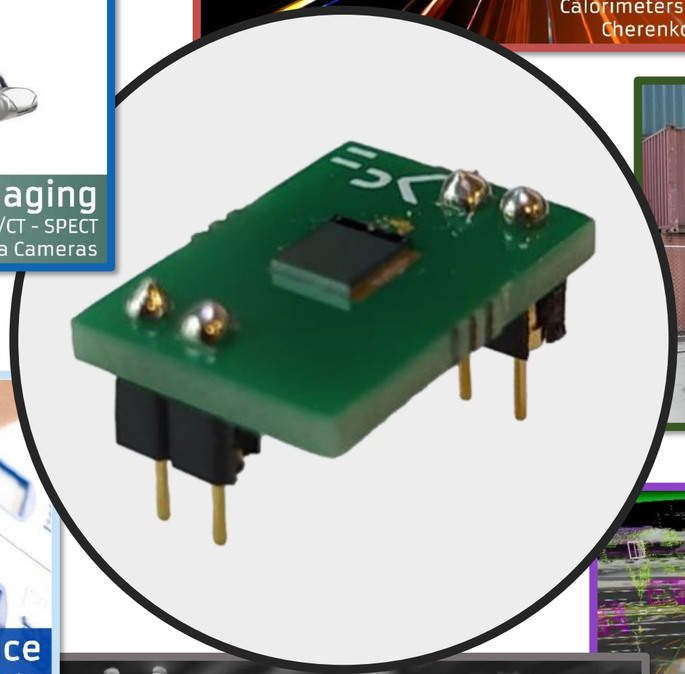
SiPMs Performance for Calorimeter Requirements
- Cross Talk and Photon Detection Efficiency (PDE): NUV-HD-MT and NUV-DJ
- Single Photon Time Resolution (SPTR)
- 2.5D and 3D Integration with Through Silicon Vias Technologies
- Single-SPAD TSV and microSiPM
- NUV-BSI SiPMs

Conclusions

Introduction
SiPM Applications















CRS CUSTOM RADIATION SENSORS

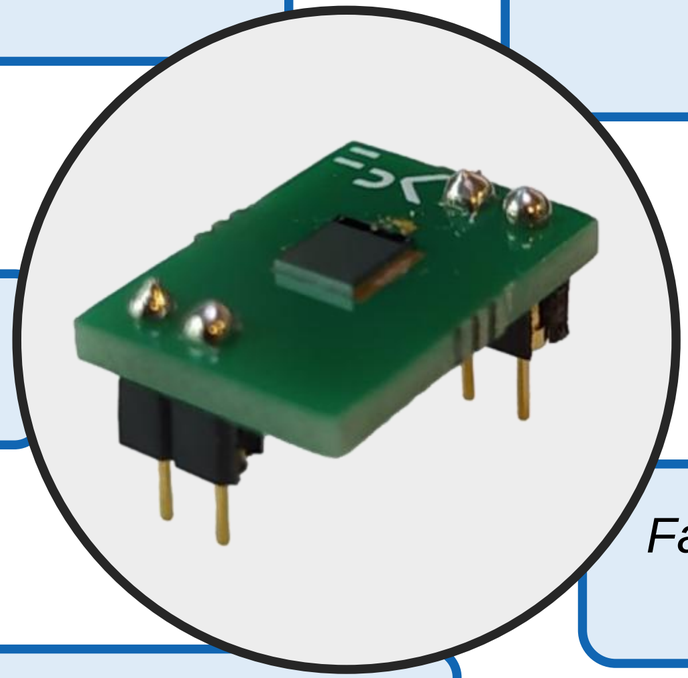
SiPM Technologies for Calorimetry Applications

SiPMs Performance for Calorimeter Requirements

Introduction
SiPM properties for Calorimetry Applications

Extended sensitivity (UV-range to IR)

Large active area.

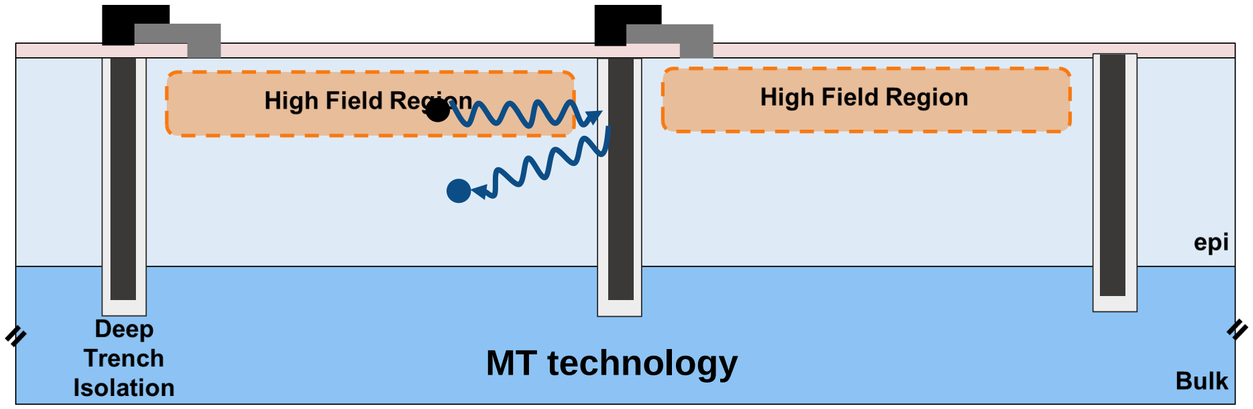


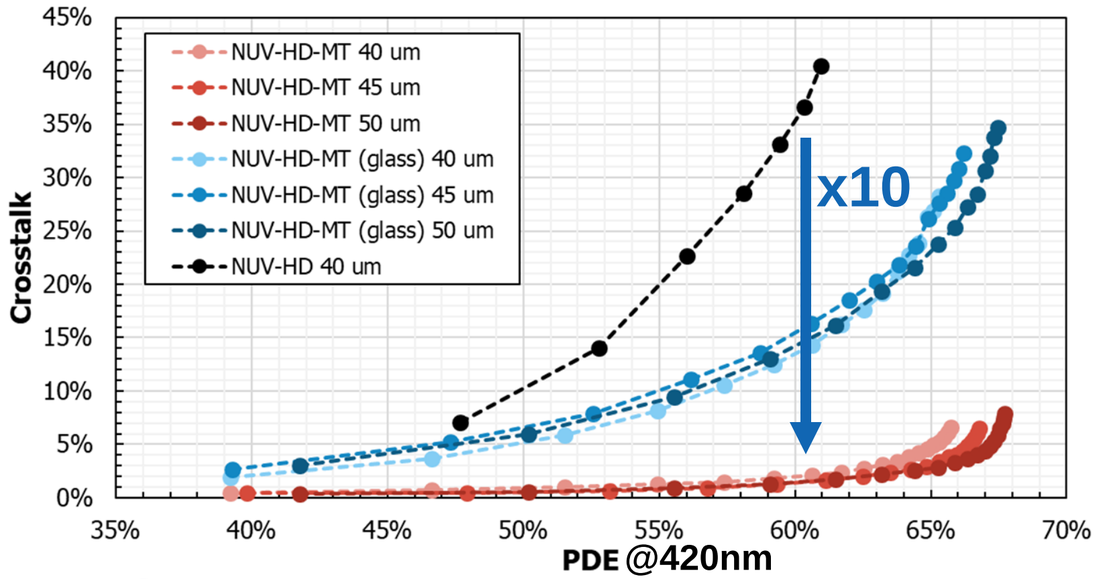
Fast response time.

Fast recovery time and small cell size.

Low inter-pixel CrossTalk

SiPMs Performance for Calorimeter Requirements
FBK NUV-HD SiPMs with metal-filled trenches (MT)





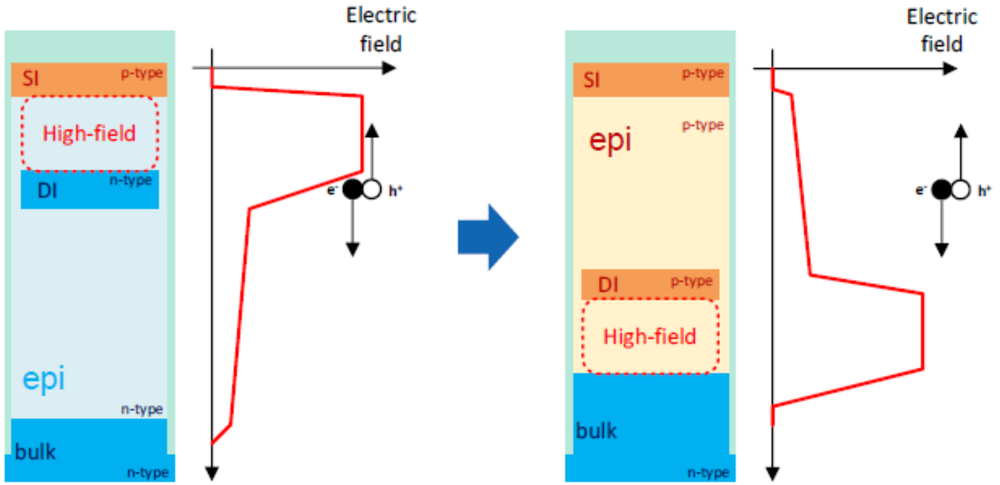
Collaboration with Broadcom

- Metal-filled trenches to **optically isolate adjacent microcells**
  - Significant **reduction** of the **internal crosstalk probability**
  - Significant increase of the maximum operating bias voltage
  - Saturation of avalanche triggering probability (in the NUV)
  - **PDE~65% @420 nm**

Low inter-pixel CrossTalk

SiPMs Performance for Calorimeter Requirements
FBK NUV-HD-MT and NUV-DJ SiPMs

- By *moving the high-field region towards the bottom of the epitaxial layer*, the PDE is enhanced.
- *Avalanche* is mostly *triggered by electrons.*



Conceptual drawing of the different NUV.MT and NUV-DJ microcell structures (cross-sections, not to scale)

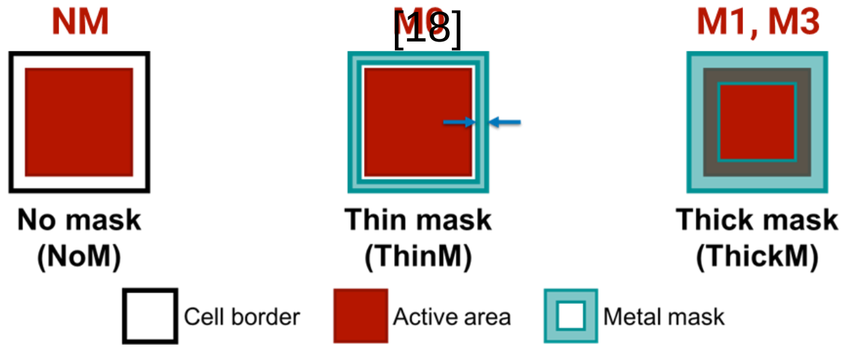
[1] *Sensors*2019, *19*(2), 308; https://doi.org/10.3390/s19020308
[2] https://docs.broadcom.com/doc/AFBR-S4N22P014M-NUV-MT-SiPM-Data-Sheet

Extended sensitivity (UV-range to IR)

CUSTOM RADIATION SENSORS

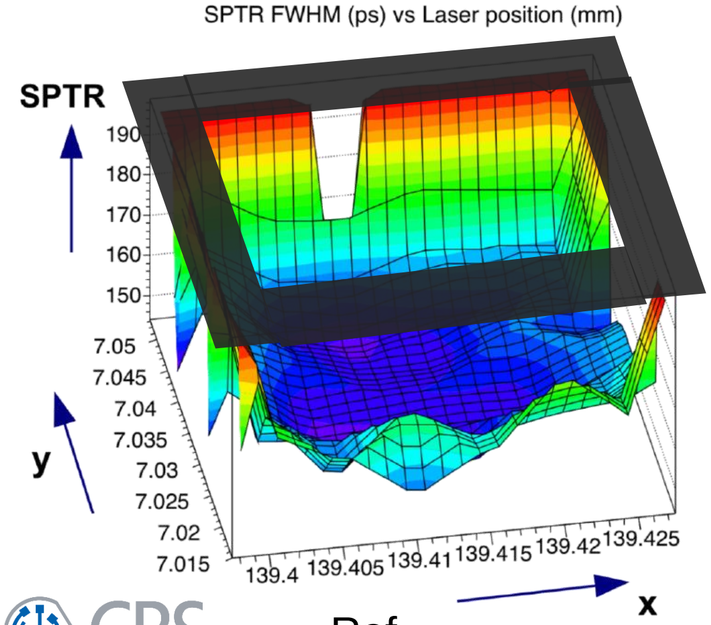
Single Photon Time Resolution
Metal Mask Layouts

Fast response time.

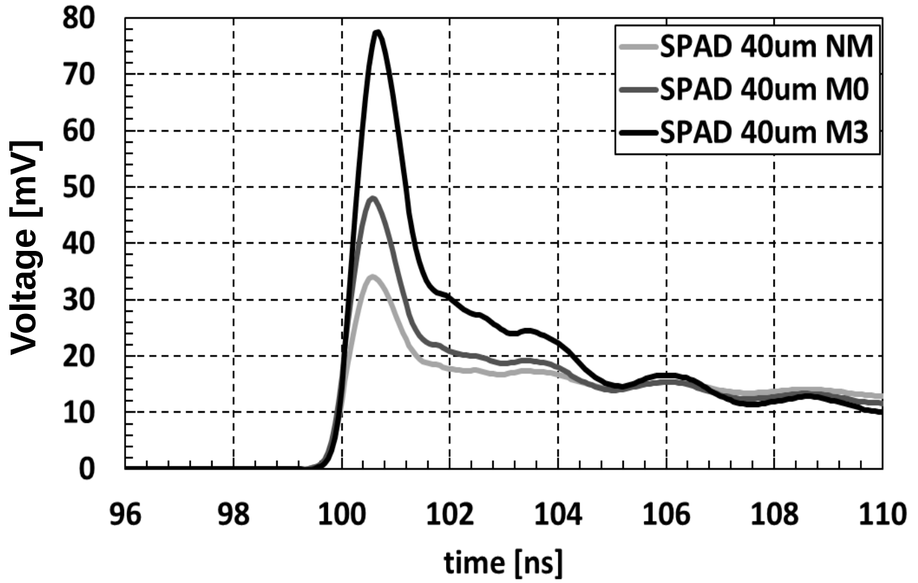


Ref. [18]

1. Remove the **outer areas** of the SPAD which show **worse SPTR**
2. A **higher capacitive coupling** between anode and readout: increase the fast peak of the single cell response
3. Better **signal extraction / integrity**: metal grid layout affects the TTS [17]



Ref. [19]



[17] F. Acerbi, A. Gola, A. Ferri, N. Zorzi, G. Paternoster, and C. Piemonte, “Analysis of transit time spread on fbk silicon photomultipliers,” Journal of Instrumentation, vol. 10, no. 07, p. P07014, 2015.

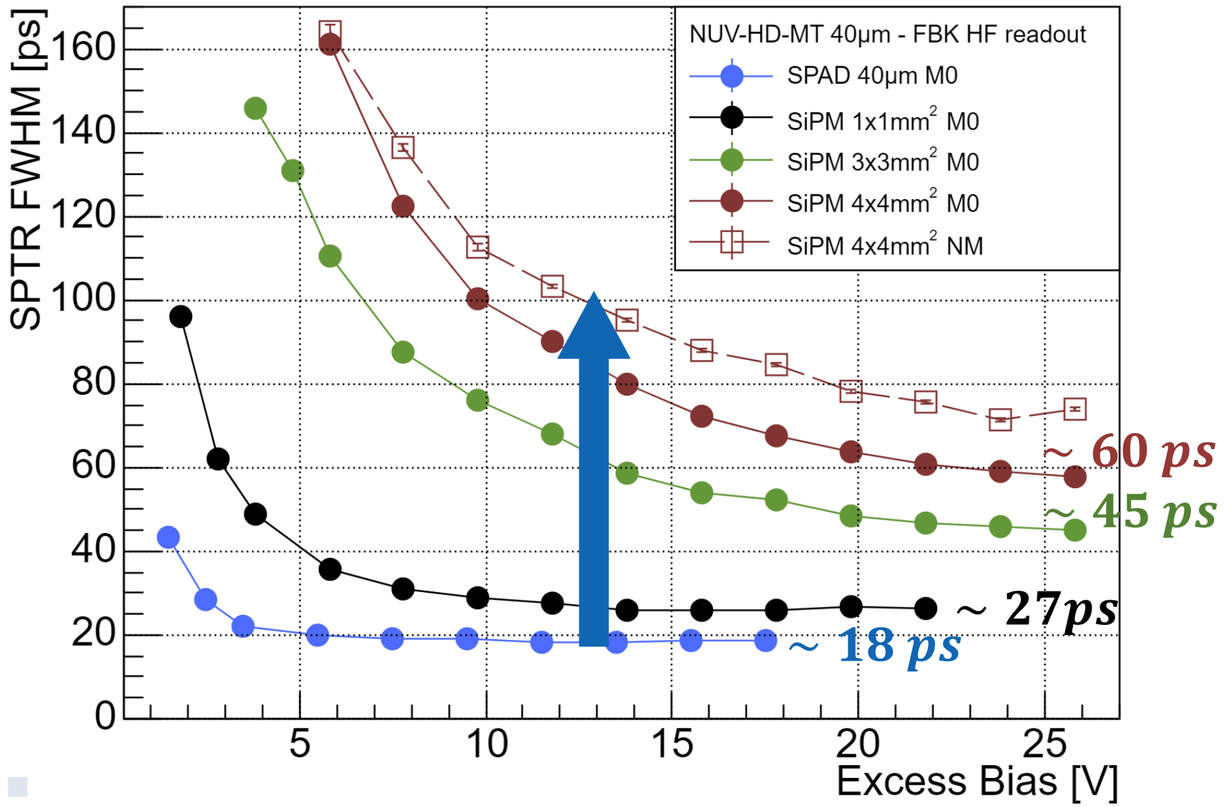
[18] S. Gundacker, G. Borghi, S. Cherry, A. Gola, D. Lee, S. Merzi, V. Schulz, and S. I. Kwon, “On timing-optimized sipms for cherenkov detection to boost low cost time-of-flight pet,” Physics in medicine and biology, vol. 68, 08 2023.

[19] M. Nemallapudi, S. Gundacker, and E. Auffray, “Single photon time resolution of state of the art sipms,” Journal of Instrumentation, vol. 11, pp. P10016–P10016, 10 2016.

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SPTR Results
Effect of SiPM area on SPTR

Fast response time.

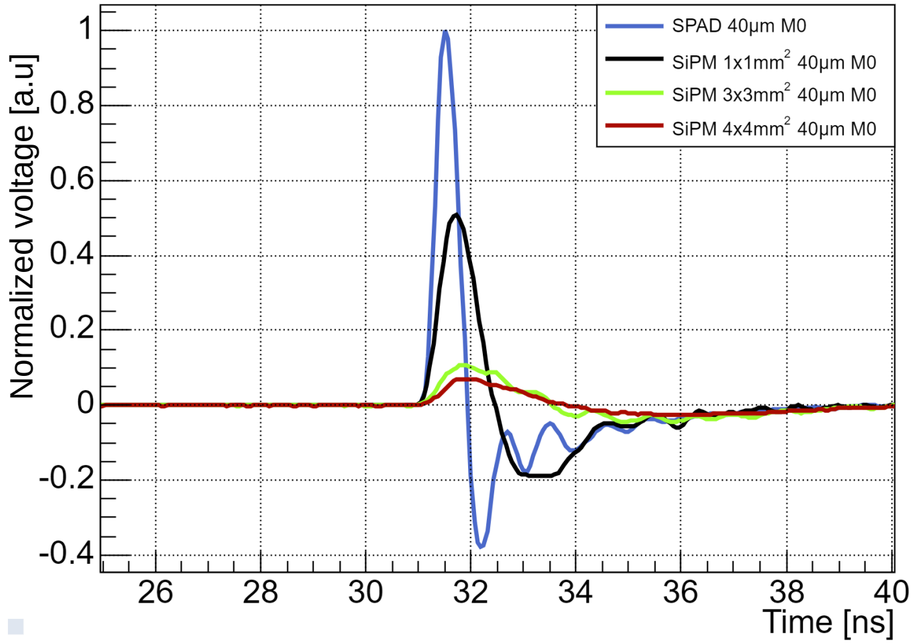


SPTR vs. excess bias for NUV-HD-MT 1x1 mm² SiPMs and SPADs, featuring a *layout optimized for timing and using a high-frequency amplifier*.

SPTR get worse for bigger SiPMs.

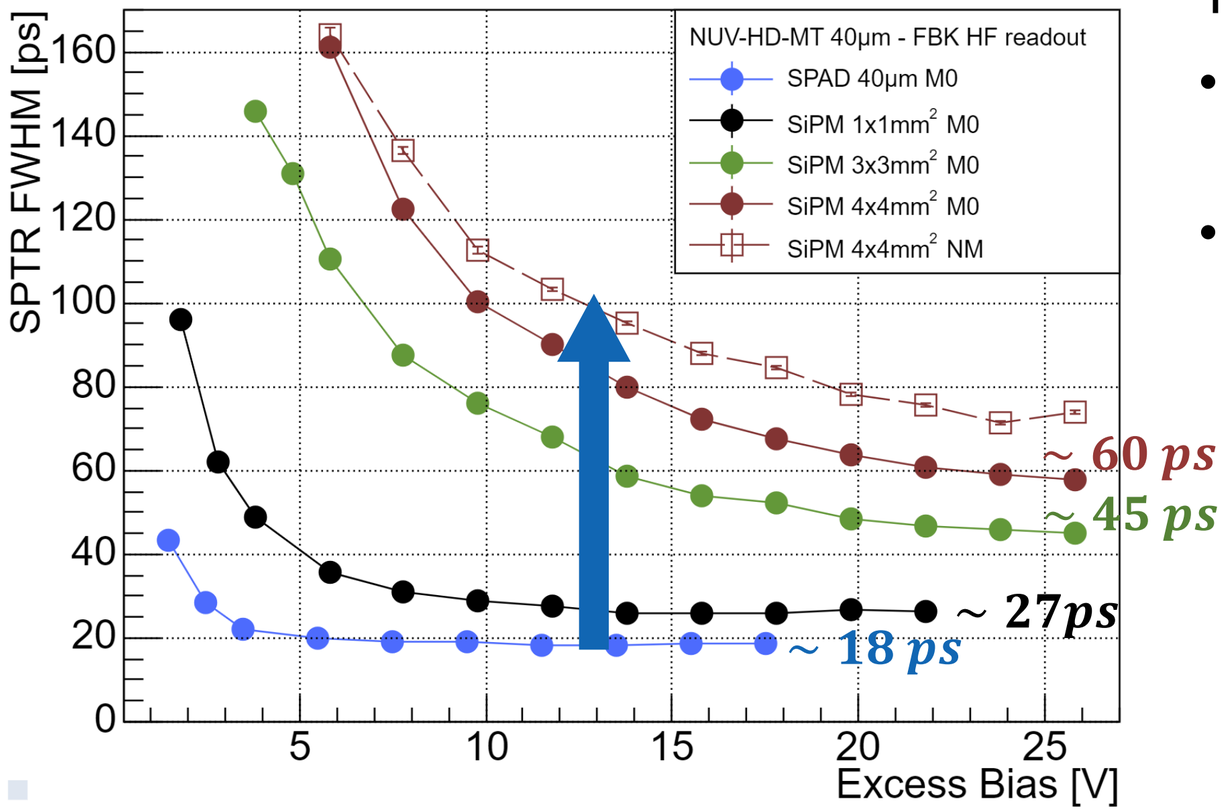
Working hypotheses:

- **Transit Time Spread**
- **Self-filtering effect**



SPTR Results
Effect of SiPM area on SPTR: segmented area

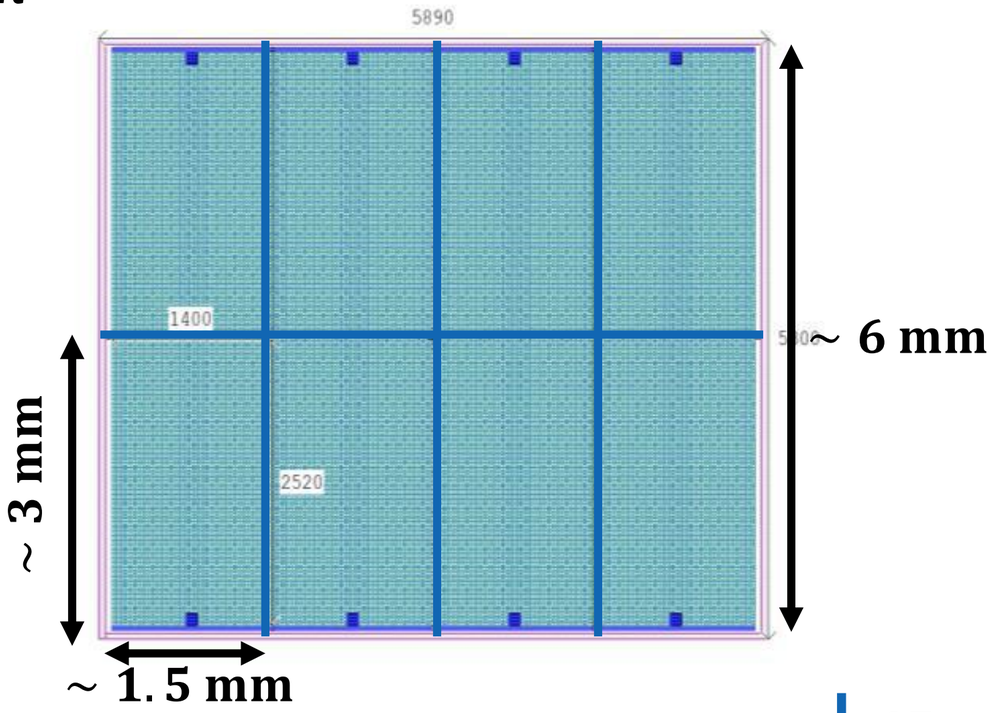
Fast response time.



SPTR vs. excess bias for NUV-HD-MT 1x1 mm² SiPMs and SPADs, featuring a *layout optimized for timing and using a high-frequency amplifier*.

The SPTR can be preserved by:

- *Segmenting the active area into smaller pixels, or miniSiPMs*
- *with separate 2.5D / 3D connection to readout*



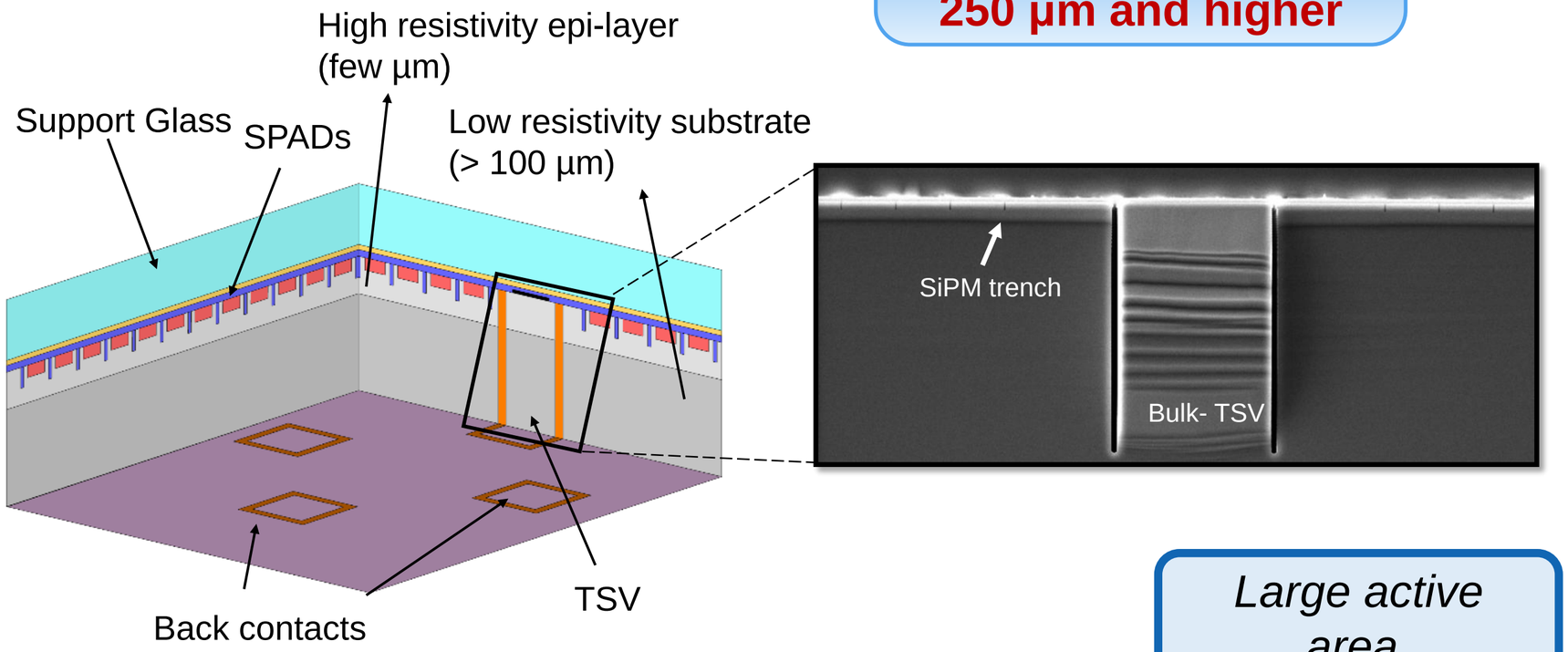
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Medium pitch interconnection
Glass-less, bulk TSV, via-last

In the bulk TSV process, the TSV is formed *after the fabrication of the SiPM, without modifying its process flow*. In the via, the *conductor is the highly-doped silicon bulk*.

- *No metal in the TSV*, by exploiting the low resistivity of the silicon substrate (allowing glass-free solution).
- Single via resistance upper limit is ~10 Ω.
- 10-100 TSVs/mm^2 (depending on the thickness of the final wafer).

Interconnection **pitch: 250 µm and higher**

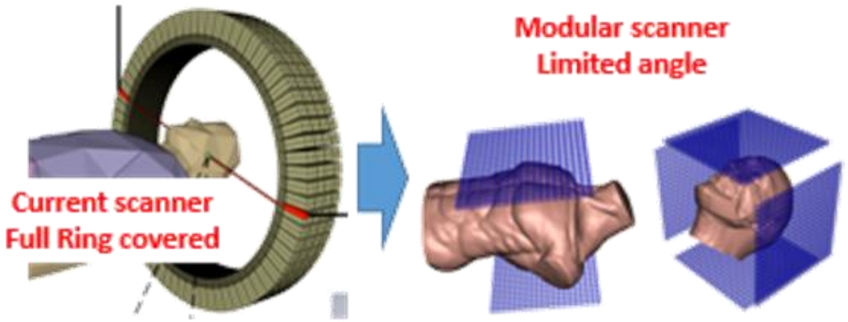


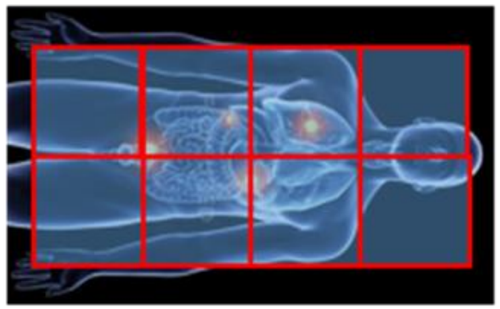
Large active area.

2.5D and 3D Integration
2.5D integrated SiPM tile for timing

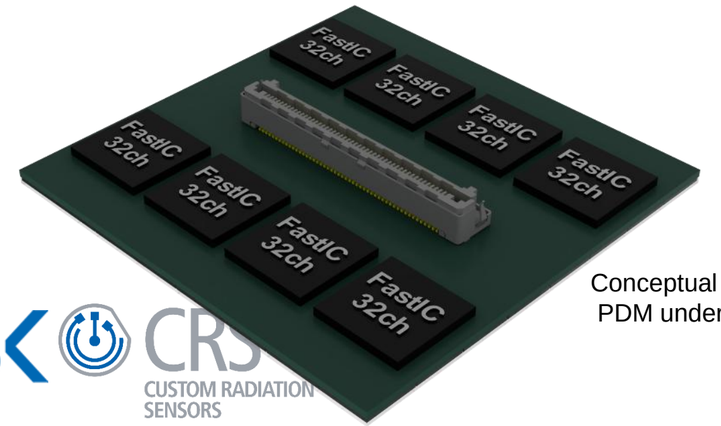
The 2.5D integrated PDM (50x50 mm^2) will be the basis of a *30x30 cm^2 ToF-PET panel*, which will be used to build limited-angle ToF-PET systems, for brain PET, Cardiac PET and full-body scanners.

We *expect very good timing performance*, supported by preliminary measurements achieved with NUV-HD SiPMs coupled to FastIC ASIC.

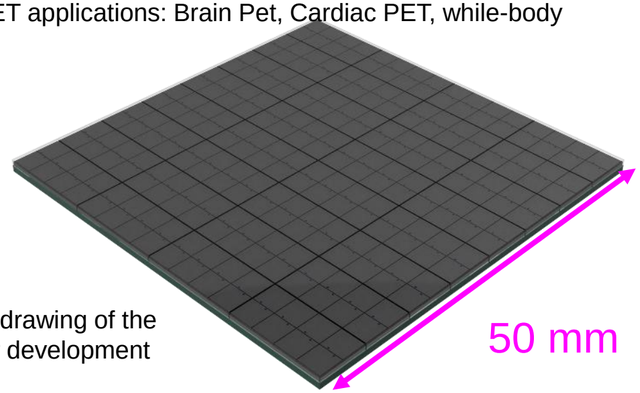


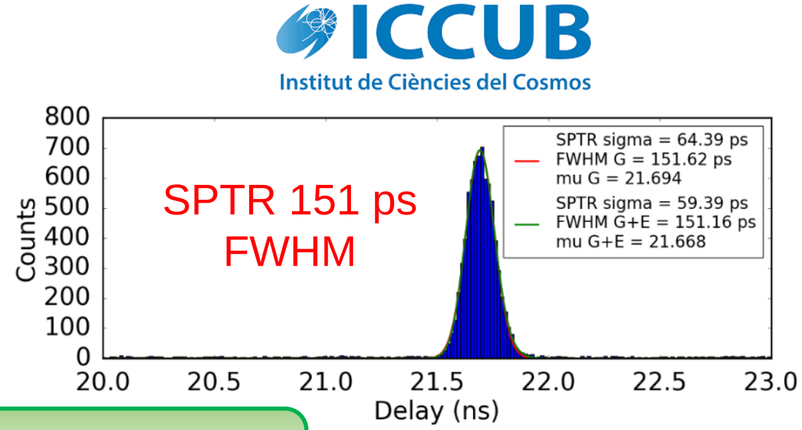


Application of the PDM to build large panes used in new, limted-angle PET applications: Brain Pet, Cardiac PET, while-body PET

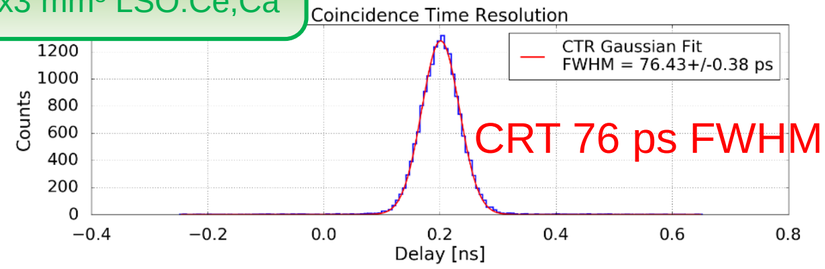


Conceptual drawing of the PDM under development





2x2x3 mm^3 LSO:Ce,Ca



SPTR and CRT measured at FBK NUV-HD-SiPMs read by the FastIC ASIC developed by ICCUB.
Sensor: NUV-HD-LFv2 SiPMs, 3x3 mm^2
Scintillator: 2x2x3 mm^3 LSO:Ce,Ca
Power consumption: 3 mW / channel

Large active area.

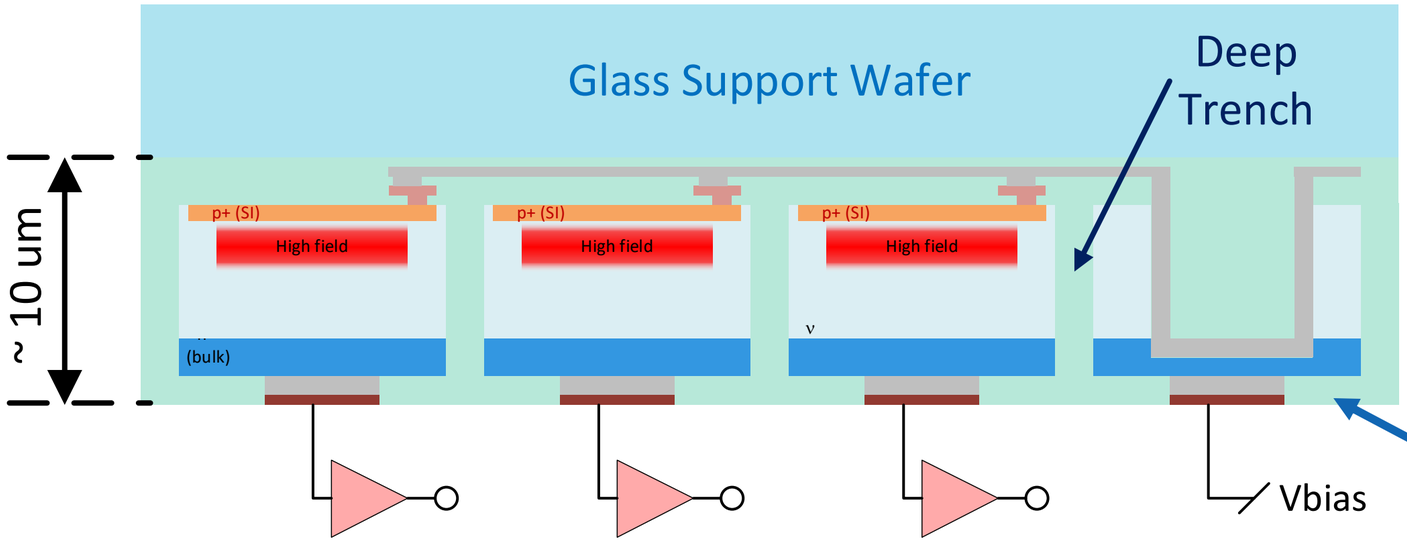
Single-SPAD TSV
Cross-section

Exploiting the Deep Trench Isolation, which is anyway present between adjacent SPADs in most SiPMs, we can achieve single SPAD isolation if we thin the wafer down sufficiently (use of a glass support wafer is needed).

We can exploit this isolation to *build a "bulk" TSV just below and coincident with each single SPAD*.

The *resistors* are still on the front-side (no change in signal shape is expected).

Common connection for bias is on the front and requires a TSV to bring it from the bottom.



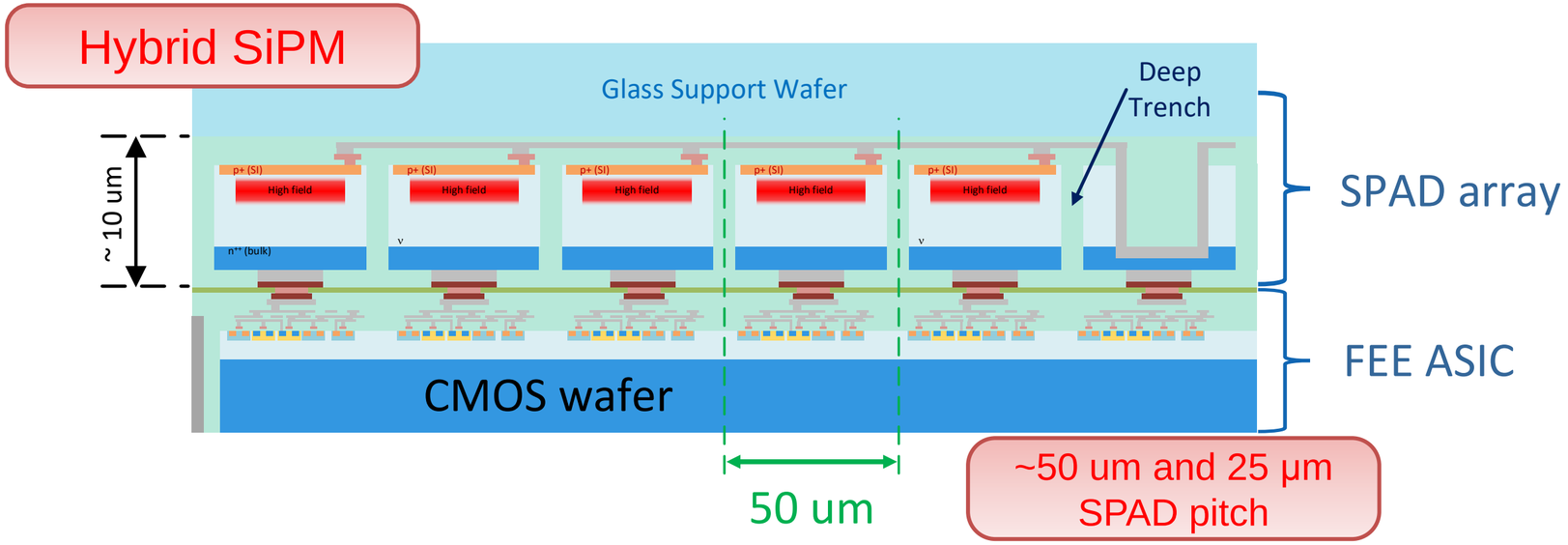
Experimental: lower TRL

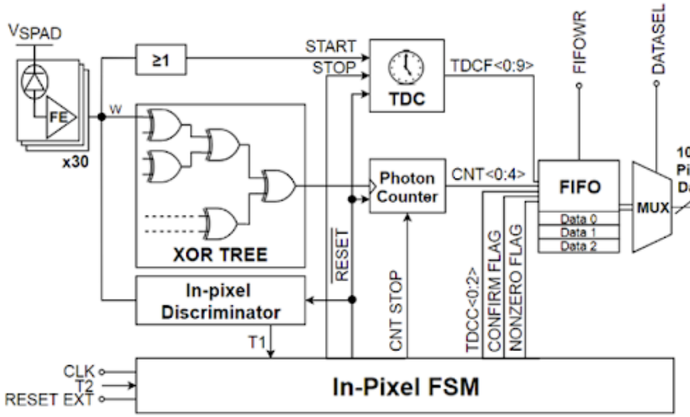
Optional metal redistribution layer (might as well be in the ASIC)

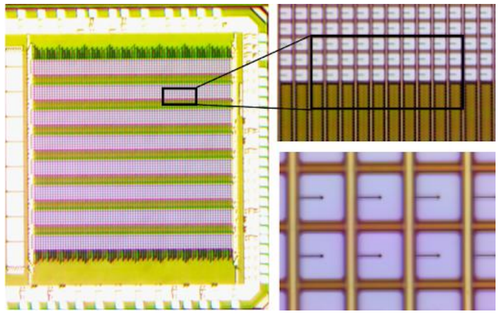
A. Gola et al., "FBK roadmap towards the next-generation of 3D-integrated SiPM and SPAD technologies", PD 2024, Vancouver

3D Integration
Full 3D integration with micro TSVs: Hybrid SiPM

FBK will also employ the single-SPAD TSV to achieve *single cell connection*. While complexity of the system increases, it might provide *ultimate timing performance*.







Example of dSiPM architecture developed at FBK (SBAM project)

- FBK can apply all the *know-how on system architecture* already developed in the filed of digital SiPMs.
- Finally solve the duality between analog and digital SiPM: *Hybrid SiPM concept*.

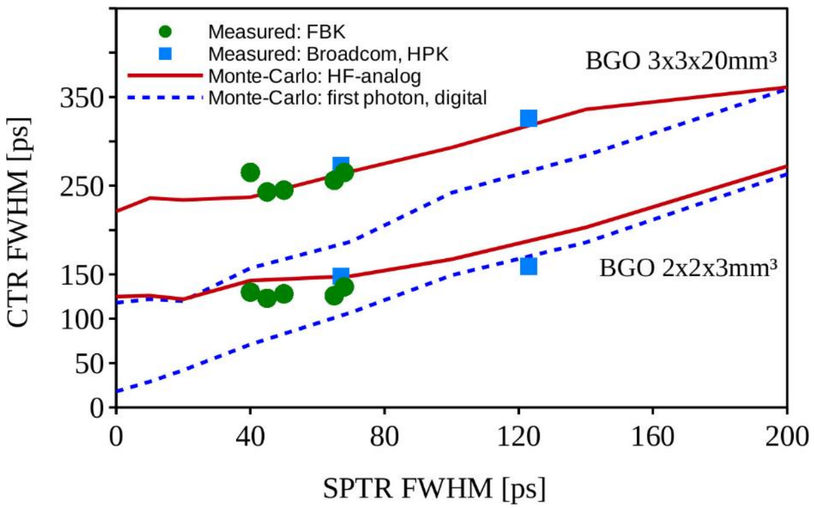
A. Gola et al., "FBK roadmap towards the next-generation of 3D-integrated SiPM and SPAD technologies", PD 2024, Vancouver

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microSiPM
High-density integration: DIGILOG

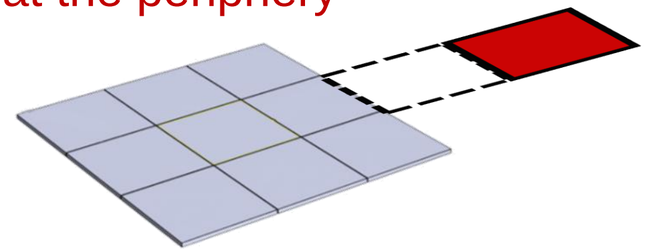
DIGILOG investigates higher density interconnections to *approach the dSiPM performance without the complexity of single-SPAD access*.

FBK will employ the Single-SPAD TSV to support the DIGILOG project, removing the need to replace the central SPAD in the uSiPMs with a TSV, thus achieving the *highest PDE possible*.

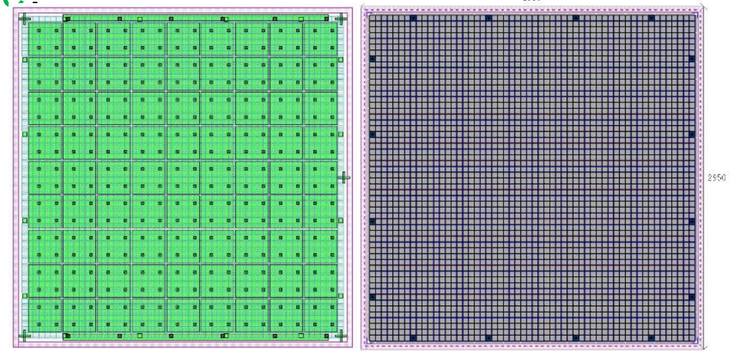


S. Gundacker, et al., A. Gola, E. Charbon, V. Schultz *NSS* 2023
S. Gundacker, et al., *to be published* 2023

SPAD size: 50x 50 µm^2
µSiPM: 3x3 or 6x6 microcells
µTSVs at the periphery



- µSiPMs with µTSVs
- µASICs with *in situ* TDCs

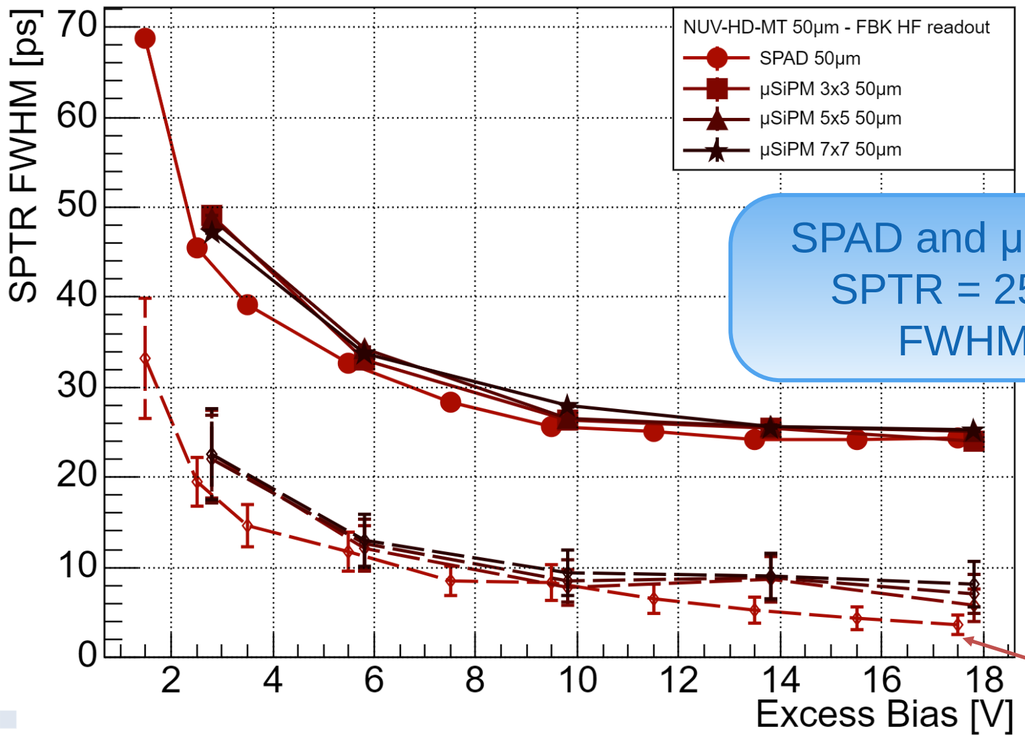


DIGILOG chip under fabrication at FBK:

- 3x3 mm^2, 50 µm cell, M0 layout
- Bias contacts at periphery
- 6x6-element µSiPM

microSiPM
Timing performance: SPTR with µSiPMs

Segmentation of the SiPM active area in *µSiPMs preserves the SPAD Single Photon Time Resolution*, when using the high-frequency readout (FBK implementation).



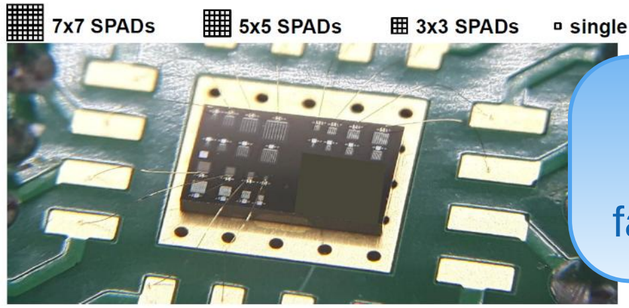
SPAD and µSiPM: SPTR = 25 ps FWHM

(calculated) time jitter caused by the front-end electronic noise

SPTR measured on SPADs and µSiPMs, built with the NUV-MT FBK SiPM technology and featuring 50 µm microcell size and M0 layout, optimized for timing.

Additional challenges:

- Get the *same timing performance with ASIC readout*
- How to better exploit time information
- *3D integration to ASIC at 150 – 300 µm pitch*, less complex than with fully digital approach.

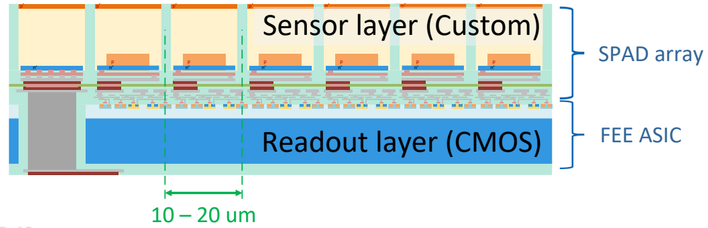


µSiPM test structures fabricated by FBK

NUV-BSI SiPMs
Next-generation development: Backside Illuminated SiPMs

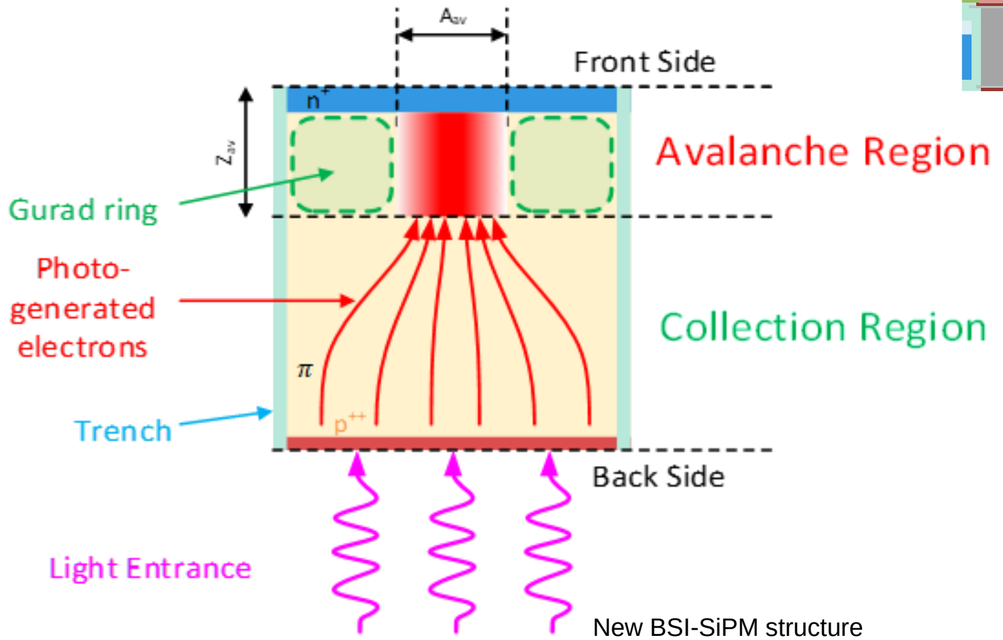
The next-generation of developments, currently being investigated at FBK, is building a *backside-illuminated, NUV-sensitive SiPM*. Several technological challenges should be overcome.

Clear *separation between charge collection and multiplication regions*.



Potential Advantages:

- Up to 100% FF even with small cell pitch
- Ultimate Interconnection density: < 15 um
- High speed and dynamic range
- Low gain and external crosstalk
- (Uniform) entrance window on the backside, ideal for enhanced optical stack (VUV sensitivity, nanophotonics)
- Local electronics: ultra fast and possibly low-power.



Development Risks:

- Charge collection time jitter
- Low Gain → SPTR?
- Effectiveness of the new entrance window

Radiation hardness:

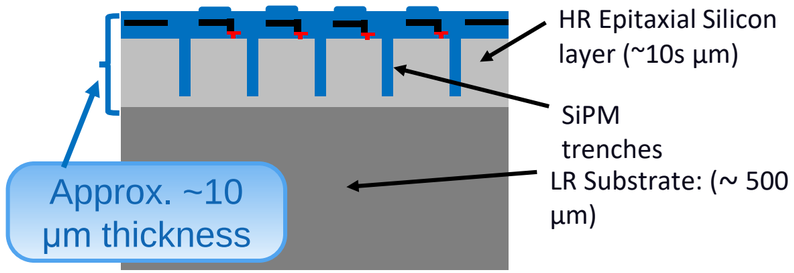
- The SiPM area sensitive to radiation damage, is much smaller than the light sensitive area
- **Assumption**: the main source of DCR is field-enhanced generation (or tunneling).

Presentation in NSS-03 Photodetectors-I

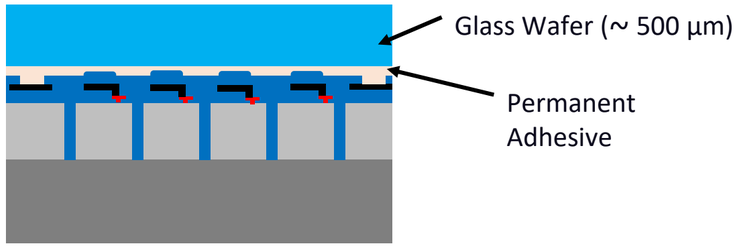
NUV-BSI SiPM technology
Backside process flow

After the new microcell fabrication from the frontside, we *thin the wafer* from the backside to ~10 um and *we form the new entrance window*.

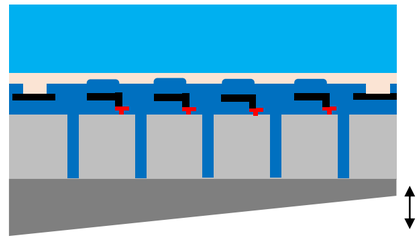
1. Starting Wafer (6”)



2. Edge Trimming + Adhesive Permanent Bonding to Glass Wafer

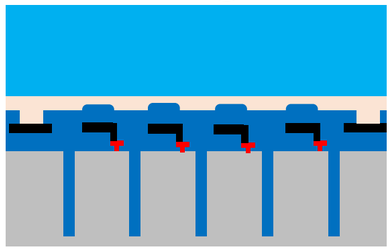


3. Wafer thinning (Substrate Removal)



TTV ~ 6 µm
Too large.

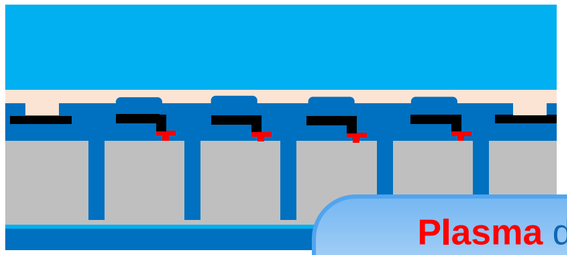
4. TTV regularization step



Second step of substrate removal and reaching the epi/sub interface by reducing the final TTV

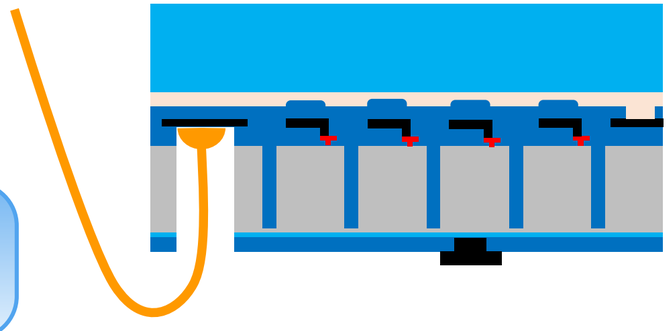
TTV ~ 0.9 µm achieved
Bulk removed.

5. Back junction Formation



Plasma doping +
Laser annealing + ARC
(anti-reflective coating)

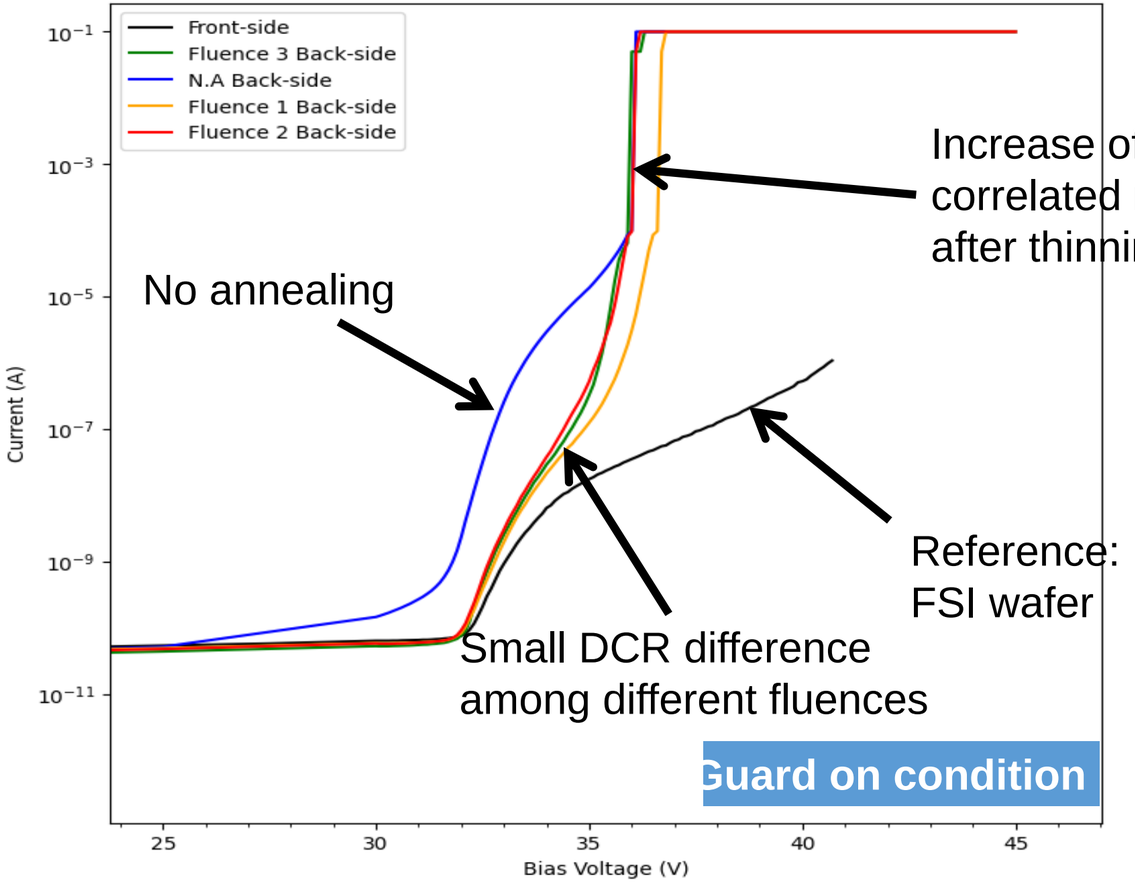
6. Contact formation



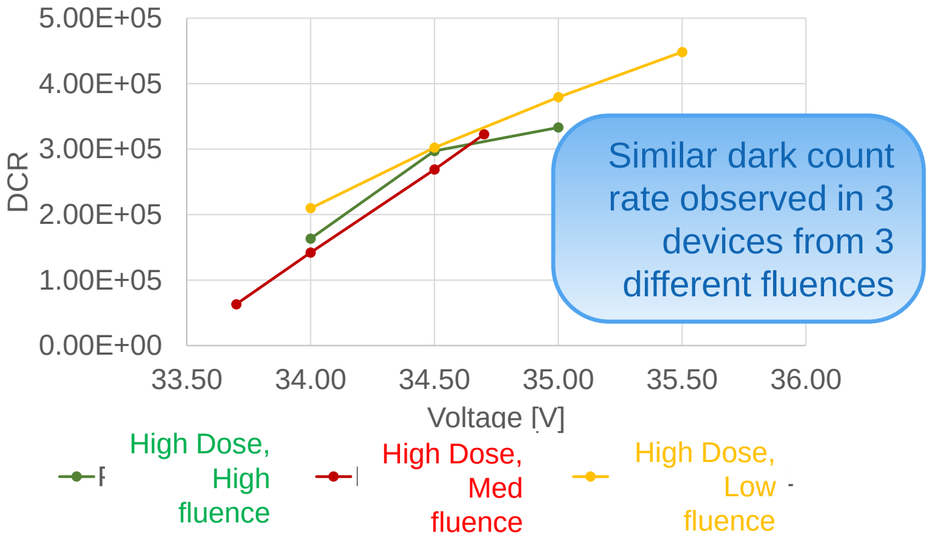
Anode and cathode contacts from the backside

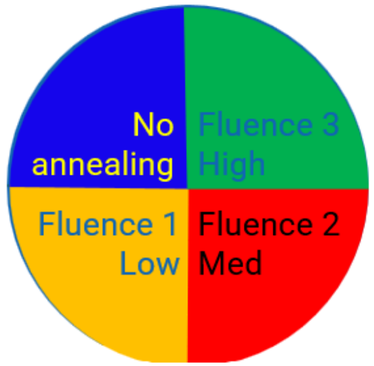
NUV-BSI wafers
Wafer-level reverse IV characteristics

Backside processing was successful. It introduces an *increase of both primary and correlated noise*. which is dependent upon the processing split → *backside annealing fluence*.



- Median IVs of 100 1 mm^2 SiPMs of 20 um cell size on one wafer
- Done at room temperature
- Wafer received high dose of doping and 3 different laser annealing fluences

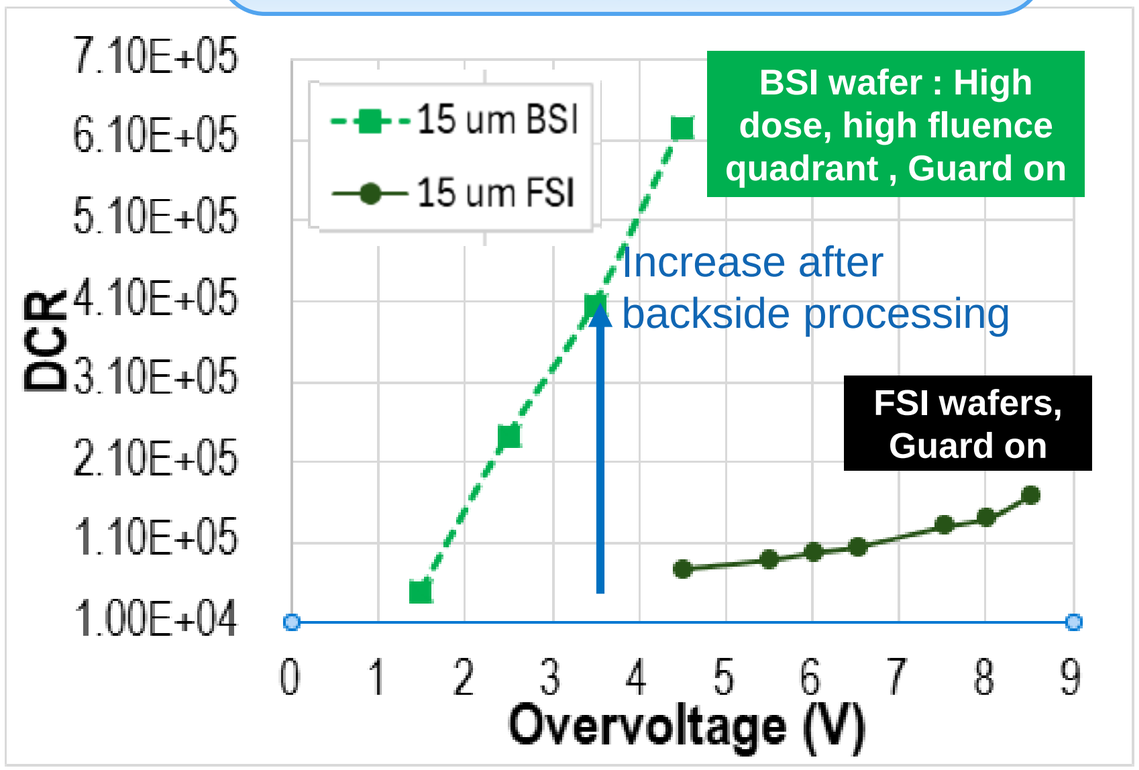




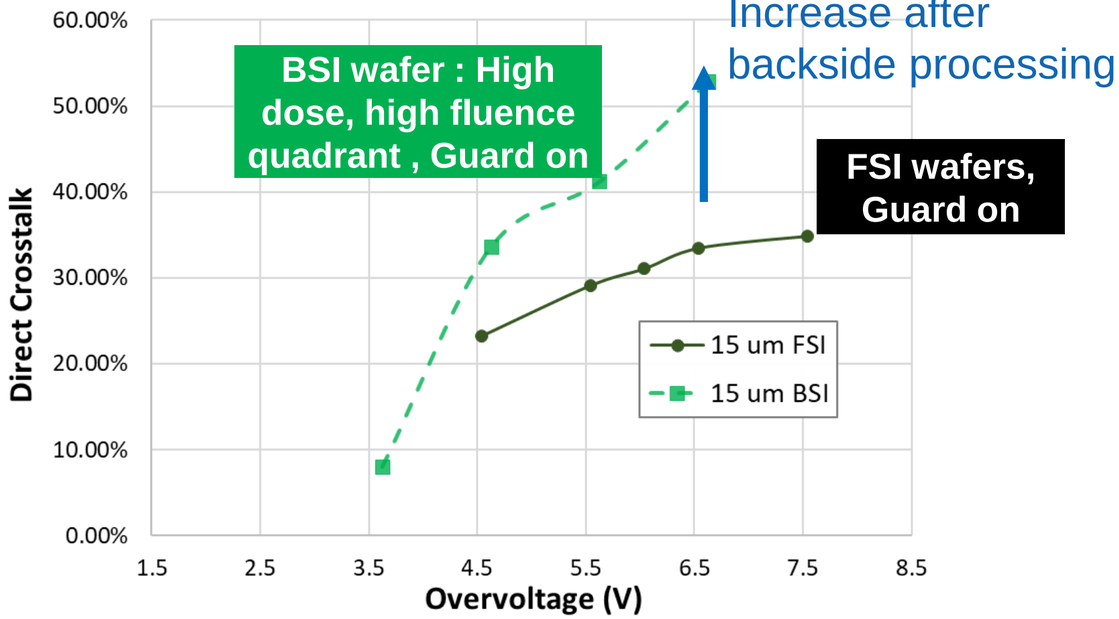
CRS CUSTOM RADIATION SENSORS

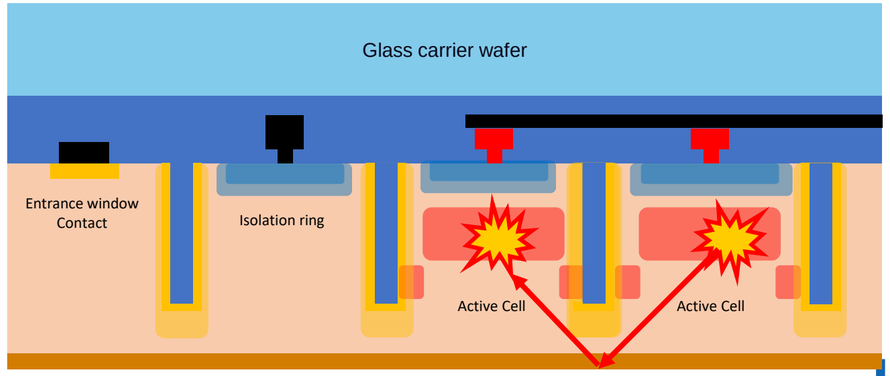
NUV-BSI wafers
DCR and Optical Crosstalk

DCR : 1x1 mm^2 SiPM 15 um cell, at room temperature, High annealing fluence

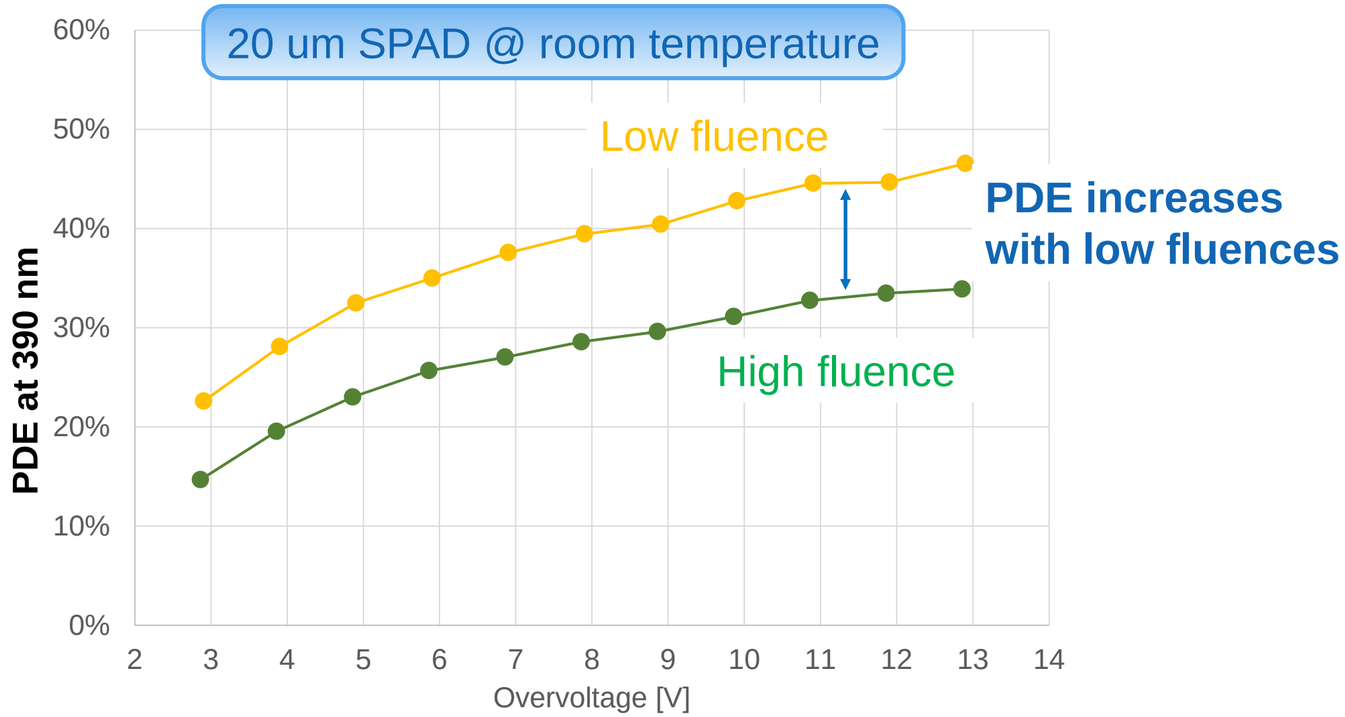


DiCT : 1x1 mm^2 SiPM 15um cell, at room temperature, High annealing fluence

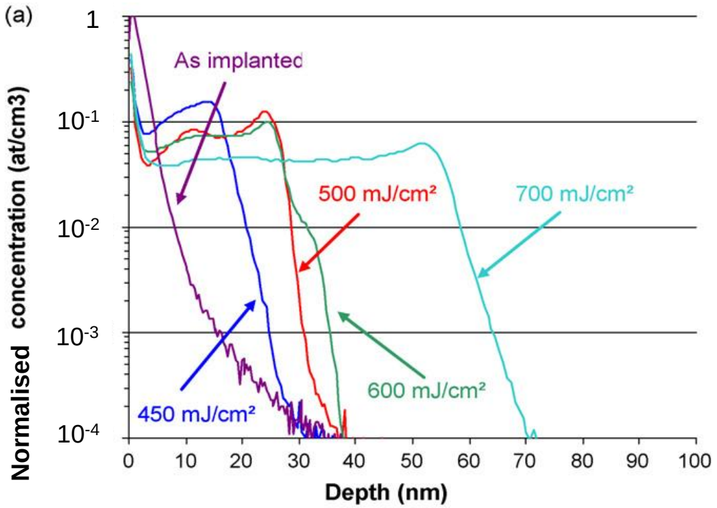




NUV-BSI wafers
PDE @ 390 nm vs Overvoltage – NUV sensitivity



Typical surface dopant profiles for different annealing fluences



Taken from DOI:
10.1016/j.apsusc.2008.11.010

- PDE vs bias measurement on SPAD of 20 um shows increasing PDE with decreasing fluence with guard ring on
- *Hypothesis :* The ultra shallow activation of dopants with low fluence creates a heavily-doped junction on the backside reducing the recombination and drifting photo-generated charge carriers to the high field region
- **To confirm this, we are building a collimated PDE setup to focus the photons at SPAD-level**

CUSTOM RADIATION SENSORS

Backside processing

PRELIMINARY

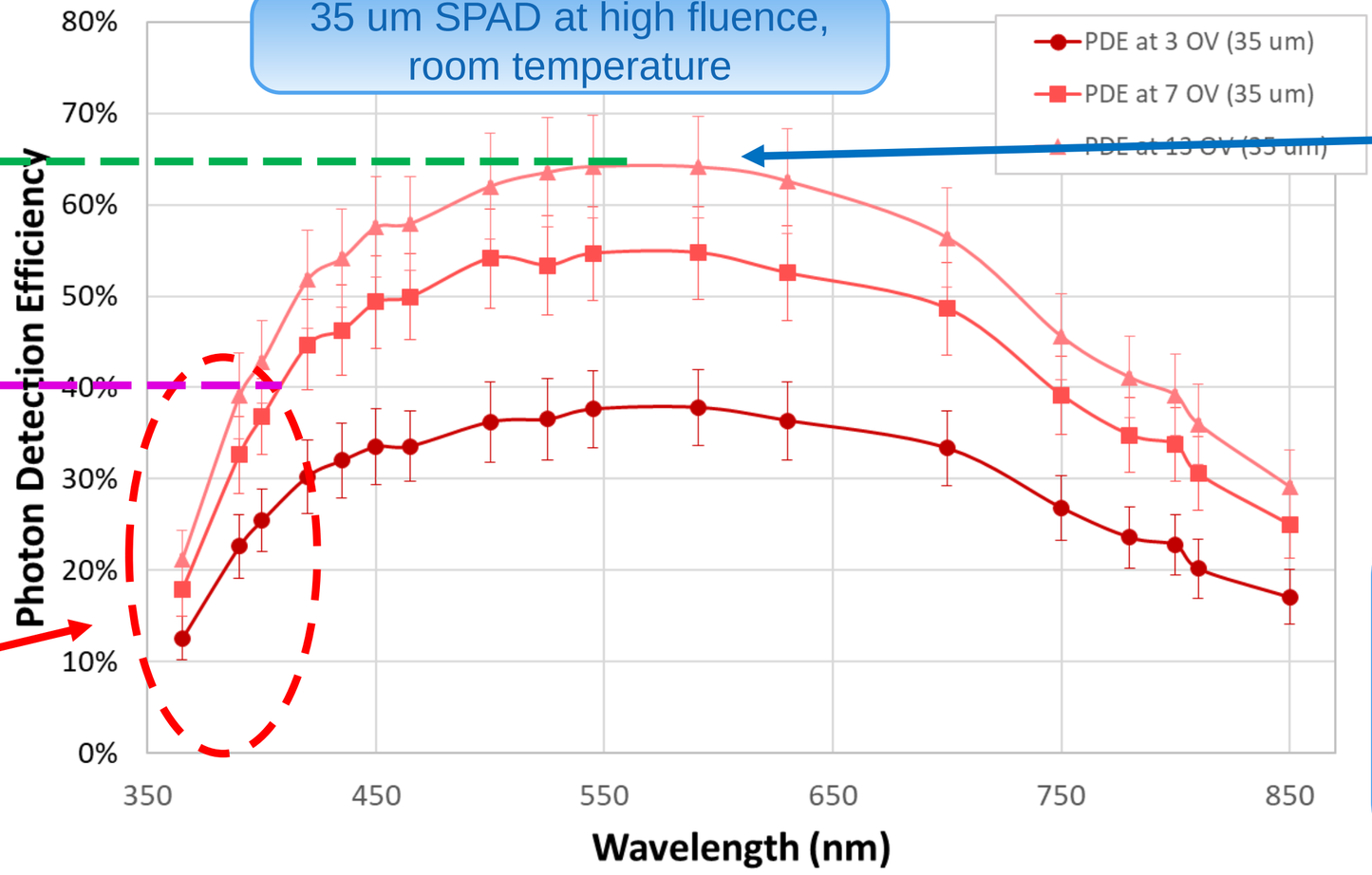
NUV-BSI wafers
PDE vs wavelength

Optimization of the PDE spectrum at *short wavelengths* relies on the *optimization of the process for the formation of the backside entrance window*.

35 um SPAD at high fluence, room temperature

~65% PDE @ 550 nm

~40% PDE @ 400 nm



Metal-filled DTIs are crucial to achieve high Over-voltage

PDE at short wavelength depends on the backside processing optimization.

More process splits are being evaluated.

Next steps :
- Confirm depletion conditions
- Confirm PDE on **smaller cell sizes**

CRS CUSTOM RADIATION SENSORS

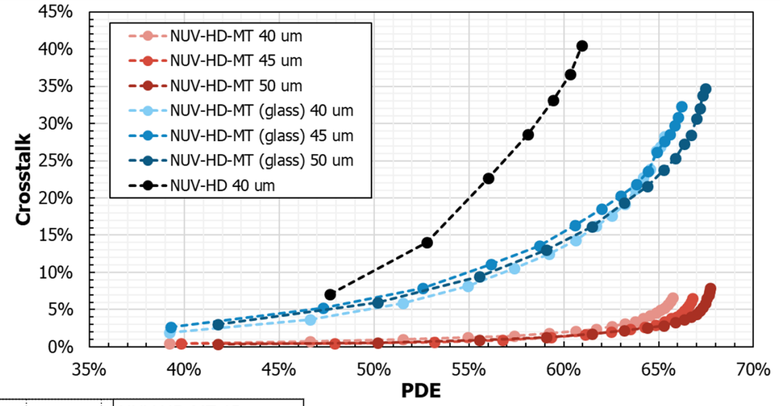
Conclusions (1)
Conclusions

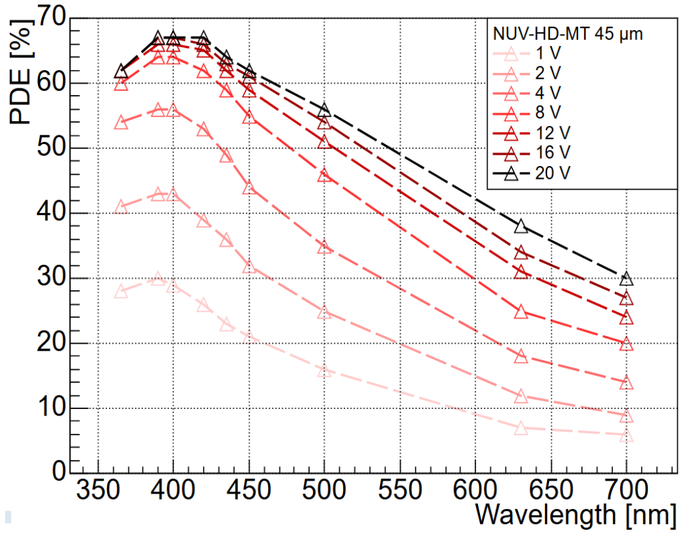
Extended sensitivity (UV-range to IR) and low inter-pixel CT

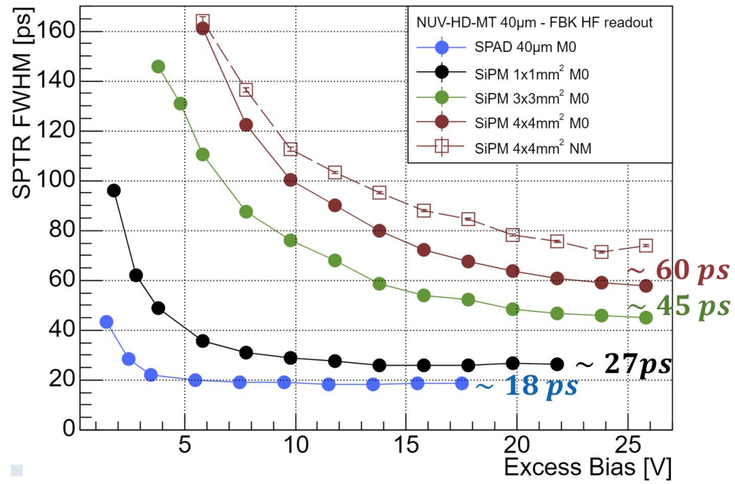
- NUV-HD-MT @Vov=10V:
  - PDE 65% @400nm
  - PDE 40% @500nm
- NUV-DJ @Vov=10V
  - PDE 50% @500nm

Fast response time and fast recovery time and small cell size.

- Rq (and cell size) can be tuned by layout to tailor the recharge time constant.
- 60ps FWHM SPTR can be achieved with HF readout @390nm with a SiPM 4x4mm2 40um M0







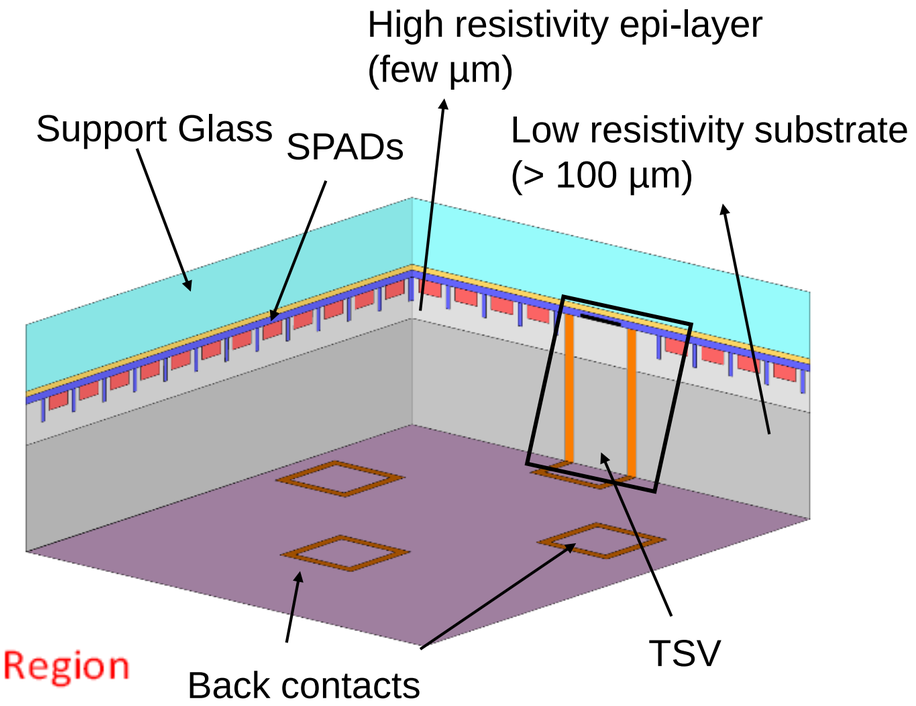
CRS CUSTOM RADIATION SENSORS

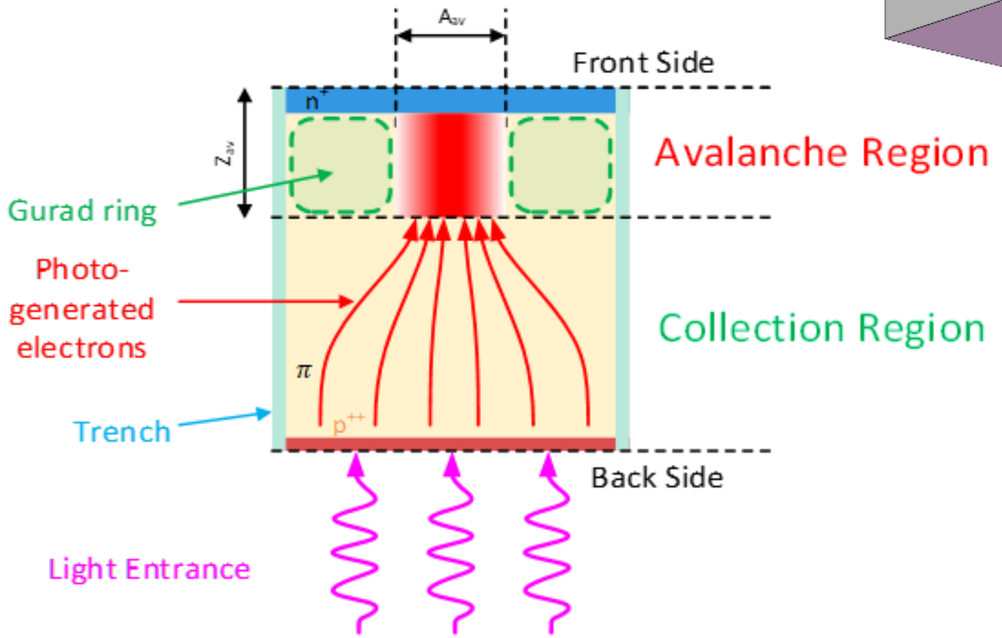
Conclusions (2)
Conclusions

Large active area.

- *TSV-enabling technologies:*
  - *Single SPAD TSV*
  - *MicroSiPM*

BSI SiPM







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FUTURE BUILT
ON KNOWLEDGE

