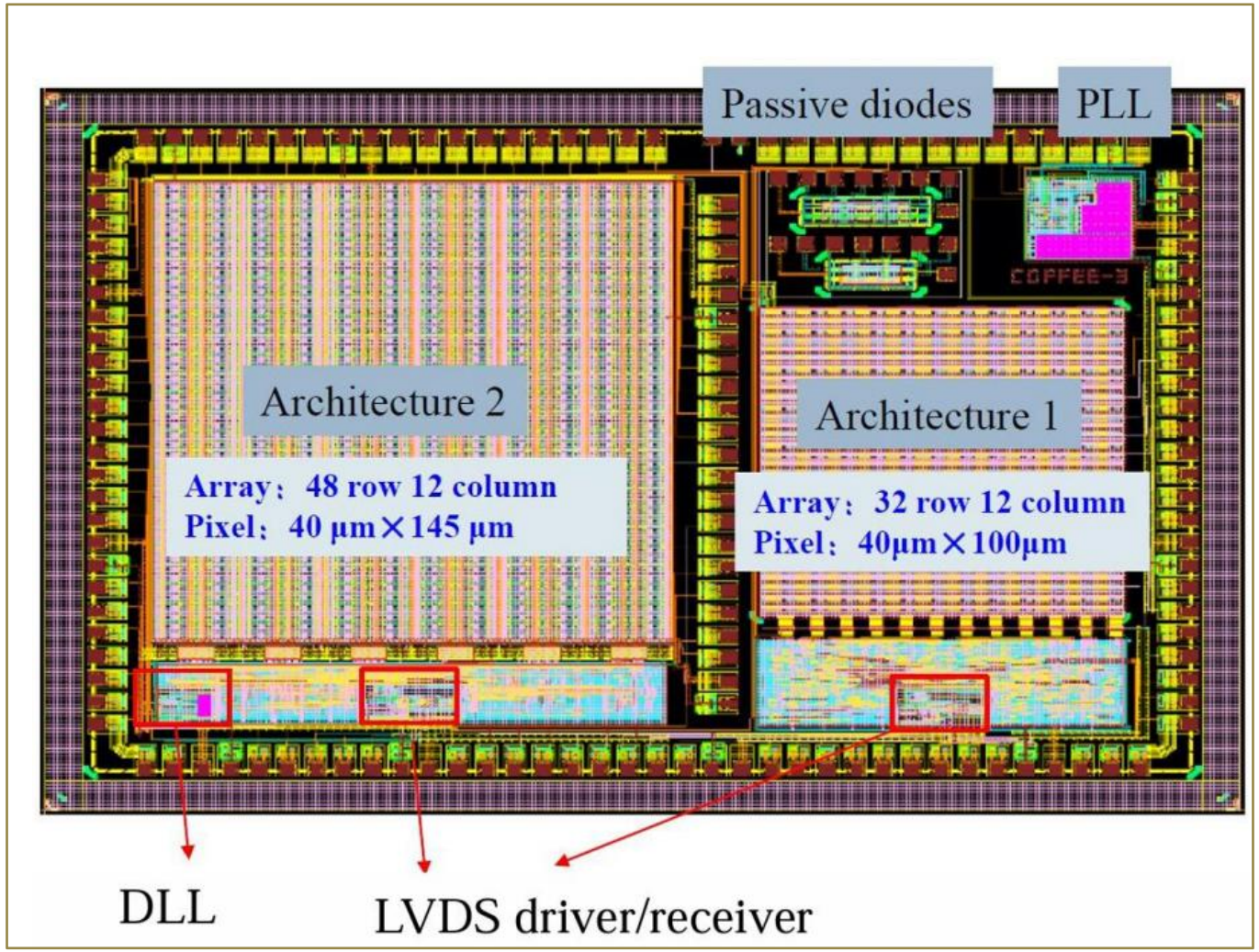
Performance Study of COFFEE3 Chip

COFFEE3 Test Team

2026/03/17

Outline

- **Left-side pixel array**
  - **IP validation**
    - LVDS
    - DLL
  - **Pixel array**
    - Laser test
    - Charge injection
    - ^{55}Fe test
- **Right-side pixel array**
  - **IP validation**
    - **Passive diodes**：IV/CV test
    - PLL
  - **Pixel array**
    - Laser test
    - Charge injection
- **X-ray Test for TID experiment**



COFFEE3 Chip Layout

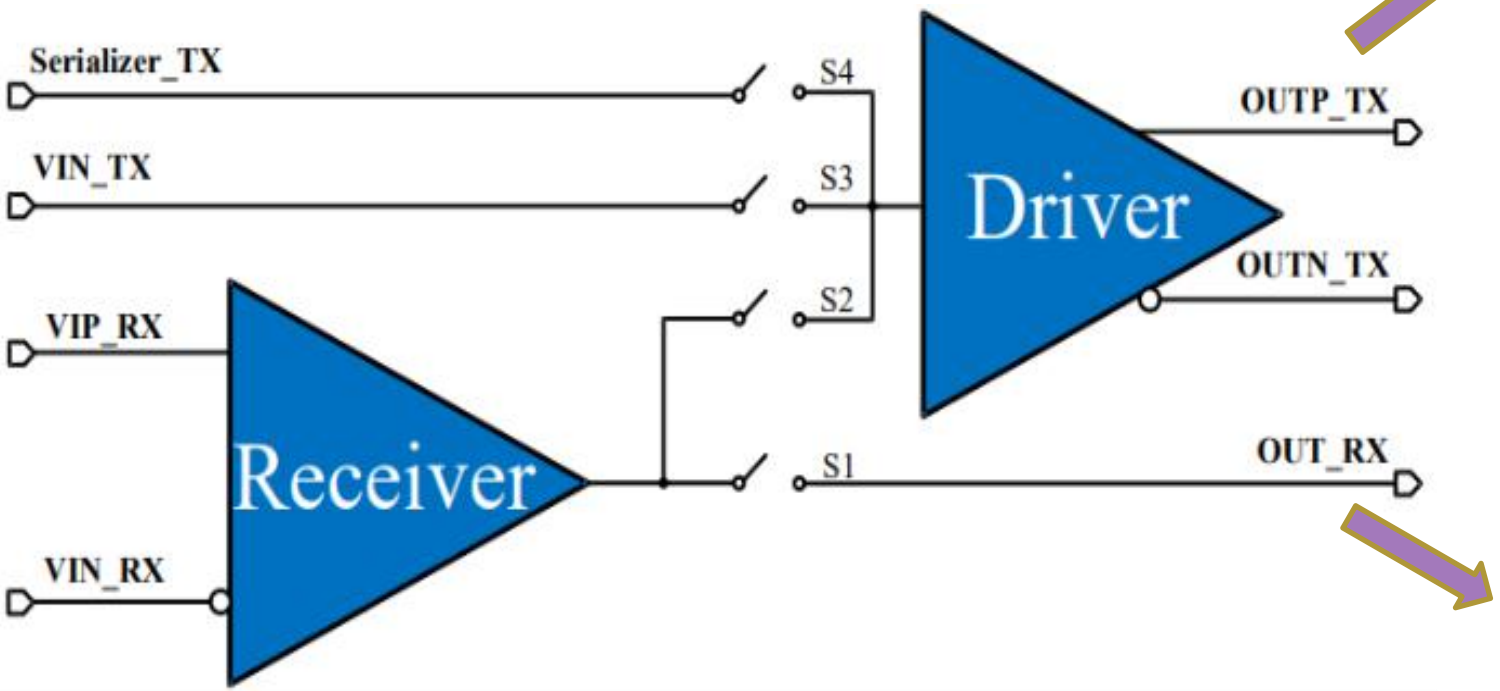
Preliminary testing of the left-side pixel array

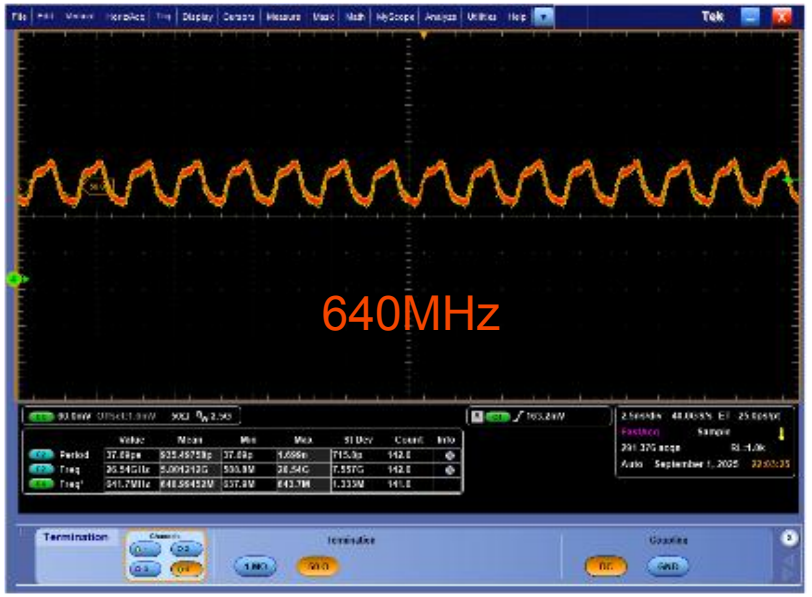
Peripheral Circuitry

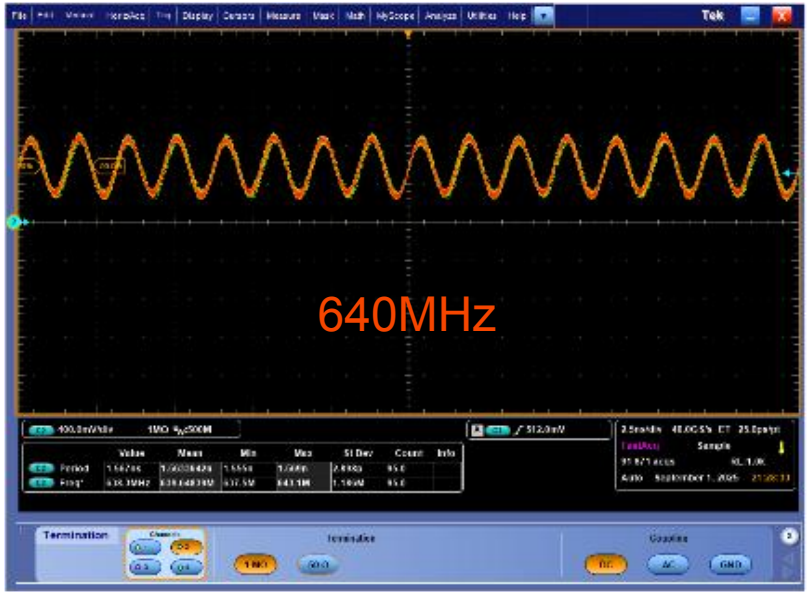
- **LVDS test**

➢ Configured SI5345 to generate a 640 MHz clock; converted to a differential signal and fed through VIN_RX / VIP_RX

➢ LVDS driver functions well







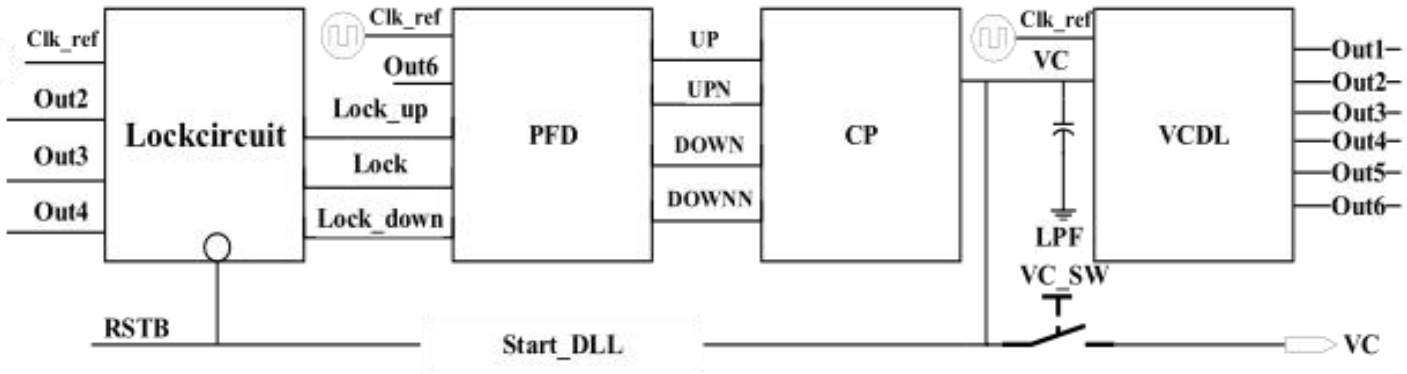
➢ Same 640 MHz differential input

➢ LVDS receiver functions well

Peripheral Circuitry

- **DLL test**

  - SI5345 clock (320 MHz) fed into the LVDS input (lvds_bypass = 0); the chip master clock is derived from the LVDS receiver output
  - The DLL produces 6-phase, divide-by-8 outputs at 40 MHz, with successive phase offsets of π/3
  - All 6 DLL output frequencies measured correctly
  - The phase difference between DLL1 and DLL4 is π, consistent with the design specification



Peripheral Circuitry

- **Empty Packet test**

➢ Reset sequence: Xpixl_RSTN = 0 → XRSTN = 0 → REN = 0 → XRSTN = 1

➢ LVDS_fclk = 200 MHz; single-bit duration = 5 ns

➢ Packet period = 210 ns, containing 42 bits — consistent with the expected frame length

➢ Bit-by-bit decoding from the measured waveform matches the expected empty packet content (0x37_89_AB_CD_EF): 0100 11 0111 1000 1001 1010 1011 1100 1101 1110 1111

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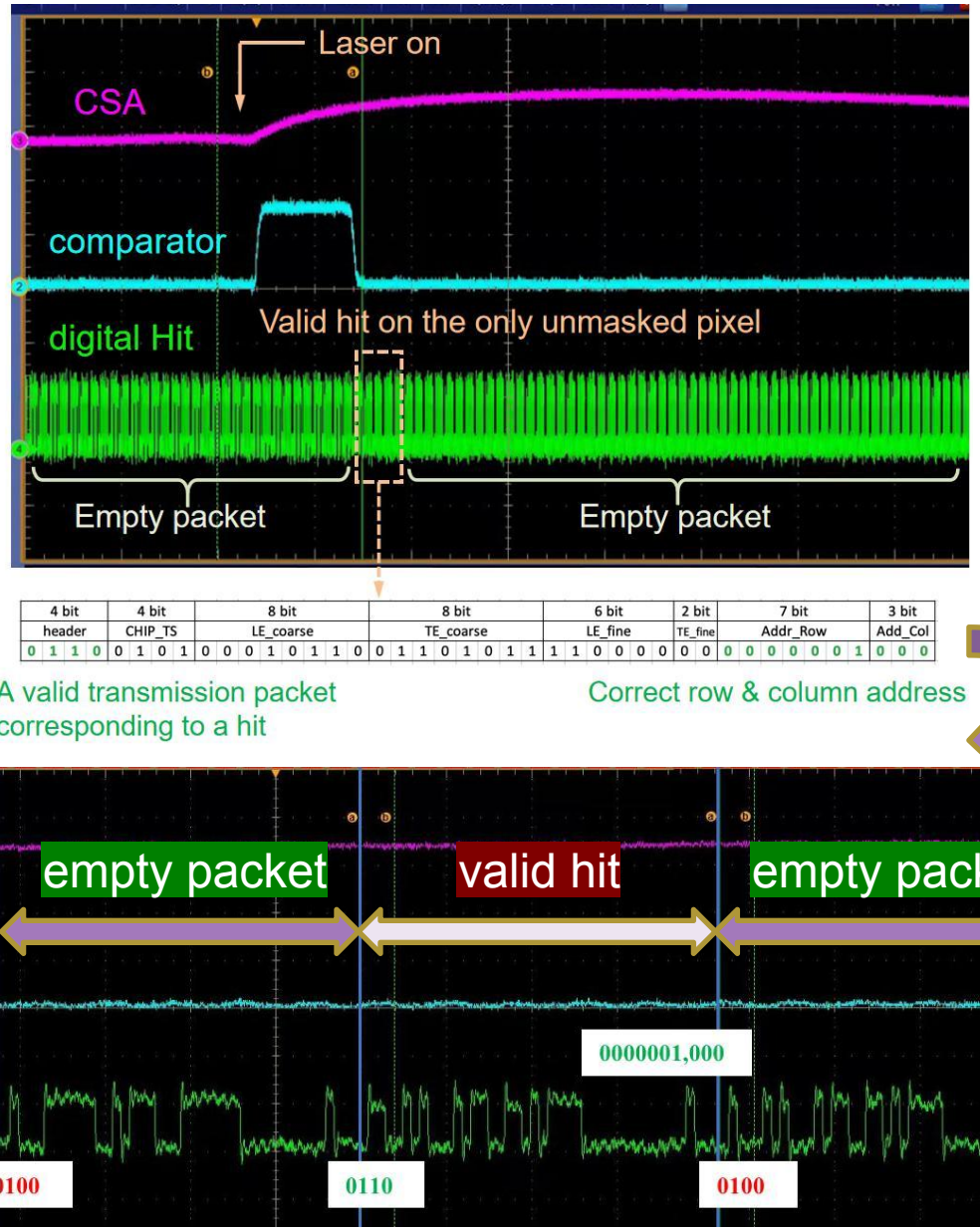
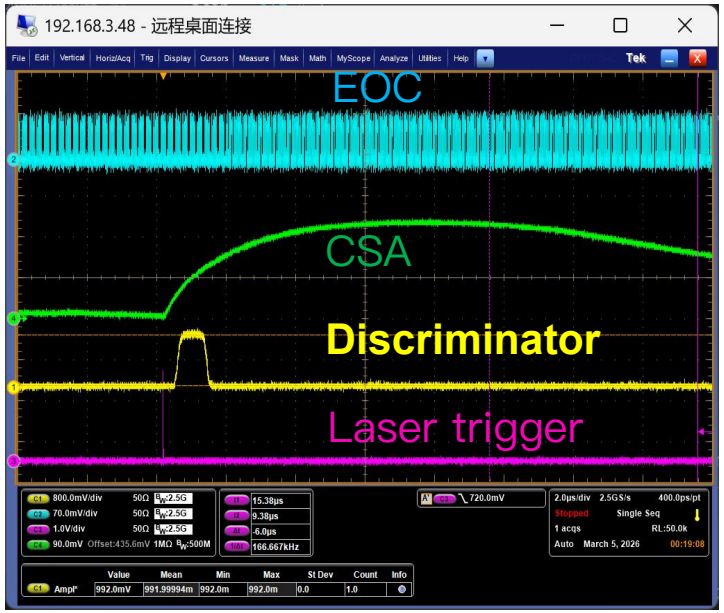
- **Pixel Mask test**

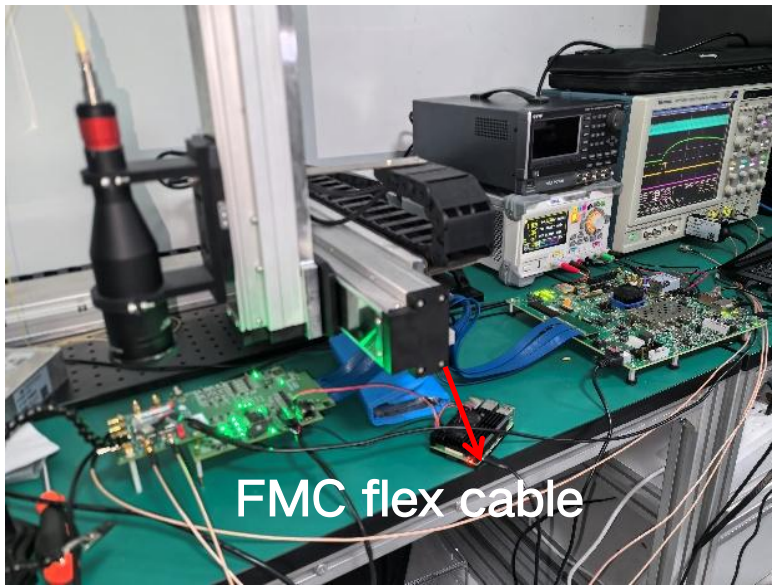
  - Only the second pixel of the first double column in the left-side array was unmasked (ROW = 0000001, COL = 000)
  - Successfully validated the single-pixel masking functionality



Laser Test: Single-Pixel Results

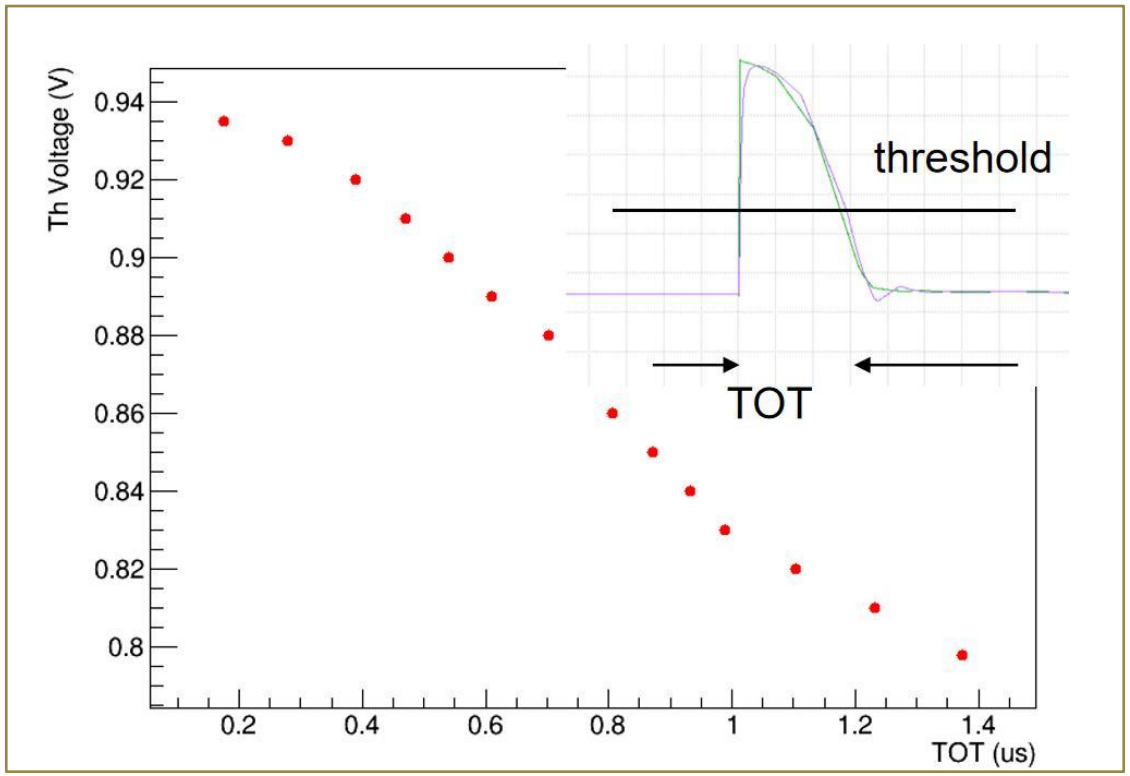
- ✓ Successfully achieved the full readout chain for a single pixel (Col0 Row1) under laser illumination (1 kHz)
- ✓ Verified that the ZCU102 + CaR Board operates correctly via the FMC flex cable
  - ✓ Preparing for X-ray and beam experiments



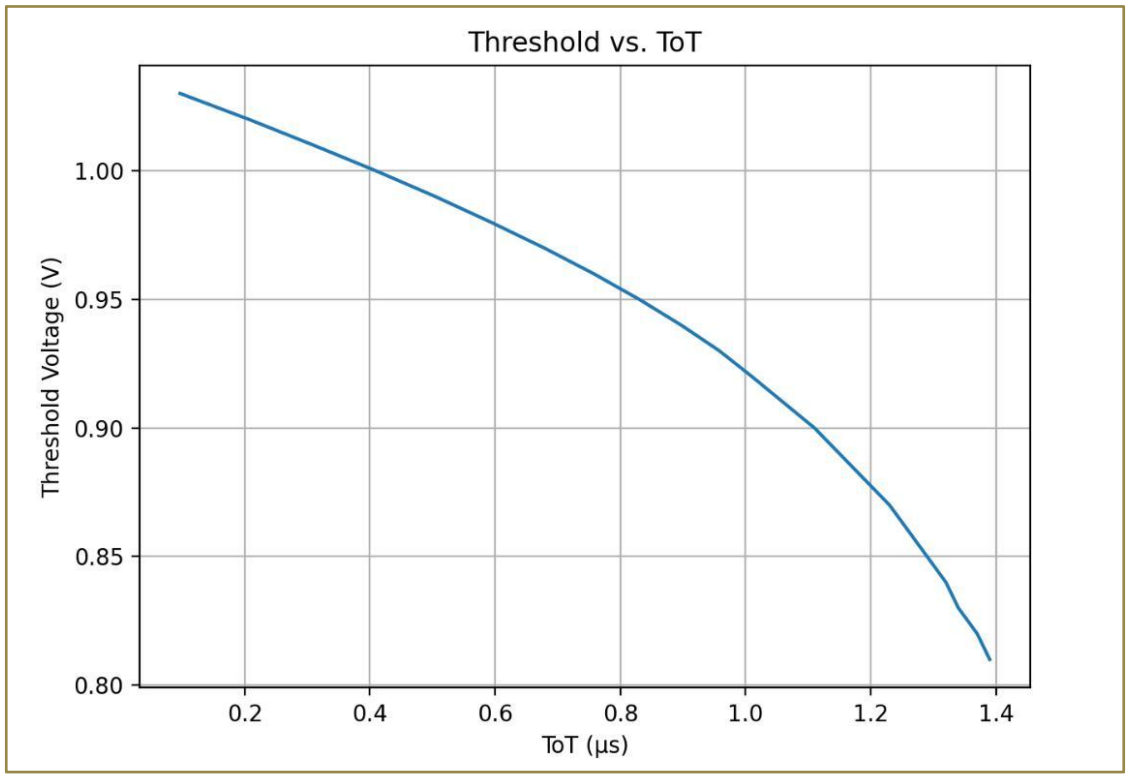


Laser Test: Single-Pixel Results

- A 660 nm laser was used to illuminate Col3 Row1
- Scan Th， HV= -60V， CSA analog output cable disconnected to avoid probe loading
  - ➢ Measured the discriminator output TOT to infer the CSA pulse shape
  - ➢ Measured TOT ≈ 2.5 μs, in good agreement with the circuit simulation



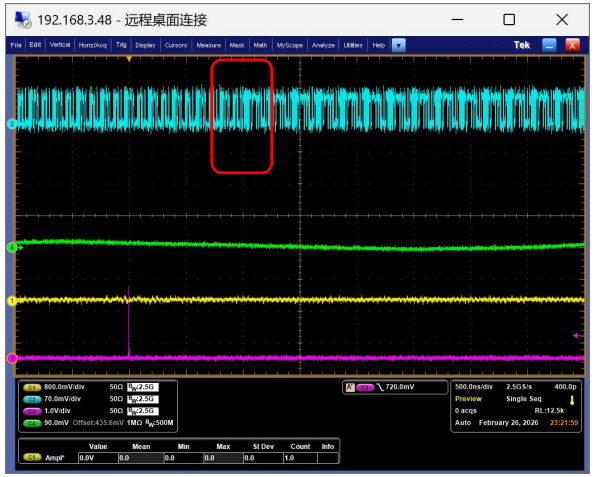
Test

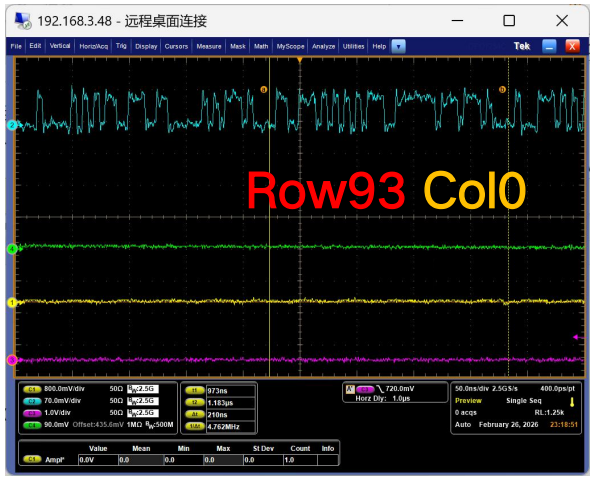


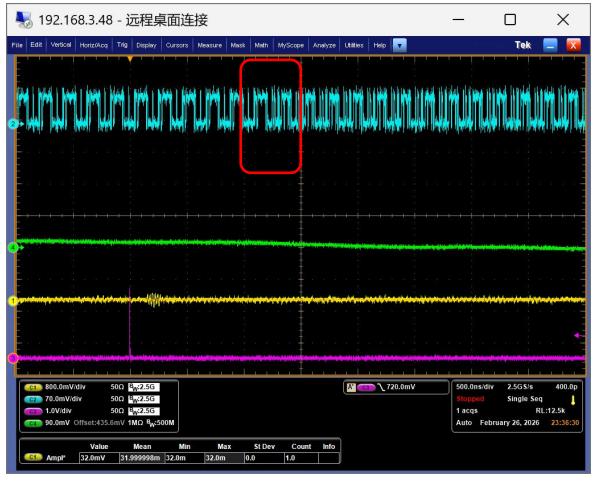
Simulation

Laser Test: Single-Pixel Results

- ✓ Successfully achieved full readout chain operation for additional single pixels (Col0, Row93 or Row48) under laser illumination
- ✓ Only Row93 or Row48 was unmasked; discriminator threshold raised from 0.84 V to 1.00 V.
- ✓ A single transition in the digital output was observed after each laser trigger
  - Blocking the laser yields only empty packets, confirming the laser spot is incident on Row93 or Row48
    - Conclusion: The digital hit is induced by the laser







Laser Test: Multi-Pixel Results

- ✓ Successfully achieved simultaneous readout of two pixels under laser illumination
  - unmask Row46&47&48
  - At Th = 1.00, two consecutive valid data packets were observed following the laser trigger (1 kHz)

Note: the threshold had to be raised by 160 mV, and no data packet from Row46 was observed

Laser Test: Multi-Pixel Results

- ✓ Successfully achieved simultaneous readout of two pixels (Col0, Row0 & Row1) under laser illumination
  - unmask Row0&1
  - At Th = 0.825, two consecutive valid data packets were observed after a laser trigger (1 kHz)

However, results are not stable — spurious valid data packets were observed even before the laser trigger

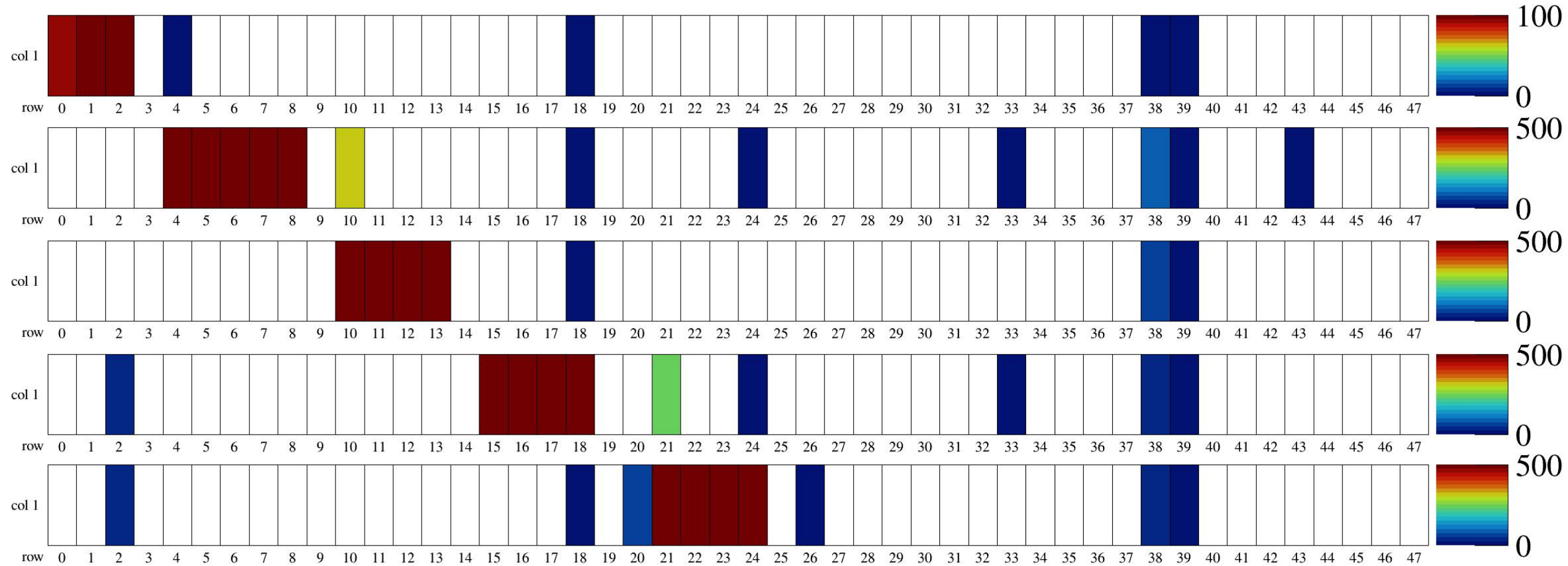
Laser Test: Threshold Scan

- ✓ Performed a threshold scan on the second column of the first double column to determine the optimal shared-threshold operating range: 0.93 V – 1.05 V

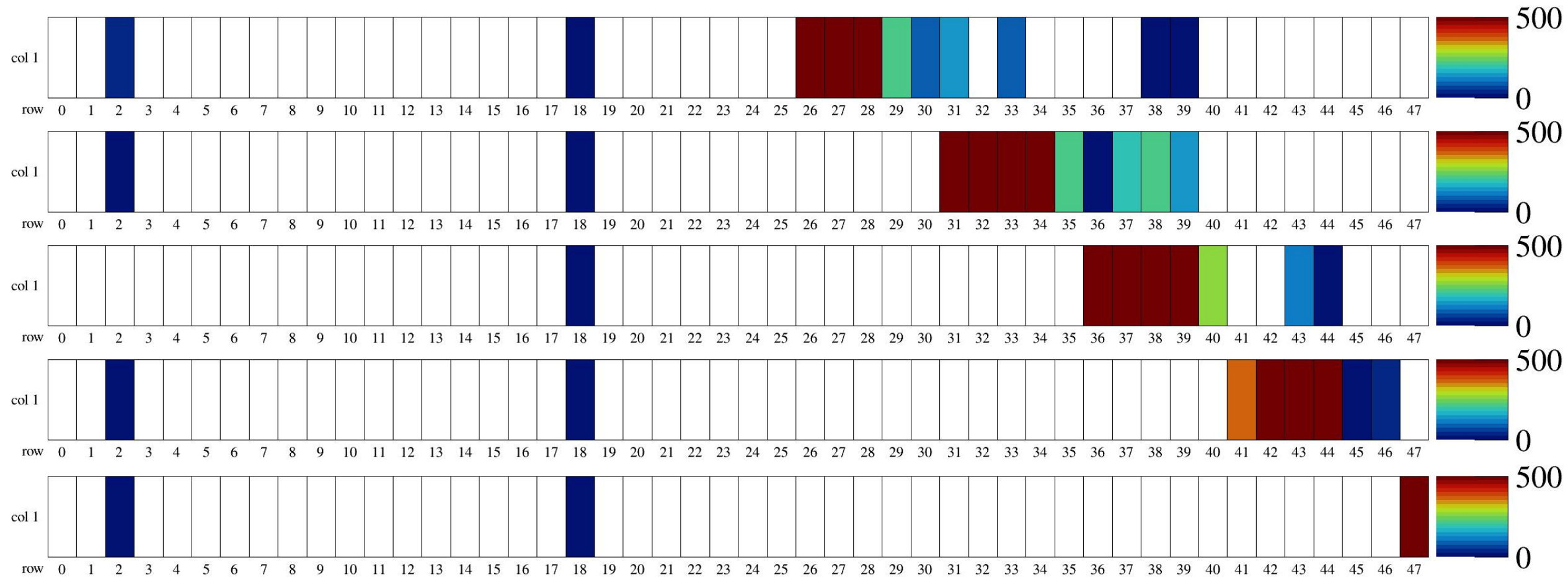
Row Number	Laser High Th	Laser Low Th	Th Range	No Laser High Th
1	1.06	0.86	0.20	0.86
2	1.12	0.92	0.20	0.92
5	1.13	0.92	0.21	0.86
6	1.07	0.87	0.20	0.87
9	1.12	0.87	0.25	0.87
45	1.08	0.86	0.22	0.87
46	1.07	0.86	0.21	0.87
49	1.12	0.89	0.23	0.92
50	1.10	0.86	0.24	0.88
53	1.12	0.89	0.23	0.90
86	1.13	0.89	0.24	0.91
89	1.10	0.90	0.20	0.92
90	1.08	0.86	0.22	0.87
93	1.10	0.89	0.21	0.89
94	1.08	0.88	0.20	0.89

Laser Test: Multi-Pixel Results

- ✓ Successfully achieved multi-pixel readout of an entire column (second column of the first double column) under laser illumination
  - All pixels of the second column of the first double column were unmasked
  - At Th = 1.03, the laser was scanned along the column from Row 0 to Row 47 in steps of ~200 µm

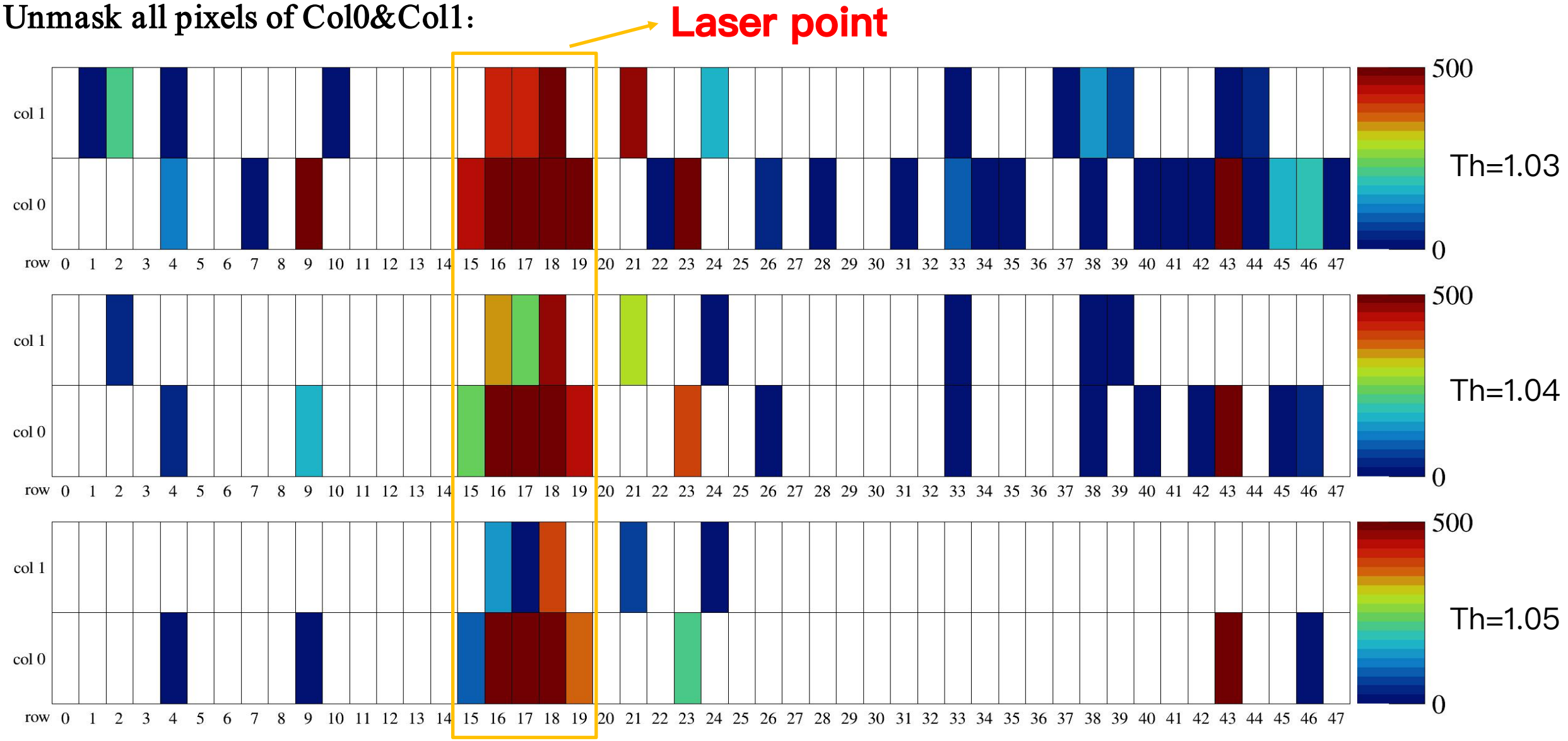


Laser Test: Multi-Pixel Results



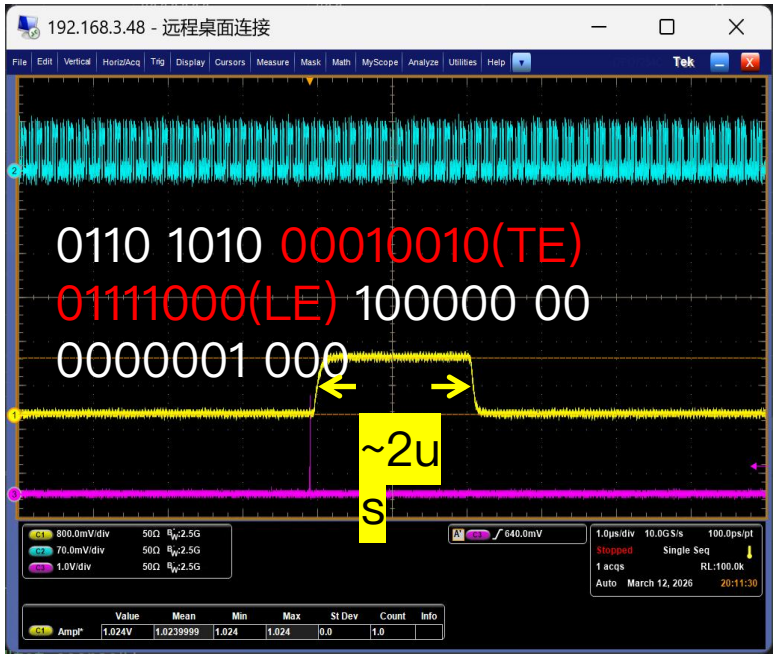
Laser Test: Multi-Pixel Results

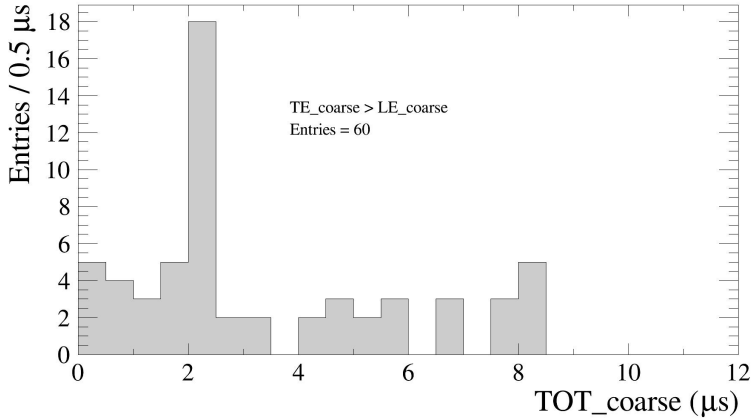
Unmask all pixels of Col0&Col1:

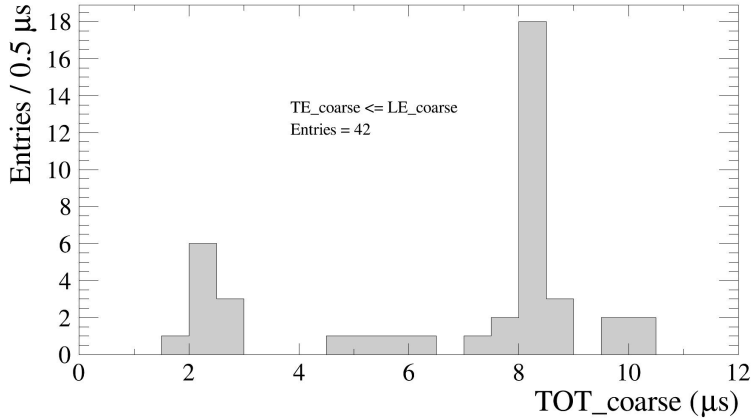


Laser Test: Single-Pixel TOT Decoding

- Using pixel C0R1 as an example, the TOT (Time-over-Threshold) information was extracted following the TOT decoding protocol and compared with the measured discriminator pulse width
- Configuration: LVDS clock = 200 MHz, laser (1 kHz) aimed at Col0 Row1, Th = 0.9, only C0R1 unmasked
- Gray-to-binary conversion yields: 00011100 (TE), 01010000 (LE)
- Calculated TOT = (0x50 − 0x1C) × master clock period = 2.08 μs, consistent with the measured comparator output pulse width
- However, a significant number of anomalous TOT values were also observed, requiring further investigation

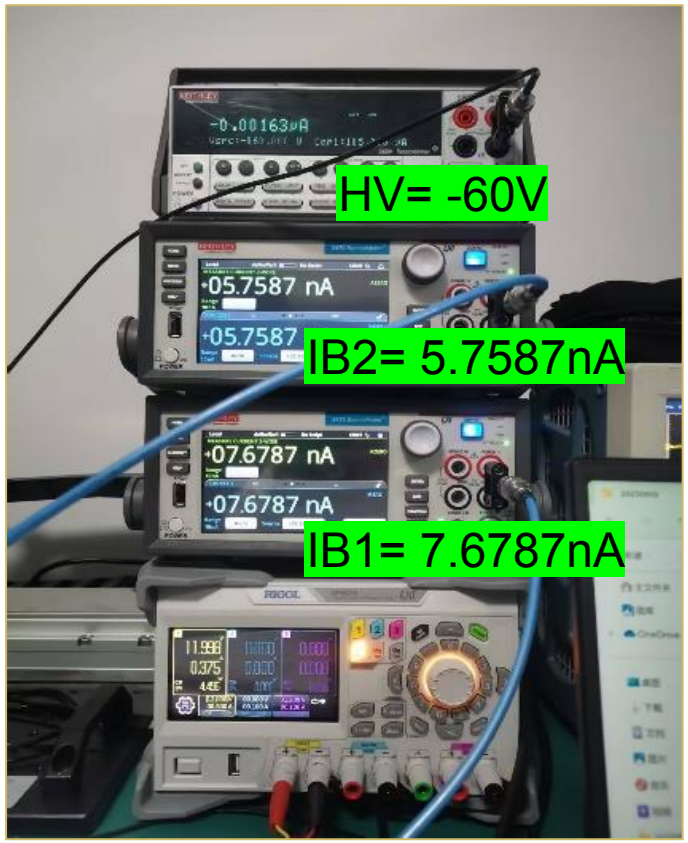


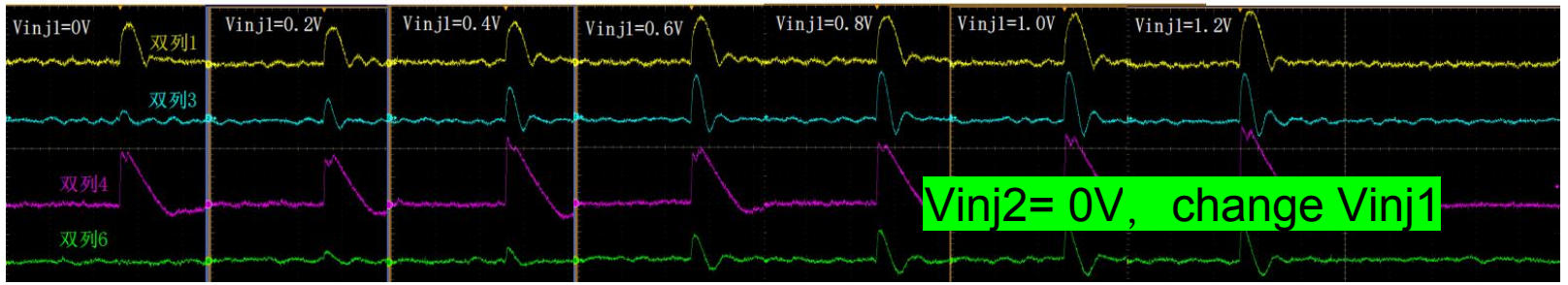


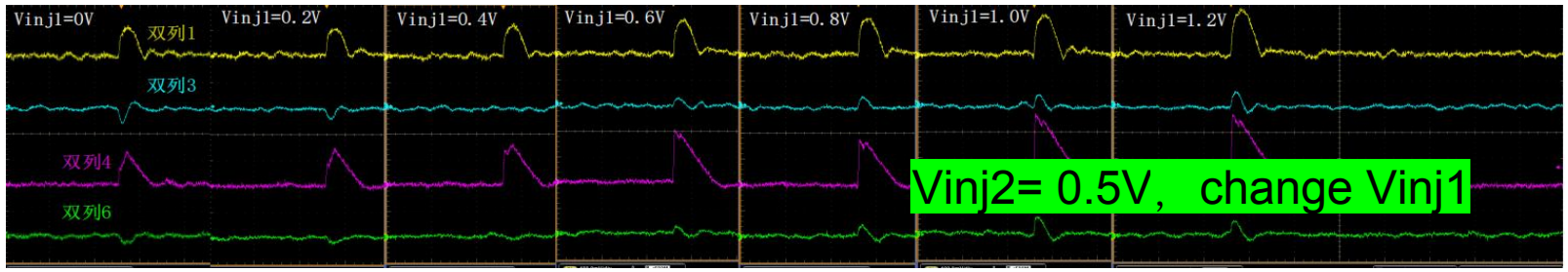


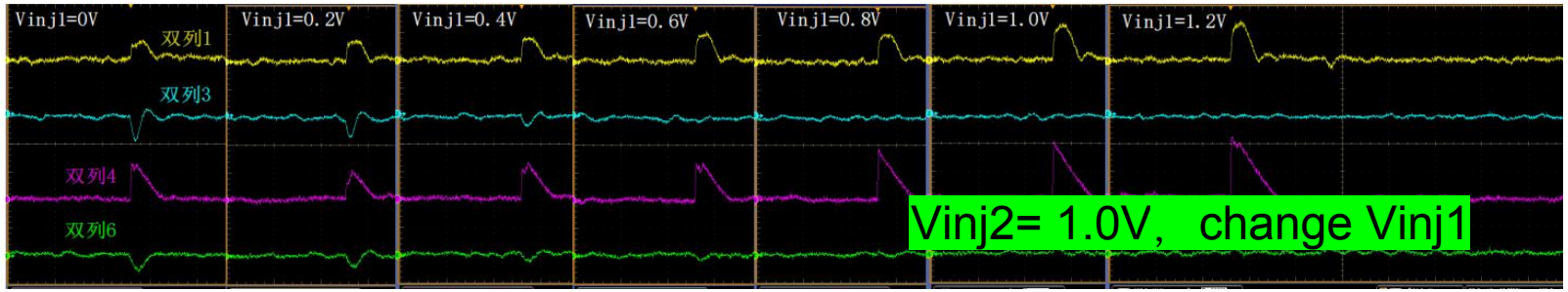
Charge Injection Results

- Bias voltages set: B1 = 0.93, B2 = 0.8, B3 = 0.75, B4 = 0.6, A1 = 0.45, A2 = 0.94, A3 = 0.97
  - ➢ The CSA output amplitude for all four double columns increases with the injected charge (Vinj1 − Vinj2), as expected



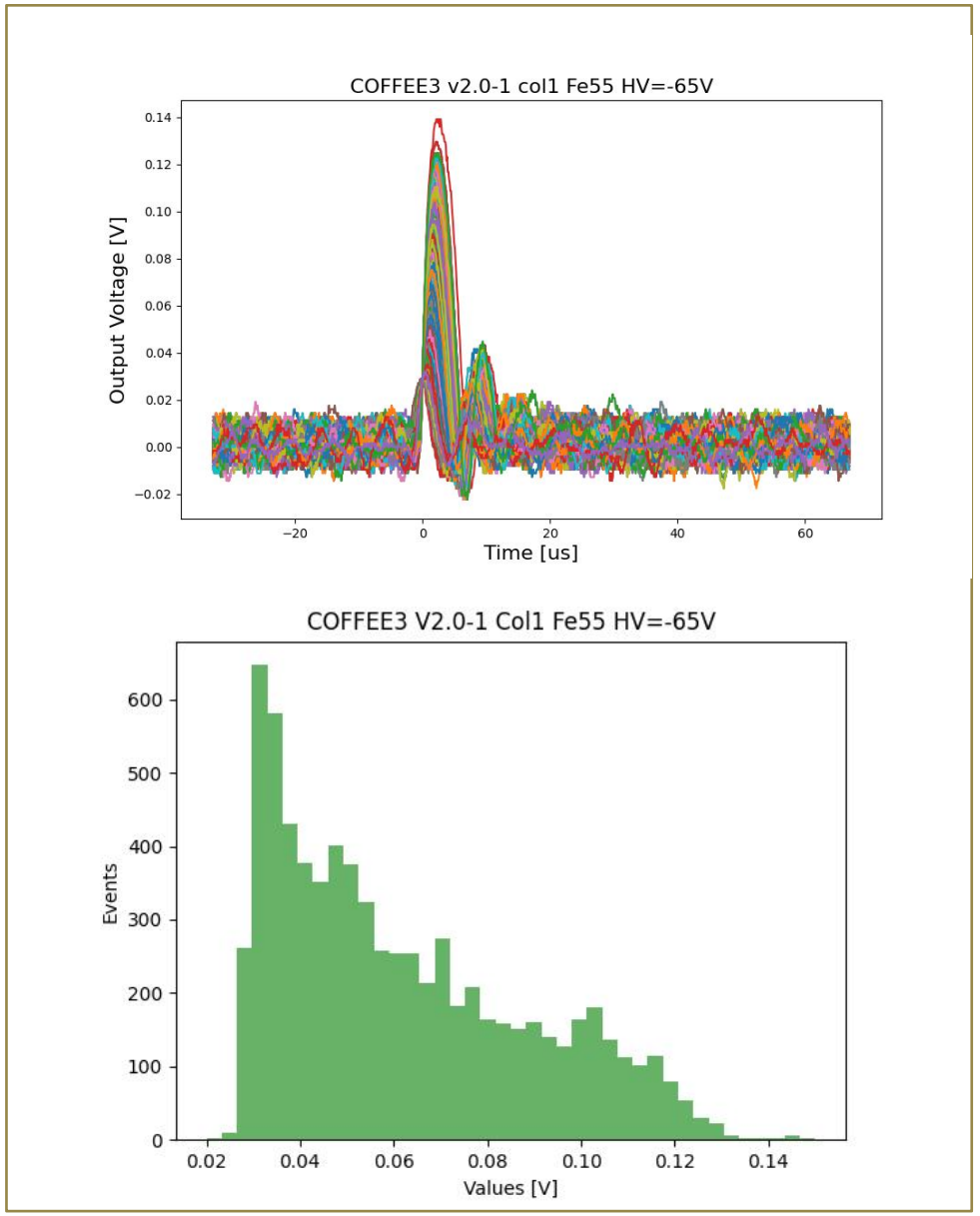






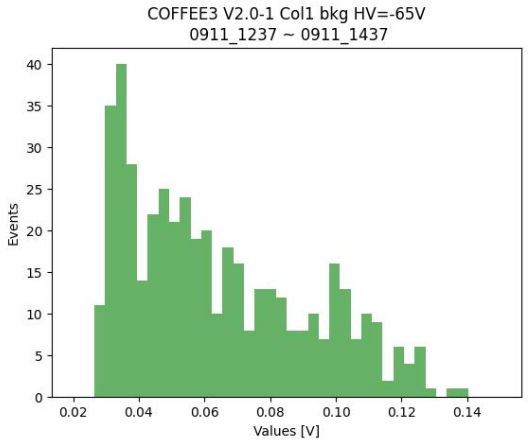
^{55}Fe Test Results

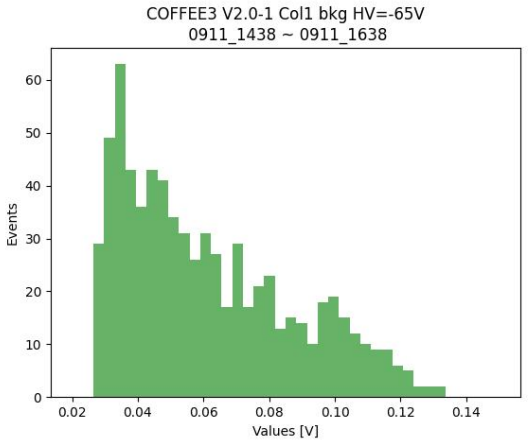
- **Test Col0 Row1 using a ^{55}Fe X-ray source**
  - Operating parameters:
    - IB1= 0.235, IB2= 0.159
    - A1= 0.45, A2= 0.97, A3= 0.97, A4= 0.55
    - B1= 0.93, B2= 0.8, B3= 0.8, B4= 0.6
  - Sensor bias= -65V
  - Oscilloscope trigger threshold = 29.6 mV
  - Results with ^{55}Fe source:
    - vent rate above threshold: ~8 events/min
    - Total above-threshold events collected: 3,727

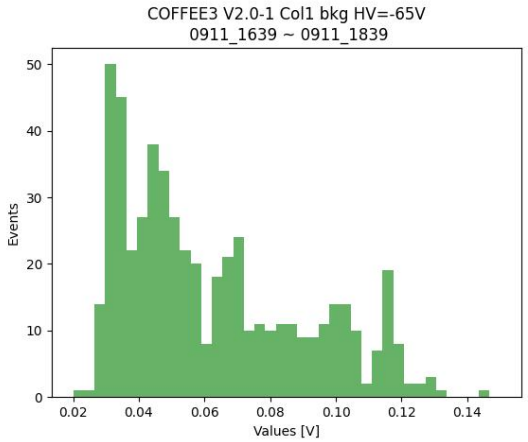


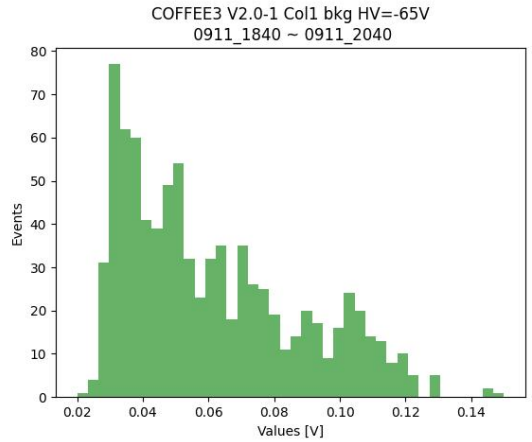
^{55}Fe Test Results

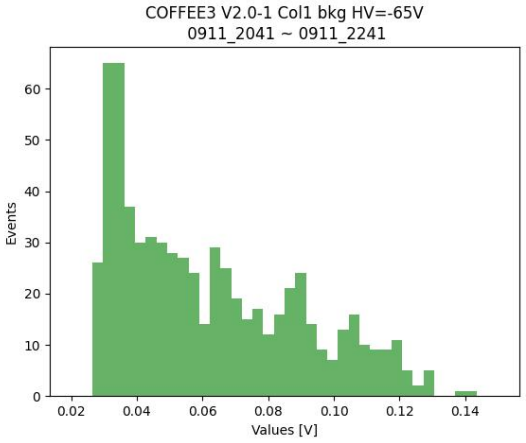
Data-taking results binned in 2-hour intervals (histogram plots):

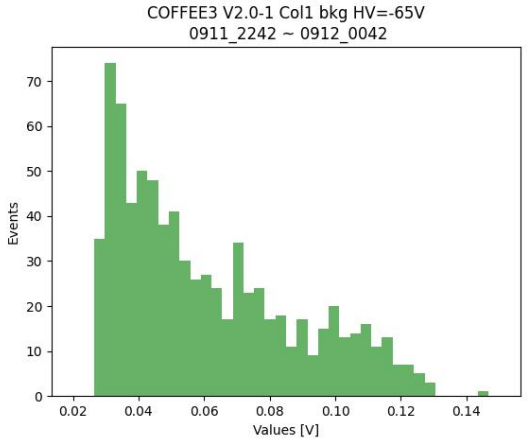


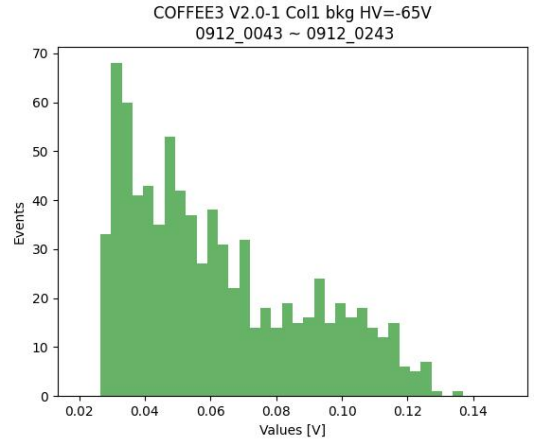


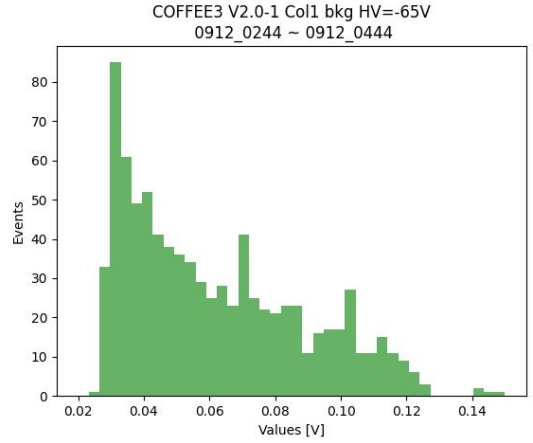






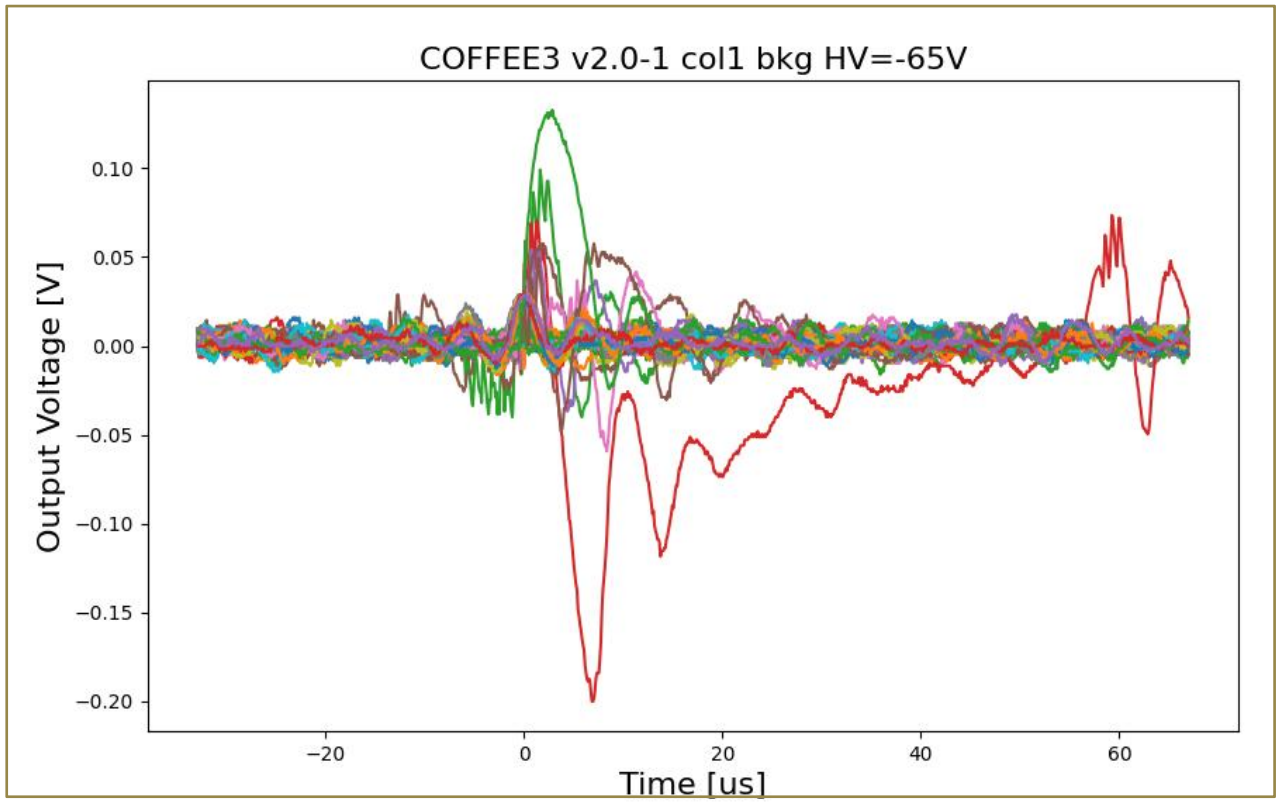


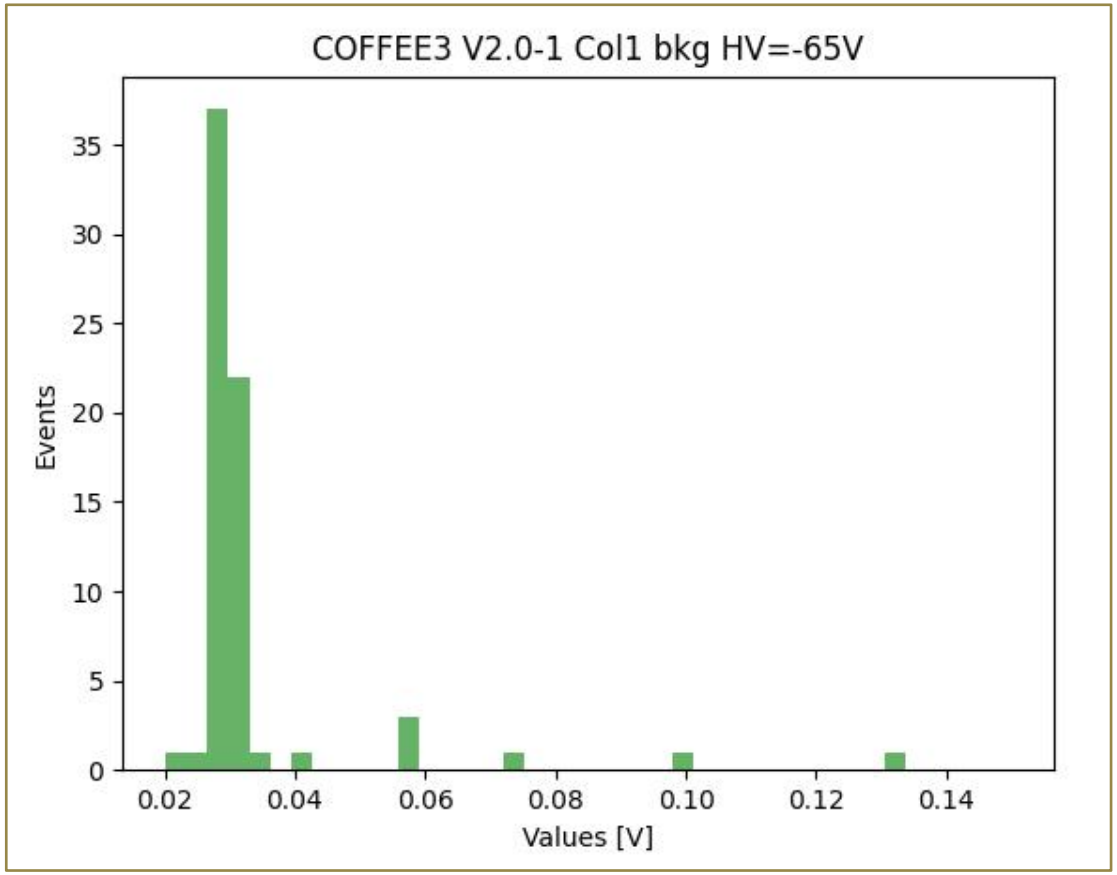




^{55}Fe Test Results

- Background-only measurement (no ^{55}Fe source):
  - Background rate: ~1 event above threshold per 5 minutes
  - Total above-threshold events: 69
  - Noise peak position at ~30 mV, correlated with the trigger threshold setting



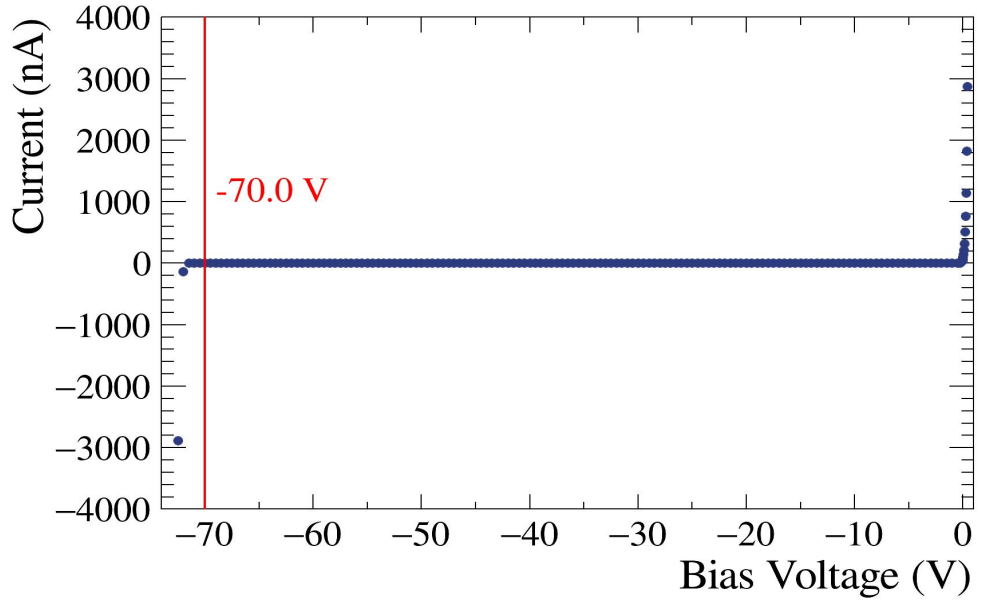


Preliminary testing of the right-side pixel array

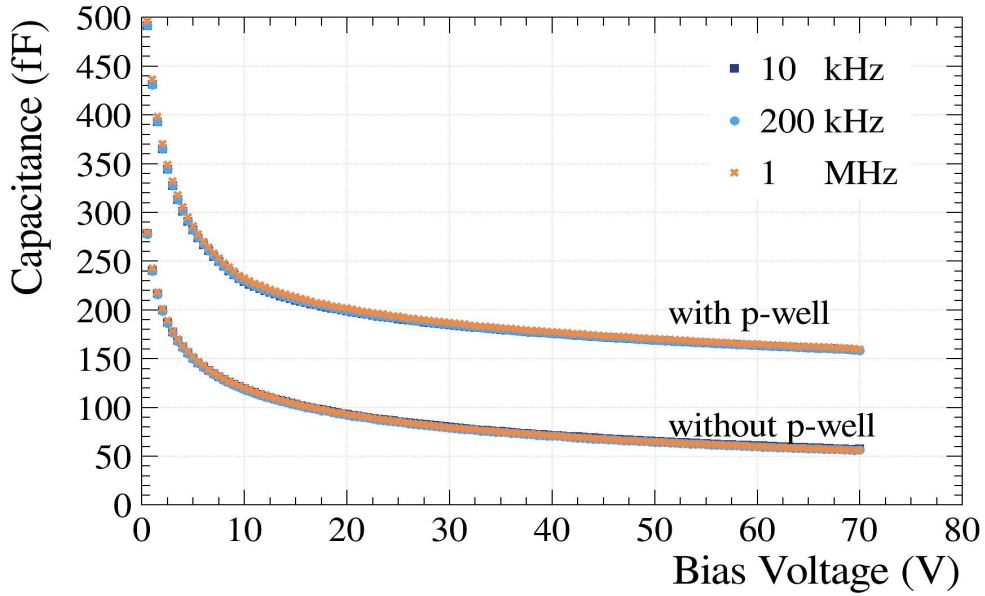
Passive diodes matrix

- Two 3 × 3 sub-arrays
- 45 × 145 μm² (upper) and 40 × 100 μm2 (lower), corresponding to left and right pixel matrix, respectively.
- The results from **40 × 100 μm²** sub-array 2 are presented, with its CV curve offset by a parasitic capacitance of ~247 fF.

IV test:
breakdown at ~ –70 V. Leakage current is ~140 pA at –70 V, as expected for a regular resisitivity (10 Ω· cm) wafer.



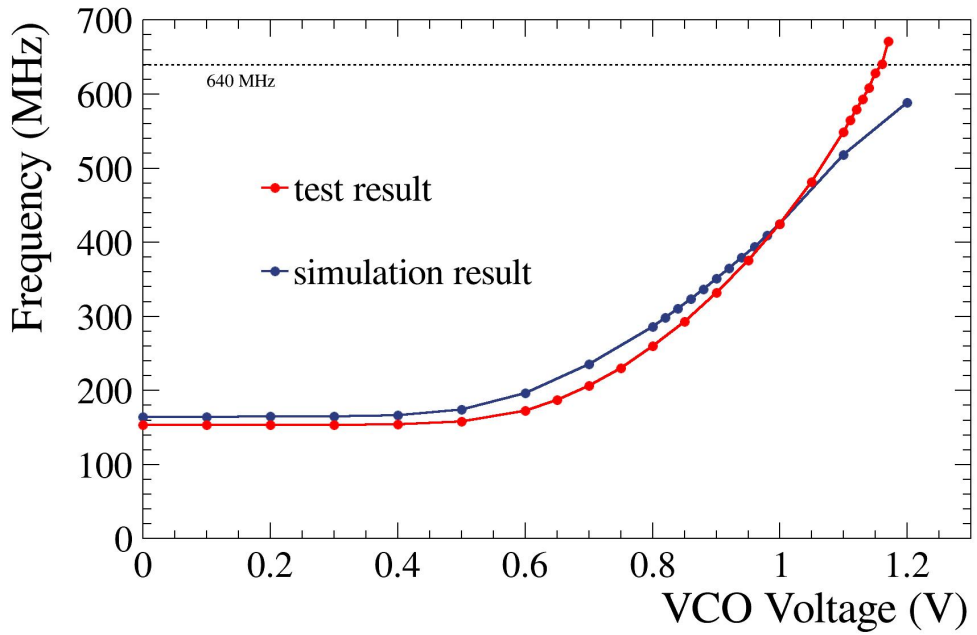
CV test:
single pixel has capacitance of ~50 fF at –70 V due to depletion.



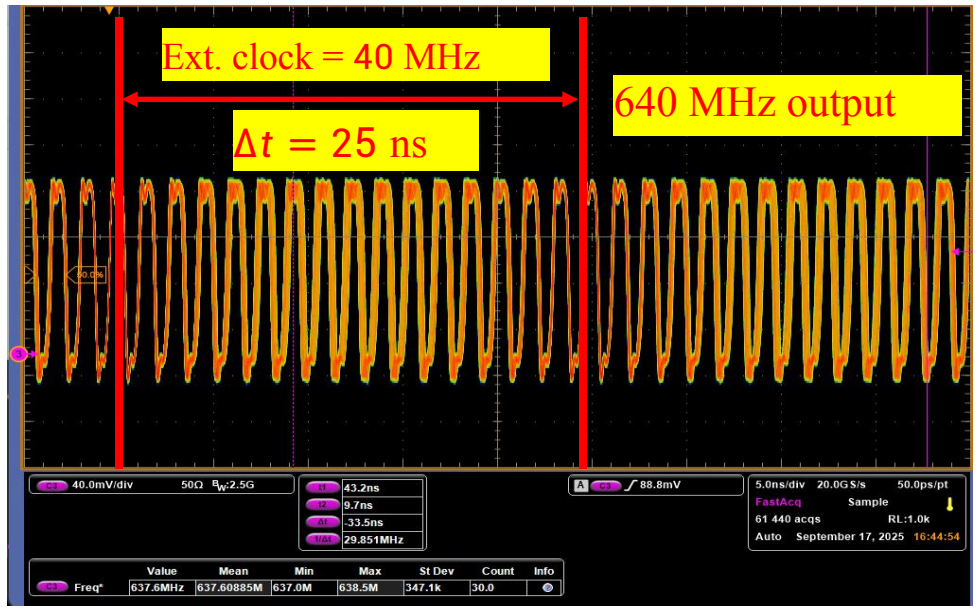
PLL test

- PLL was designed to supply output clock with frequency of up to 640 MHz at working voltage of 1.2 V.
- Stable 640 MHz output can be obtained, with analogue power reaches 1.7 V exclusively.

☐ Standalone frequency clock of VCO output



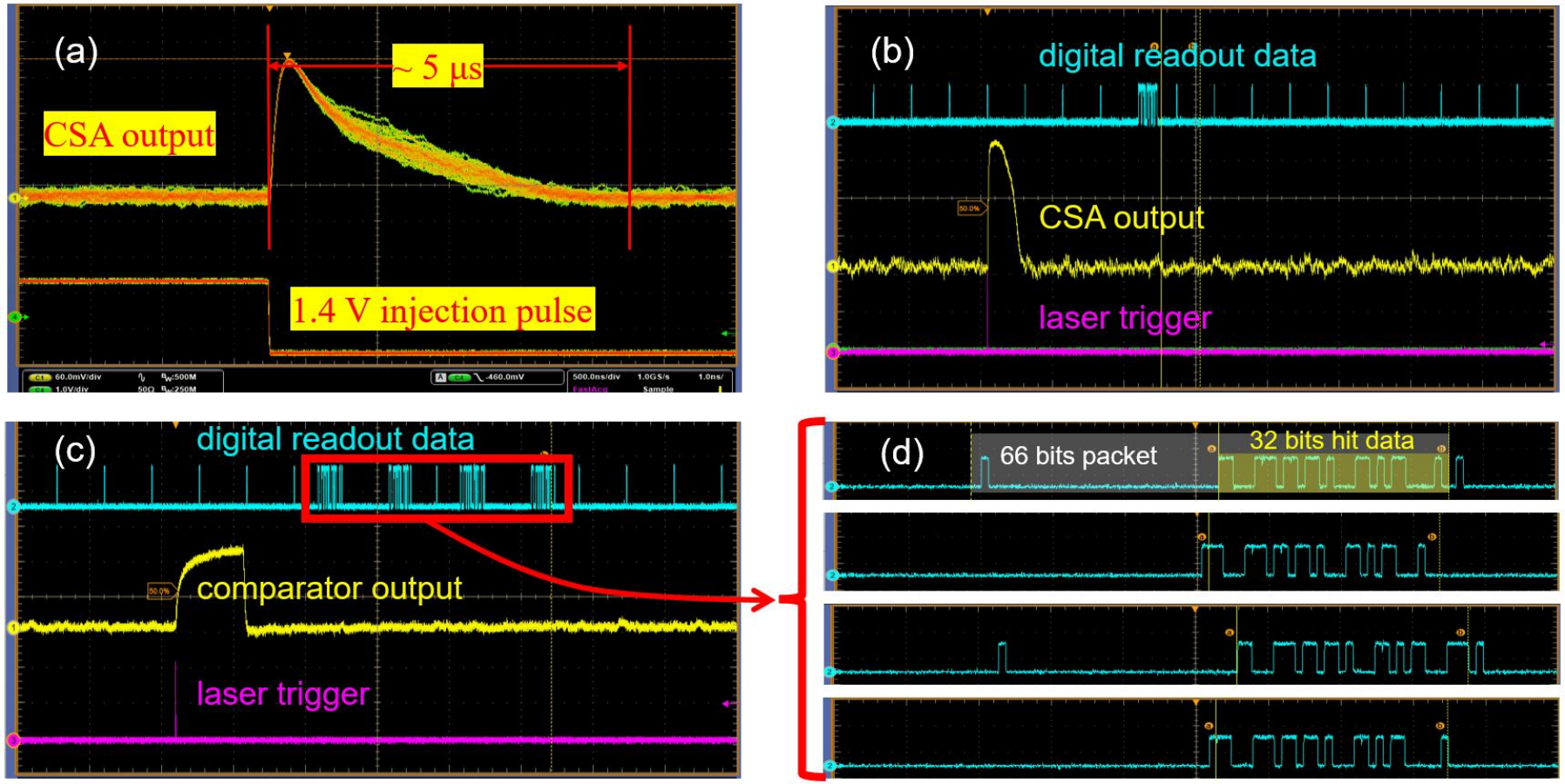
☐ 16x frequency multiplication of input 40 MHz clock.



Full chain readout functionalities

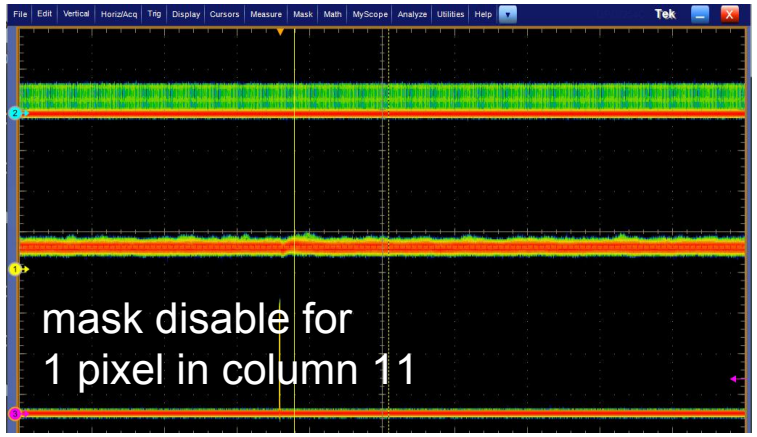
- Every pixel (12 × 32) has its 4-bit register functioning as mask (1 bit) & tunning DAC (3 bits)
- Tunning DAC (TDAC) will affect comparator response threshold of single pixel for ~12.5 mV / step.

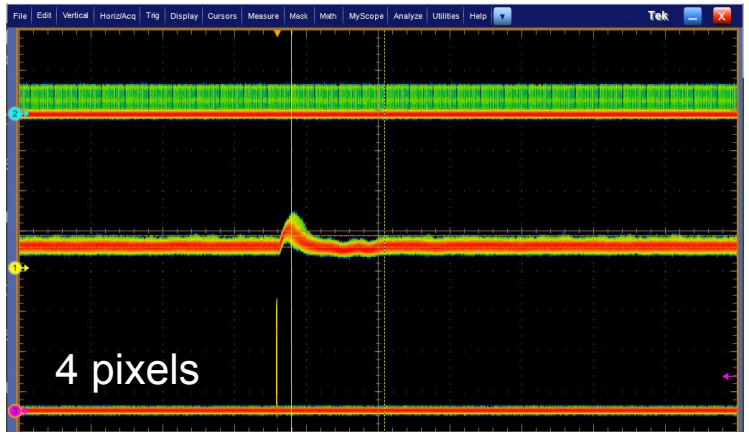
☐ CSA and comparator output of single pixel, and multi-pixel readout.

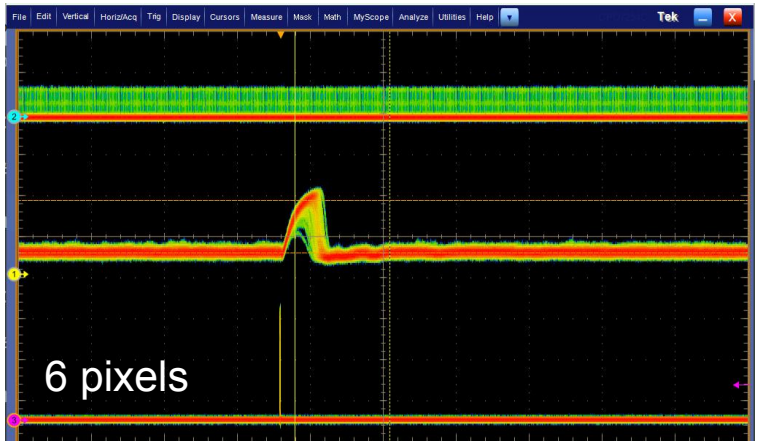


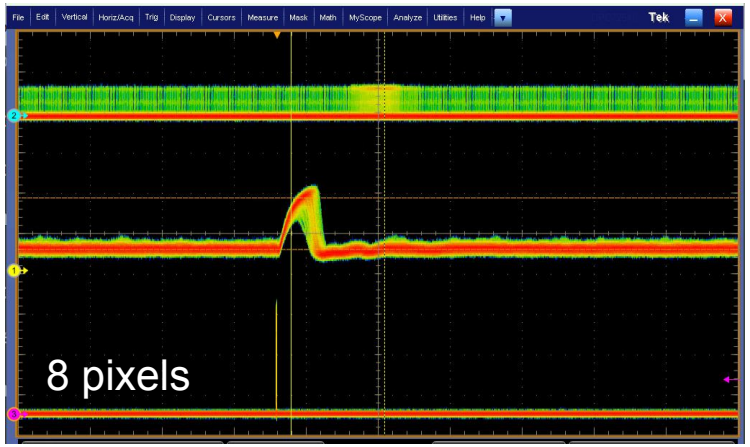
Full chain readout functionalities

- However, inter-pixel crosstalk over a same column is significant.
  - Comparator output of pixel at column 11 row 0 when:





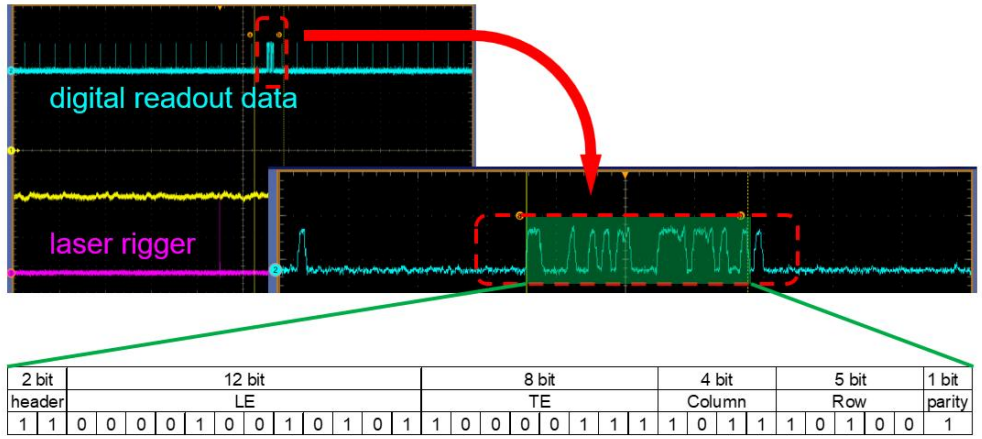




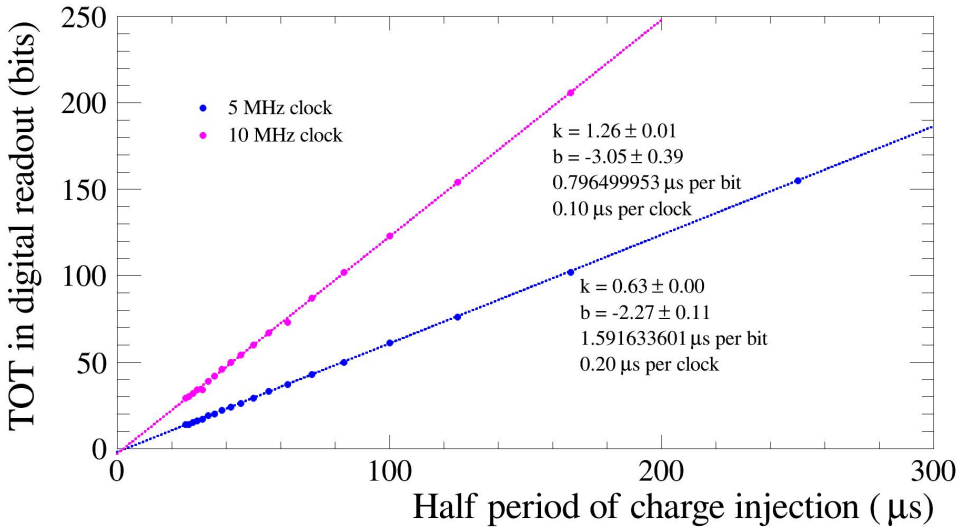
Full chain readout functionalities

☐ Data-taking:

- **Good news**: Exclusive readout (address, TOT) for any single pixel is correct.
  - ➢ Data of column and row are consistent with laser position & mask.
  - ➢ Time unit of LE and TE is 8 times of main clock period as designed.
  - ➢ TOT = 8 × main clock period × (TE – LE) consistent with external charge injection period.



- column = 0b1011 = 11, row = 0b10100 = 20
- TE = 0b000110000111
- LE = 0b000010010101

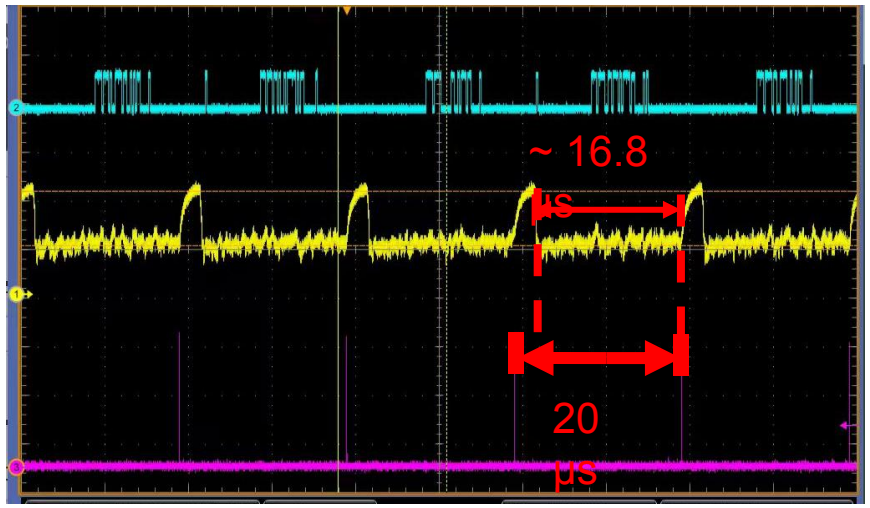


Full chain readout functionalities

☐ Data-taking:

- **Bad news**: Comparator output was flipped 3 times before it reaches EOC.
  - ➢ Single pixel readout is working

    only when Threshold = 0.6 (very low) & TDAC= 0b111 & laser zoomed on.
  - ➢ Recorded TOT is timespan of comparator low-level state rather than high-level.

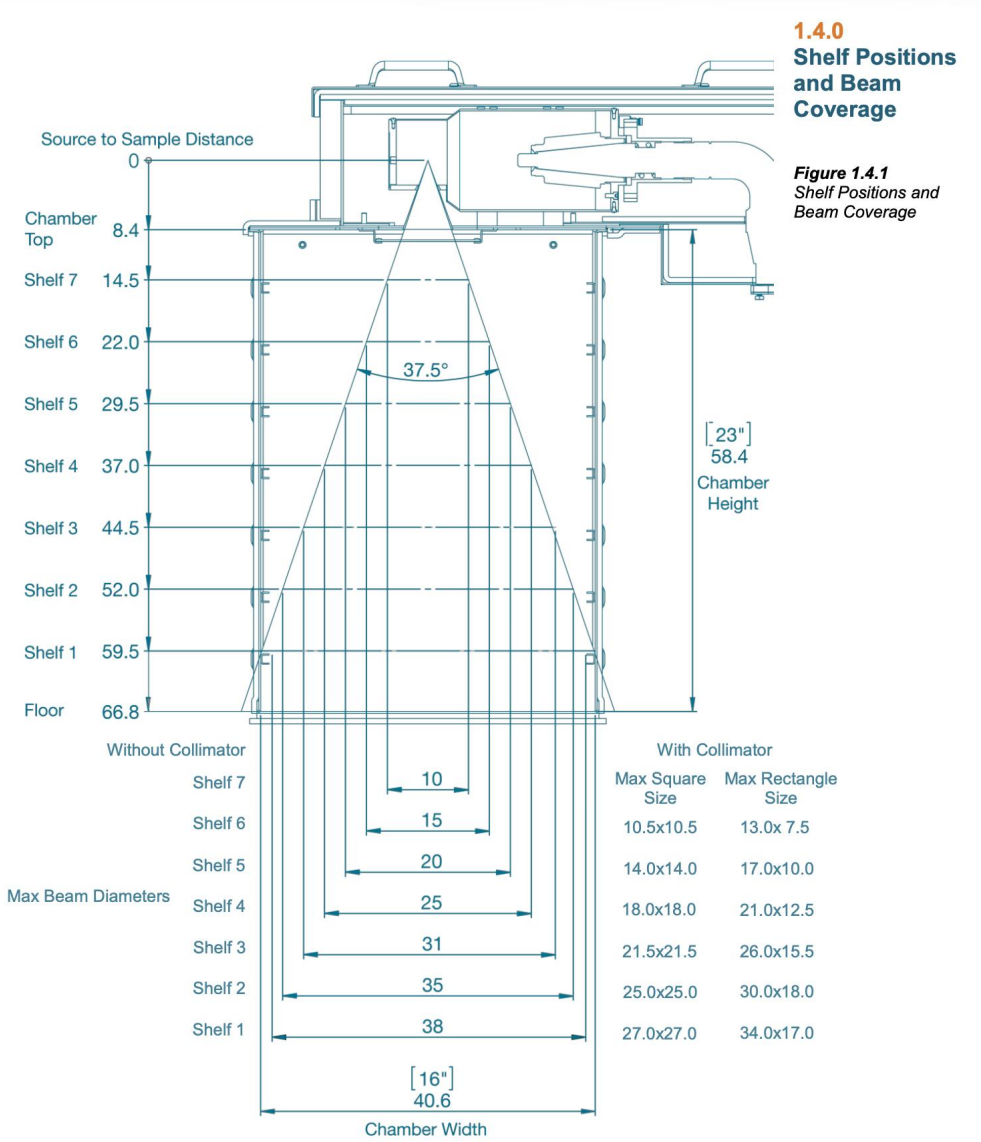


Data	LE	TE	Width	Column	Row
#11010111	238	249	11	11	0
#11010111	251	5	10	11	0
#1101100(	7	18	11	11	0
#1101100(	20	30	10	11	0
#11011001	84	95	11	11	0
#11011001	97	107	10	11	0
#11011001	109	120	11	11	0
#11011001	122	132	10	11	0
#11000001	101	111	10	11	0
#11000001	113	124	11	11	0
#11000001	126	136	10	11	0
#1100001(	138	149	11	11	0
#1100001(	151	161	10	11	0
#11000101	122	133	11	11	0
#1100011(	135	145	10	11	0
#1100011(	147	158	11	11	0
#1100011(	160	170	10	11	0
#1100111(	180	190	10	11	0
#11001111	192	203	11	11	0
#11001111	205	215	10	11	0

- Laser = 5 kHz, external clock = 5 MHz
- TDC unit = 0.2 × 8 = 1.6 µs
- TOT = (10)11 × 1.6 = (16.0)17.6 µs ≈ 16.8 µs

X-ray calibration for COFFEE3 TID experiment

X-ray calibration



- **Faxitron MultiRad 160**
  - fully shielded
  - 32 Gy/min with 2 mm Al Filter
- **Radiation absorbed dose calibration (general)**
  - Beam quality (Half-Value Laye)
  - Fixed DUT placement plane
  - Air-kerma rate (Traceable Ionization Chamber)
  - Air Kerma to Rad (Si) conversion
  - Beam uniformity mapping
- **Calibration via silicon sensor**
  - Test conditions dependency => Relative dose
  - A known sensor performance => DUT dose

Summary

- Peripheral digital readout of the left-side array verified to be fully functional:
  - ✓ LVDS, DLL, Empty Packet, and Pixel Mask tests all passed
  - ✓ Pixel array: CSA (amplifier) and discriminator output signals are nominal
  - ✓ The left-side array exhibits clear responses to charge injection, laser test, and ^{55}Fe X-rays
- Segments on right-side are working well despite some hanging issues
  - ✓ IV, CV performance of passive diodes are confirmed.
  - ✓ PLL output is in agreement with design.
  - ✓ Pixel sensors give correct CSA and comparator output, as well as serailizer.
- Verified that the ZCU102 + CaR Board operates correctly via the FMC flex cable
  - ✓ Preparing for X-ray and beam experiments