CEPC Inner Tracker development

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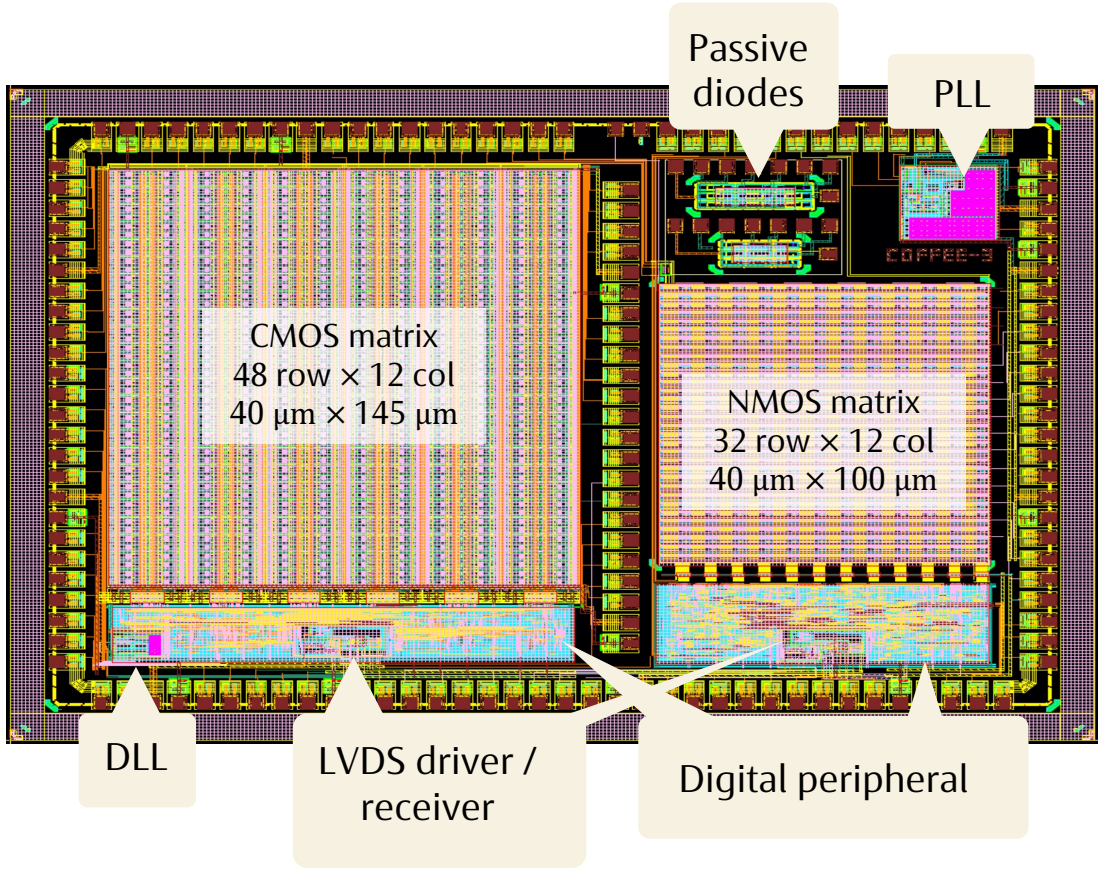
On behalf of the Inner Tracker team

CEPC Physics & Detector meeting, 18th Mar 2026

Contents

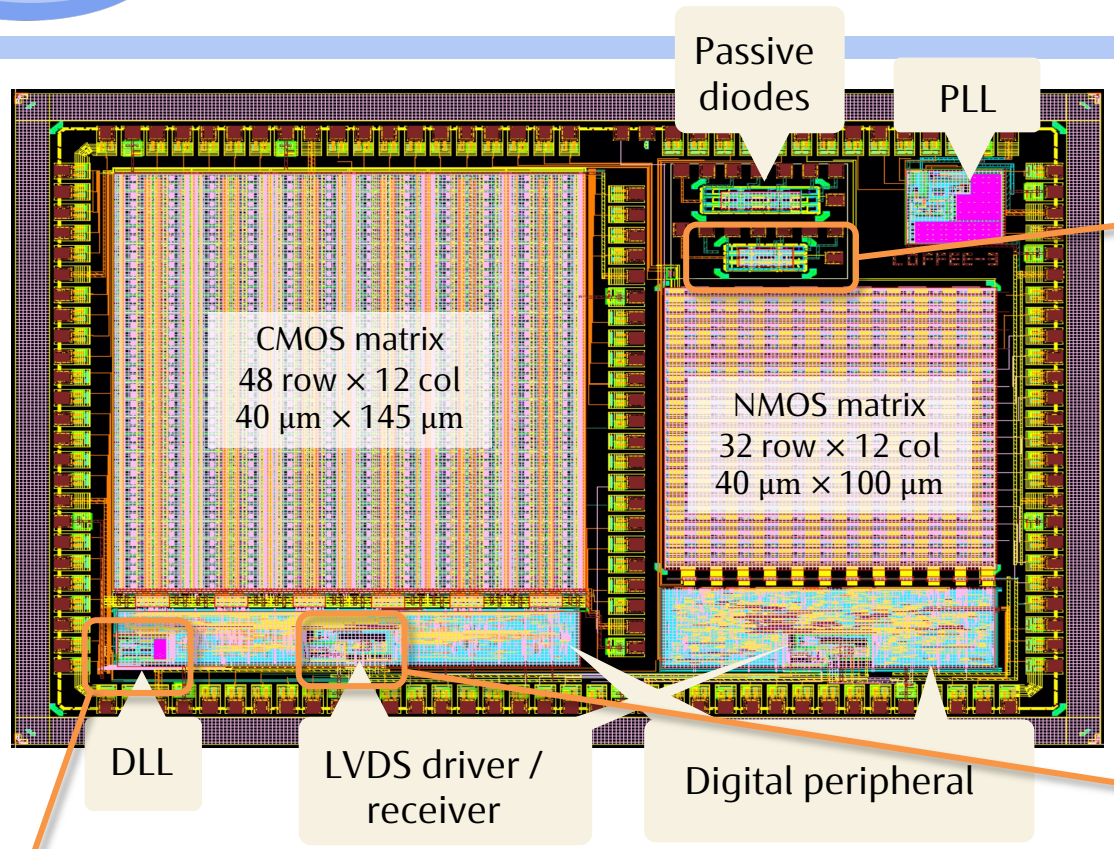
- Sensor development
  - COFFEE3 test progress
  - CHiR with modified process
- Module prototyping
  - New ideas towards low-material system
  - Serial powering
  - Wireless transmission

COFFEE3

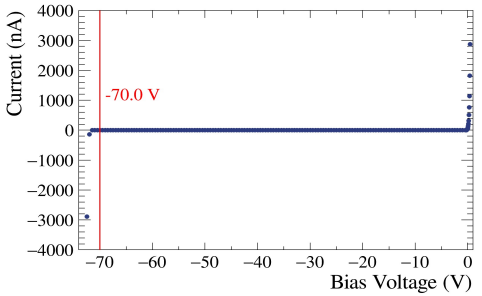


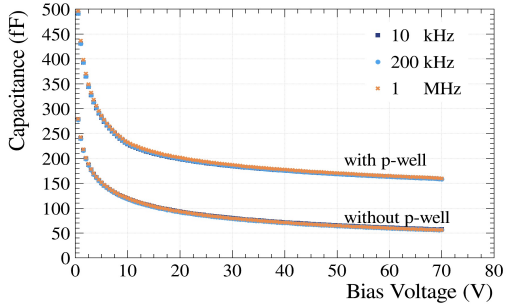
- Prototype developed in 55nm HVCMOS process
  - 4 mm x 3 mm
  - Passive diodes for sensor study
  - 'CMOS matrix': digital TDC in pixel
  - 'NMOS matrix': limited design flexibility yet no crosstalk using 3-well process
  - IP validations: PLL, DLL, LVDS driver/ receivers …

COFFEE3



Passive diodes



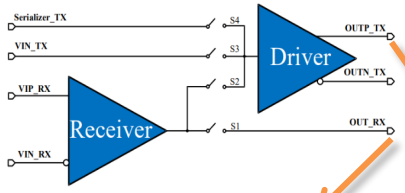


IV:
breakdown at -70V, expected for low-res (10 Ω·cm) wafer

CV:
- Single pixel C ~ 50fF at -70V
- Higher with circuits (+ p-well)

DLL

Input clock (320 MHz) successfully delayed by 6 phases to achieve finer timing

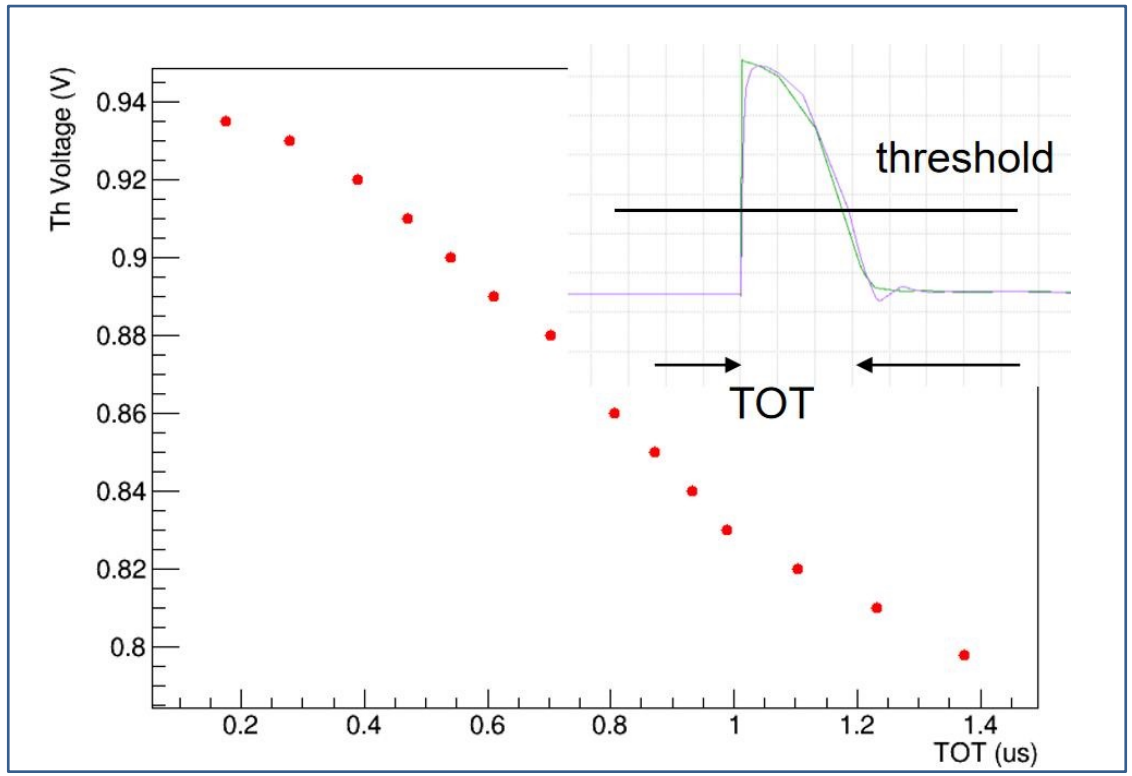


LVDS

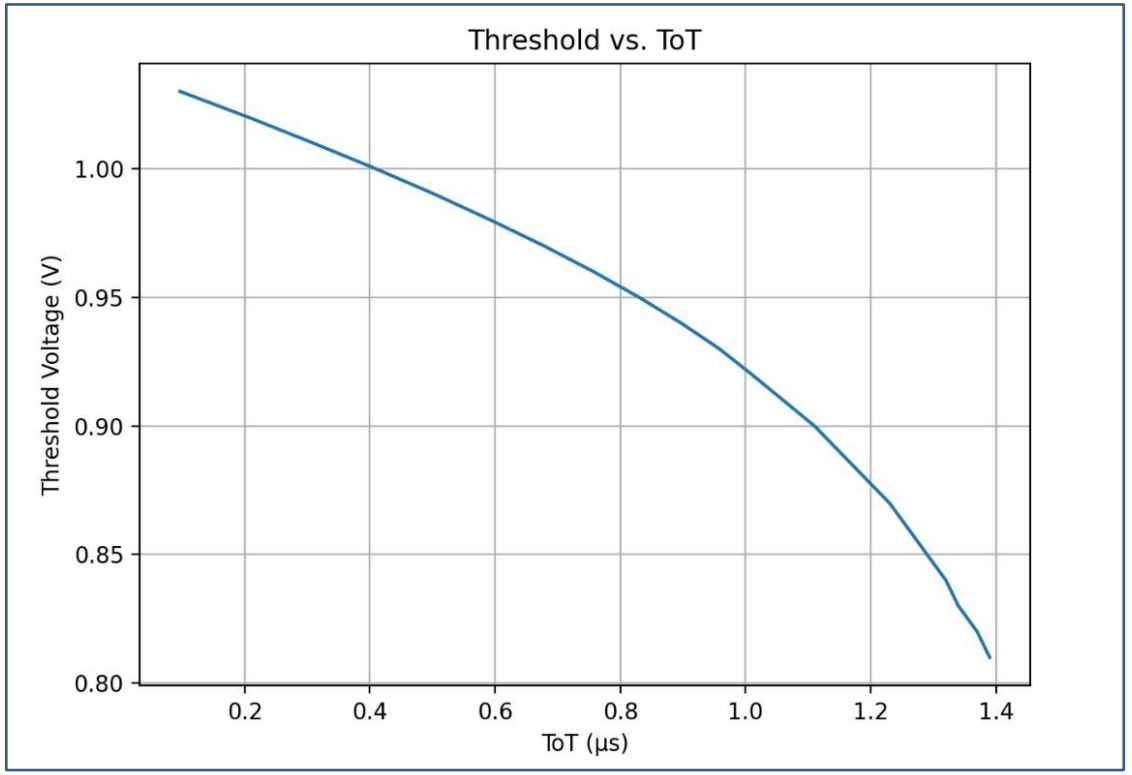
Both driver & receivers function well with 640 MHz clock

COFFEE3 'CMOS array'

- Laser on single pixel:
  - threshold scan of TOT values consistent with simulation



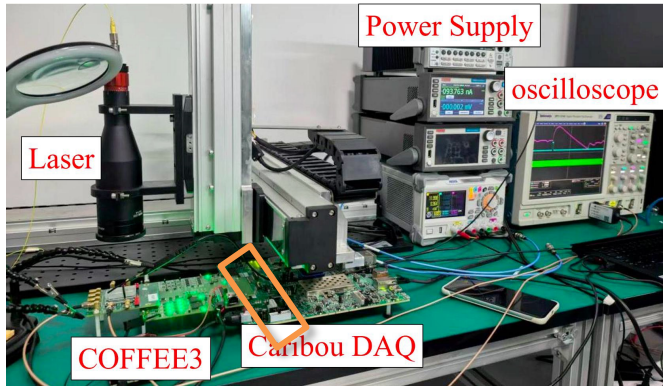
Test



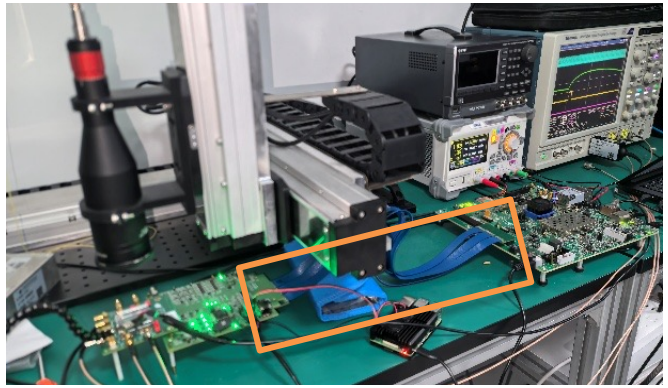
Simulation

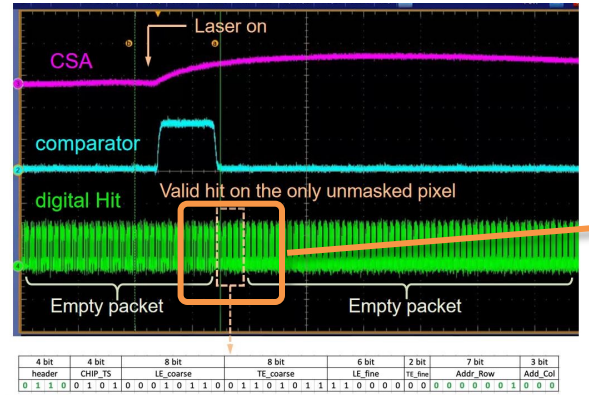
COFFEE3 'CMOS array'

- Readout chain of a single pixel successfully demonstrated using laser
- Setup updated and the results can be reproduced



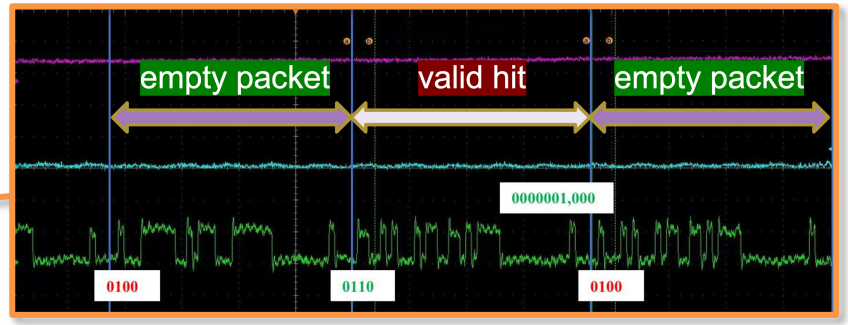
Car – FPGA connection replaced by FMC flex cable facilitating testbeams

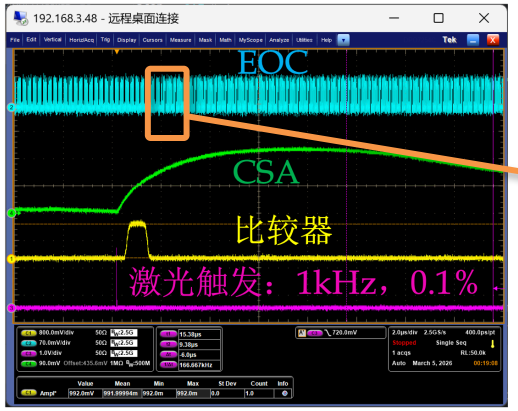




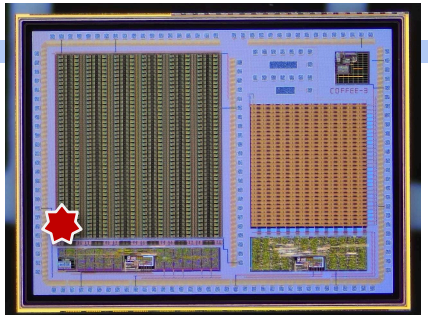
A valid transmission packet corresponding to a hit

Correct row & column address

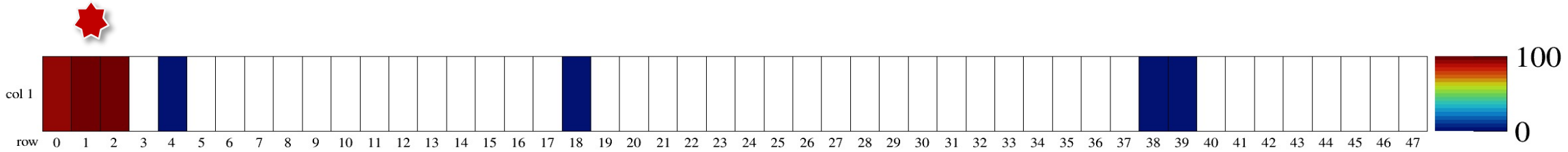




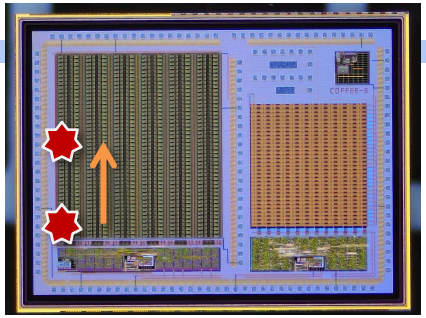
COFFEE3 'CMOS array'



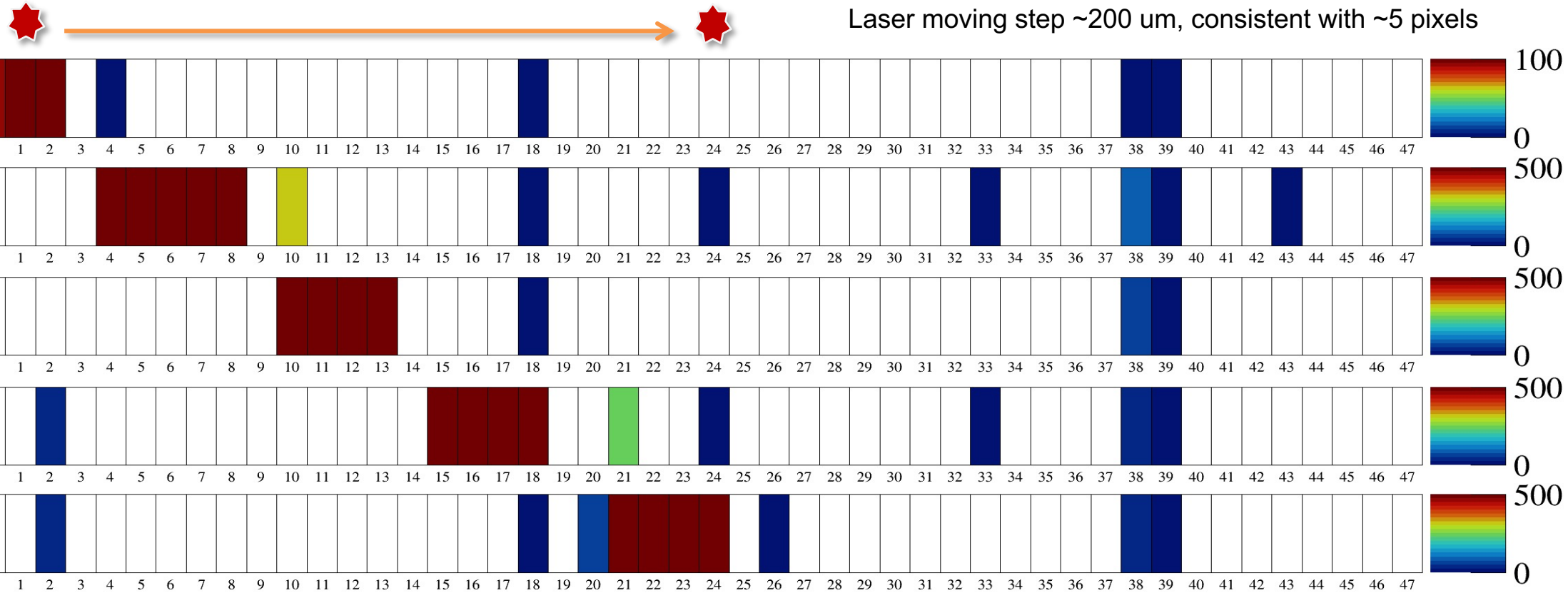
- Readout of a full column successful



COFFEE3 'CMOS array'

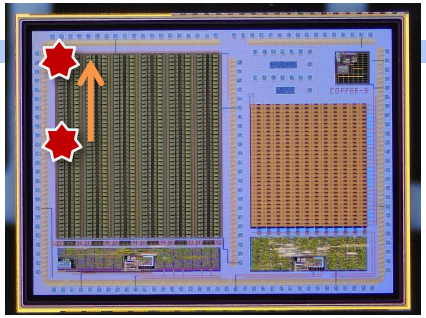


- Readout of a full column successful
- Clear response to a laser spot moving along the column



CAI Yuman, WANG Boxin, LIU Kang, LY, XU Zijun

COFFEE3 'CMOS array'



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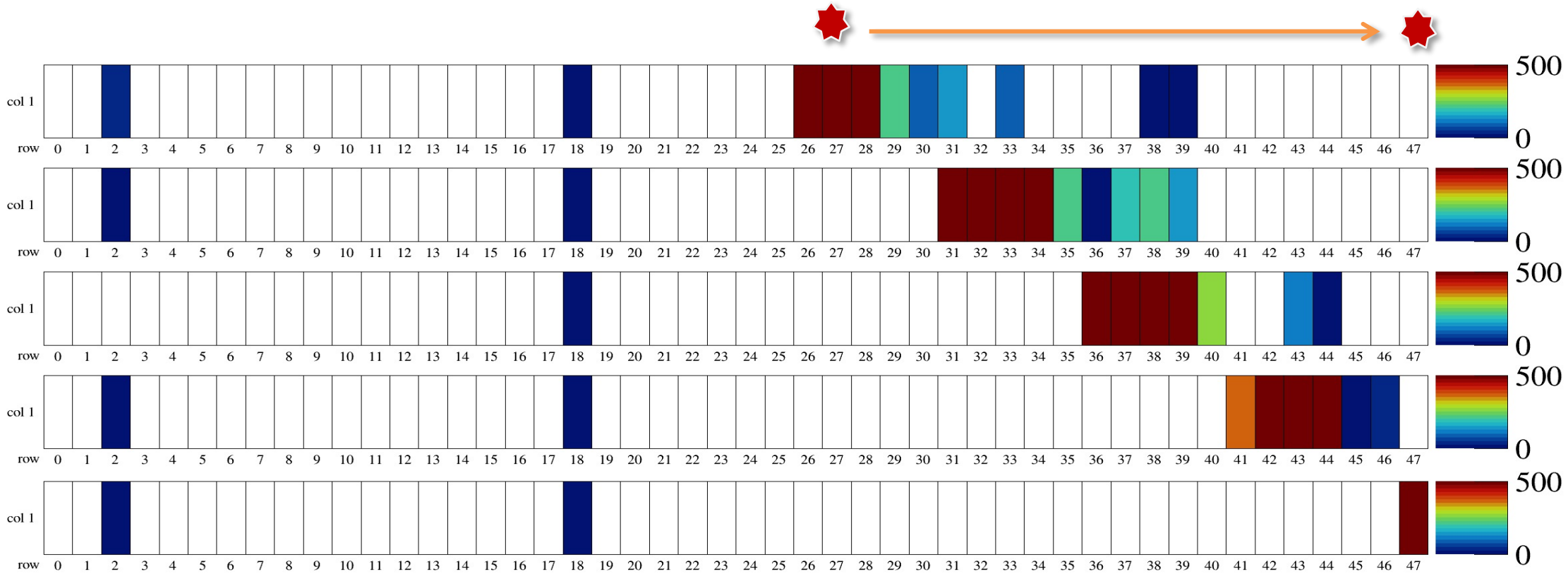
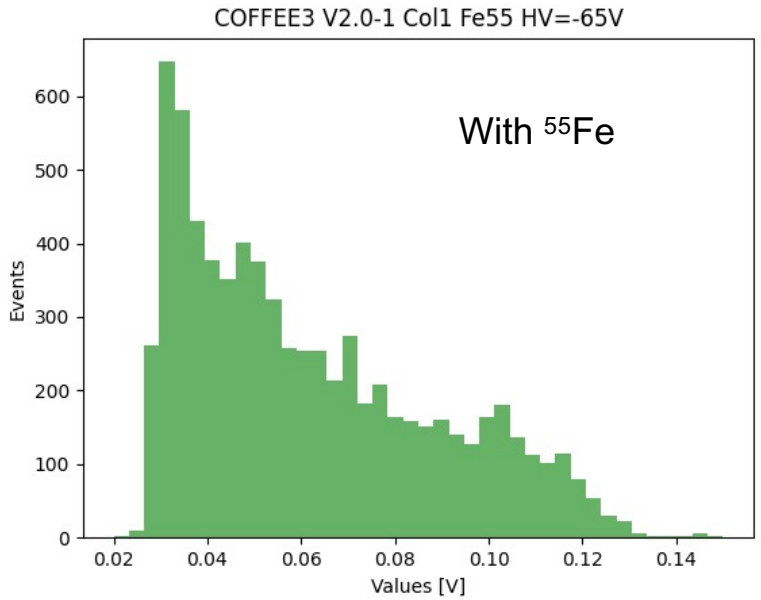
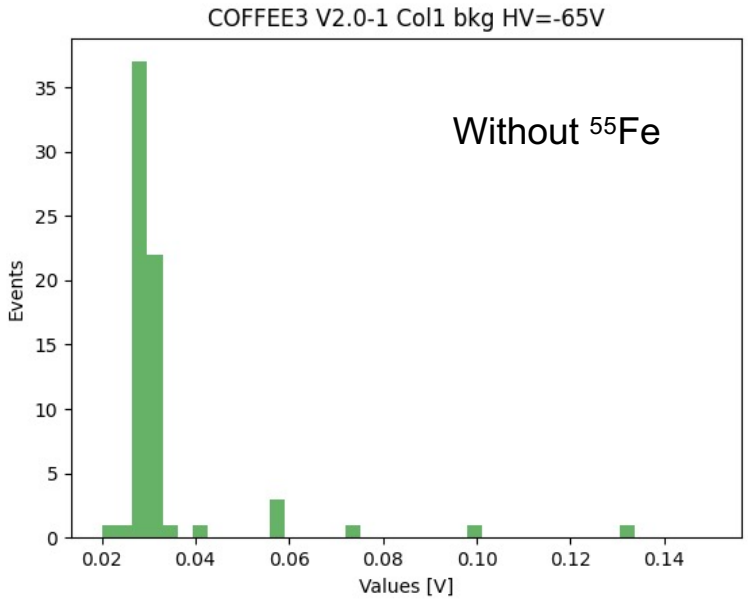


CAI Yuman, WANG Boxin, LIU Kang, LY, XU Zijun

^{55}Fe test

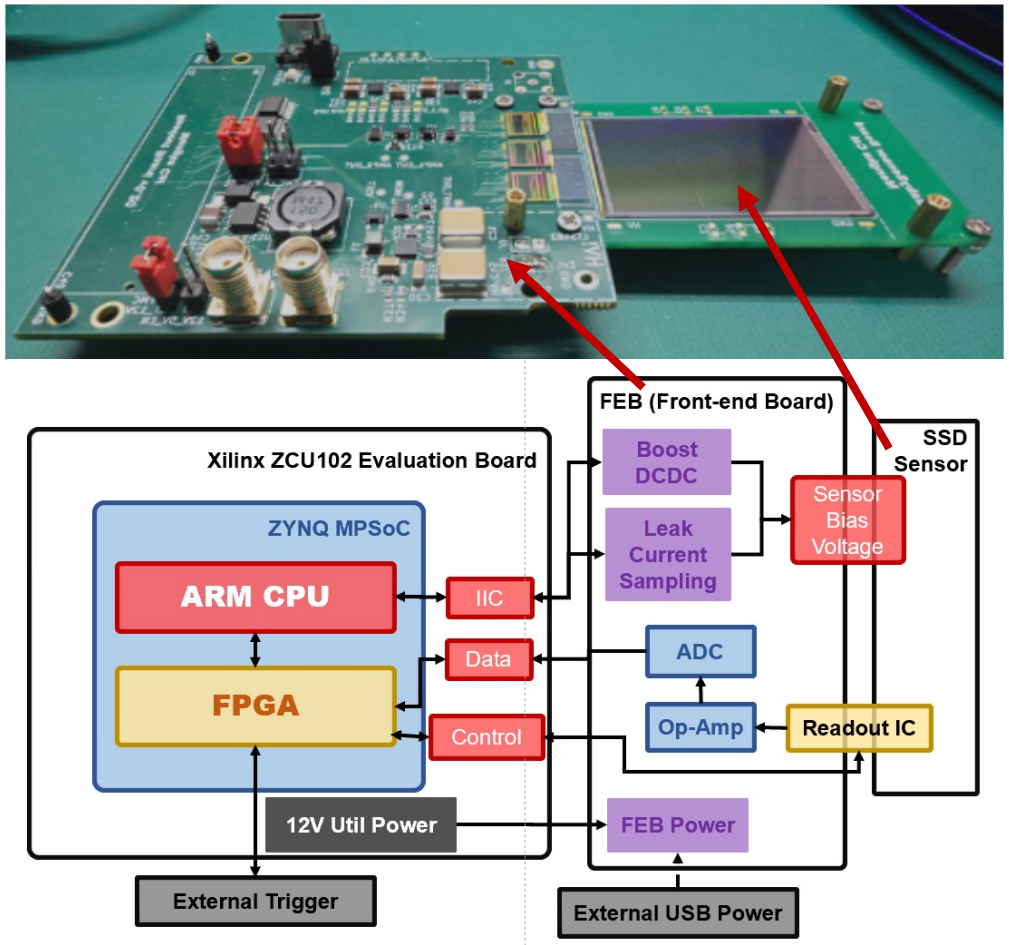
- Single pixel response to ^{55}Fe sources observed
- Noise is large
  - Consistent with low-resistivity wafer (and shallow depletion)
  - Pedestal position determined by Oscilloscope trigger; could improve with full DAQ





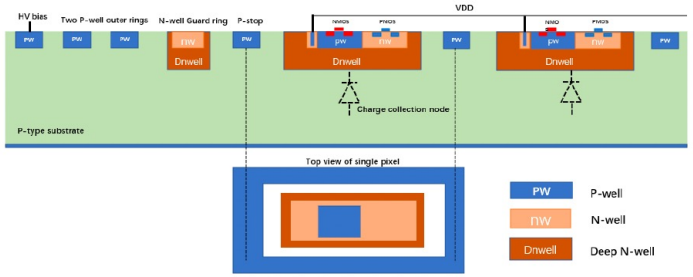
Test plans

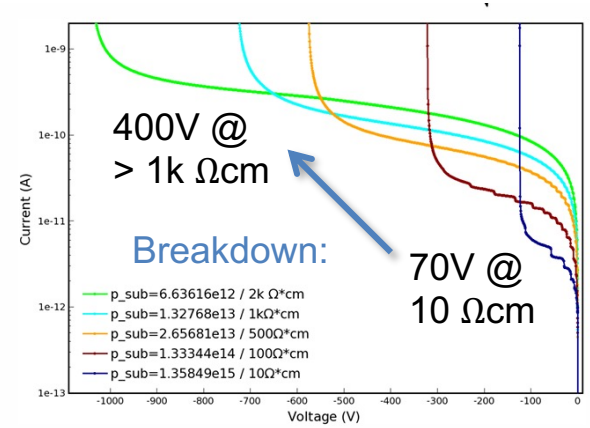
- Working towards full array
  - Threshold tuning (using TDAC) needed for a uniform response
  - DAQ firmware under development
- Potential beamtest being planned
  - Possible slot in May or July
  - Beam monitor / tracking layer based on silicon strip sensors being developed

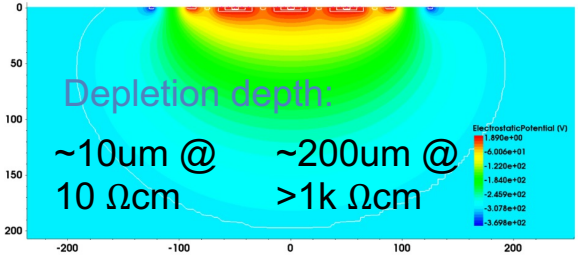


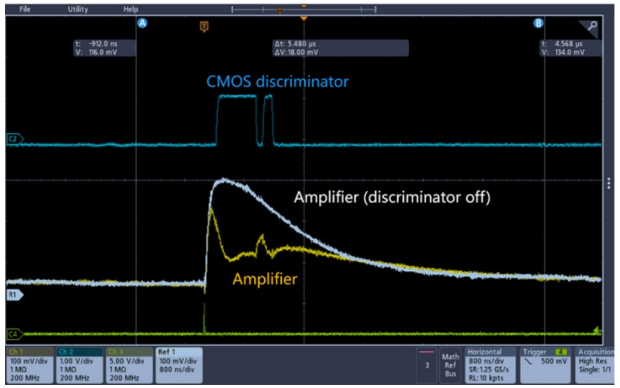
Limitation of current process

- Limitation of previous foundry:
  - No access of high-resistivity wafers
    - Small depletion, large capacitance, low S/N ratio
  - Triple-well process → cross-talk between sensor (deep-n) and PMOS circuit





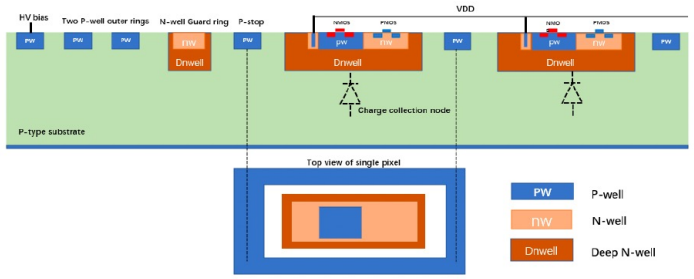


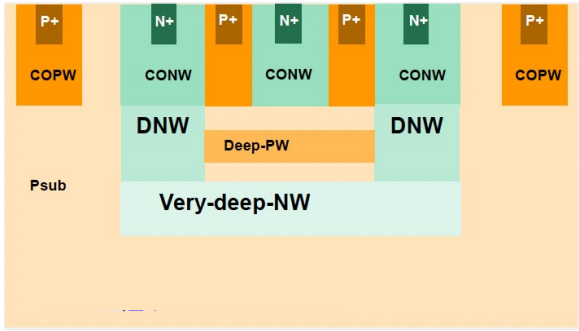


Crosstalk betw sensor &
digital circuit @ COFFEE2

COFFEE status: CHiR chip submitted

- Limitation of previous foundry:
  - No access of high-resistivity wafers
  - Triple-well process → cross-talk between sensor (deep-n) and PMOS circuit
- Agreement with a new foundry to carry on R&D
- First MPW submitted in early January 2026
- CHiR (COFFEE-HiRes) design goal
  - Priority: to validate the process with high-res wafers
    - 1k/2k/4k Ohm cm wafers available from two manufactures
  - Radiation effects of simple components (eg. MOS) with or w/o radiation hardening
  - Implementation of “Five-well process”: to validate basic IP not affected by process modification

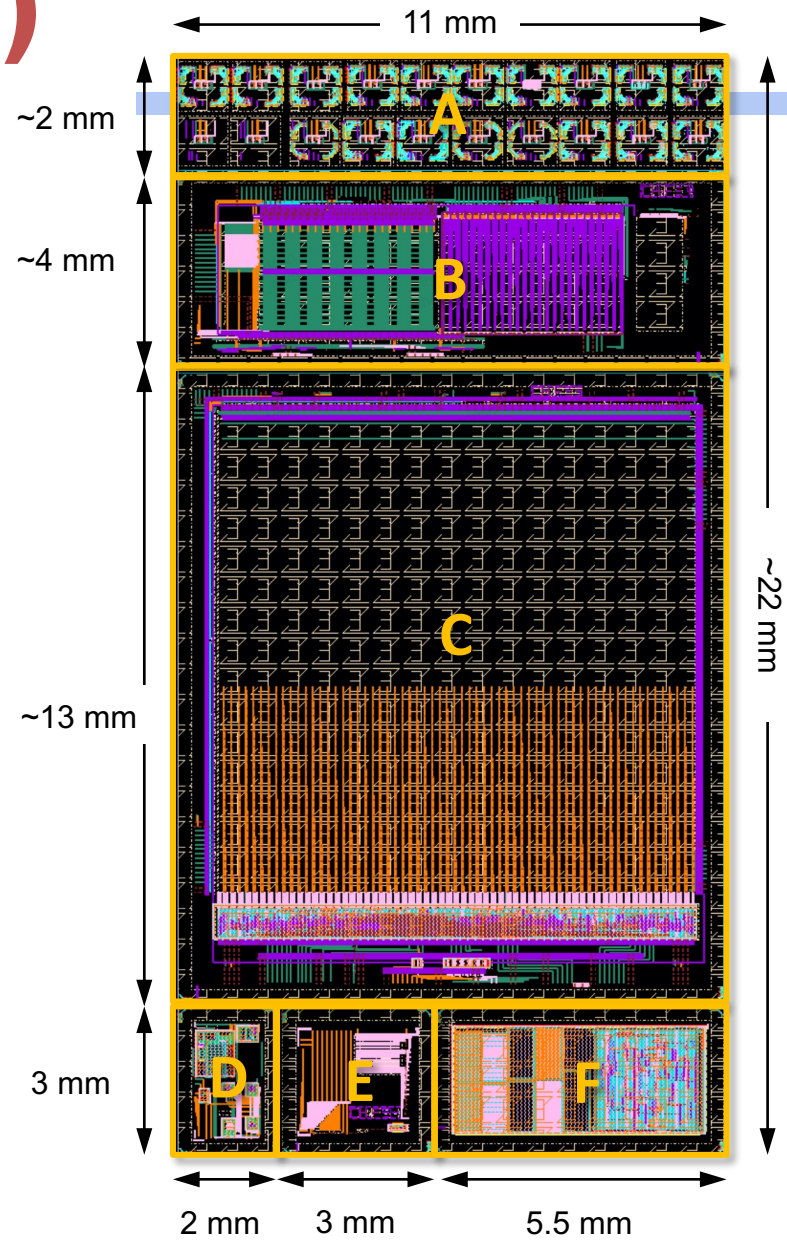




CHiR chip(s)

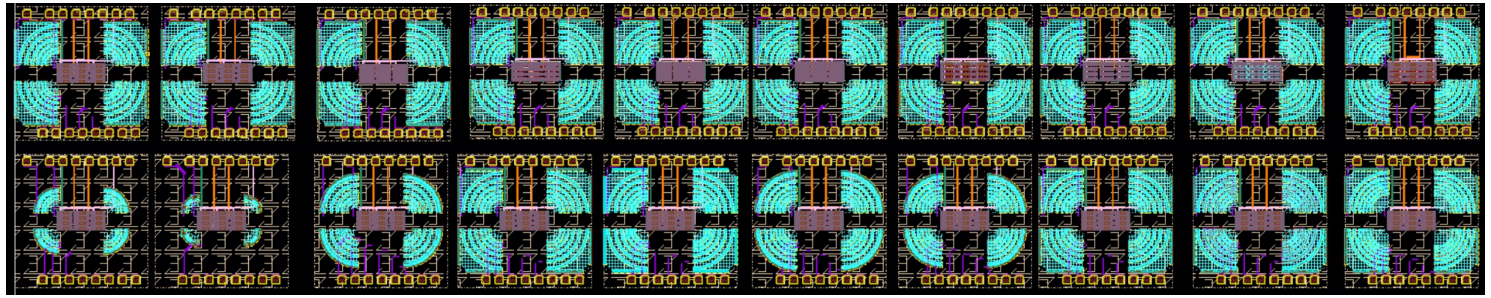
- Can be diced into a number of chips serving various goals
- Passive sensor validation:
  - (A) 20 arrays of 3x4 passive pixels with diff guard ring designs, each can be diced into individual 1x1 mm^2 chip
  - Pixel size: 38 um x 175 um
- Pixel array design
  - (B) 9 variations of in-pixel frontend designs
  - (C) main pixel array of 256 x 64 pixels; similar as COFFEE3 with readout data format compatible with 32-bit UP spec
- IP validations
  - (D) necessary analog Ips: PLL, DLL, LVDS transceivers …
  - (E) alternative small pixel arrays
  - (F) digital modules and transistors for TID and SEE studies

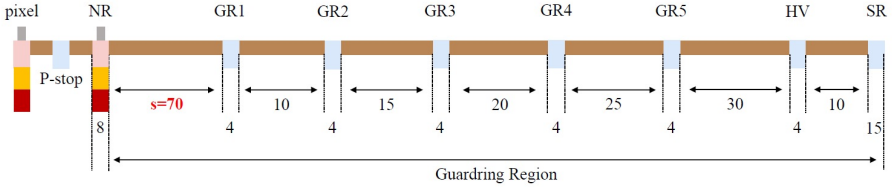
Details in ZHOU Yang's report at 3rd Feb CEPC Inner Tracker meeting



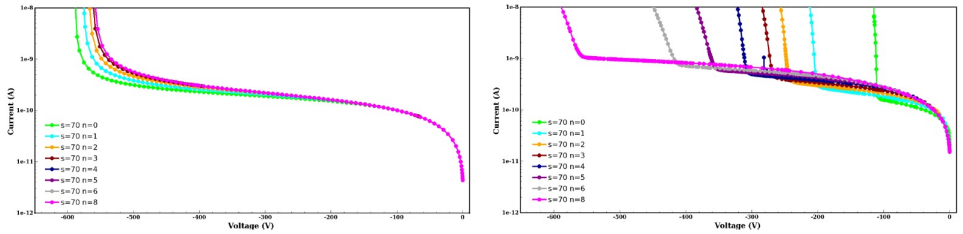
CHiR chip(s)

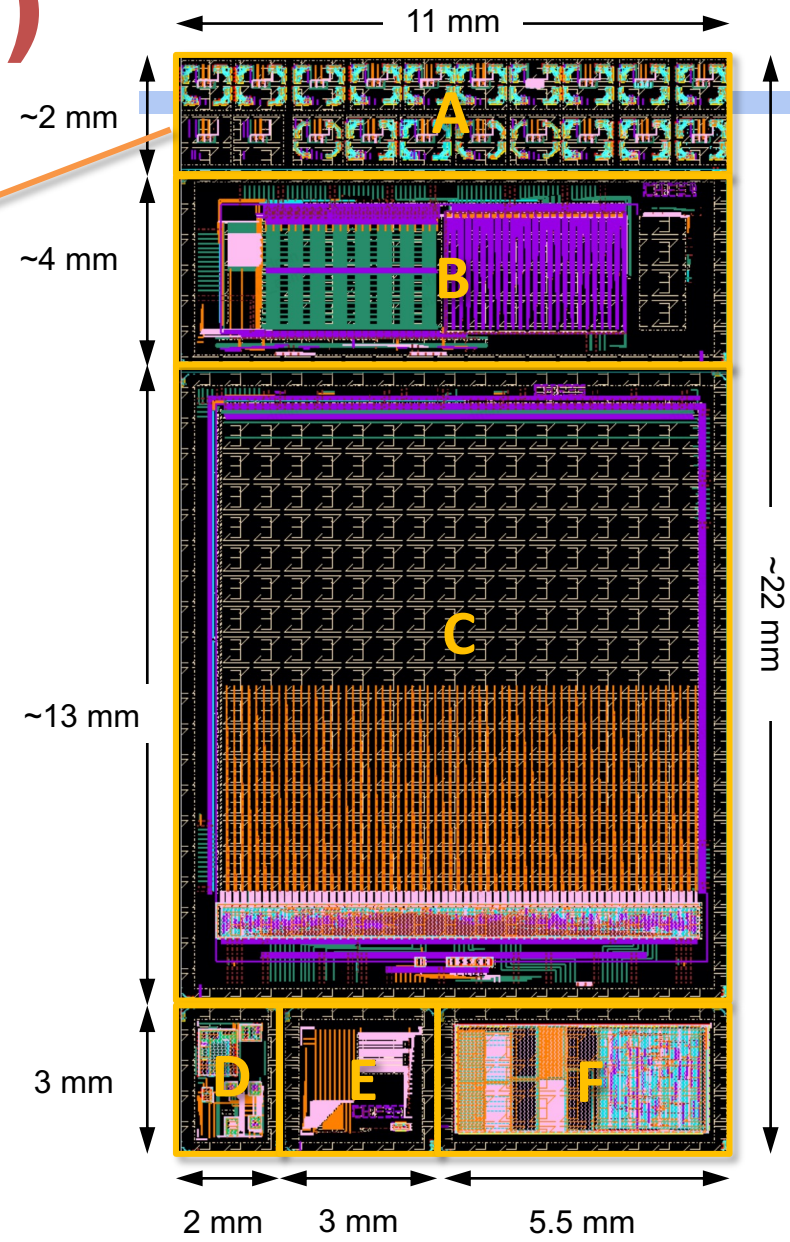
- (A) Guard rings and passive sensors





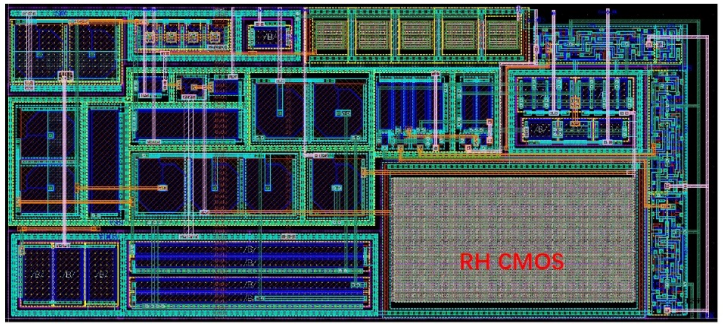
Improve the breakdown voltage before and after irradiation

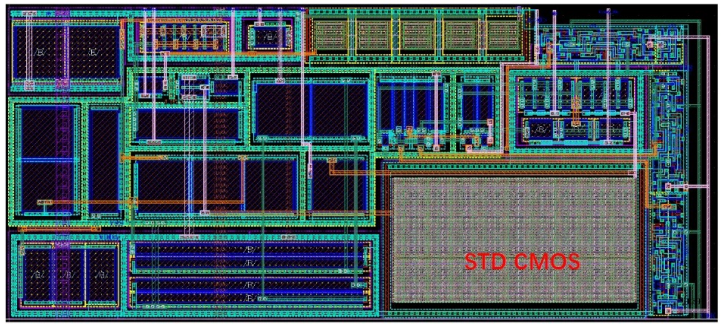


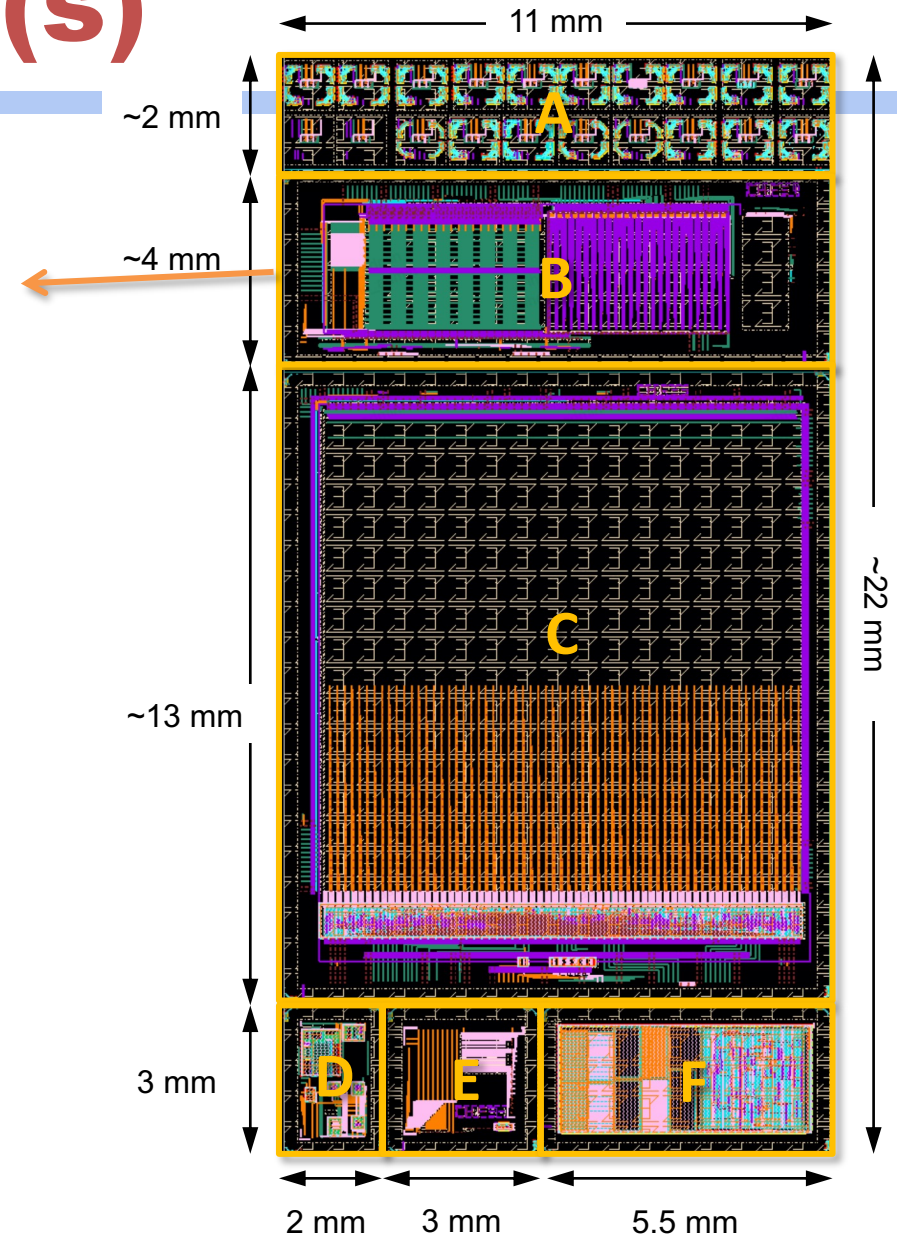


CHiR chip(s)

- (B) Pixel FE design verification
  - 9 variations of in-pixel frontend designs
  - From no ELT to all-ELT protected

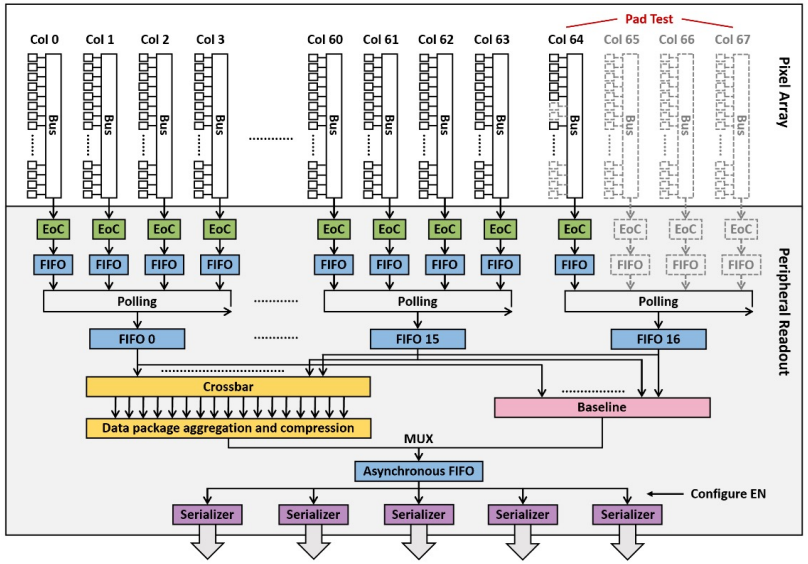


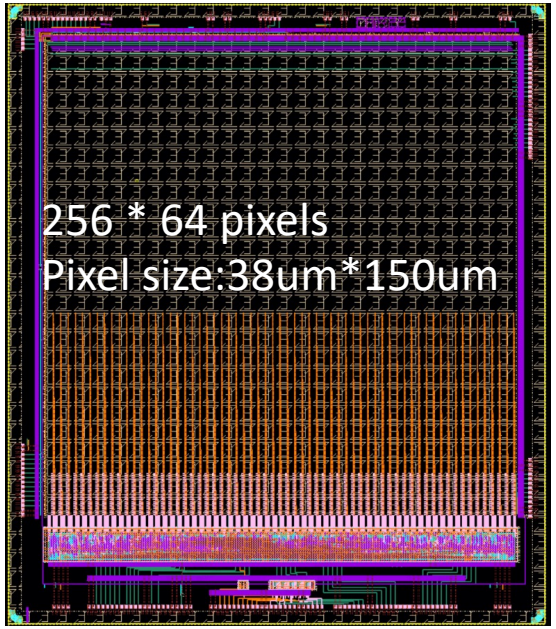


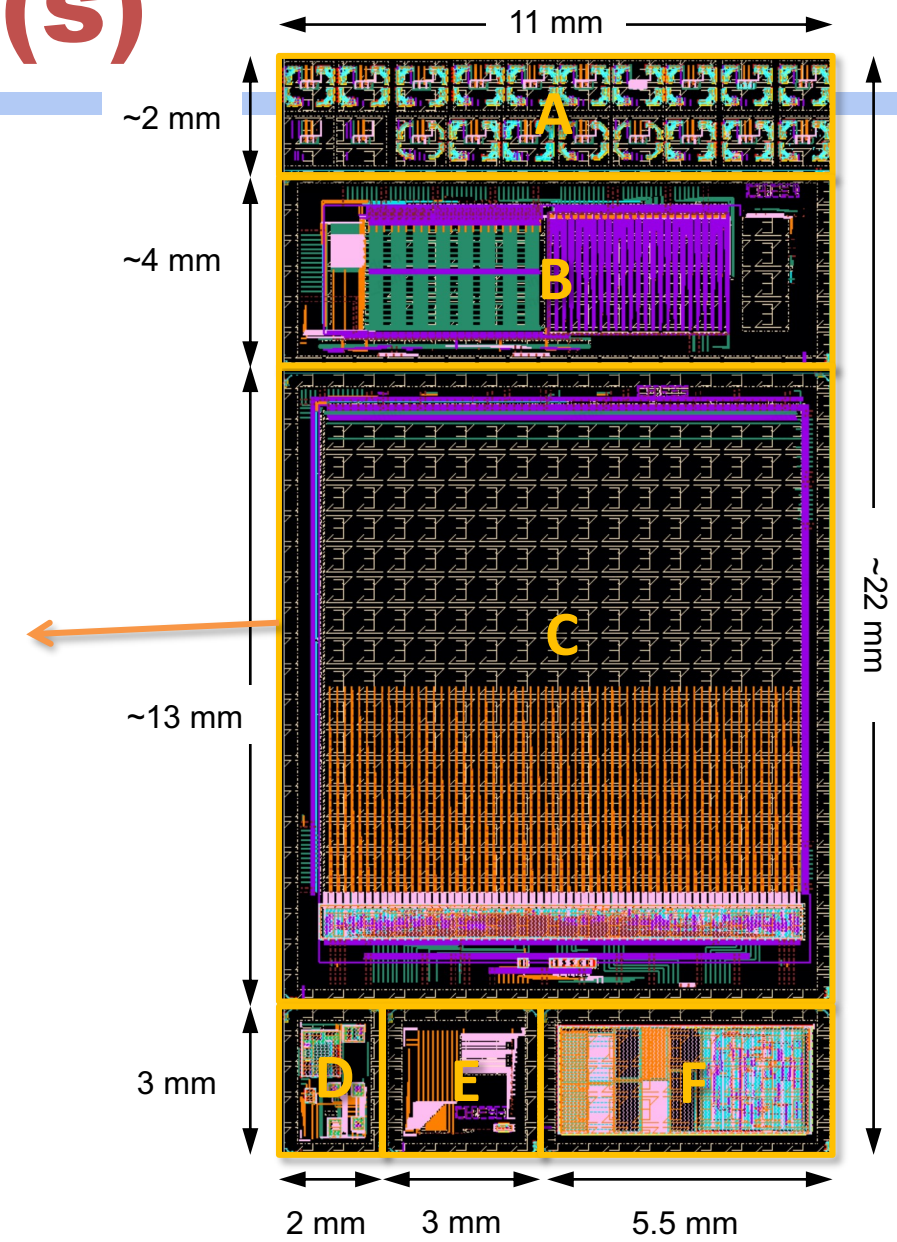


CHiR chip(s)

- (C) Large-size array verification
  - Full functional pixel, config mode: mask, pulse injection, sensor, in-pixel DAC…..







ZHOU Yang, WEI Xiaomin, LI Leyi, + many others

COFFEE timeline

COFFEE

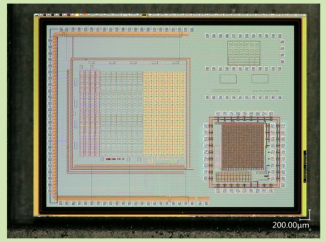
CMOS SENSOR IN FIFTY-FIVE NM PROCESS

NIM A1069 (2024) 169905
JINST 20 (2025) C10011

COFFEE 2

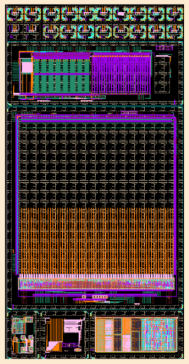
First HVCMOS 55nm prototype chip

- Breakdown at -70V
- Responsive to laser, X-/beta-ray sources



CHiR (COFFEE-HiRes)

- Validation of process modification
- Key design feature



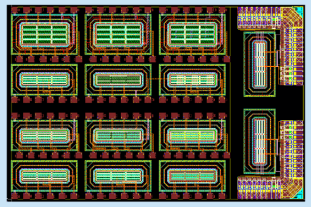
Quarter-size chip submission

… | 2022 | 2023 | 2024 | 2025 | 2026 | 2027

Submission timeline

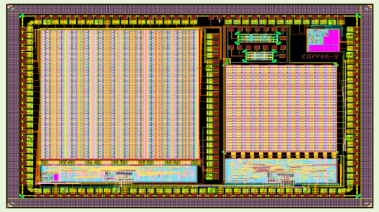
COFFEE1

- Prototype in LL process
- Validation of deep N-well structure



COFFEE3

- Two pixel arrays with data-driven readout
- Designed for good timing resolution and moderate power consumption



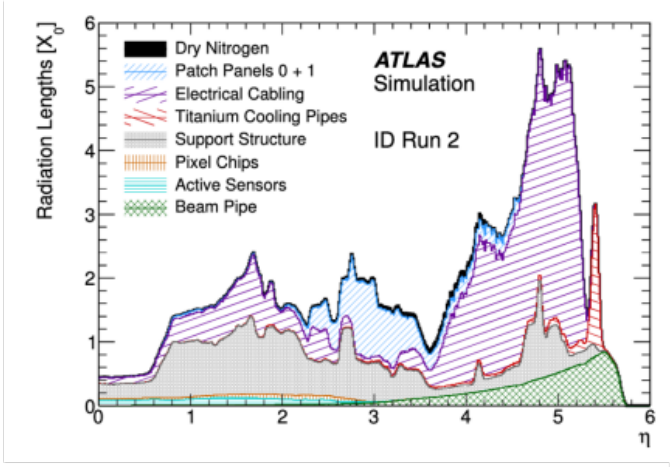
Large prototype planned ~end 2027

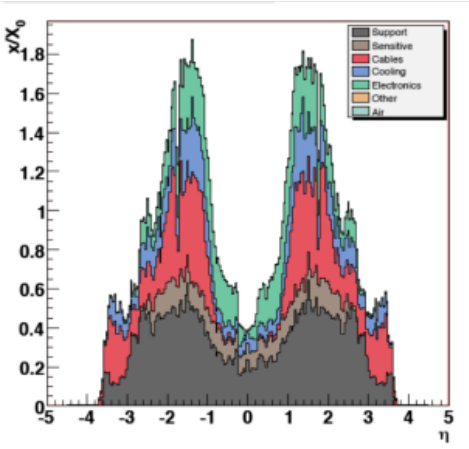
COFFEE team

Leyi Li, Xiaoxu ZHANG, XiaoMin WEI, Weiguo LU, Pengxu LI, Mei ZHAO, Yang ZHOU, Bingchen Yan, Anqi WANG, Yuanhong JIAO, Yang CHEN，Yujie WANG, Huimin Wu, Zexuan ZHAO, Yu ZHAO, Zheng Wei, Jianpeng DENG, Zhan SHI, Kunyu XIE, Xinhao XIE, Xiaolong WANG, Ziying ZHANG, He HUANG, Junyuan YAN, Shenyao TANG, Hui ZHANG, Ruoshi DONG, Yang CHEN, Xuekang LI，Xinyang GUO, Zhuojun CHEN, Hui ZHANG, Zhiyu XIANG, Zijun XU, Zeng CHENG, Kang LIU, Menke CAI, Boxing WANG, Yuman CAI, Mingjie FENG, Lei ZHANG, Meng WANG, Hongbo ZHU, Yiming Li, Jianchun WANG

New prototyping innitiative

- Modern silicon pixel tracking detectors: complex system with high-density interconnections, with increasingly large area and high granularity
- Cables and services become challenge
  - Material budget! → deteriorating momentum resolution
  - Space, installation complexity, possibility to repair
  - Power consumption
  - …
- Efforts to minimize material budget:
  - Sensor thinning
  - Low-material PCB
  - Mechanics: CF, truss, foam…
  - Cooling: water, bi-phase CO_2,…
- Time to reduce cables!



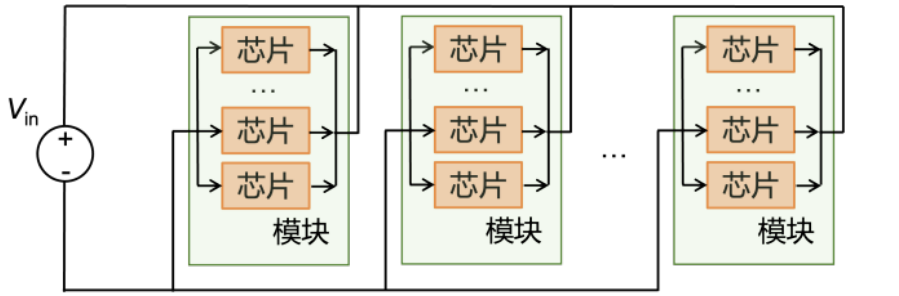


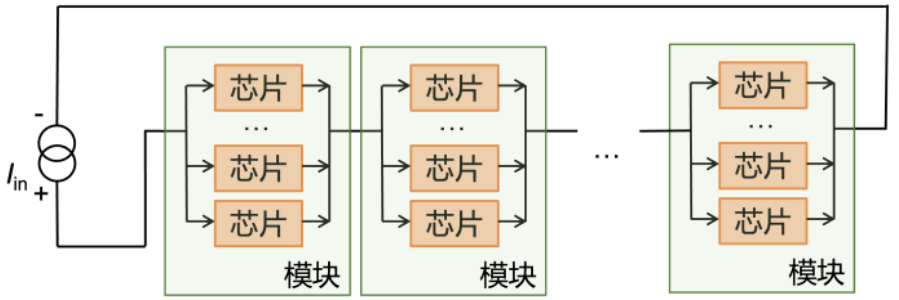
Development target

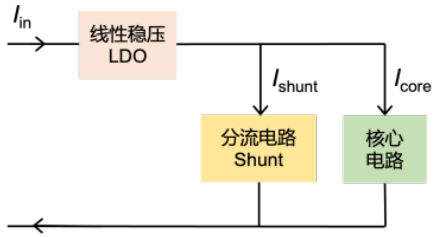
- Development of multi-module prototype for CEPC ITK (-like) system with minimum cables
- What are cables for? What are the new technology could help?
  - Power supply → Serial powering
  - Data transmission → mmWave wireless transmission
- New proposal submitted for NSFC Key project

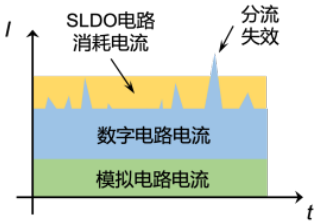
Serial powering

- As pixel size decrease by N, cables increase:
  - Parallel power (or +DCDC) by N^2
  - Serial power by N
- Adopted by ATLAS/CMS Phase II trackers
  - Hybrid pixel
- Nicely align with ongoing DRD3 project to develop demonstrator for MAPS-based tracker
  - Lead by INFN Milan + Edinburgh, regular communication at Inner Tracker meeting
- Tasks:
  - Design of SLDO for 55nm process aiming IP for integration into final chip
  - Demonstrator of multi-module tests



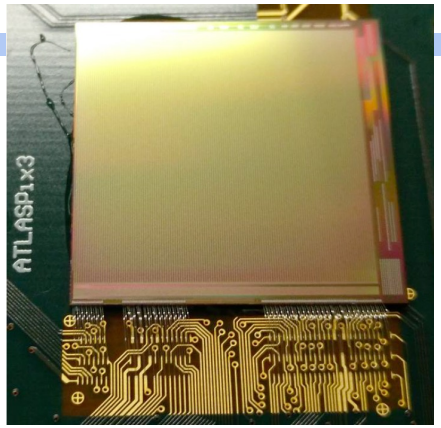


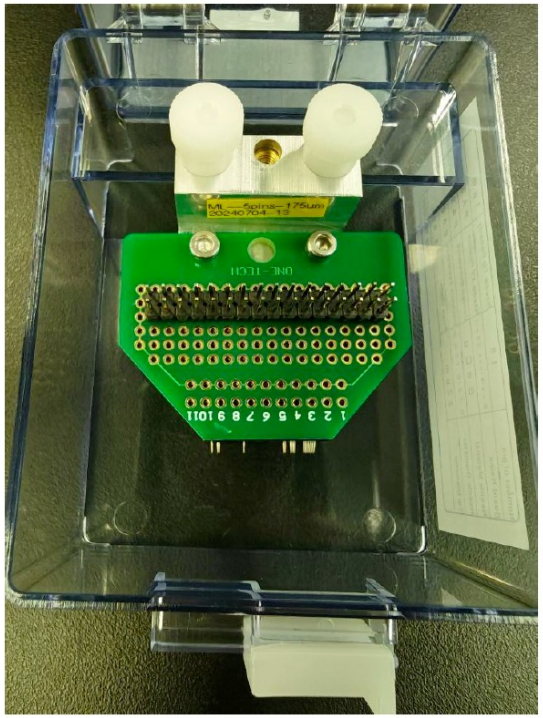


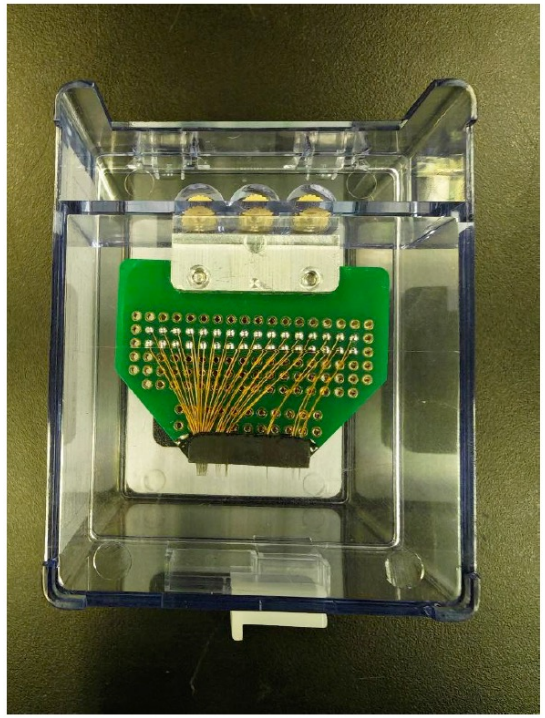


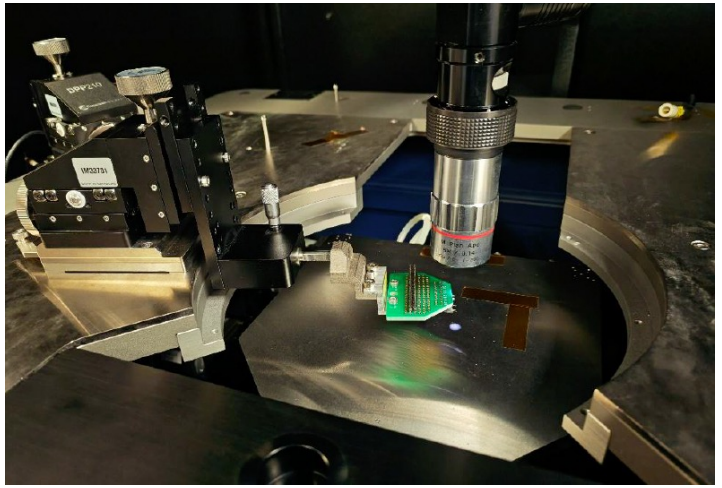
Serial powering

- Validation using ATLASPix3 chip @ IHEP started
  - Probe card designed to probe the SLDO part







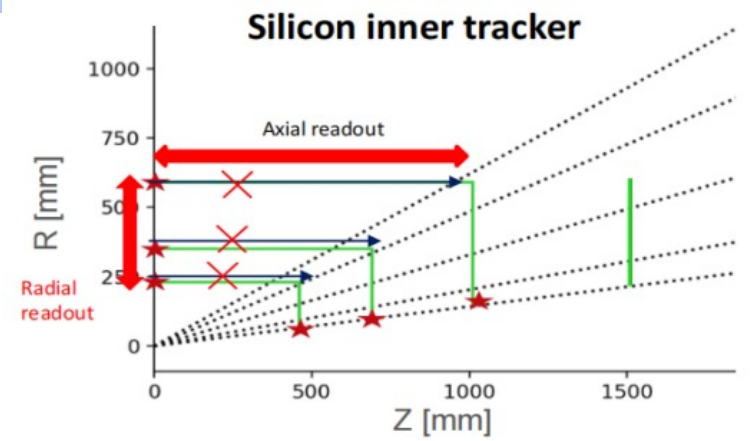


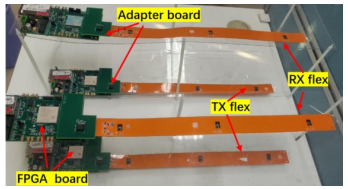
ZHANG Hui, SHI Tianyu, YUAN Xuhao, LY
With support from INFN Milan, Edinburgh, Lancaster

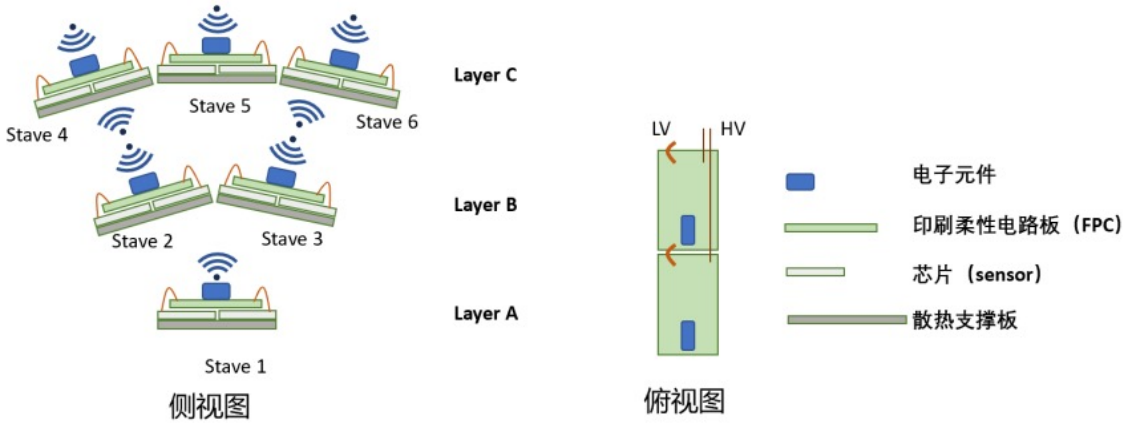
Wireless transmission

- From axial to radial readout
- Single transmission and receiving modules working for transmission ~10cm
  - See Jun's report at 3rd Feb CEPC ITK meeting
- Tasks:
  - Optimization of the antenna module
  - Multi-module demonstration
  - → to show it works in real material, with operation EM environment!

Details in HU Jun's talk at 28th Jan CEPC Day

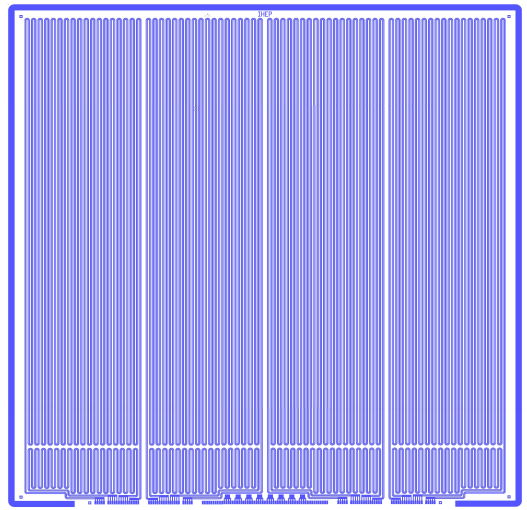






Dummy sensor preparation

- For realistic study of material budget and development of assembly procedure, dummy modules with dummy sensors + flex is the first step
- Dummy sensor in production
  - Same size as the final chip
  - With metal traces for thermal study
  - With real pads and pattern to facilitate assembly
  - Expected to be back in end April



WANG Congcong, LY, WANG Jianchun

Summary

- Tests with COFFEE3 progressing well
  - Two full columns in CMOS array working under laser, working towards full array
- CHiR chips submitted with modified process
- New prototyping efforts for low-material solutions
  - Serial powering to reduce power cable
  - Wireless transmission with realistic material budget
  - Dummy sensors produced for realistic study