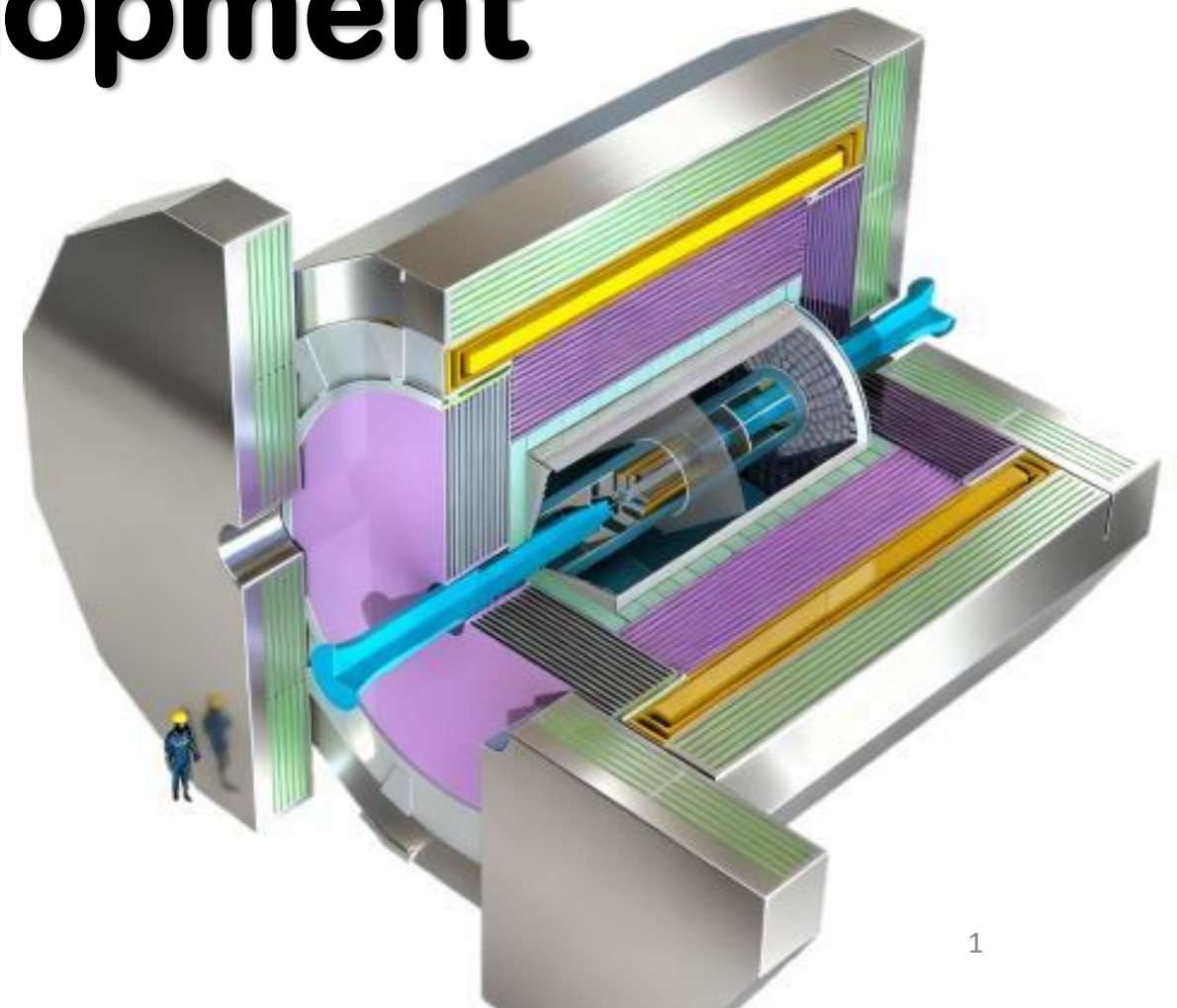
Status and plan of the overall ASIC development

Ye, Jingbo for colleagues

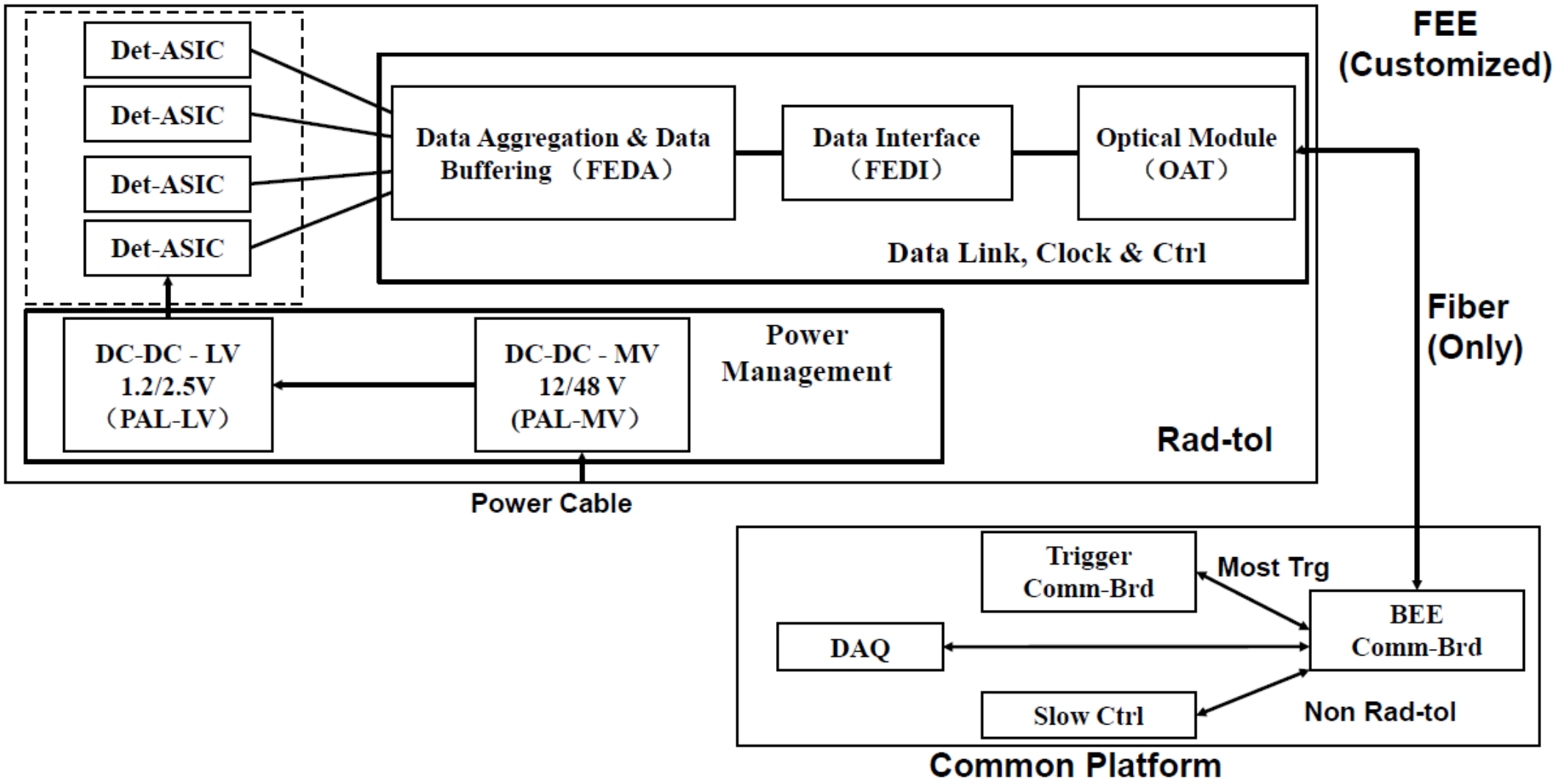
Report on the April 15, 2026 CEPC Day



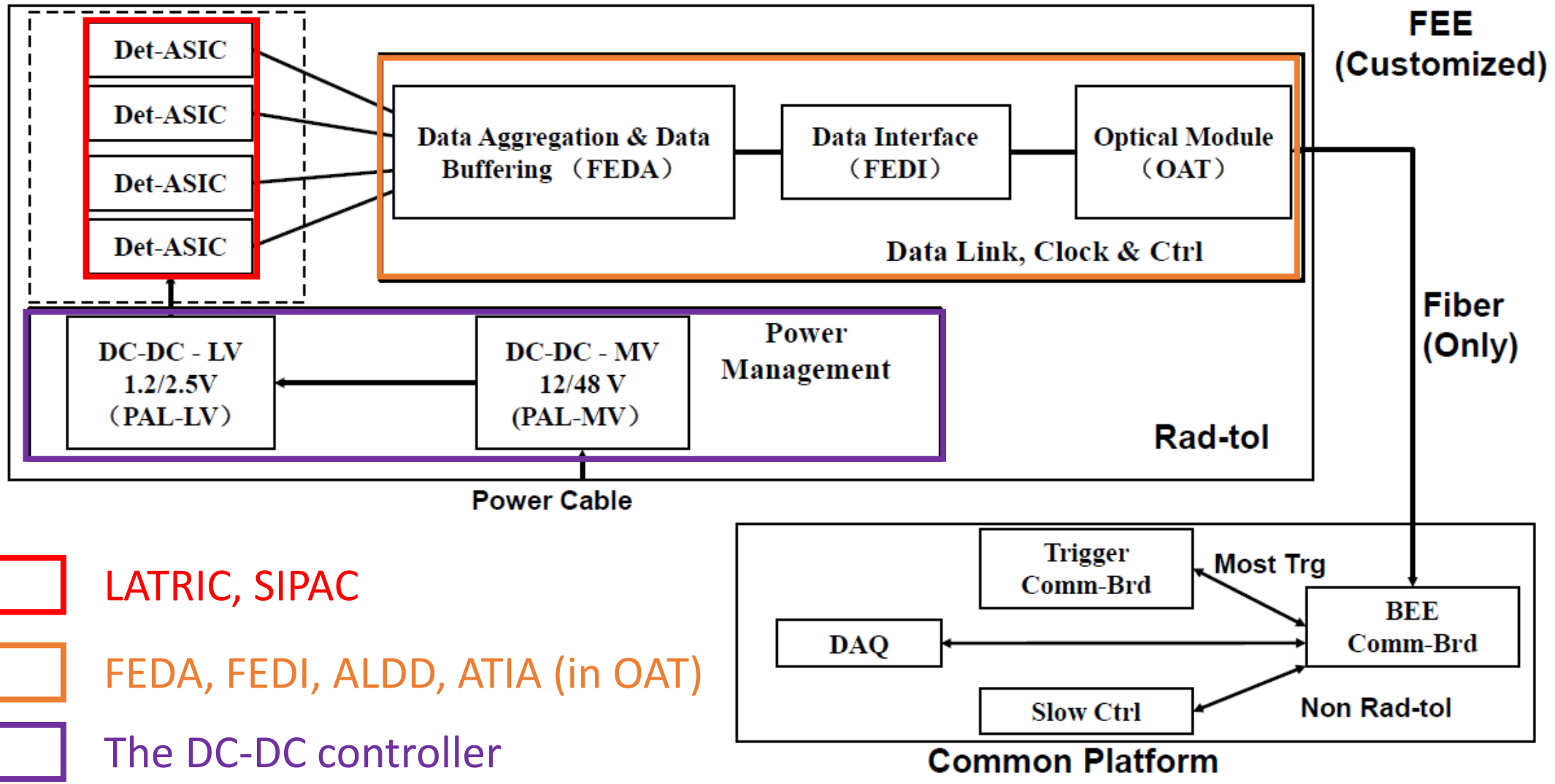
ASICs for the detector readout

- Status: the ASICs, 7 total, under design and/or testing,
  - LATRIC: LGAD Timing and Readout Integrated Chip,
  - SIPAC: A SiPM Readout ASIC for CEPC Calorimeters, Muon and LumiCal,
  - FEDA/FEDI/ALDD/ATIA: the ASIC family for data communication,
  - The DC-DC controller: for the PAL (power at load) modules.
- Going forward,
  - Continue with those that have a clear spec,
  - On hold with those that the detector is going through major changes

Ref.Det. readout architecture



Ref.Det. readout architecture



LATRIC, SIPAC

FEDA, FEDI, ALDD, ATIA (in OAT)

The DC-DC controller

LATRIC

- To read out the LGAD-strip in OTK (the Outer Tracker).
- The challenges (compared with ALTIROC, ETROC in ATLAS and CMS):
  - 30 ps time resolution from the strip that has a much larger detector capacitance than that from a pixel,
  - the 100 μm channel pitch (integration, power dissipation), and 128 channel/chip
- Status: the 8-channel prototype meeting the specs (preliminary), tests with the LGAD-strip on going.
- Details see Xiongbo's presentation.

SIPAC – for ECAL, HCAL, Muon, LumiCal

Table 7.3: Requirements of ECAL front-end electronics

Parameters	Requirements
Charge Range	0.128 pC~ 3.84 nC (0.1~3000 MIP)
Charge Resolution	10 % (1.0 MIP), 1 % (100 MIP)
Timing Resolution	200 ps (1 MIP), 100 ps (12 MIP)
Integral Non-linearity	< 1 %
Average Event Rate/channel	13 kHz
Max Event Rate/channel	230 kHz
Typical Signal Rising Edge	40 ns
Typical Signal Width	~ 1 μs

ECAL

SiPM characteristics that drive the requirements for the readout electronics

Item	Requirement
Charge dynamic range	0.8 pC~800 pC (0.1~100 MIPs)
Charge resolution	10% of 1.0 MIP
SiPM capacitance	≤ 100 pF
SiPM gain	≥ 5×10^5
Average event rate/channel	2 kHz
Max event rate/channel	50 kHz
Typical signal	2~3 mV/p.e.

HCAL

MUON requirement

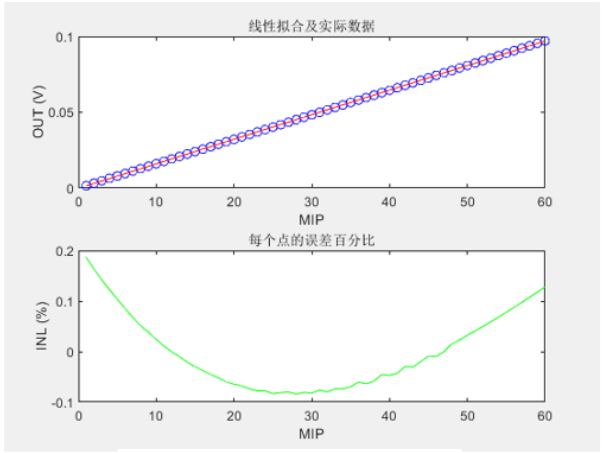
- Readout design for ECAL and HCAL covers the requirements of Muon detector $N_{pe} < 100, \sigma_T < 0.5ns$
- Use the ASIC scheme from ECAL or HCAL, and customize the FEE based on ASIC.
- Revise according to the constraints from cooling and mechanical structure of the detector

The current strategy:

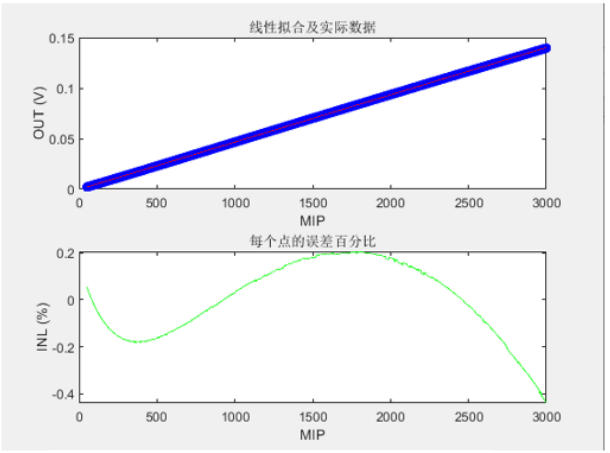
- Two ASICs, SIPAC_E and SIPAC_H to meet the different requirements
- Adapt SIPAC_E for Muon and LumiCal

SIPAC0 – design/check the key blocks

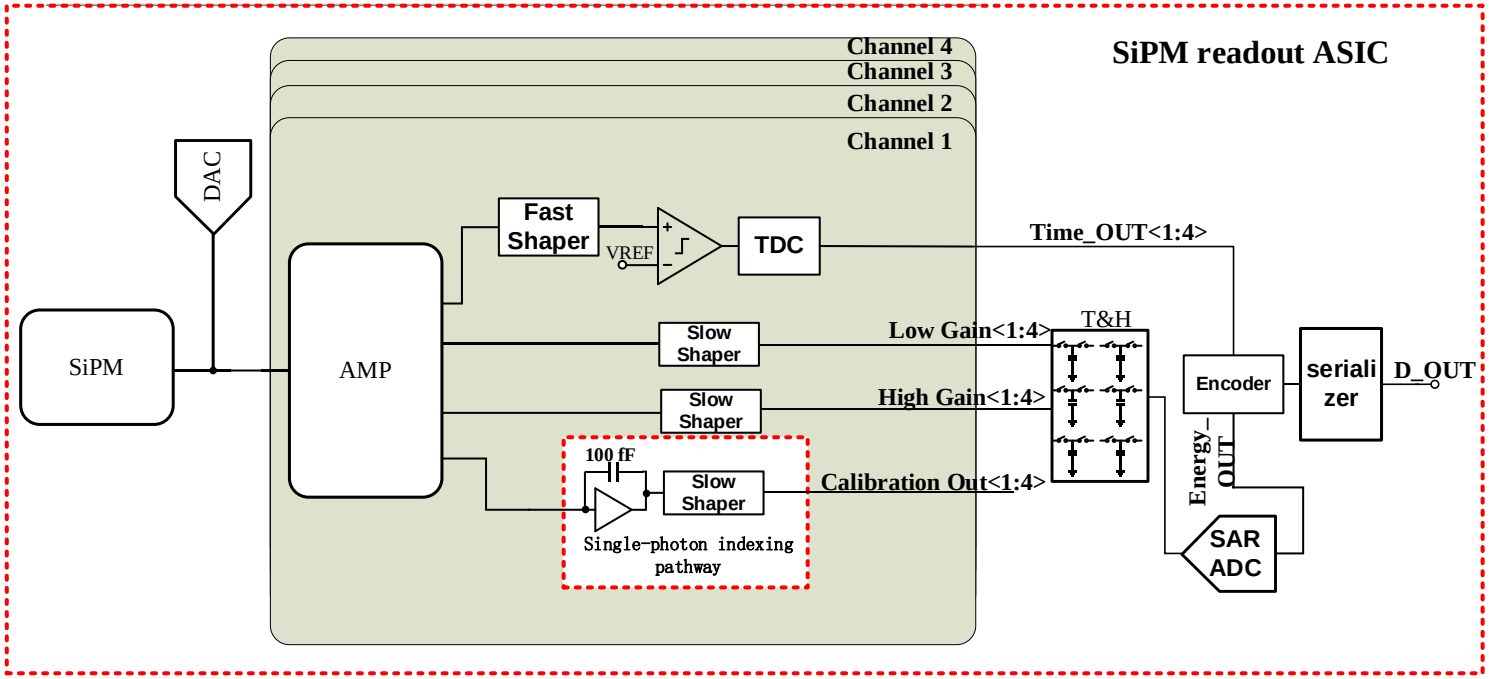
Characteristics	Value
Charge Dynamic Range	1.28 pC~3.84 nC
Charge resolution	10%@1.28pC, 1%@128pC 1%@100 MIPS
Time resolution(RMS)	200 ps @1.28pC, 100 ps @12.8pC
Detector Capacitance	≤ 100 pF
Max signal rate/channel	500 kHz/ch
ADC	10-bit
TDC resolution	8-bit
TDC bin width	100 ps
Power consumption	15mW/channel
Num. of channels	4



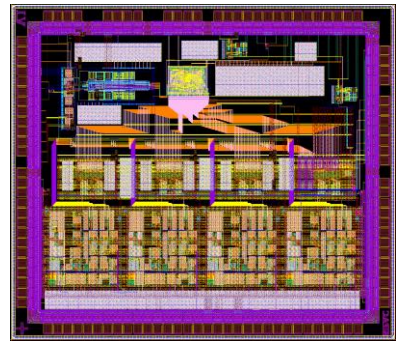
1-60MIPs, INL<0.2%



50-3000MIPs, INL<0.4%

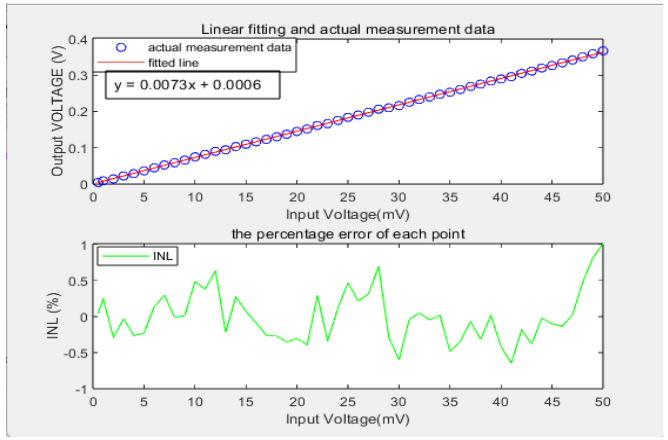


High and low gain shaper covers large dynamic range, fast shaper for timing.



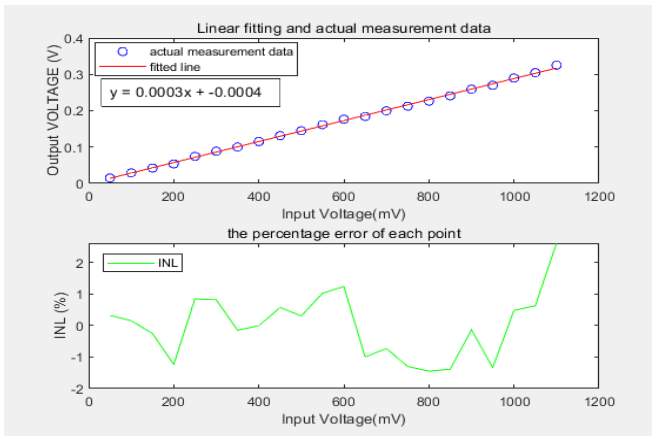
Layout size:2.0mm x 2.3mm, 55nm CMOS, taped out in April.2025.

SIPAC0 test results



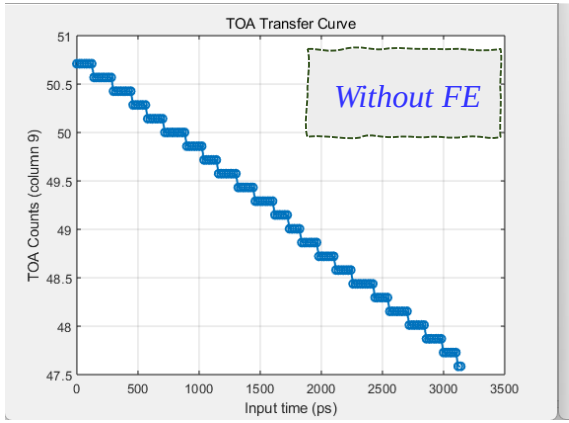
1.28 pC - 128 pC

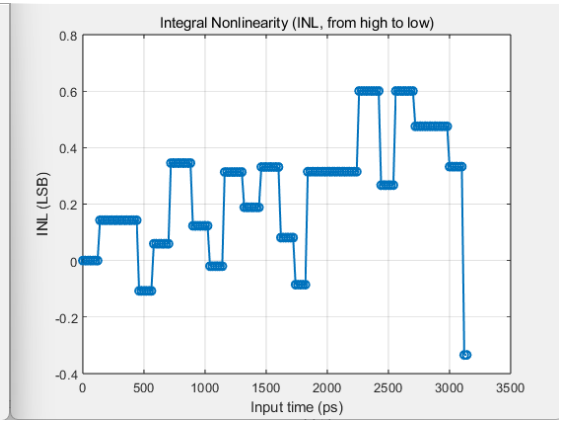
High-gain path INL



128 pC – 2.81 nC

Low-gain path INL





LSB=1/slope ≈ 142 ps

TDC transfer curve

Post-Simulation result		Test result
Input dynamic range	1.28 pC - 3.84 nC	1.28 pC – 2.81 nC
High gain path gain	8	7.3
Low gain path gain	0.5	0.3
SNR	5	4.3
TDC resolution	100 ps	142 ps
ADC resolution	ENOB 10bit	~8bit

SIPAC0 achieves:

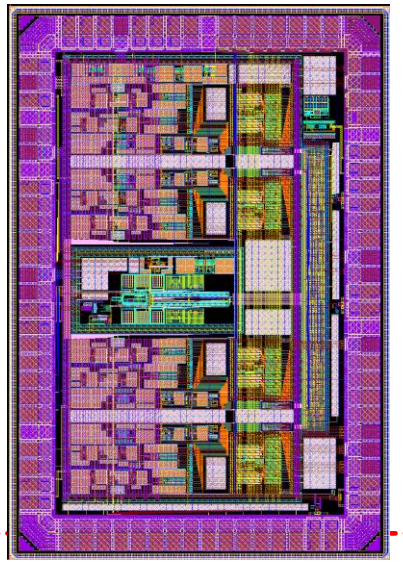
- *dynamic range: 1.28 pC to 2.81 nC with a nonlinearity < 3%,*
- *a timing precision of 142 ps.*

Issues identified:

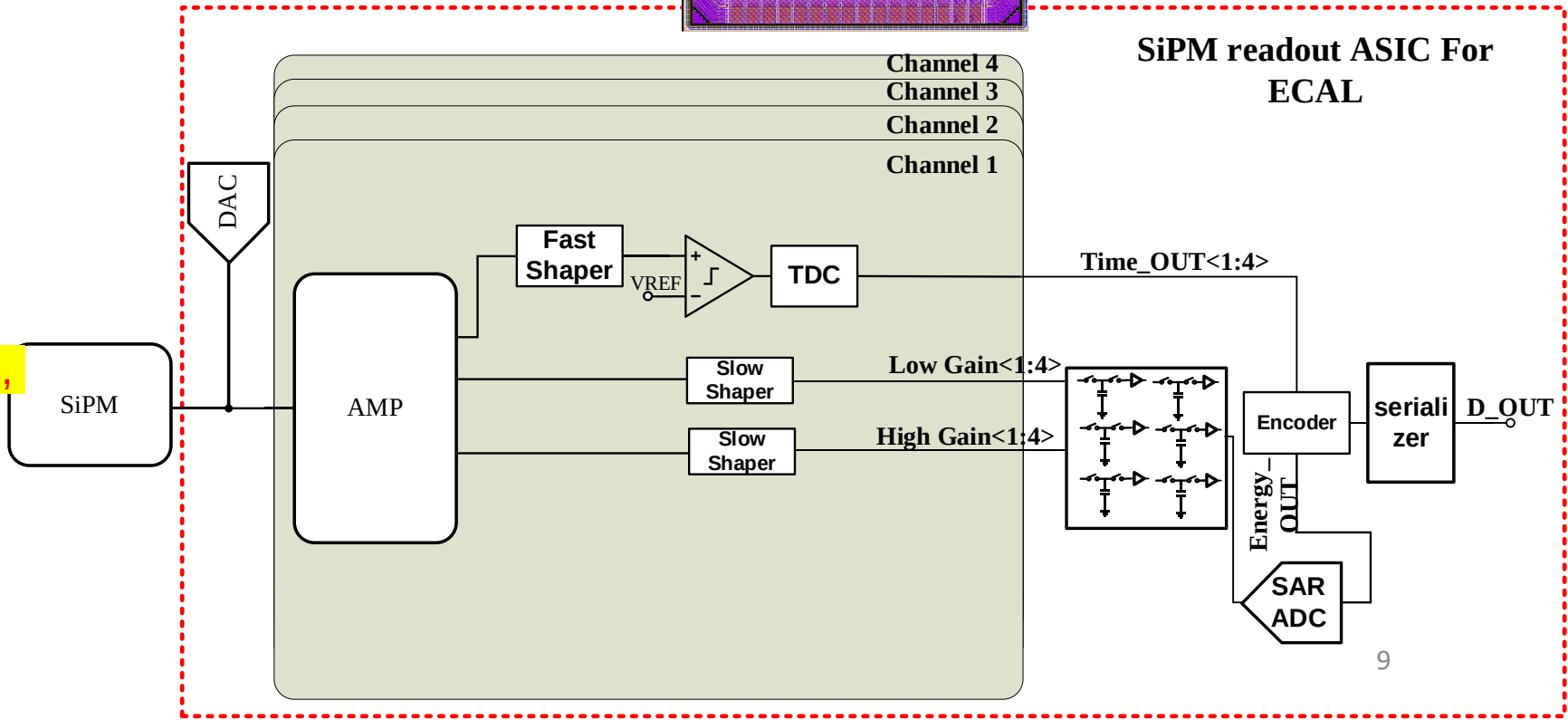
- *dynamic range limitation caused by MOS transistors entering the linear region,*
- *TDC delay results from the SS process corner,*
- *ADC sampling error comes charge redistribution.*

SIPAC_E for ECAL

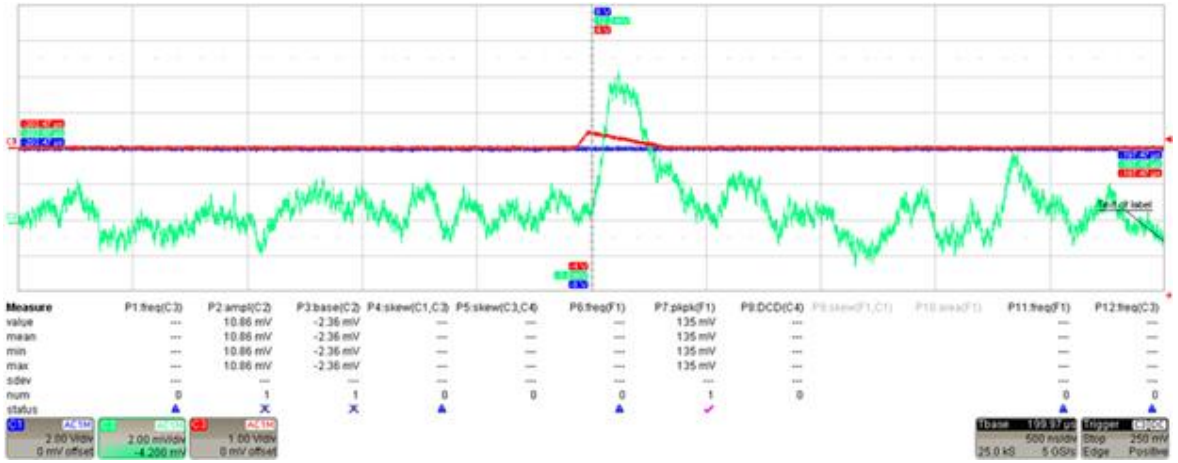
- Main revisions from SIPAC0
  - Fix identified issues
  - Optimize
    - the shaper
    - the SCA, to improve the charge sharing effect
    - the control logic
  - Re-design the digital block
  - Add test-point buffer
  - Reduce from 2.0mm x 2.3mm, to 1.3mm x 1.9mm



Taped out in Oct.2025



SIPAC_E pre.test results



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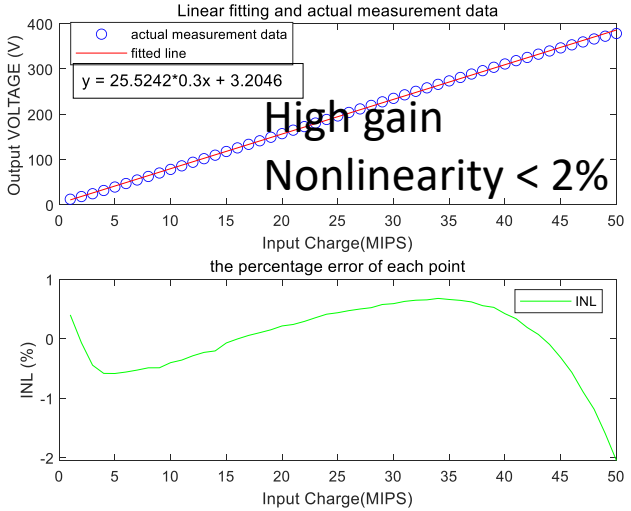
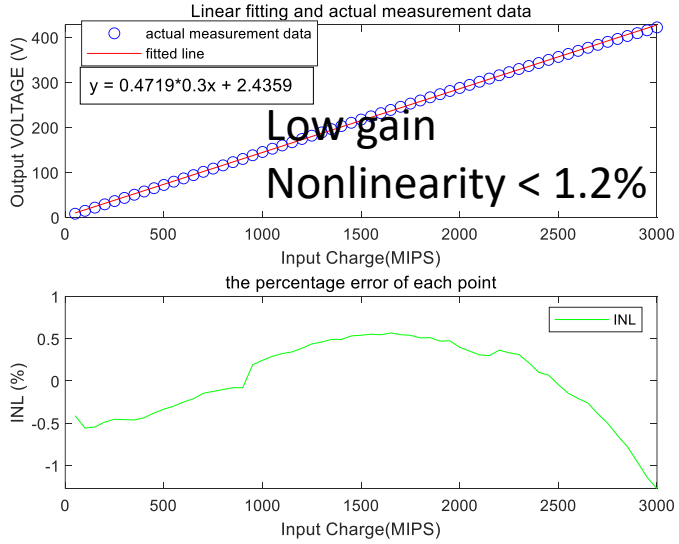




Input signal width 400 ns,

1 MIP = 300 µV, at high-gain, output amplitude 10.86 mV.

Baseline rms noise: 615 µV.

SNR = 17.65. ← needs 30

Gain: 25.52 @ High Gain,

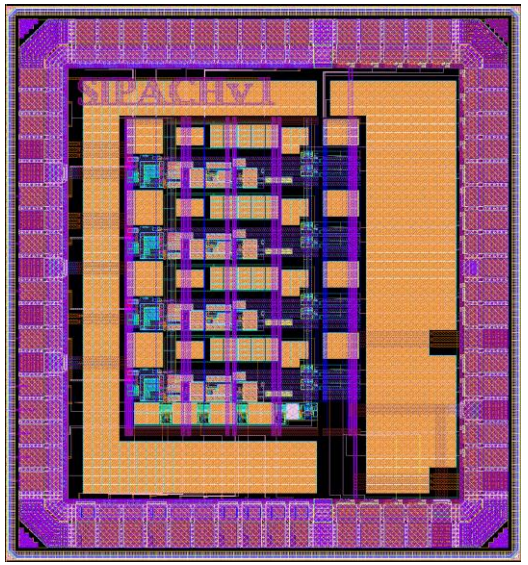
0.47 @ Low Gain

(Close to design values)

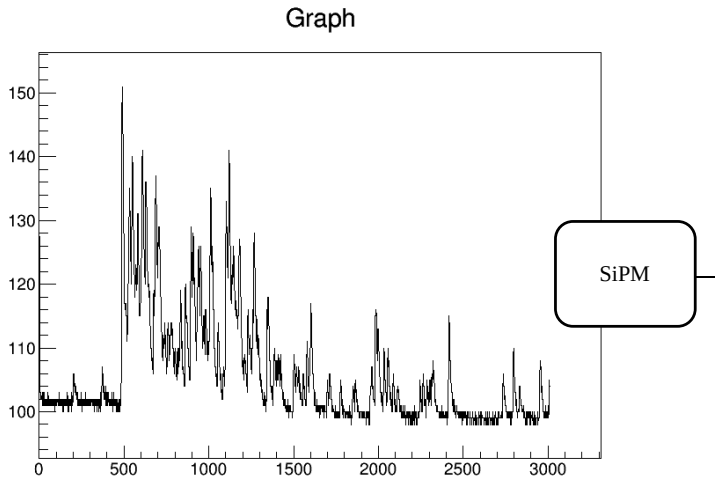
- Not yet meeting the specs.
- Needs better communications with detector people.
- Also needs to wait for the detector to settle.

SIPAC_H for HCAL

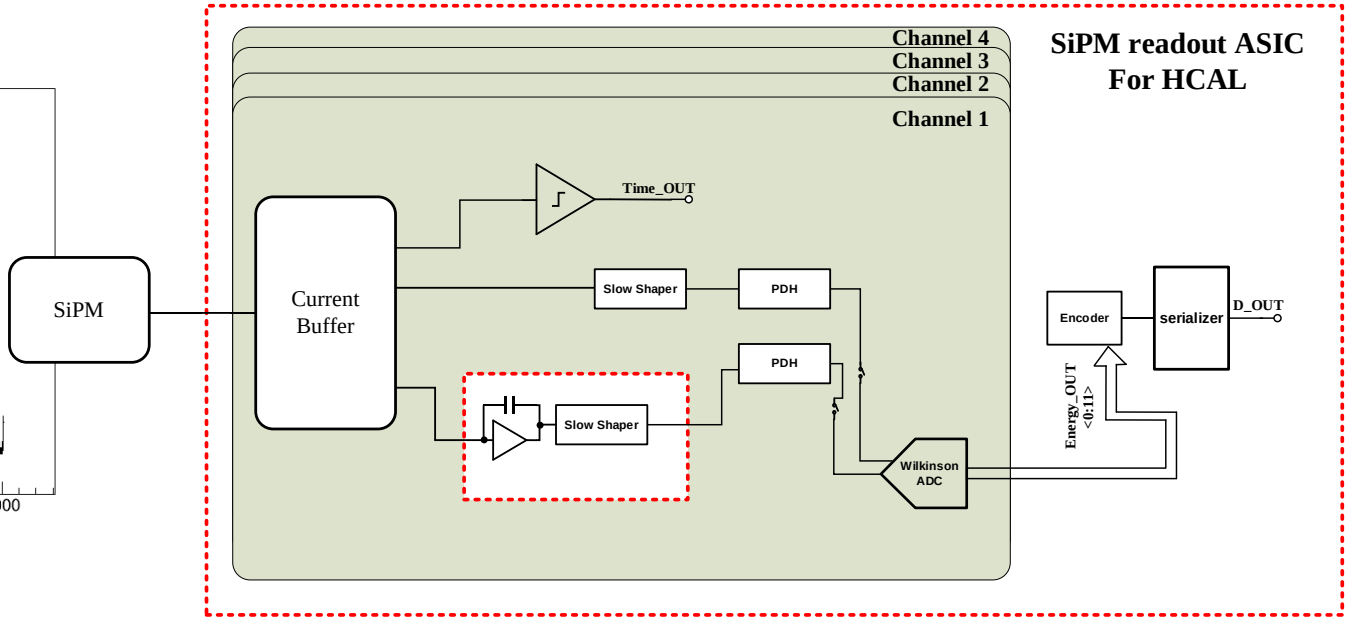
- The Glass Scintillator in HCAL has a decay time of 500 ns, resulting in more discontinuous waveforms for small signal at the MIP level, requiring an integrating preamplifier,
- We choose a current-mode preamplifier, combined with a back-end integrating circuit, to process discontinuous small signals.
- Test results are coming soon.



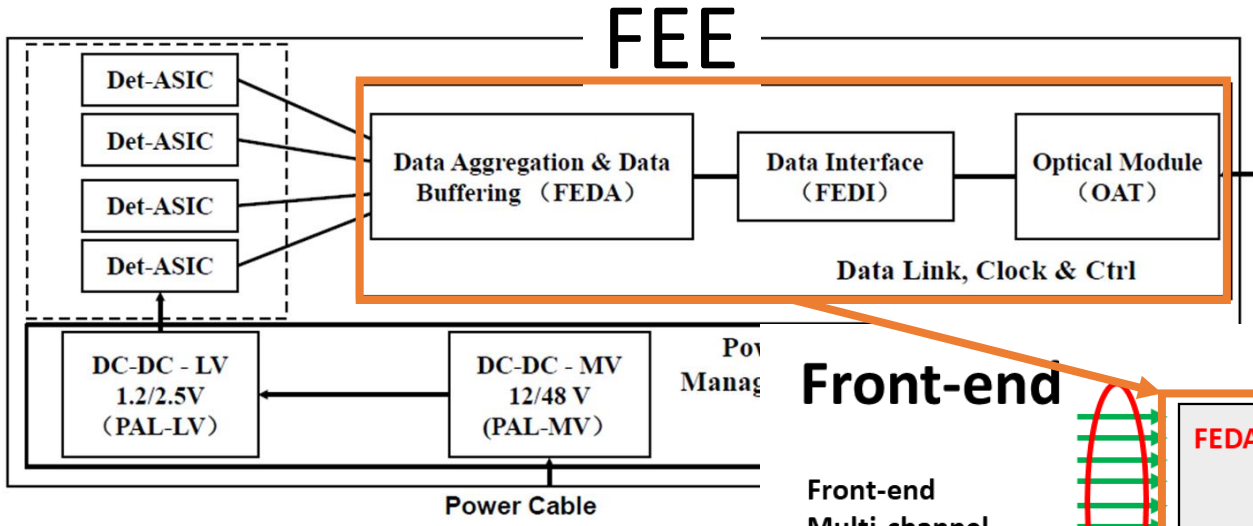
1.3mm x 1.4mm
Taped out in Oct.2025



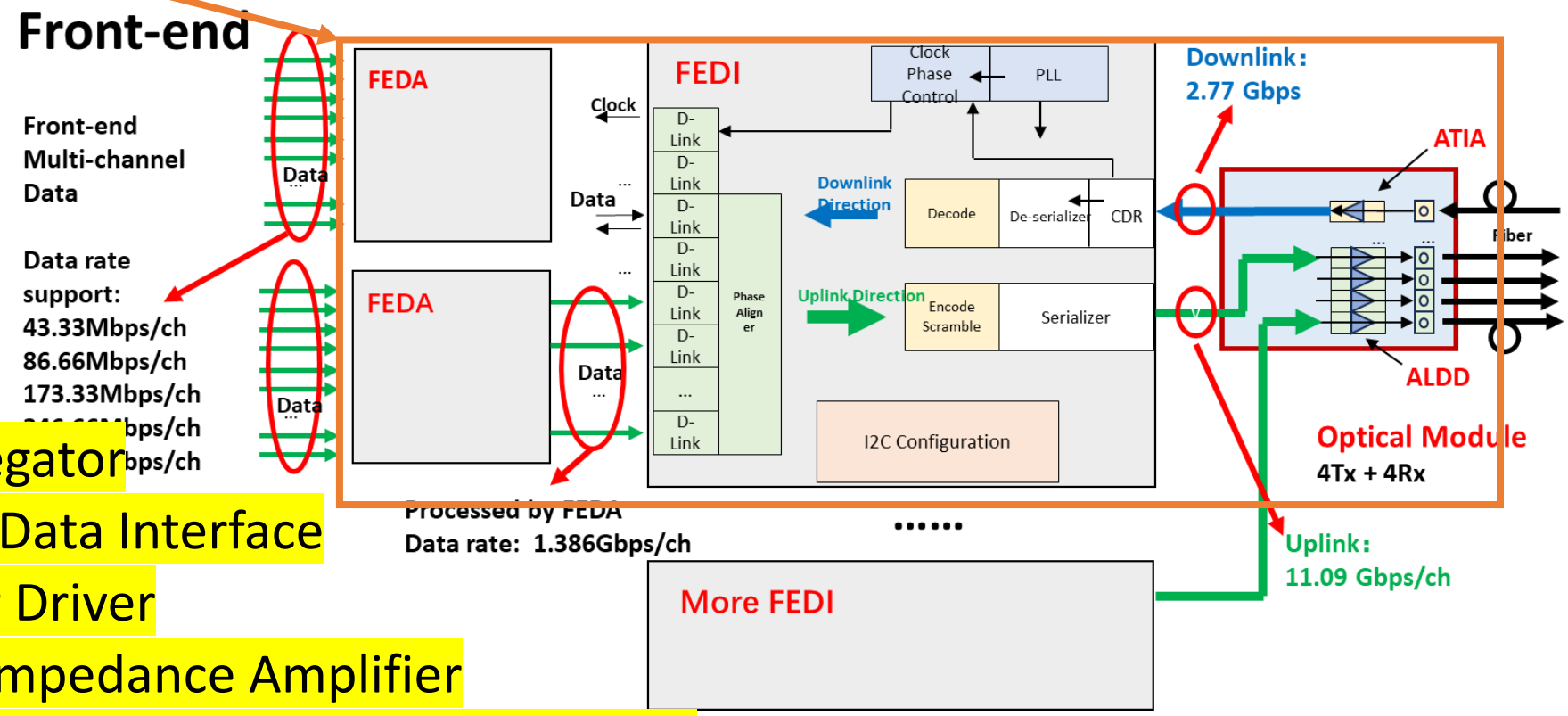
HCAL SiPM Small signal



FEDA/FEDI/ALDD/ATIA

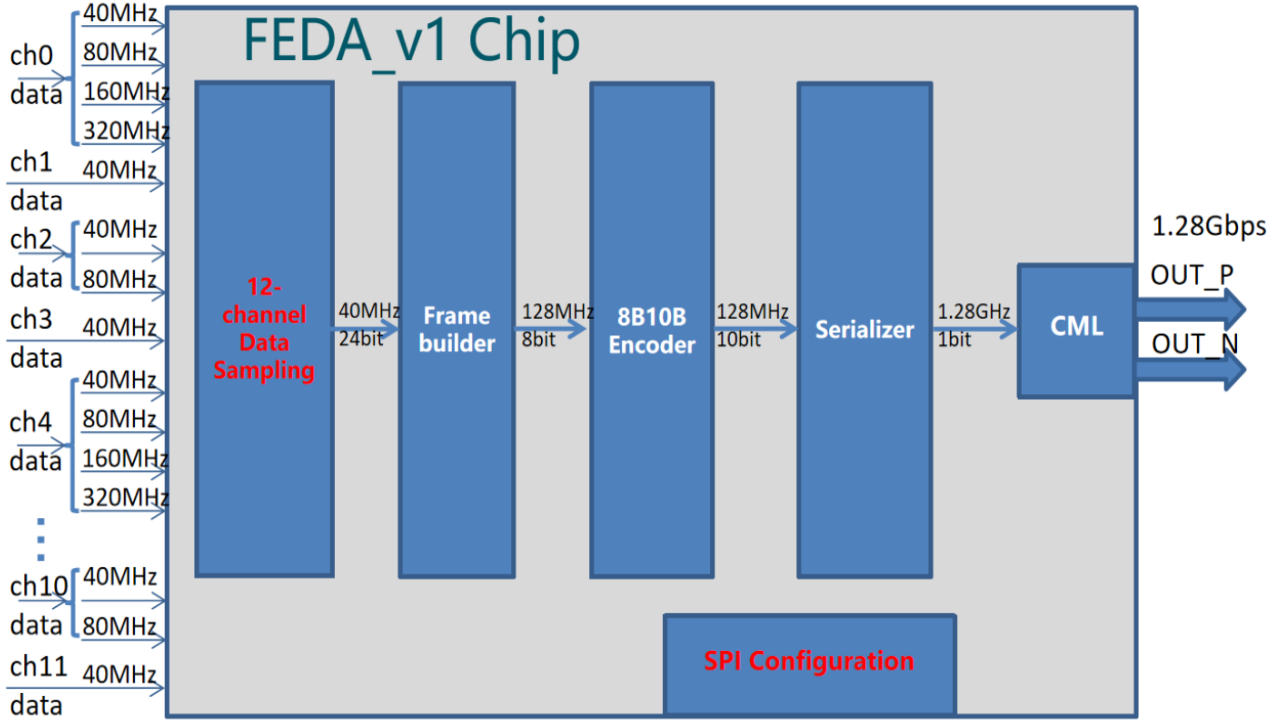


Fiber to BEE

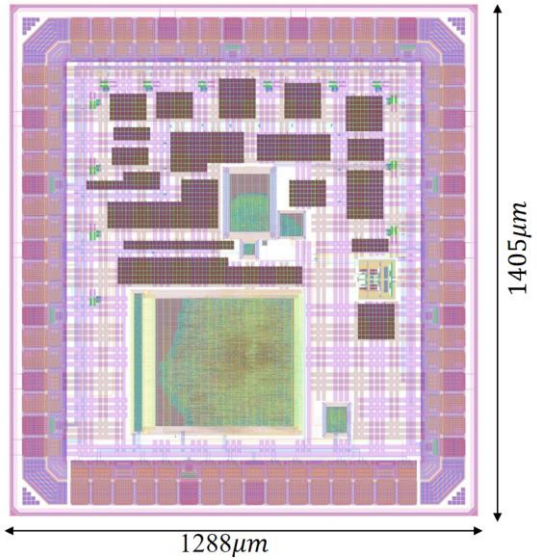


- FEDA (CCNU)： Data Aggregator
- FEDI (IHEP, CCNU, NPU): Data Interface
- ALDD (CCNU)： Array Laser Driver
- ATIA (CCNU)： Array Transimpedance Amplifier
- OAT (CCNU, IP.Sinica): the optical module, not in this talk.

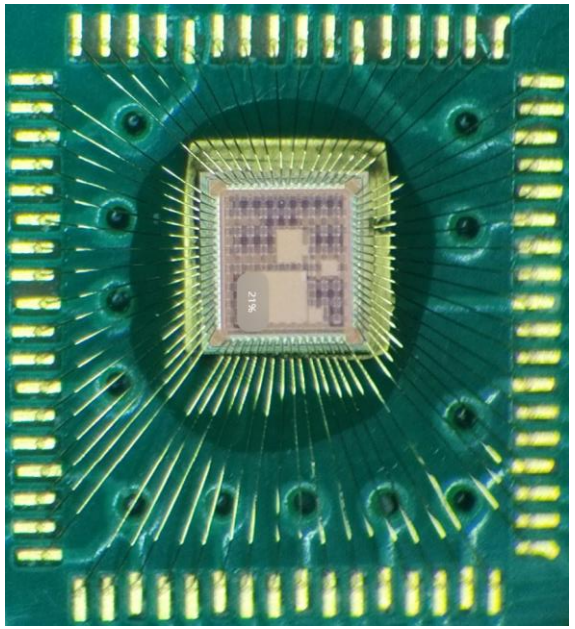
FEDA



FEDA block diagram



FEDA die layout



FEDA wire-bonded on PCB

- Post-layout simulation has verified the functionality,
- The chip was taped out in Oct. 2025,
- Testing is on-going.

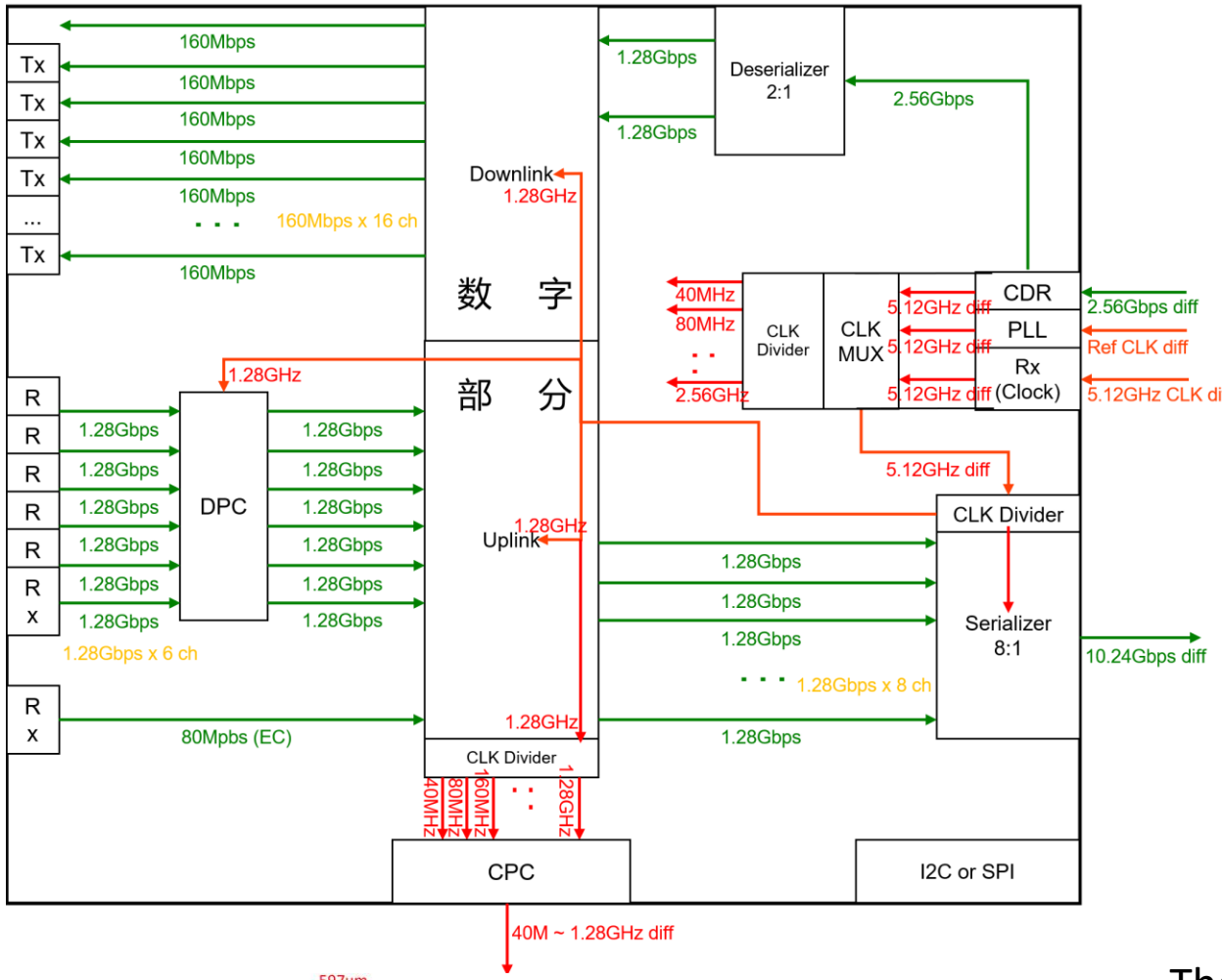
FEDI

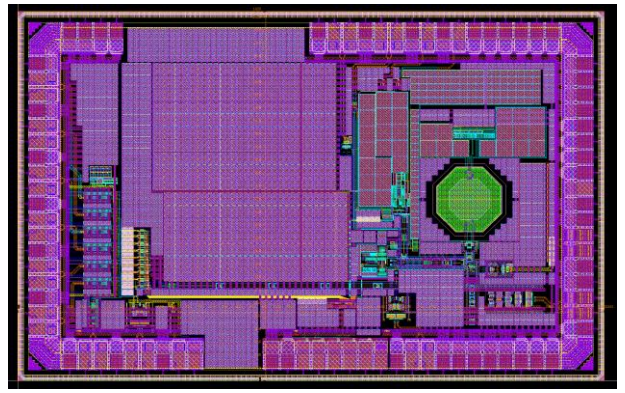
The main circuit modules in FEDI and their design status

FEDI circuit module	Design status	Status in %
the Data Phase Control （DPC）	Layout completed, in post-layout simulation and verification	90%
the Clock Phase Control （CPC）	Layout completed, in post-layout simulation and verification	90%
the overall Digital Part (including the data encoding and decoding in both up- and down-links)	Coding completed and checked, in circuit layout synthesis and verification	80%
the high-speed serializer and de-serializer	Sub-circuit blocks completed and verified, in assembling and final post-layout simulation and verification	90%
the high speed clock (PLL, CDR)	Layout almost done, in final checking and correction, then final post-layout simulation will be carried out.	95%

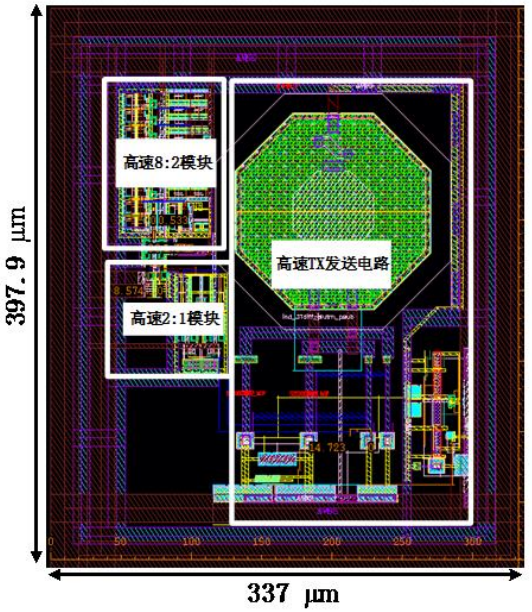
The tape-out is planned to be in July 2026.

FEDI



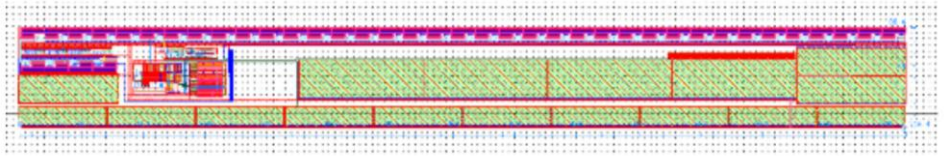


The high-speed clock module（95%）



The serializer、de-serializer module（90%）

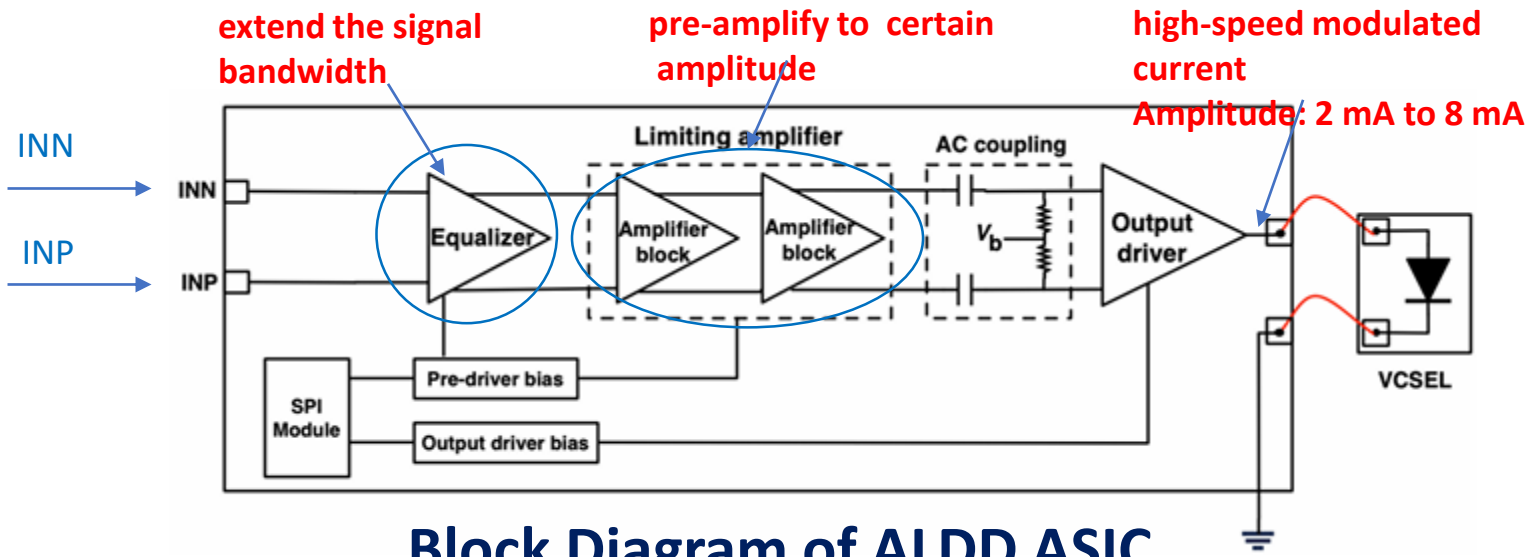
The data phase control module（90%）



Layout Area： 716x80u

The clock phase control module（90%）

ALDD,ATIA



Block Diagram of ALDD ASIC

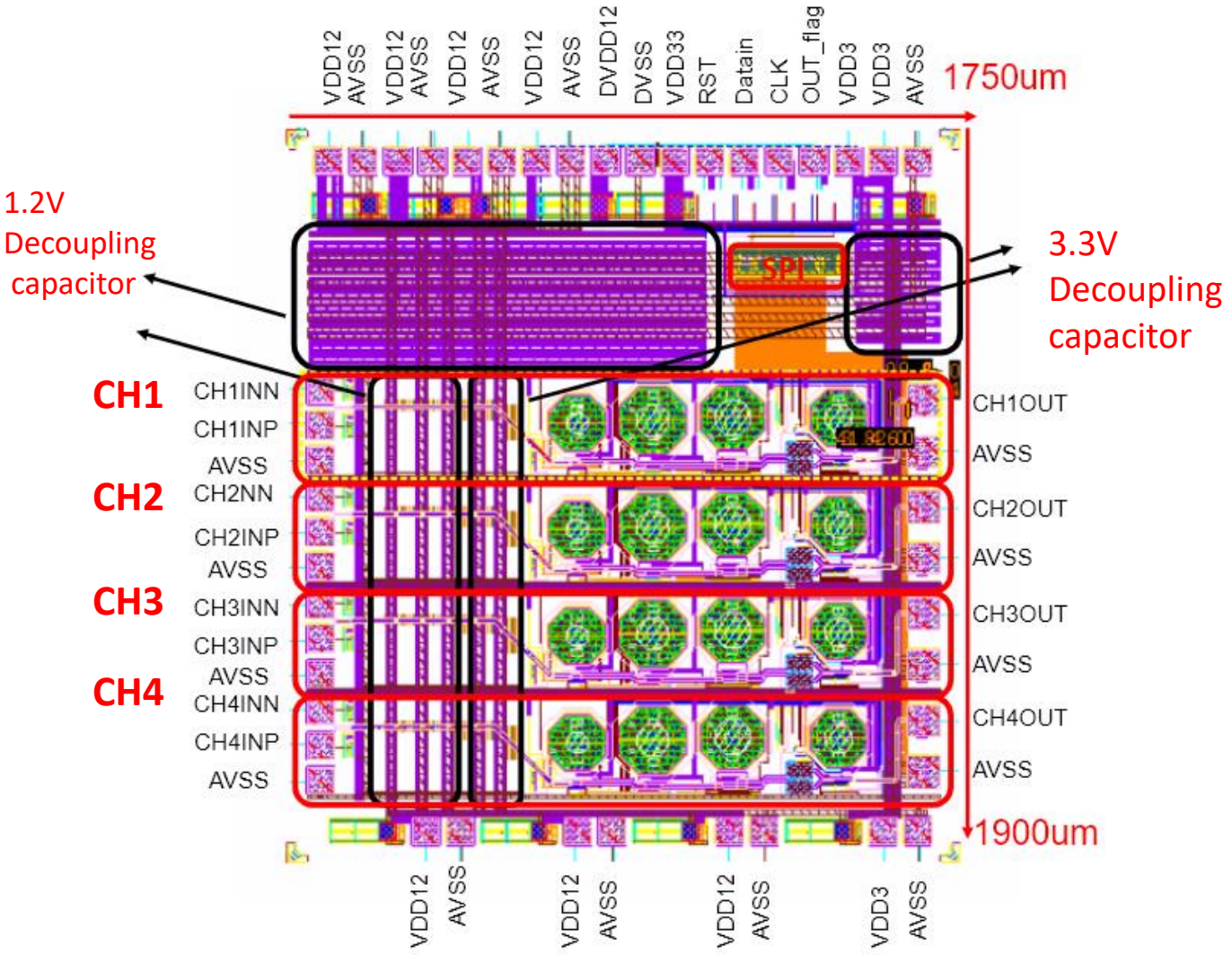
- The structure of ALDD has three main parts:
  - Equalizer
  - Limiting Amplifier(LA)
  - Output driver

Specifications

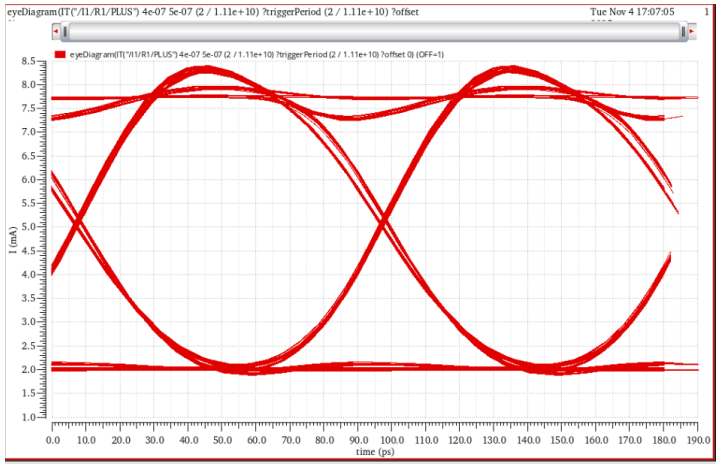
parameter	Design indicators
power supply voltage	1.2 V and 3.3 V
Power consumption	typical 50 mW/ch 200 mW when working at 4 ch x11.1 Gbps/ch
Bit rate	11.1 Gbps/ch
Differential input signal amplitude	Minimum differential peak-to-peak 200 mV
differential input impedance	100Ω
Maximum equalizer equilibrium strength	>7dB
Limiting amplification stage gain	>12dB@typical
Limiting amplification level bandwidth	>9.8GHZ@typical
Output current amplitude	5mA@typical
Maximum pre emphasis strength	>2.5dB
Simulate ISI jitter	<15ps

16

ALDD, ATIA



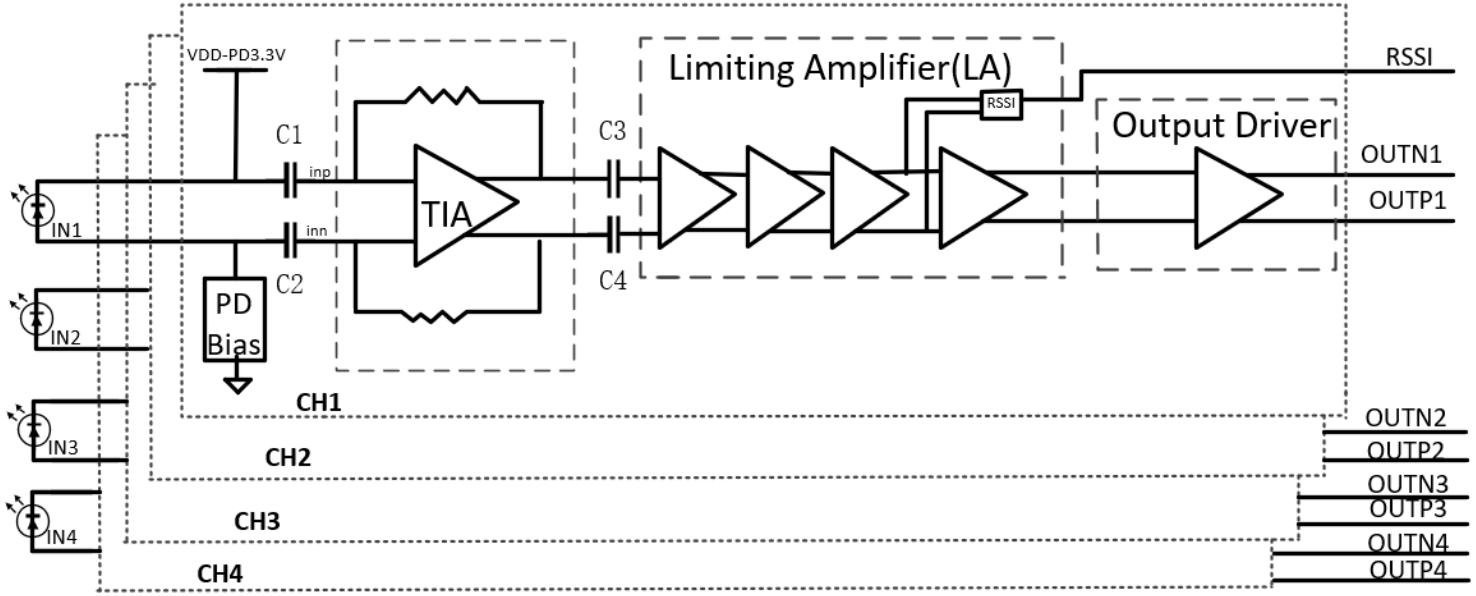
Overall layout, 4 x 11.09 Gbps/ch



ALDD simulated eye diagram, post-layout, single channel

- The die size is 1750×1900 um.
- It was taped out in Oct. 2025.
- Testing is on-going.

ALDD,ATIA



Block Diagram

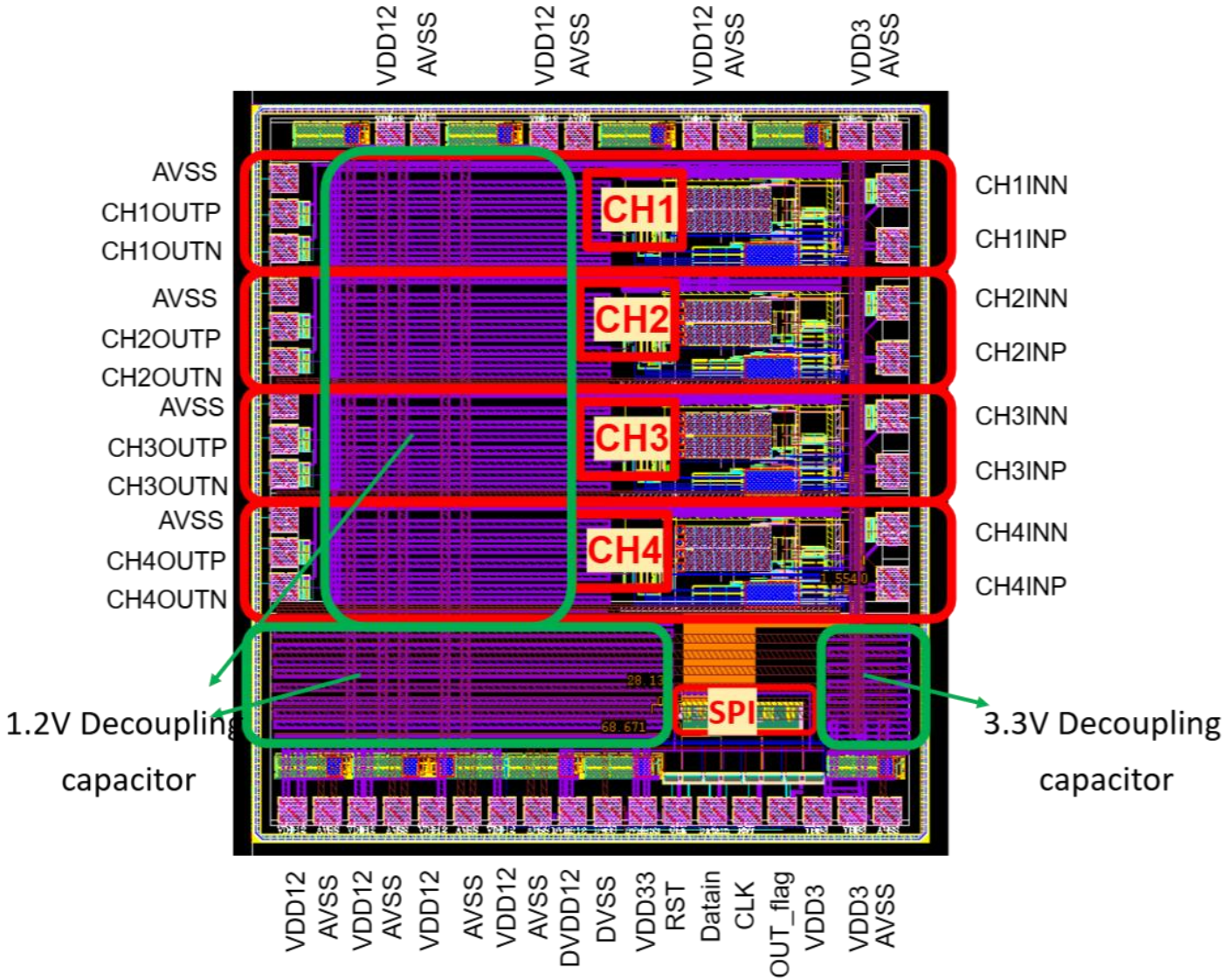
- ATIA is a 4 x 2.77 Gbps/ch transimpedance amplifier AISC, including:
  - PD Bias
  - ATIA core and LA stages
  - Output Driver
- Overall gain: 75 dB ohm
- Output differential p-p 400 mV signals with configurable pre-emphasis.

Specification

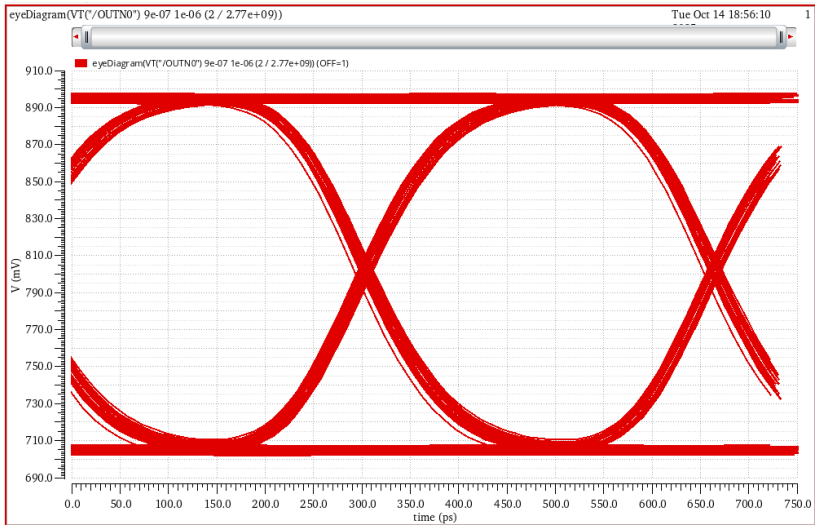
Parameter	Design indicators
Bit rate	2.77 Gbps

Parameter	Design indicators
Bit rate	2.77 Gbps
Photodiode capacitance	200fF to 2pF
High cut-off frequency	2 GHz
Low cut-off frequency	<1 MHz
Sensitivity for BER=10-12	20 uA p-p(-17dBm)
Transimpedance gain	75 dB ohm
Output differential p-p voltage	≥400 mV(50 ohm)
PD bias supply voltage	3.3V
Circuit supply voltage	1.2V
Power consumption	<100 mW/ch
Total jitter	0.085 UI(<34ps@2.77Gbps)

ALDD, ATIA



Layout of 4 x 2.77 Gbps/ch



ATIA simulated eye diagram, post-layout, single channel

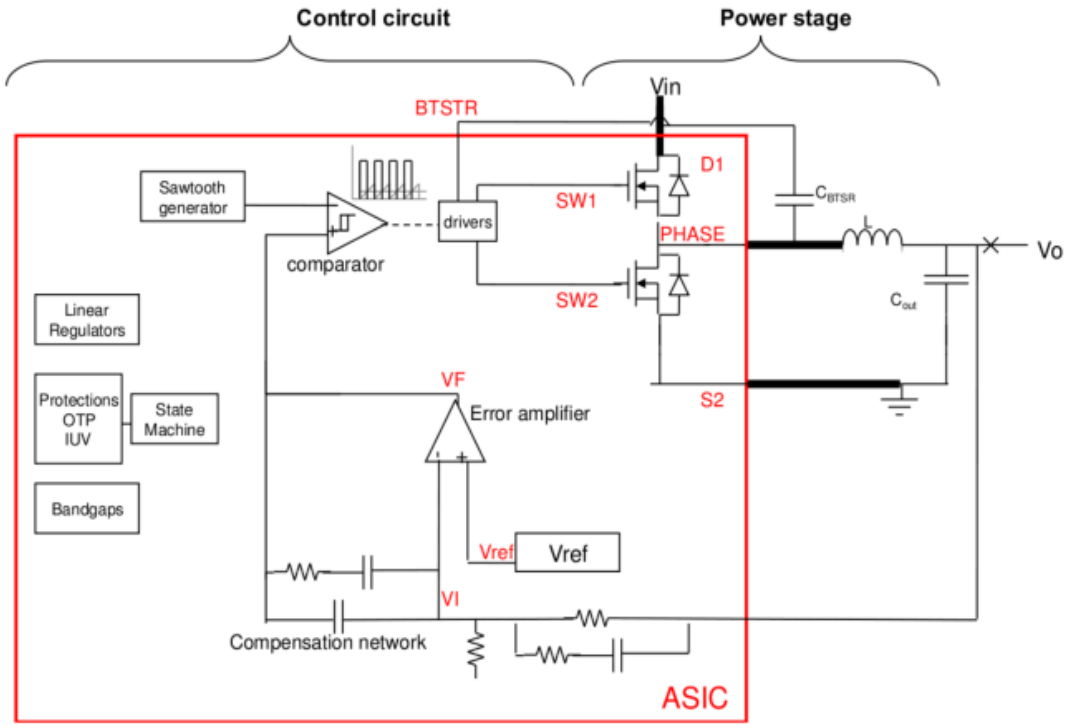
- The die size is 1750×1900 um.
- It was taped-out in Oct. 2025.
- Test is on-going.

DC-DC controller

Two will be needed: 48V → 12V, and 12V → 1.2V/2.5V. We started with the latter.

The Specifications

Parameter	Value
Input voltage	12-10 V
Output voltage	1.8/1.2 V（adjustable）
Output current	<10 A
Output ripple voltage	<10 mV
power efficiency	>80%
Power module size	<30x20x6.7mm^3
TID	4 Mrad/year
Magnetic field	3T
Switching frequency	1-3 MHz



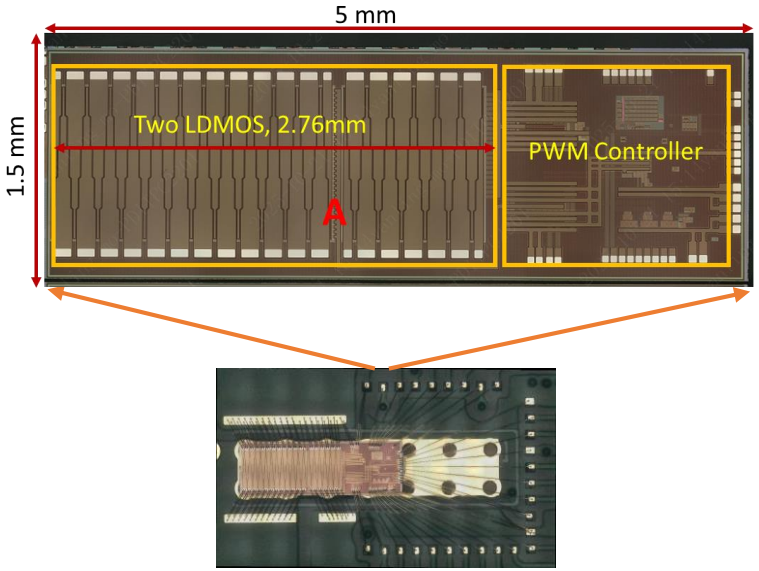
We (NPU) started with the controller, and the controller + a built-in power transistor.

But GaN power transistors are the choice for

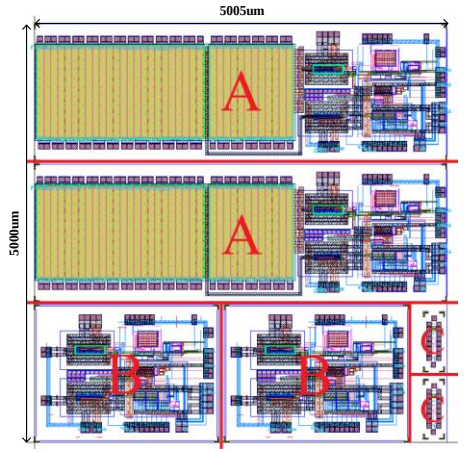
- ✓ fast switching speed
- ✓ low power loss
- ✓ high radiation tolerance
- ✓ low on-resistance

DC-DC controller

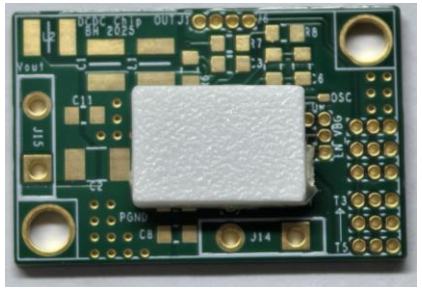
The tape-out in January 2025



Die wire-bonded on a PCB



The layout



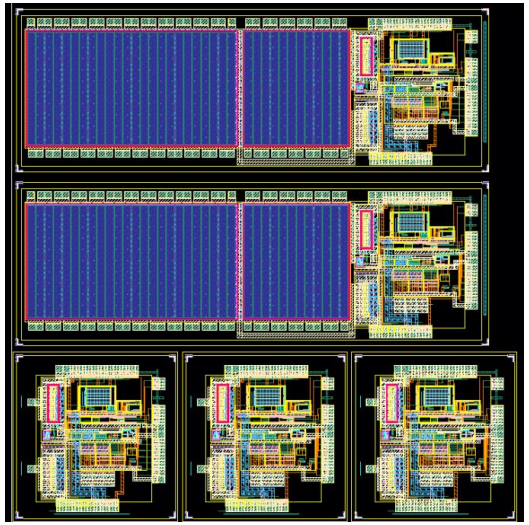
Test PCB

The built-in power transistor does not work stably, problem identified. Tests continued with an external Si power transistor. The PCBs for tests with GaN power transistors are received from the wire-bonding house. Tests are starting.

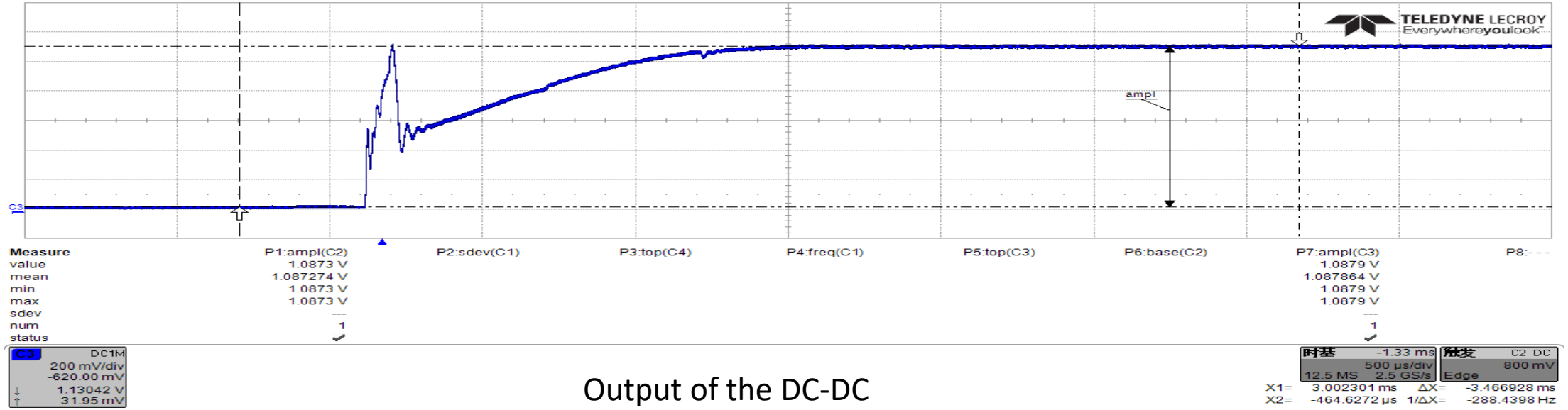
The tape-out in Junuary 2026

changes:

1. Correct the problem in the built-in power transistor to avoid current leak.
2. ESD protection only to GND
3. Removed the enabling circuit to the band-gap.
4. Improved powering up sequence, and added pre-power-drop circuit.
5. Die size reduces from 2.17*1.48 mm^2 to 1.38*1.42 mm^2
6. Test points for irradiation.



DC-DC controller



Output of the DC-DC

With an external Si power transistor, the DC-DC module works with the following issues:
Low efficiency, below 70%. We believe this is due to the Si power transistor on-resistance. If it is, the efficiency with GaN should improve.

- Start up time: T_{SS} = 23nF*760mV/10u ≈ 1.7ms
- Startup over shoot observed, and verified with simulation. Will mitigate by the VBG output capacitance.
- VBG-transit is unstable (~10us), reflecting on the output voltage. This is also addressed in the recent tape-out.

Going forward

- Tests on LGAD-strip + LATRIC1 (8-channel) will lead to the next 32- or 64-channel LATRIC development.
- SIPAC tests continue but the ASIC development will be put on hold, waiting for detector + SiPM to provide clearer specs to go ahead. We will also strengthen the communications between detector and electronics people.
- The data link system (ASICs and optical module OAT) charges forward, expecting the tape-out of FEDI this July, and test results on FEDA, ALDD, ATIA, and OAT, results likely for the CEPCWS this fall.

Going forward

- The DC-DC controller and PAL1.2/2.5 had a rough start. The group is going through internal reviews, for ways to improve: better understanding between lab and university people on the R&D for a specific detector, not a blue-sky paper-oriented job, the best approach to proof-of-principles in key elements in the project, etc.
- Not reported but necessary circuits:
  - configuration/control circuits under development: I2C (CCNU), SPI (IHEP), DAC (CCNU, IHEP),
  - Irradiation tests and tools construction for rad-tol circuit design,
  - Digital-on-Top circuit development methodology studies.