

ASIC LATRIC



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Design & Test of LATRIC ASIC

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on behalf of Elec and OTK

Electronics & Outer Tracker

Outline

- Introduction
- LATRIC0 & Test
- LATRIC1 & Test
- Conclusion

Introduction

◆ OTK

- The outermost detector of the tracking system in the reference detector of the CEPC;
- Uses AC-LGAD microstrip sensors;
- Provides both high spatial resolution (10 μm) and high time resolution (50 ps).

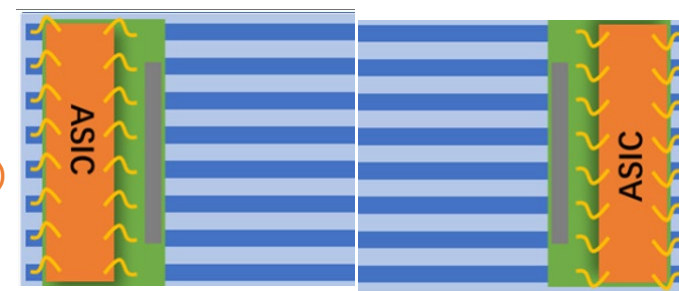
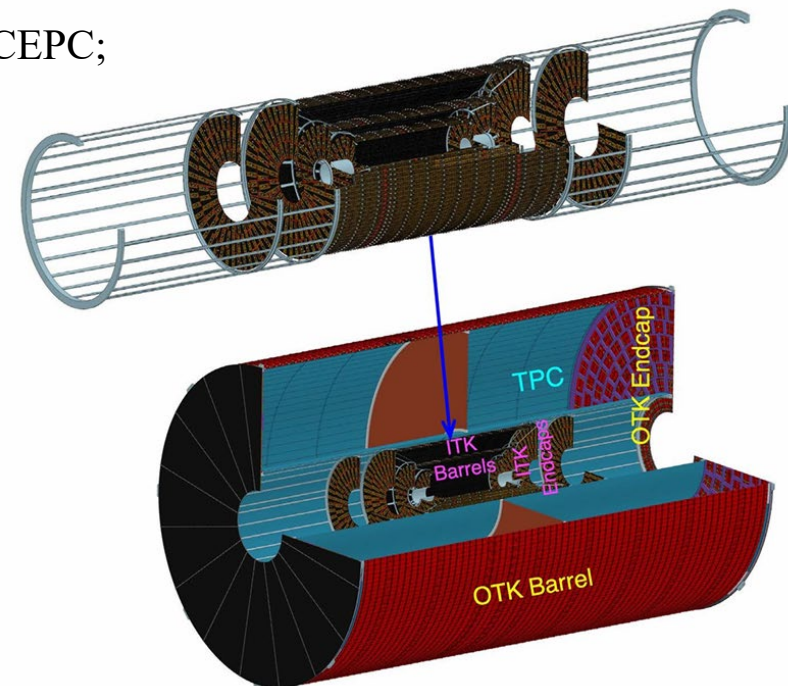
◆ ASIC specification in TDR

Table 5.12: Configuration for the LATRIC ASIC (assuming a detector capacitance $C_d = 8$ pF)

Parameter	Value	
Voltage	1.2 V	
Number of channels	128	
Channel pitch	< 100 μm	→ (Wire bonding channel to channel)
Single channel noise (ENC)	< 10,000 e^- (1.6 fC)	
Cross-talk	< 10%	
Maximum jitter	30 ps at 16 fC	→ (Assume LGAD contributes 40 ps)
Minimum threshold	4 fC	
Dynamic range	8 fC–50 fC	
TDC conversion time	< 23 ns	
Power dissipation per ASIC	1.5 W (for occupancy < 1%)	→ (Large cap leads to high consumption)
Data size per fired channel	48 bits	
e-link driver bandwidth	43.33 Mbps or 86.67 Mbps	

$$\sigma_{hit}^2 = \sigma_{Landau}^2 + \sigma_{clock}^2 + \sigma_{elec}^2$$

$$\sigma_{jitter} = \frac{e_n C_d}{Q_{in}} \sqrt{t_d} \propto \frac{C_d \sqrt{t_d}}{Q_{in} \sqrt{I}}$$



Layout of module

◆ LATRIC (LGAD Timing and Readout Integrated Chip)

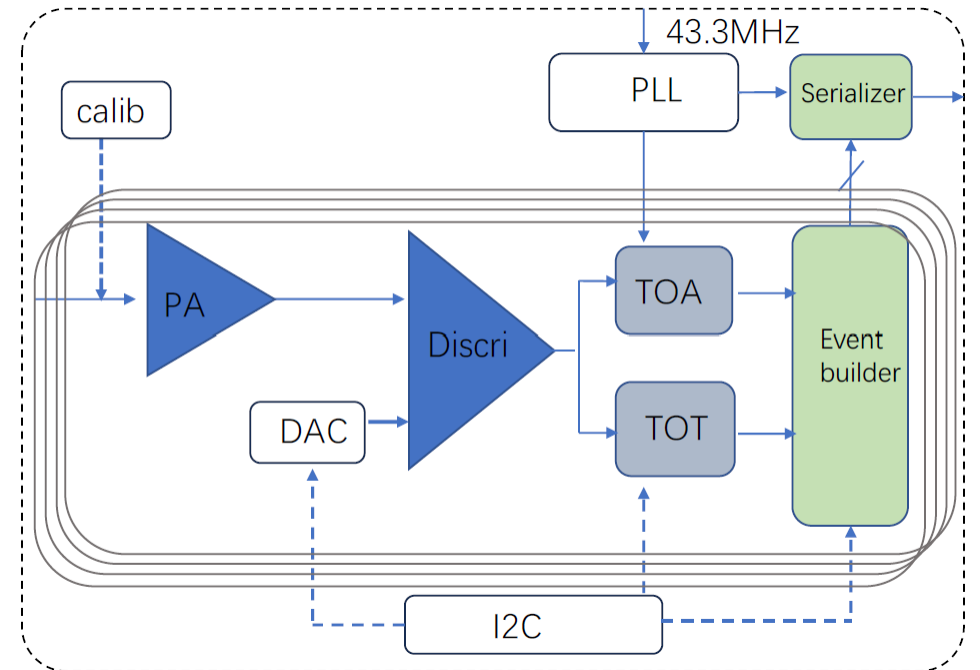
- Front-end
 - Preamplifier and Discriminator
 - Threshold DAC for each channel
- TDC
 - Time of Arrival (TOA) for arrival time
 - Time over Threshold (ToT) for signal charge
- Event builder: Data arrangement, scrambling, and packing
- PLL: Clock management
- Serializer: Data output and transmission
- I2C: Configuration of control bits

■ LATRIC0 (single-channel, April, 2025)

- Front-end, TDC, Serializer (720MHz)

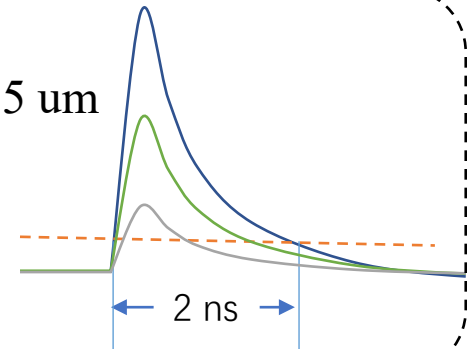
■ LATRIC1 (8-channel, October, 2025)

- Front-end, TDC (improved), Event builder, Serializer (40 MHz)
- 4 channel with Front-end, 4 channel without.



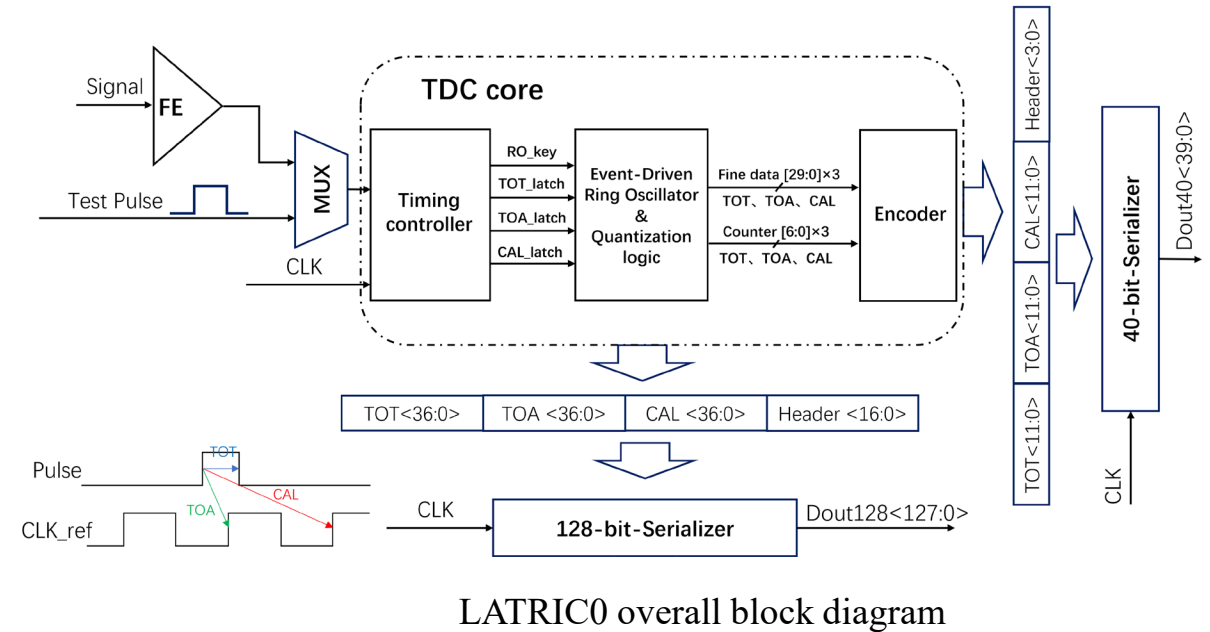
Spatial resolution:

$$50 \text{ ps}/2 \text{ ns} * 100 \text{ um} = 2.5 \text{ um}$$



◆ Architecture

- Front-End (FE)
 - An amplification and a discrimination.
- TDC core
 - Timing controller;
 - Event-Driven RO & Quantization logic;
 - Encoder.
- Output logic
 - Output the Measured CAL, TOT, TOA codes;
 - 128-bit Serializer for 111-bit raw data;
 - 40-bit Serializer for 36-bit encoded data.



■ Self-calibration

- An additional period of CLK_ref is measured for calibration: $LSB_{Cal} = T_{CLK_ref} / CAL_{code}$;
- $TOA_{time} = LSB_{Cal} * TOA_{code}$;
- $TOT_{time} = LSB_{Cal} * TOT_{code}$.

Quantization logic

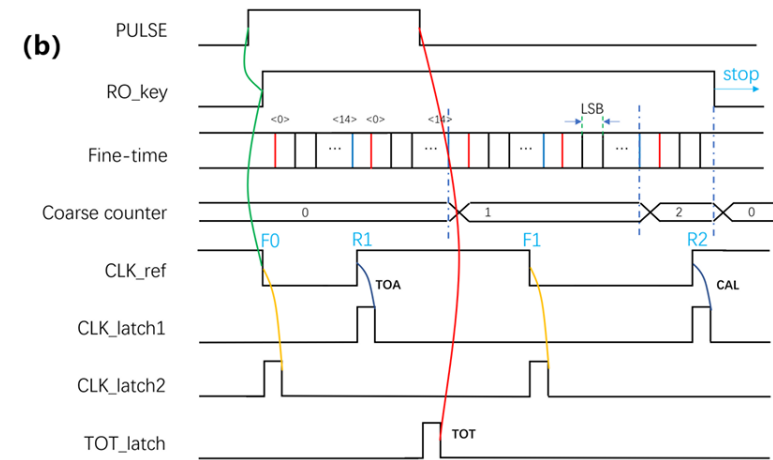
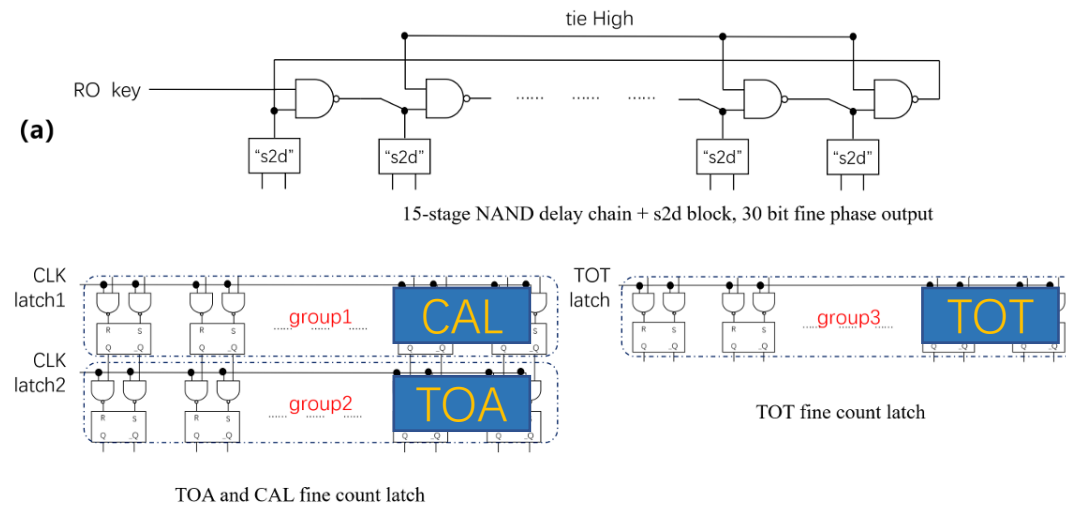
■ TDC core

➤ Ring Oscillator (RO)

- The RO employs 15 NAND-based delay cells, each providing an average delay of about 30 ps.

➤ Quantization logic

- When the leading edge of the PULSE signal arrives, the RO is activated, the CLK_ref is enabled, coarse count starts.
- The following two rising edges of CLK_ref after PULSE latches the RO states as TOA and CAL respectively.
- The trailing edge of the PULSE signal latches the RO state as TOT.



(a) Event-Driven RO & Quantization logic; (b) Quantization timing

LATRICO Test Results

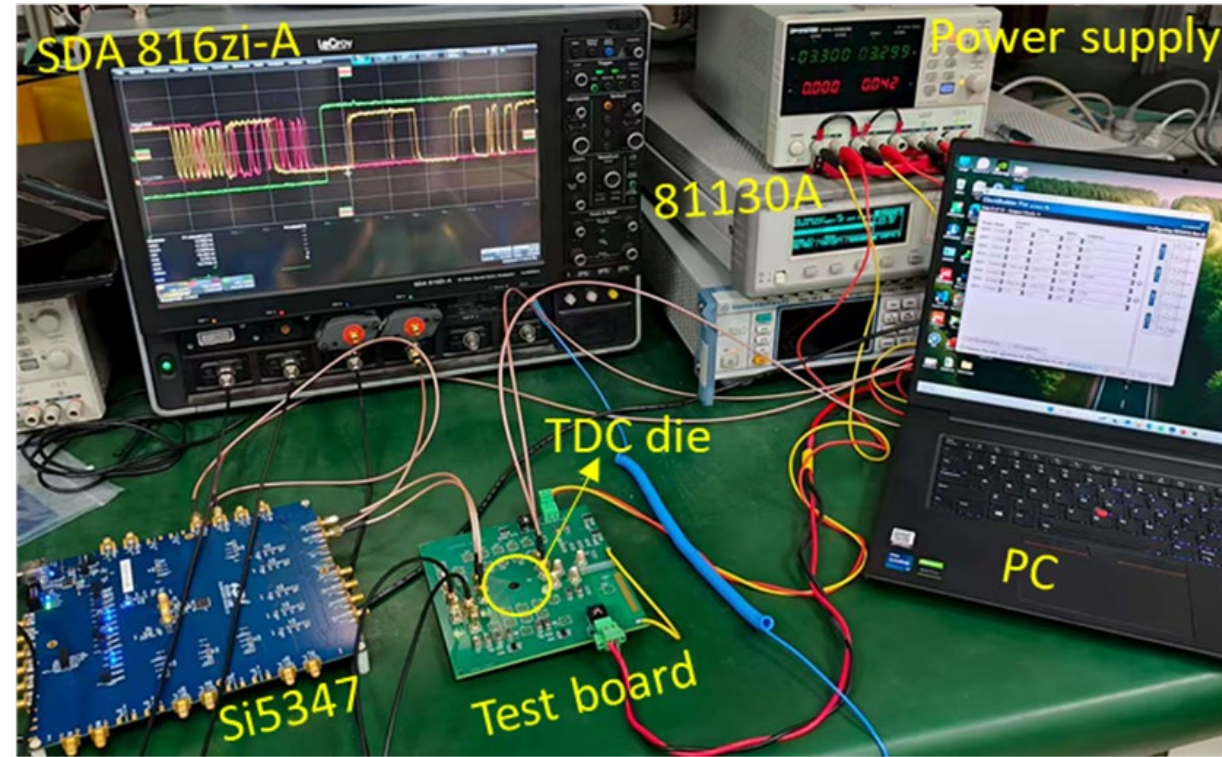
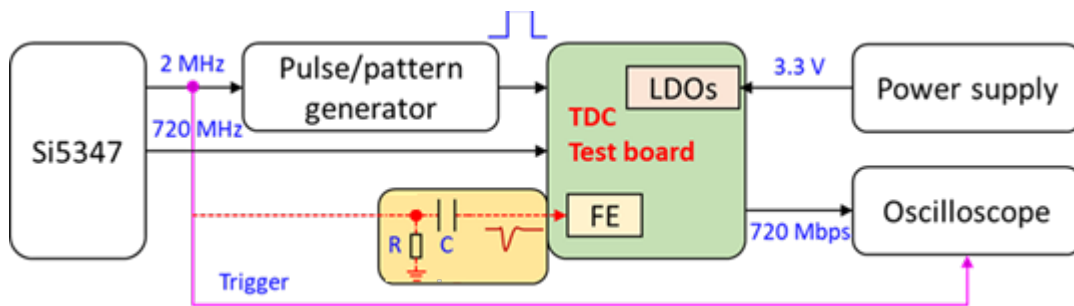
■ Test Setup

➤ Test-pulse mode

- A 720-MHz clock (Si5347) for both serializer and TDC.
- Inside divided down to 18 MHz as the reference clock for measurement.
- A 2-MHz clock (Si5347) to trigger a pulse/pattern generator (81130A).
Scanning TOA and TOT transfer curves by adjusting the pulse delay and width independently.

➤ FE-mode

- For functional verification of the FE-TDC integration.

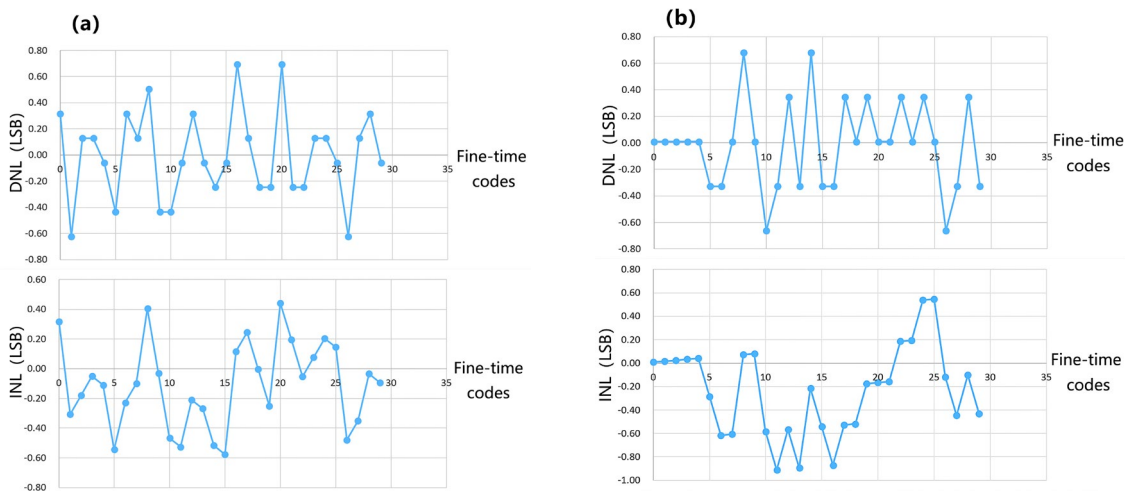


Test setup

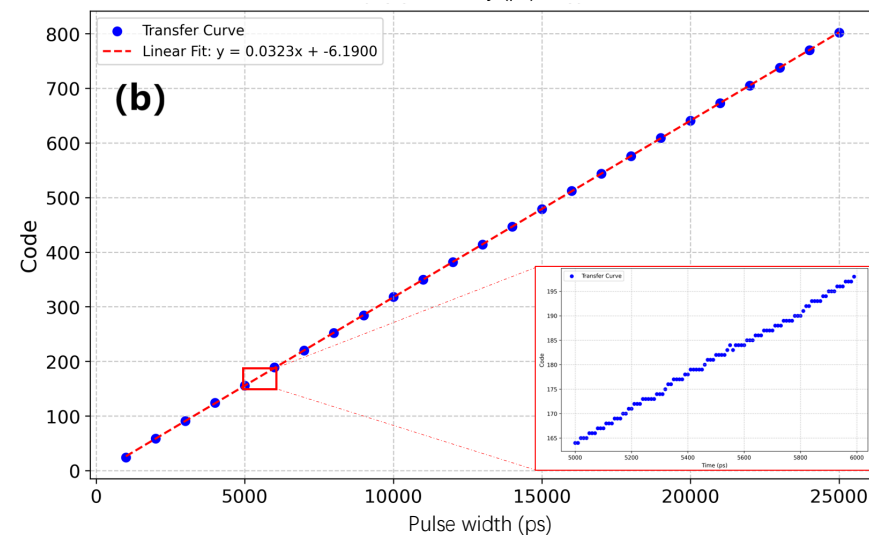
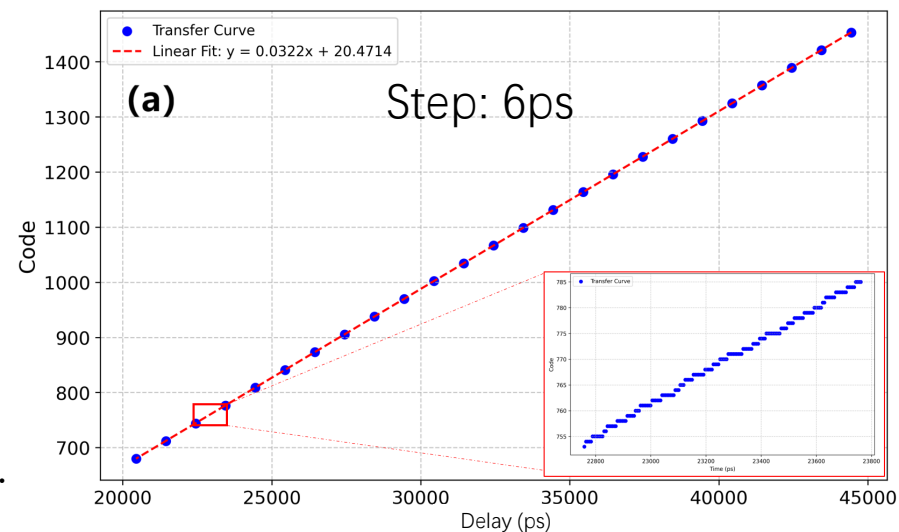
■ Timing performance (test-pulse mode)

- $LSB_{toa} \approx 31.1$ ps;
- The TOA DNL and INL without FE : less than ± 1 LSB;
- $LSB_{tot} \approx 31.0$ ps ;
- The TOT DNL and INL without FE : less than ± 1 LSB;

- $LSB_{cal} \approx 31.1$ ps ;
- These three LSB are very close, indicating the effectiveness of the self-calibration.



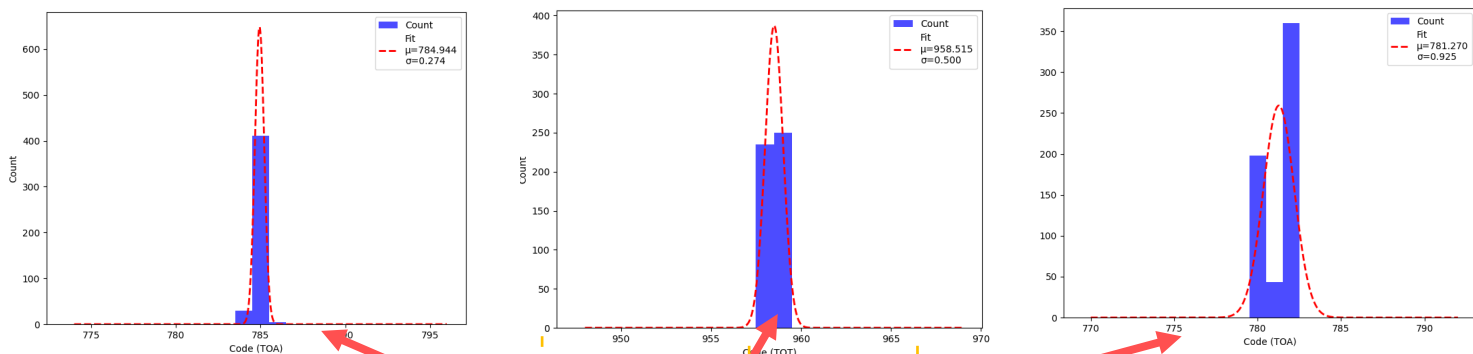
DNL & INL of: (a) TOA; (b) TOT



Measured transfer curves of: (a) TOA; (b) TOT

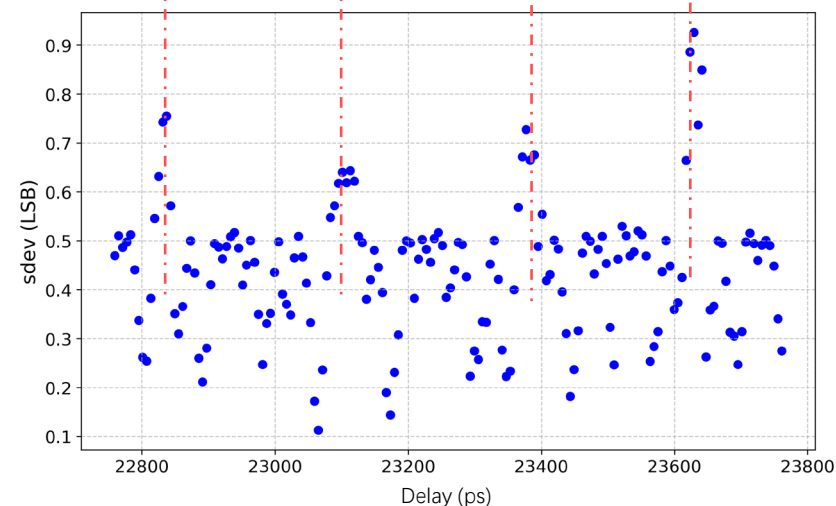
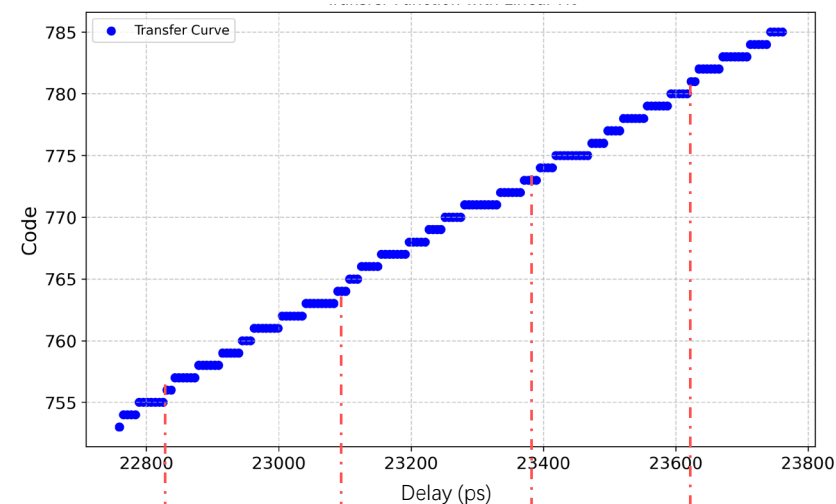
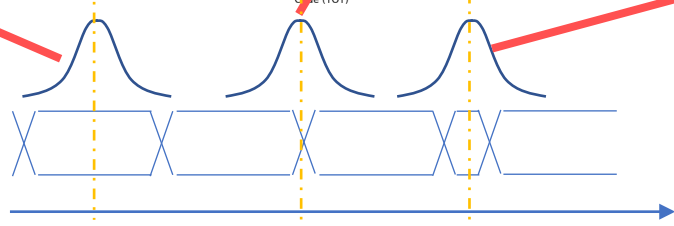
Timing performance (test-pulse mode)

- $\sigma < 0.5$ LSB for most steps
- For $\sigma > 0.5$ LSB:
 - It happens at place with smaller bin width.
 - The code varies more to the jitter of the input for smaller bin width.



TOA_latch (distribution)

Code
Time



The standard deviation of Single Shot Precision

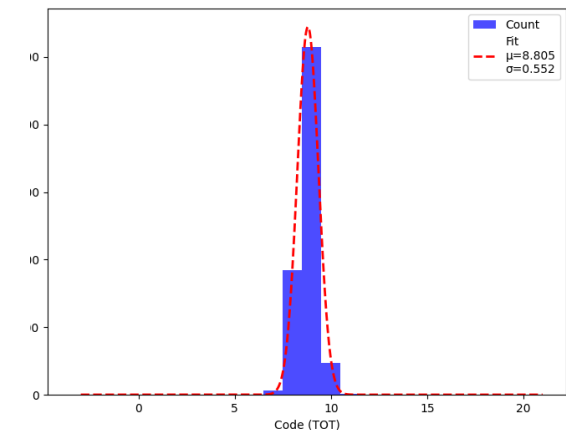
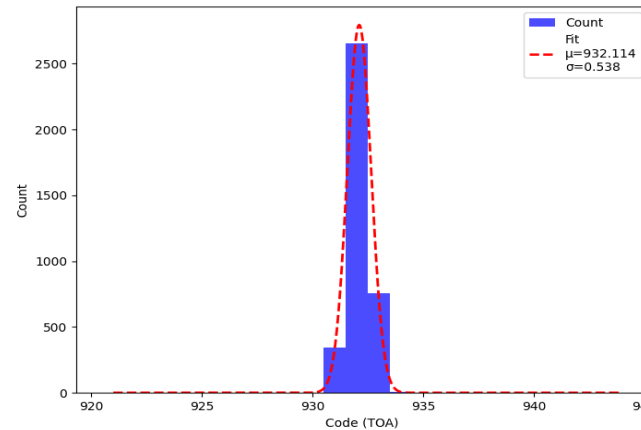
■ Timing performance (FE-mode)

- $\sigma_{\text{FE-TOA}}$ and $\sigma_{\text{FE-TOT}}$ distributions < 0.55 LSB for a 8.0 mV (8fC) input signal.

■ Power consumption

- The FE consumes 4.9 mA (1.2V).
- The power consumption of the TDC core varies with event rate.
- The total power consumption is measured to be 6.24 mW at an event rate of 1 MHz.

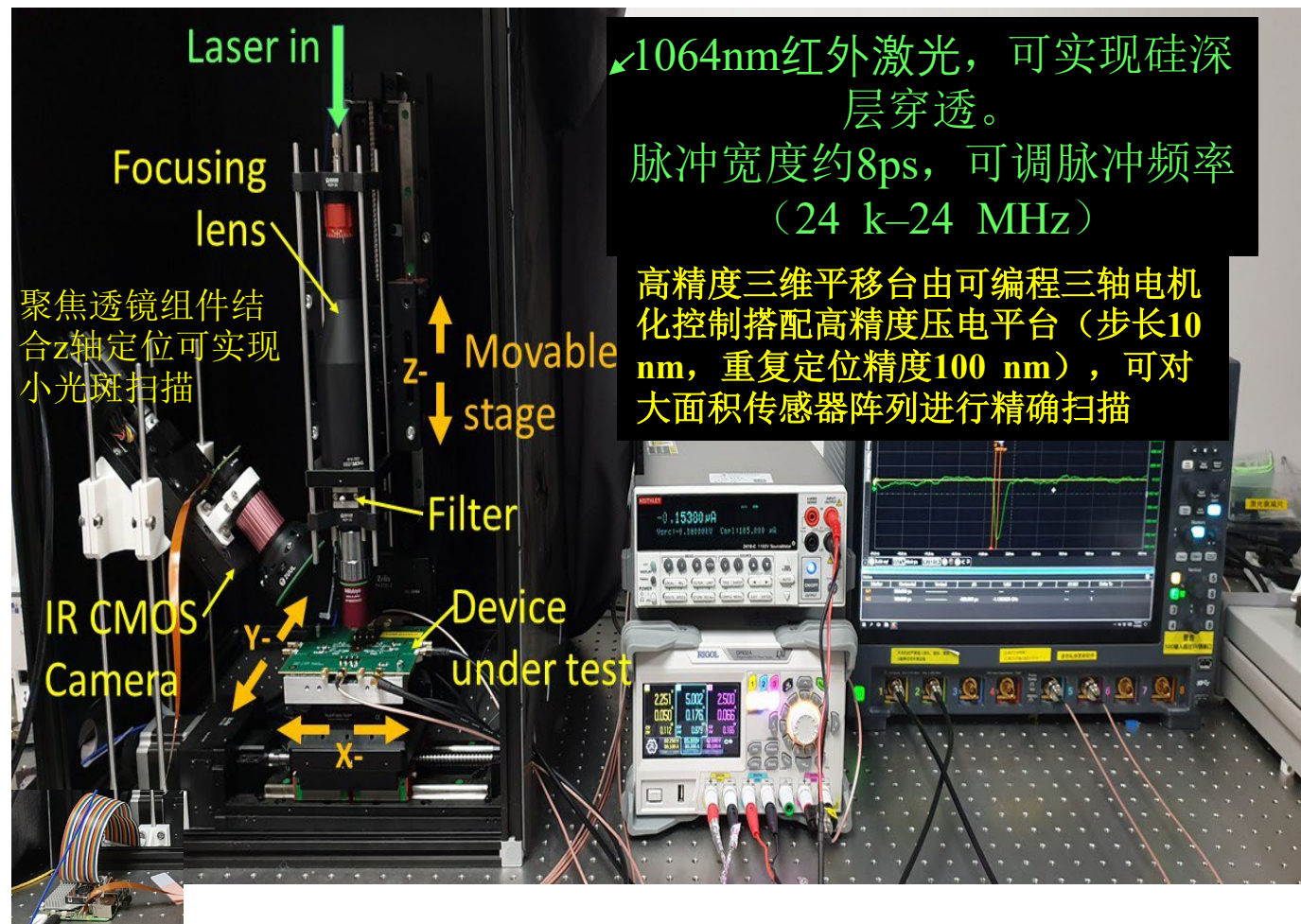
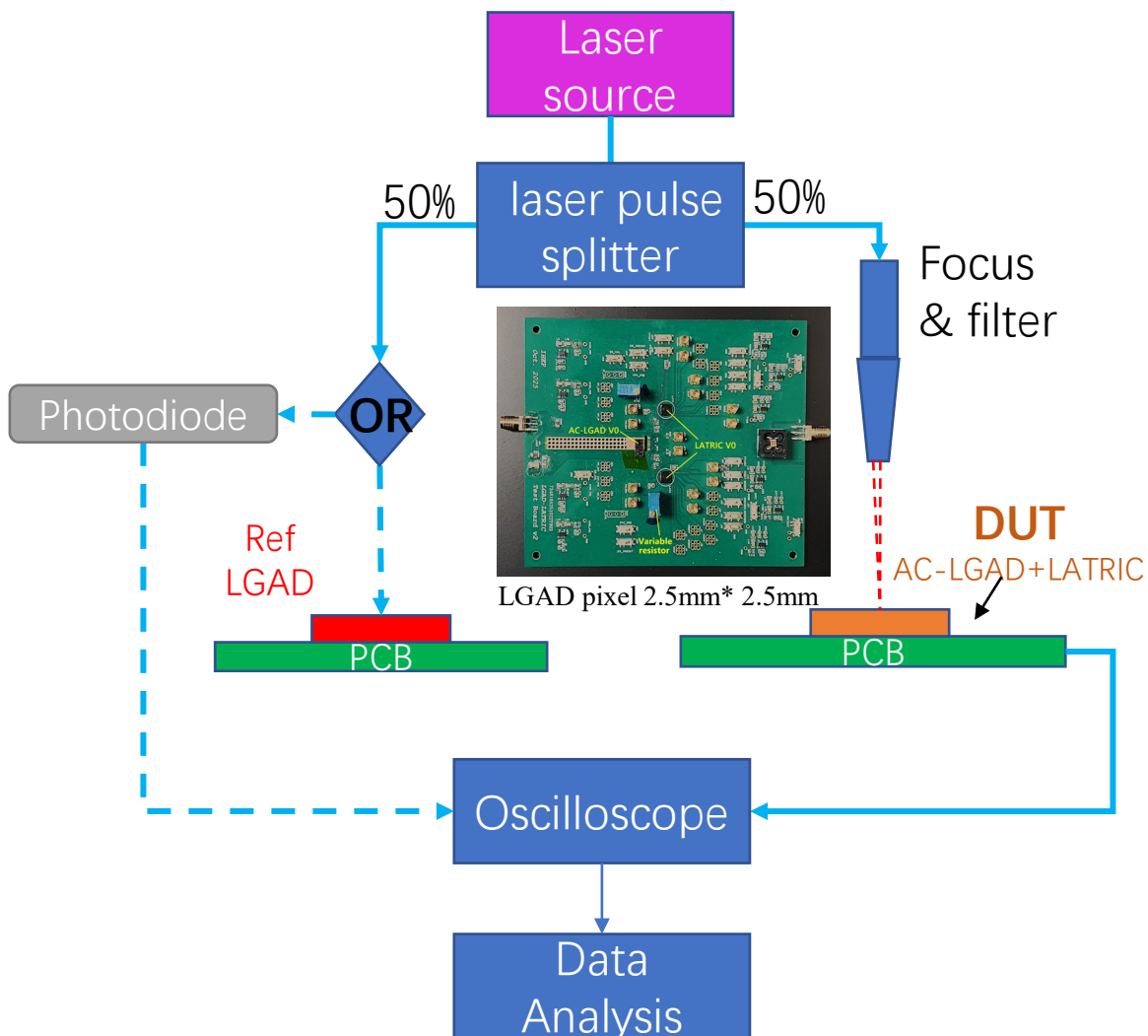
Blocks	Event rate	Operating current
TDC part	2 MHz	~ 0.5 mA
	1 MHz	~ 0.3 mA
	500 kHz	~ 0.1 mA
Pre-amplifier		~4.9 mA



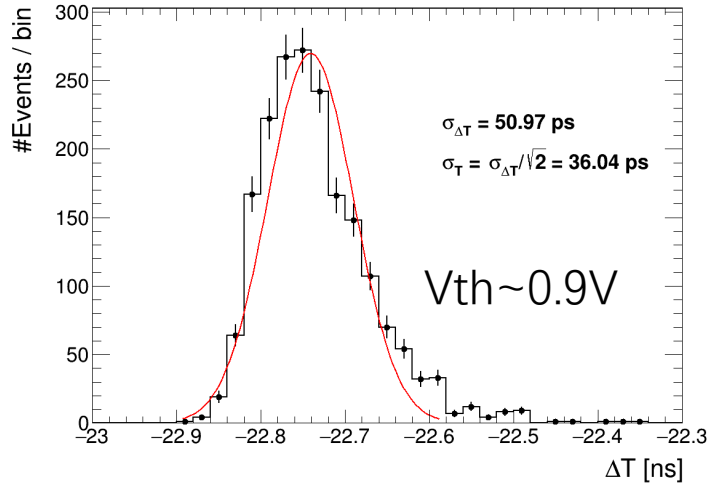
The statistical standard deviation for single shot
(input 8fC, $V_{\text{th}}=830\text{mV}$)

Time measurement step up

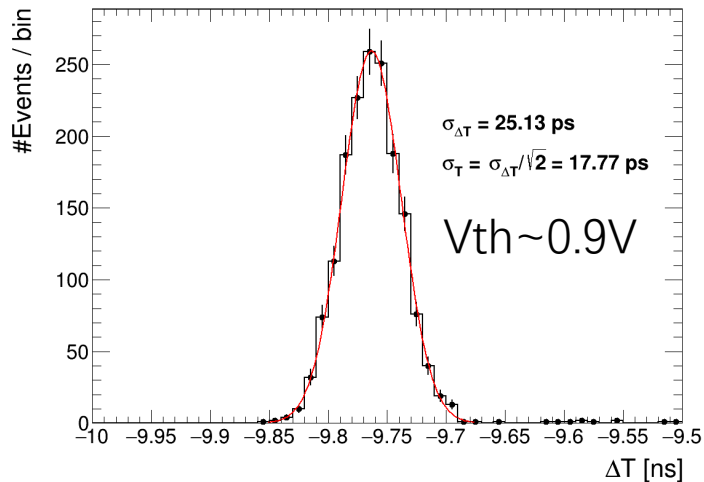
Transient Current Technique, TCT



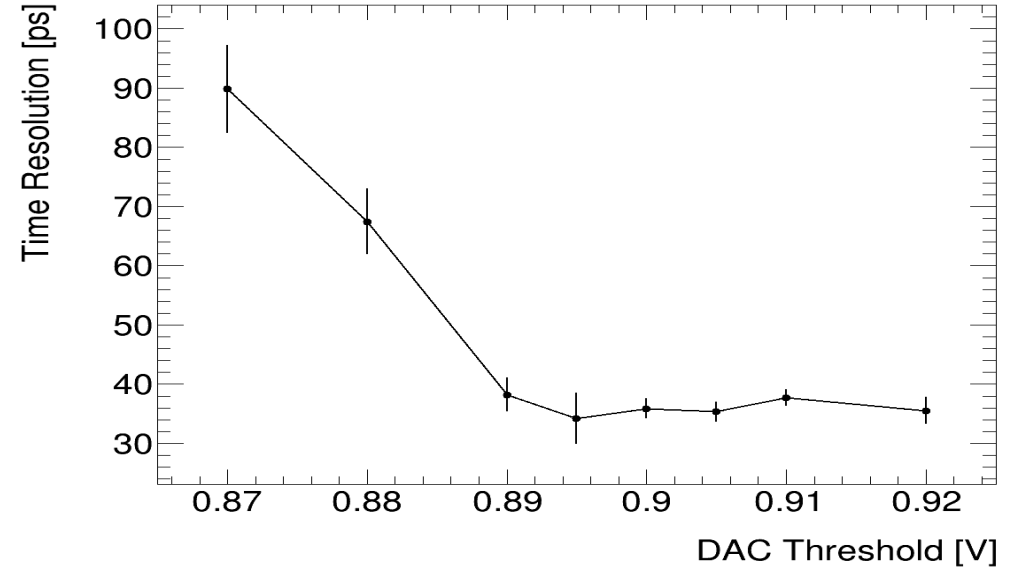
Coincidence test (LGAD+LATRIC0)



TOA coincidence time resolution @
Laser intensity equivalent to MIP



TOA coincidence time resolution
@ 100% laser intensity

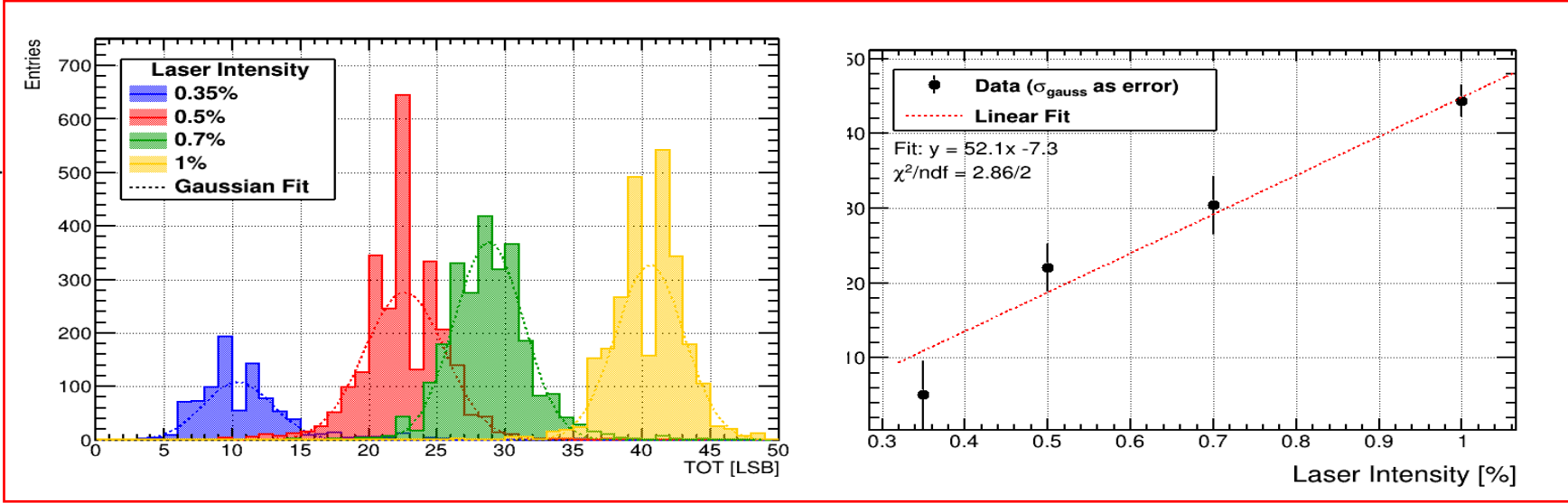


- The resolution decreases with threshold with an equivalent MIP laser.

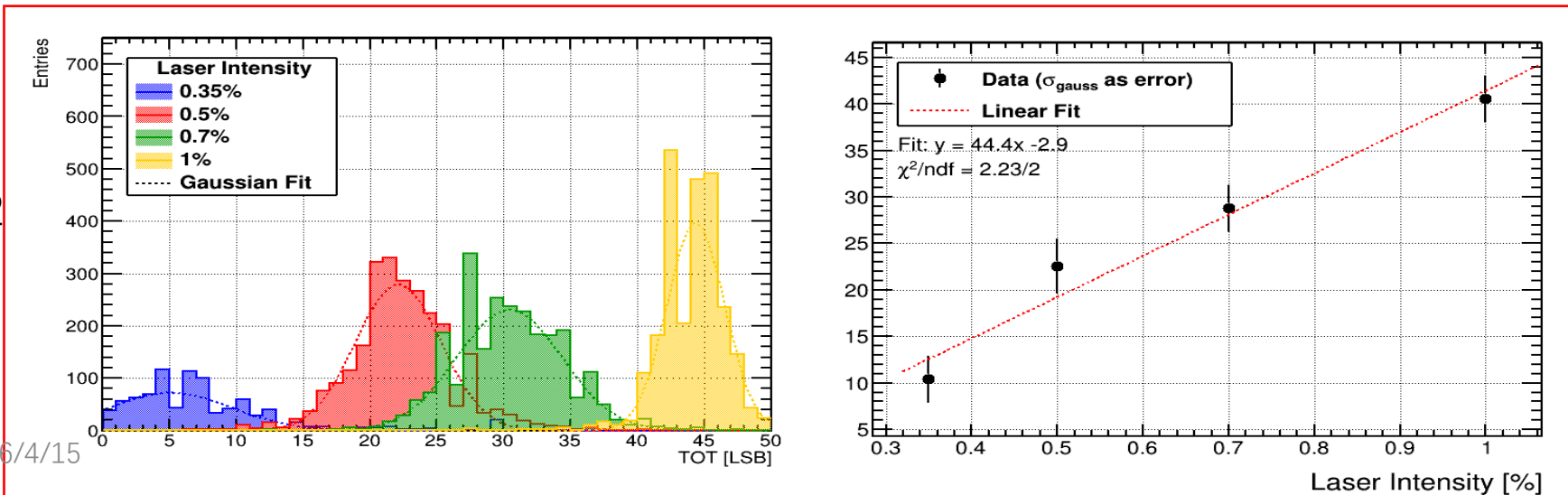
TOT with different Laser intensity

◆ TOT changes with the laser intensity, more study needed

LATRICO-1



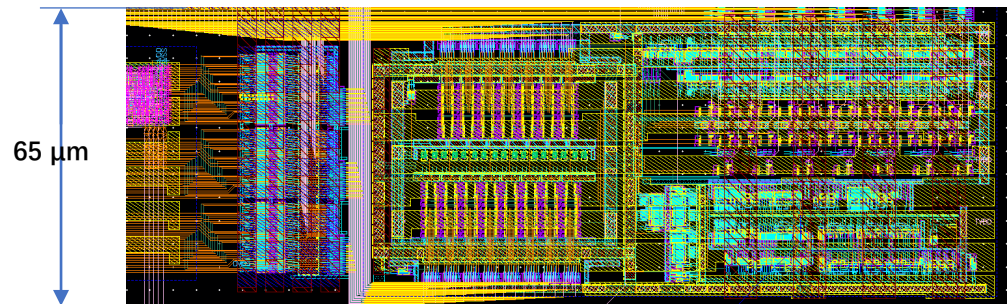
LATRICO-2



LATRIC1

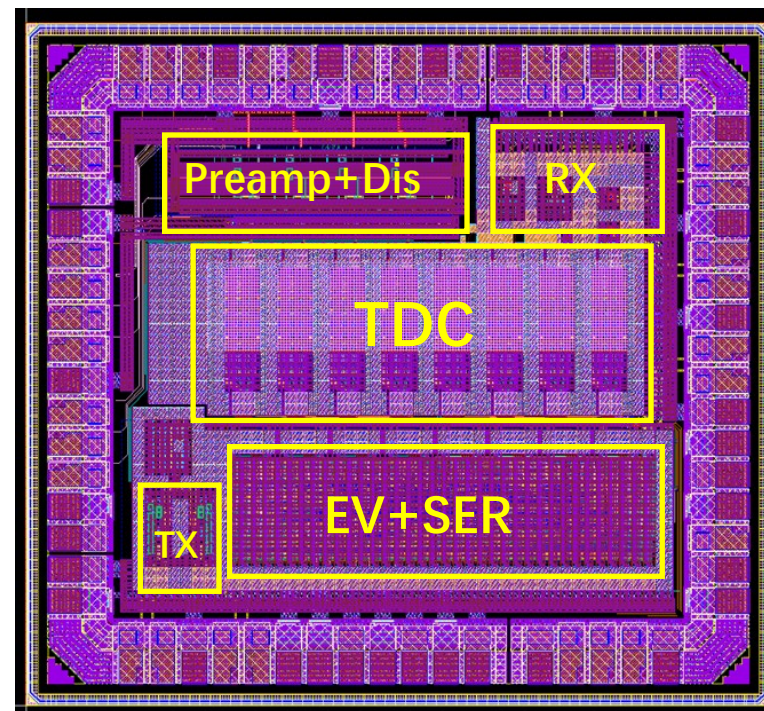
■ LATRIC0

- Successful integration of FE and TDC in LATRIC0
- High timing precision with low power consumption
- Effective self-calibration with consistent LSB values
- Meets CEPC requirements for OTK readout, including the height constrain of layout.



■ LATRIC1

- Submitted for tape-out in October 2025, received in Feb, 2026
- 8 channels; 4 channels with front-end; 2 kinds of delayline
- Increase the gain of preamplifier;
- Improve the encoder logic;
- Add event builder and timestamp;
- 100 μm channel pitch match the LGAD.

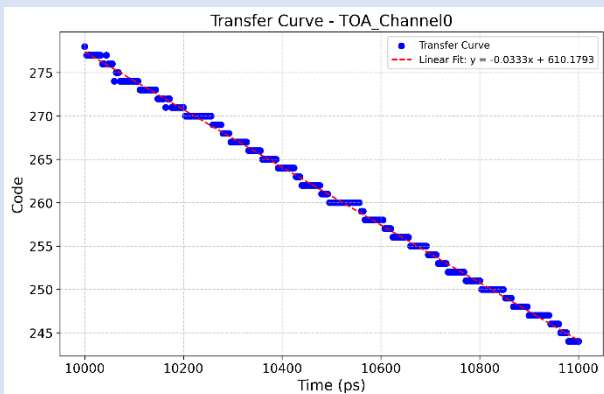


LATRIC1 layout

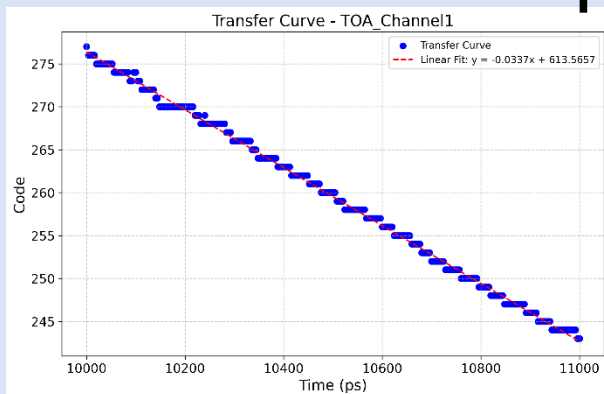
LATRIC1 Test - Transfer Curve

◆ Resolution(LSB): CH0 ~29.80 ps , CH1 ~ 29.44 ps, CH2 ~ 27.09 ps, CH3 ~ 27.58 ps (step: 4ps)

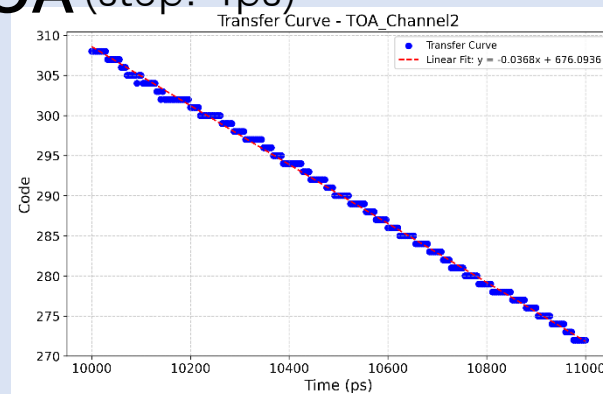
TOA (step: 4ps)



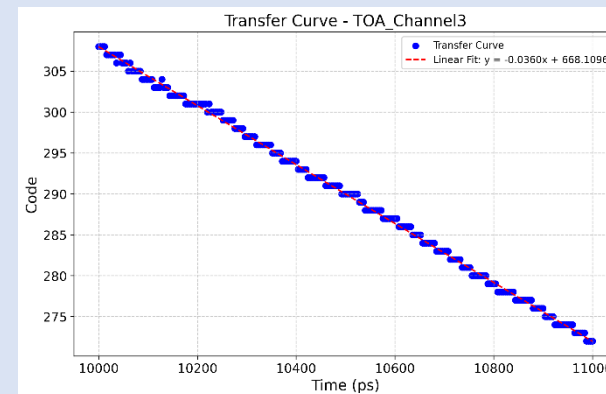
Channel0



Channel1

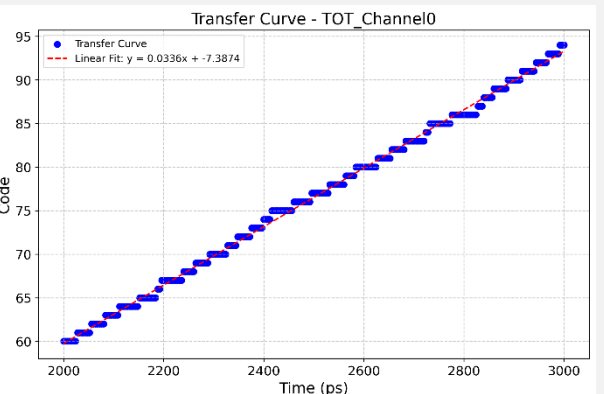


Channel2

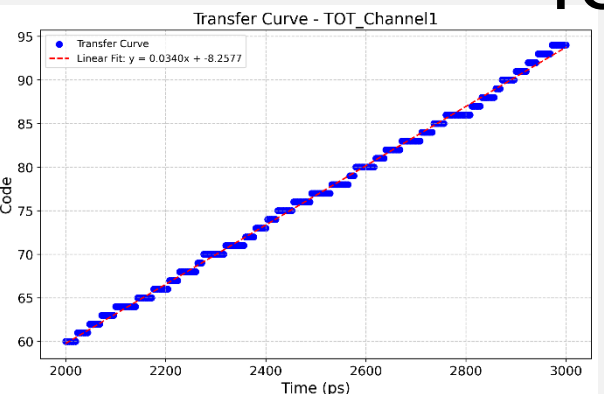


Channel3

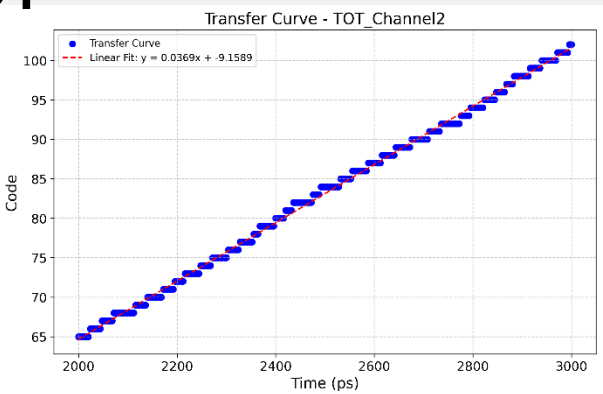
TOT



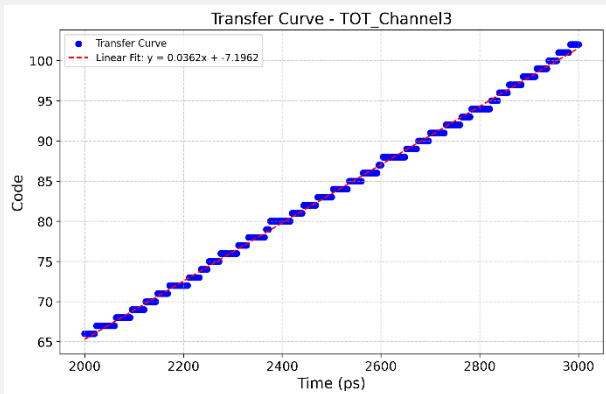
Channel0



Channel1



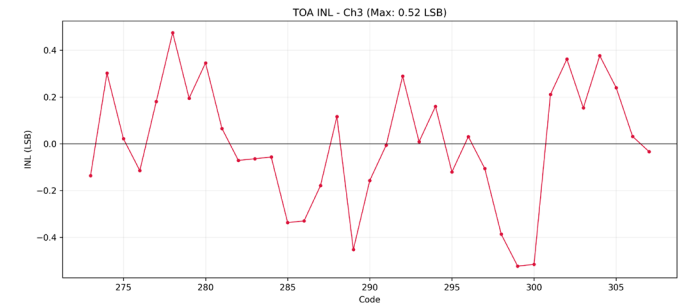
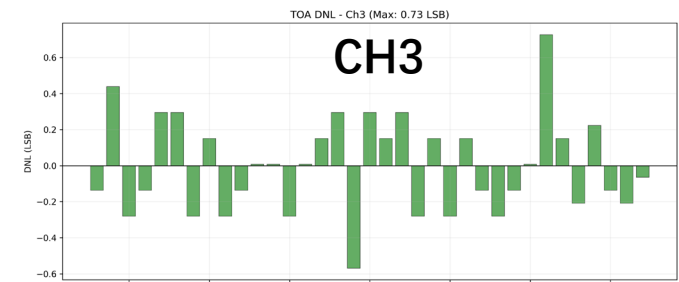
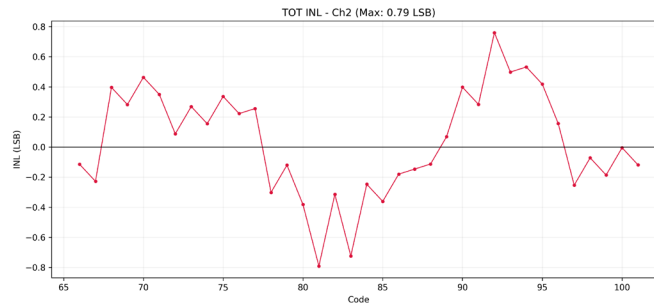
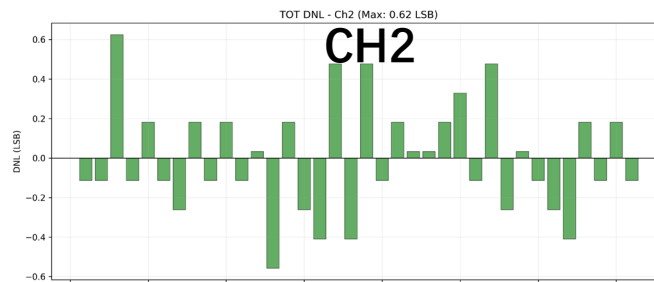
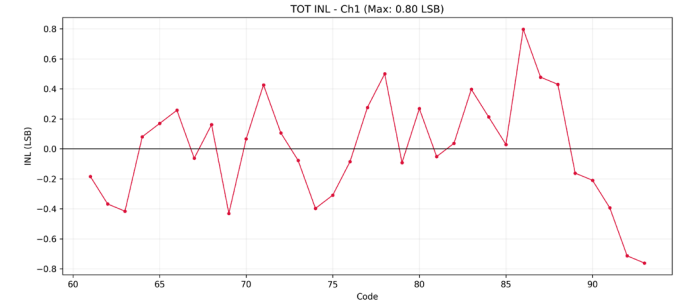
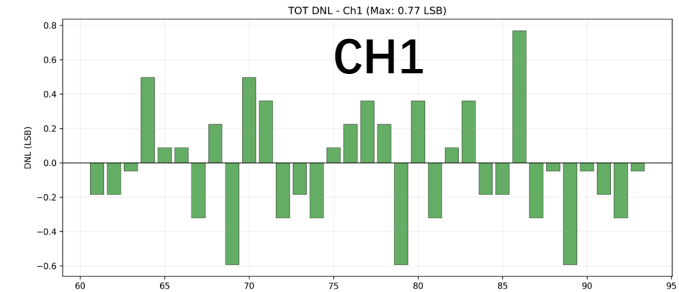
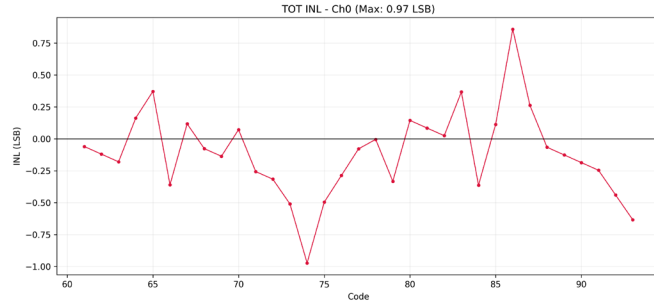
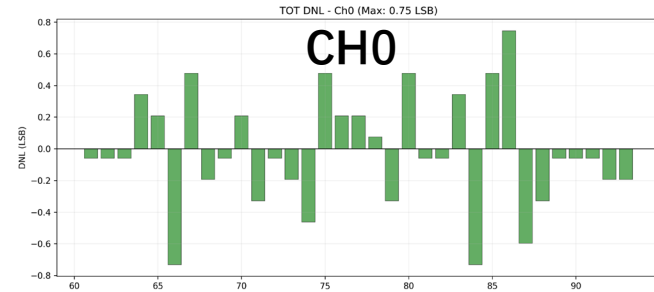
Channel2



Channel3

LATRIC1 Test - Linearity

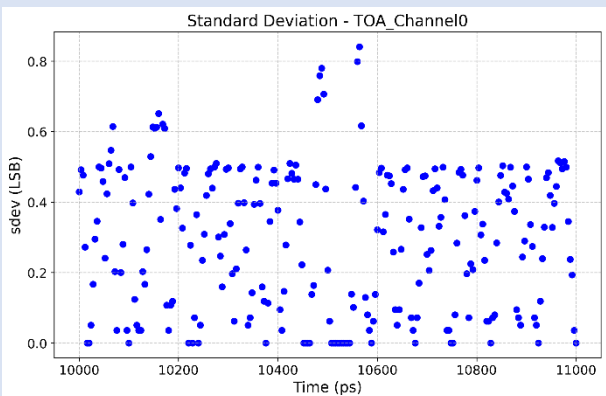
- CH0
 - INL: ± 0.97 LSB
 - DNL: ± 0.75 LSB
- CH1
 - INL: ± 0.77 LSB
 - DNL: ± 0.80 LSB
- CH2
 - INL: ± 0.79 LSB
 - DNL: ± 0.62 LSB
- CH3
 - INL: ± 0.52 LSB
 - DNL: ± 0.73 LSB



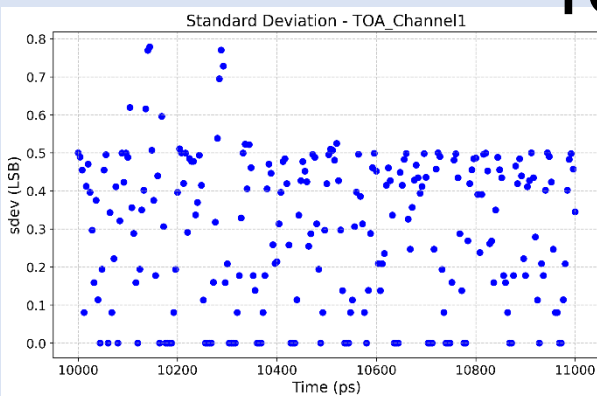
LATRIC1 Test - Single Shot Precision

◆ $\sigma_{\text{TOA}} \sim 0.5 \text{ LSB}$, $\sigma_{\text{TOT}} \sim 0.5 \text{ LSB}$

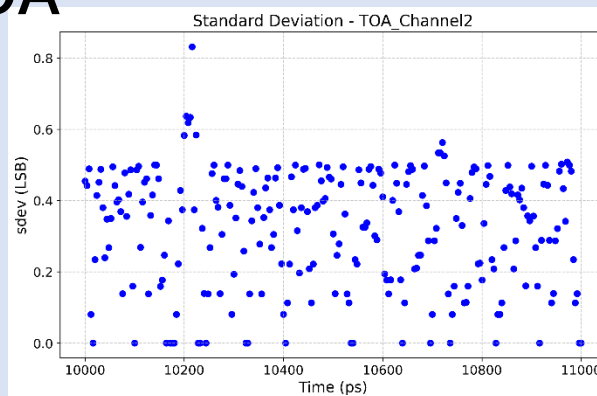
TOA



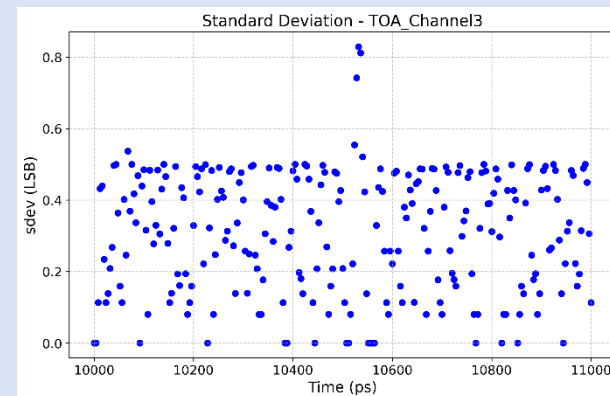
Channel0



Channel1

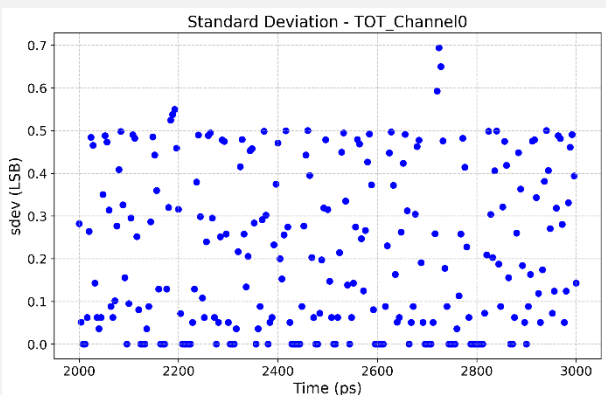


Channel2

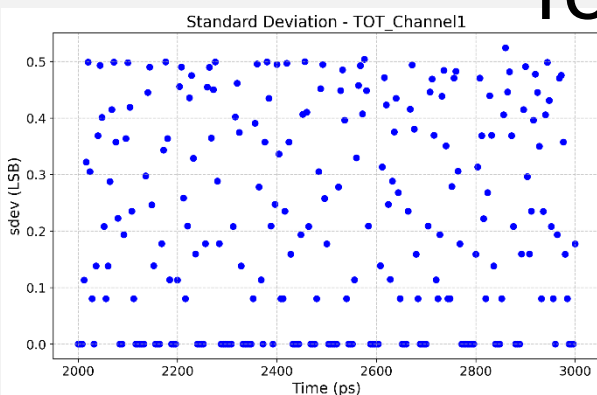


Channel3

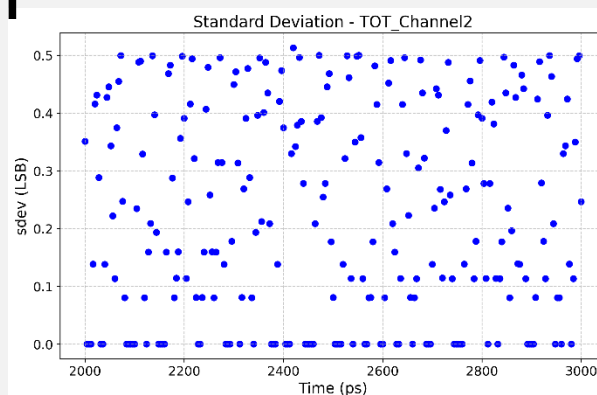
TOT



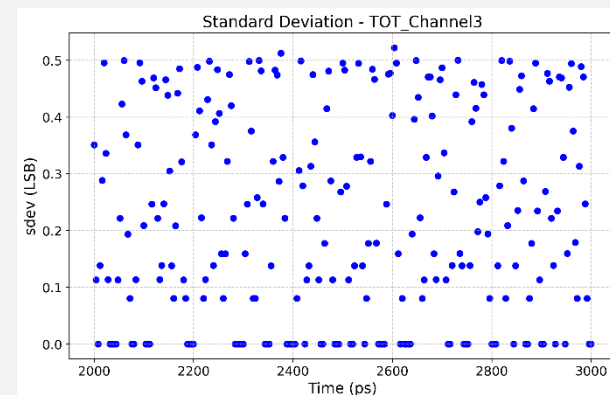
Channel0



Channel1



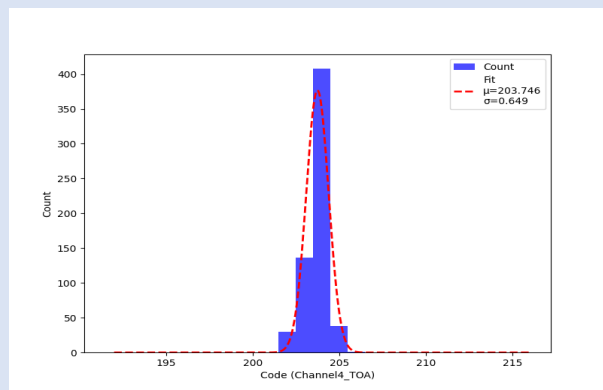
Channel2



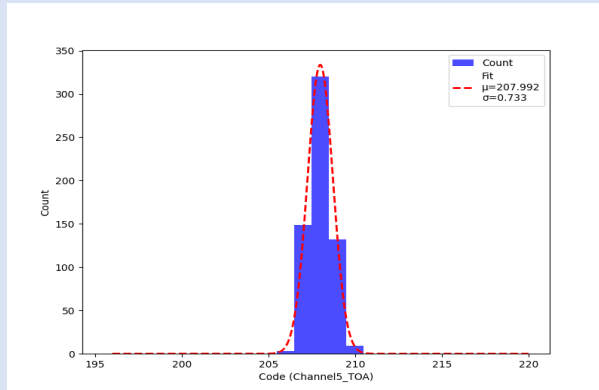
Channel3

◆ $\sigma_{TOA} < 0.77$ LSB, $\sigma_{TOT} < 1$ LSB @ 8fC input. 4 channels share same Vth

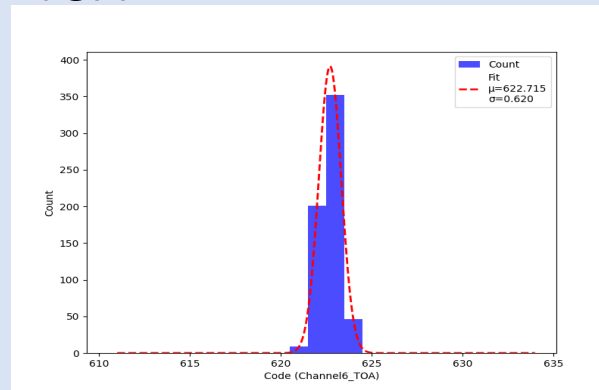
TOA



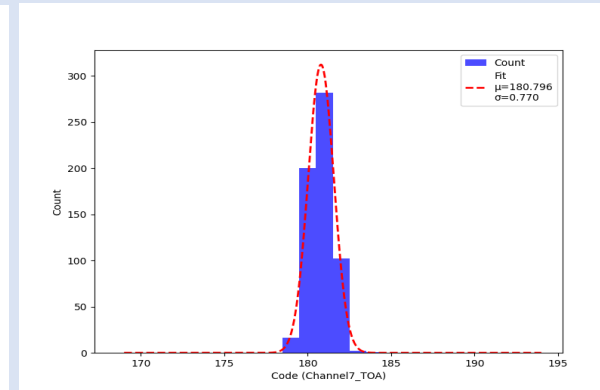
Channel4



Channel5

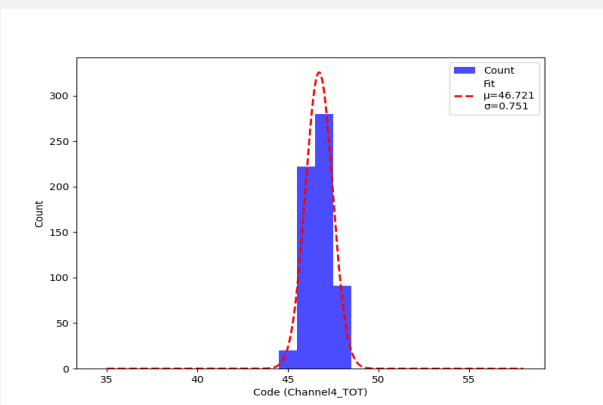


Channel6

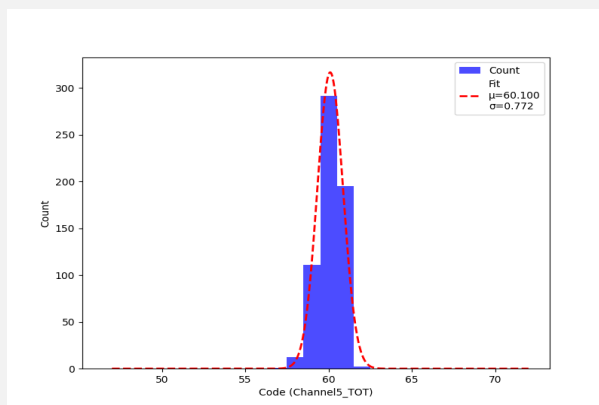


Channel7

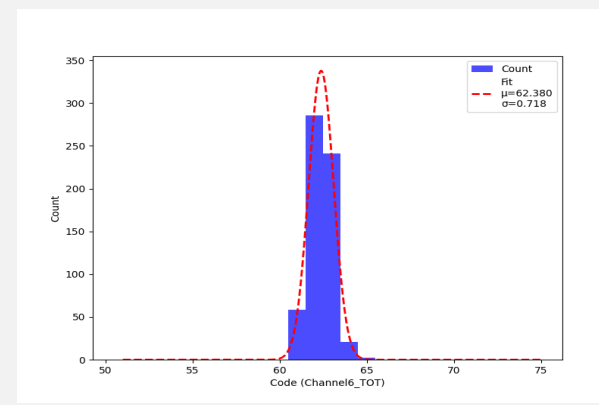
TOT



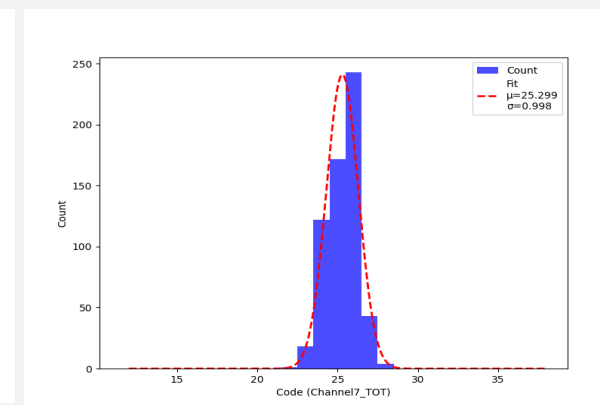
Channel4



Channel5



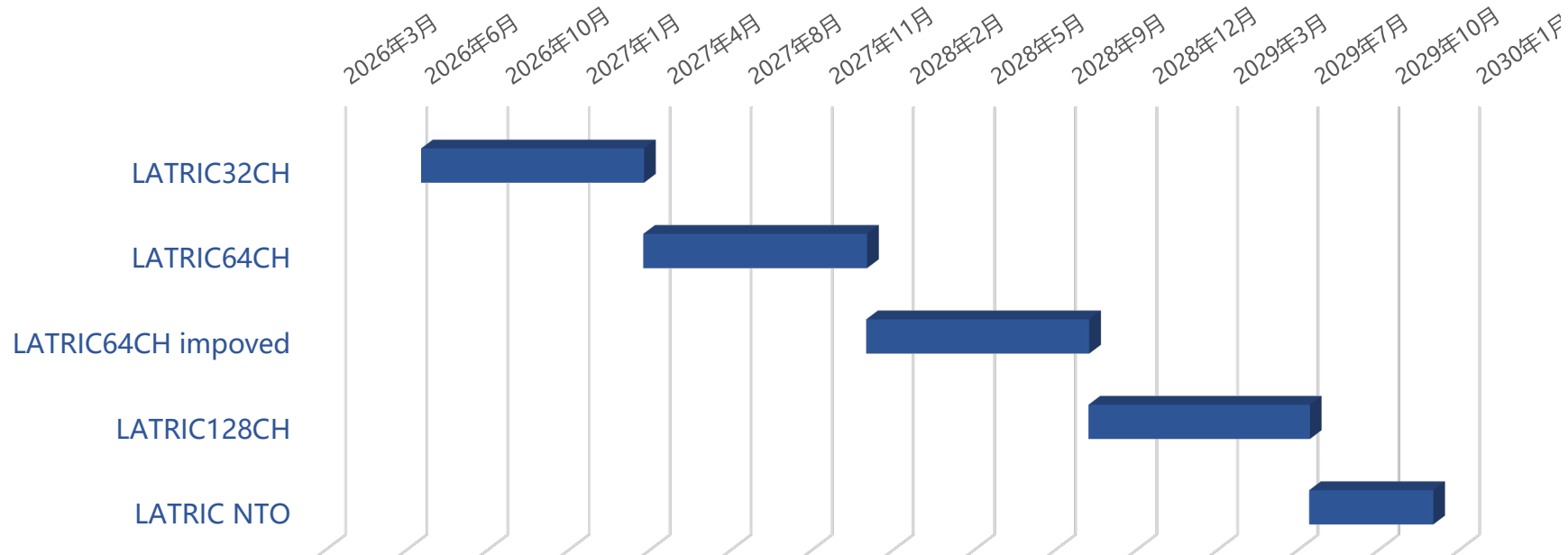
Channel6



Channel7

Conclusion

- ◆ LATRIC0 time resolution is proved with pixel LGAD by Laser, while performance test by β is ongoing.
- ◆ Spatial test system is debugging.
- ◆ LATRIC1 time performance is proved preliminarily, need more study.



Thank you!