Summary of SiPM discussions at the Lisbon workshop

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On Behalf of Colleagues
15-4-2026

Content

SiPM requirement

- SiPM requirement for CEPC detectors: ECAL, HCAL, muon, Cherenkov detector

	ECAL	GS-ECAL	HCAL	Cherenkov detector
Sensor size	3mm×3mm	3mm×3mm	3mm×3mm	1x1 mm^2(one readout for each SiPM); or 3x3 mm^2or 6x6 mm^2(with charge sharing readout)
Pixel size	6μm	20μm	20μm	50μm
Wavelength	350- 600 nm	350 – 600 nm	350 – 600 nm	>300 nm
PDE	>30% (@ 420-480nm)	≥45% (@400nm)	≥45% (@400nm)	50% (@420nm)
Gain	~10^5	≥5×10^5	≥5×10^5	~10^6
DCR	≤ 150 kHz/mm²	≤ 150 kHz/mm²	≤ 150 kHz/mm²	<100~200 kHz /mm²
Cross talk	<1%-3%	<1%-5%	<1%-5%	<1%-5%
Radiation hardness	100 krad and 10^{11} n_{eq}/cm^2 per year	100 krad and 10^{11} n_{eq}/cm^2 per year	N/A	100krad /year $1x10^{12}$-$1x10^{13}$ N_{eq}/cm^2 for 10 years running
Timing resolution				100-200ps, spatial resolution~300μm
Number of SiPM	57.1 *10k	430*10k	520 *10k	17 *10k(3x3mm^2)

Refer to Zhijun, Yong Liu, Hengne, Yuekun and Zhonghua's talk at CEPC workshop

Results of SiPM candidates

	ECAL requirement	**NDL EQR06**	**NDL EQR10**	**HPK S14160-3010PS**
Sensor size	**3mm×3mm**	3mm×3mm	3mm×3mm	3mm×3mm
Pixel size	**6µm**	6µm	10µm	10µm
Wavelength	**350–600nm**			
PDE	**>30% (@ 420-480nm)**	30% (@420nm)	36% (@420nm)	18% (@460nm)
Gain	**$\sim 10^5$**	8×10^4	1.7×10^5	1.8×10^5
DCR	**$\leq$ 100 kHz/mm^2**	2.5 MHz	3.6 MHz	700 kHz
Cross talk	**<1%-3%**	12%	N/A	<1%
Capacitance (pF)		45.9 pF	31.5 pF	530 pF

Improvement: small pixel size(6 µm) with lower cross talk

Refer to Zhijun, Yong’s talk at CEPC workshop

Results of SiPM candidates

	HCAL requirement	**HPK S14160-3015PS**	**HPK S14160-3050PS**	**NDL EQR20-11-3030-S**	**JBT JSP-TP3050-SMT**
Sensor size	**3mm×3mm**	3mm×3mm	3mm×3mm	3mm×3mm	3mm×3mm
Pixel size	**20μm**	15μm	50μm	20μm	50μm
Wavelength	**350–600nm**				
PDE	**≥45% (@400nm)**	32%(@450nm) 27% (@400nm)	50%(@450nm) 47% (@400nm)	47.8%(@420nm) 45% (@400nm)	35%(@420nm) 33% (@400nm)
Gain	**$\geq 5\times10^5$**	3.6×10^6	2.5×10^6	8.0×10^5	2.1×10^6
DCR kHz/mm²	**≤ 150**	700-2100	10-100	150-450	120-270
Cross talk	**<1%-5%**				
Capacitance (pF)		530	500	157.5	170(fF)

Improvement needed: high PDE

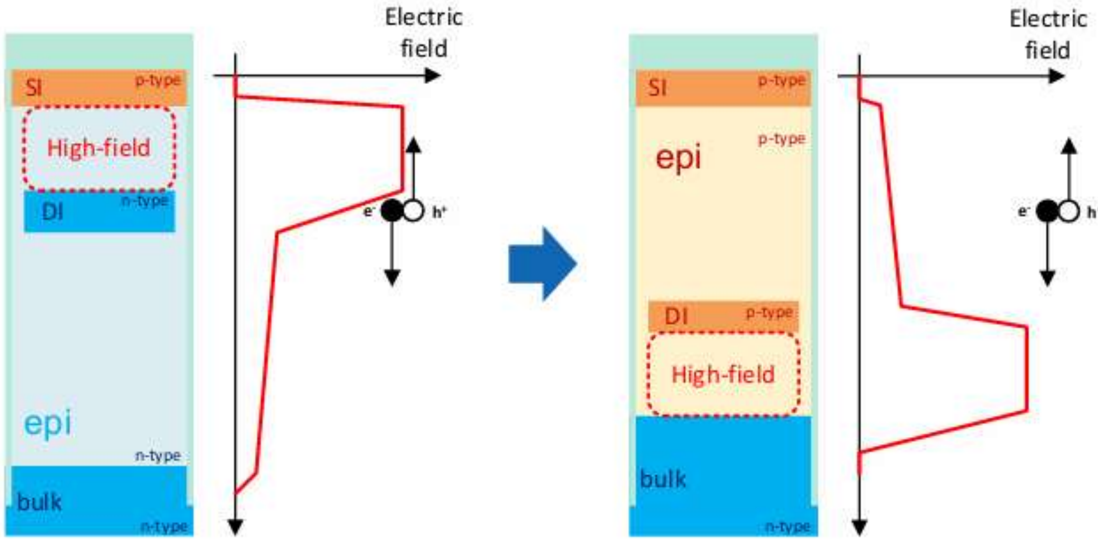
Refer to Zhijun, Hengne's talk at CEPC workshop

Technologies: NUV-DJ development

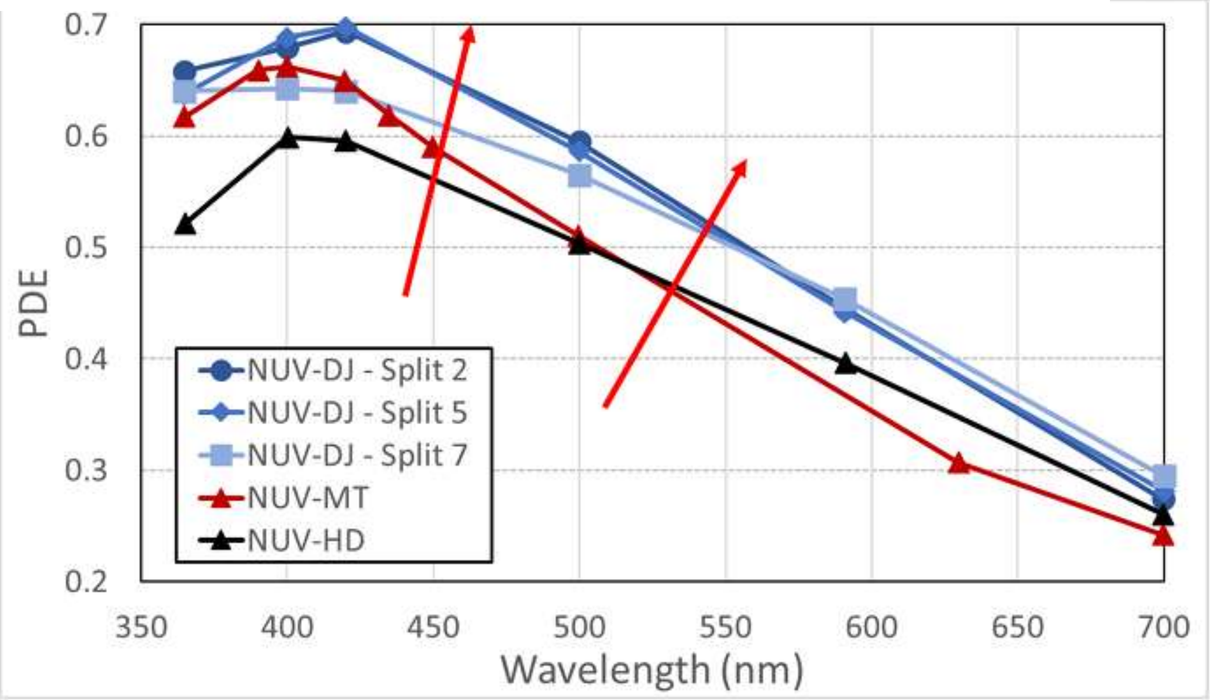
FBK

Alberto Gola's talk

By moving the high-field region towards the bottom of the epitaxial layer, the PDE is enhanced. Avalanche is mostly triggered by electrons.



Conceptual drawing of the different NUV.MT and NUV-DJ microcell structures (cross-sections, not to scale)

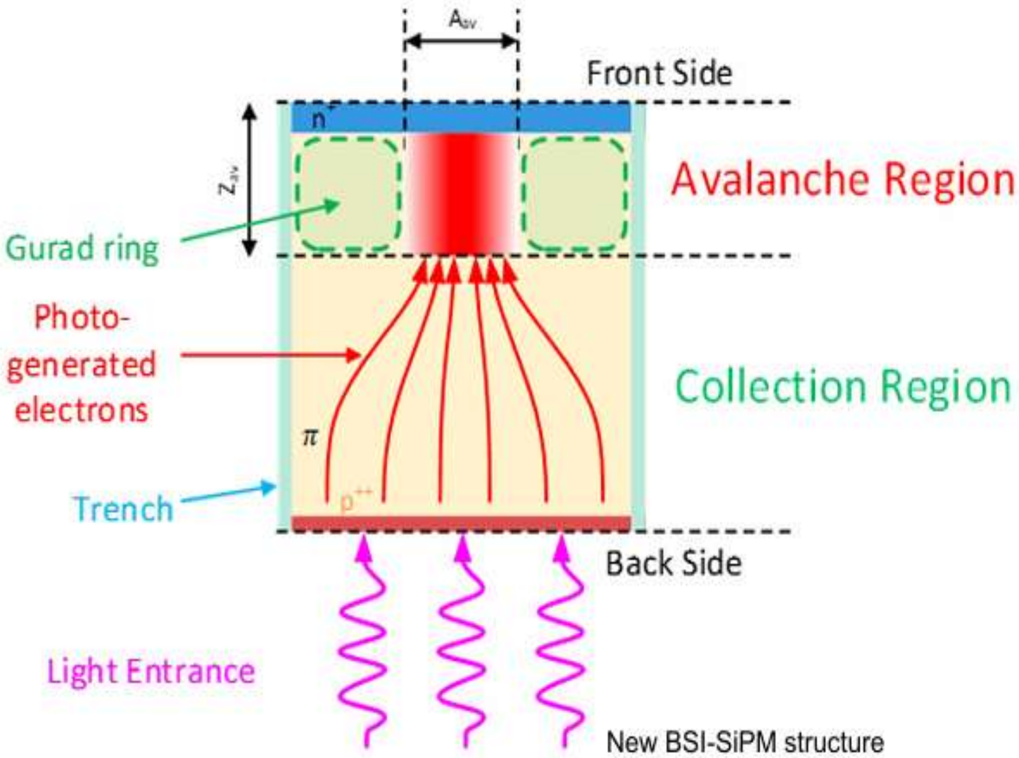


PDE vs. wavelength measured on the 45 μm cell of the NUV-HD-MT technology (12 V) and on the 40 μm cell of the NUV-HD and of the newly introduced NUV-DJ SiPM technologies (9 V).

P-type EPI on n-type wafer and High energy implantation (deep injection) for p-type layer

Technologies: Backside Illuminated SiPMs

- DRD4: Rok Pestotnik’s talk
- FBK: Alberto Gola's talk



Potential Advantages:

- Up to 100% FF even with small cell pitch
- Ultimate Interconnection density: < 15 um
- High speed and dynamic range
- Low gain and external crosstalk
- (Uniform) entrance window on the backside, ideal for enhanced optical stack (VUV sensitivity, nanophotonics)
- Local electronics : ultra fast and possibly low-power

Development Risks:

- Full microcell depletion
- Charge collection time jitter
- Low Gain
- Effectiveness of the new entrance window

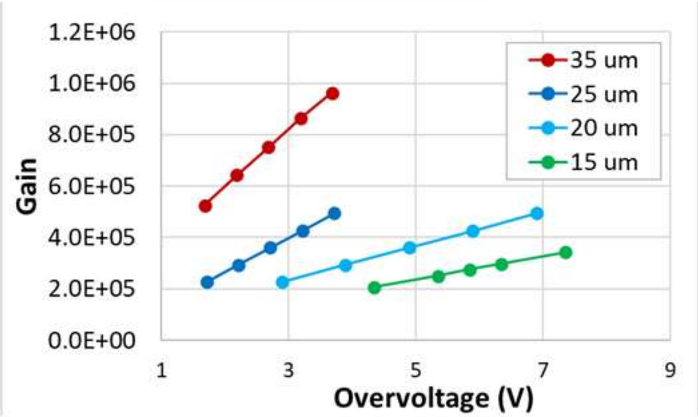
Double side process

Technologies: Backside Illuminated SiPMs

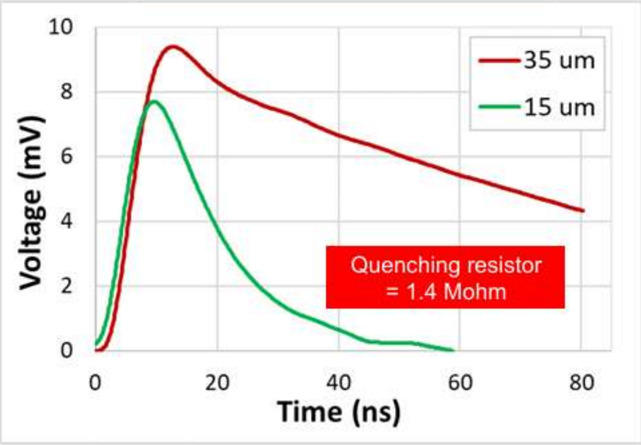
- FBK： Alberto Gola's talk

The gain and the recharge time constant of the microcells are significantly reduced

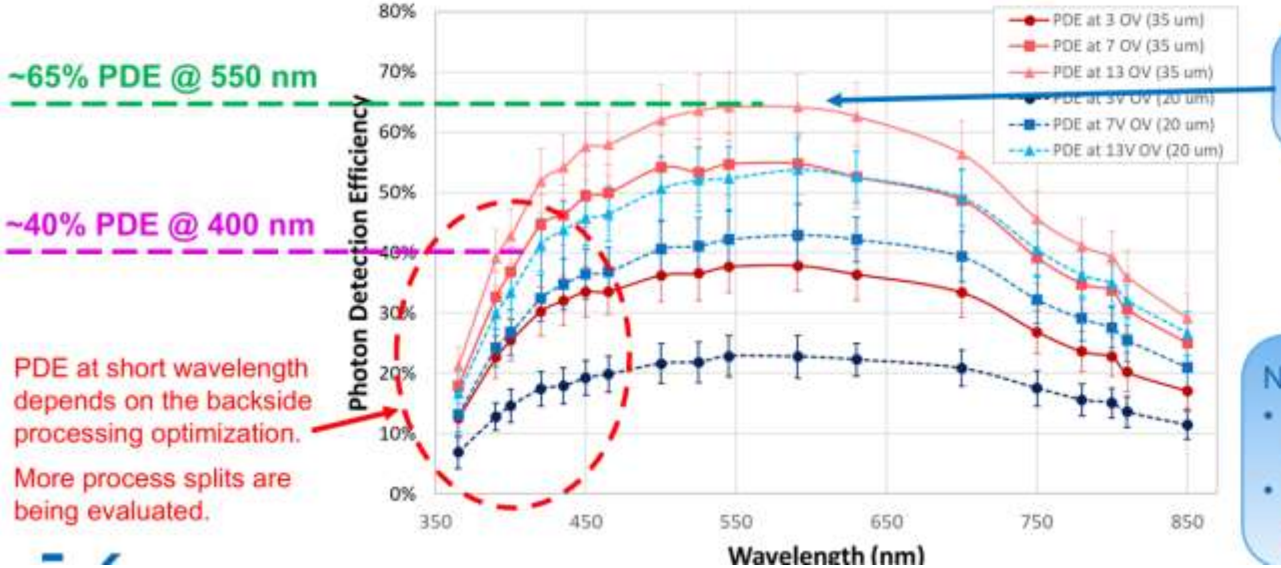
Avalanche Gain



Single cell response 15 µm cell



PDE spectrum at short wavelengths: optimization of the process for the formation of the backside entrance window.



~65% PDE @ 550 nm

~40% PDE @ 400 nm

PDE at short wavelength depends on the backside processing optimization.

More process splits are being evaluated.

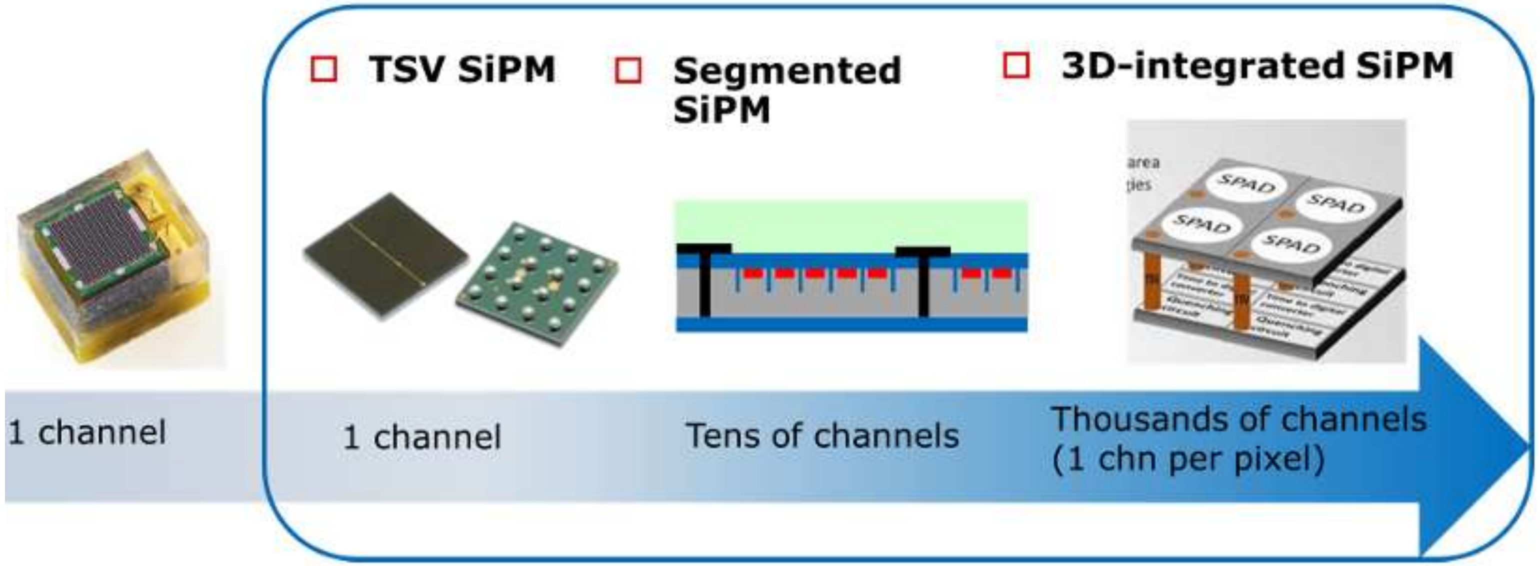
Metal-filled DTIs are crucial to achieve high Over-voltage

Next steps :
- Confirm depletion conditions
- Confirm PDE on **smaller cell sizes**

Technologies: 2.5D and 3D integrated SiPMs / SPADs

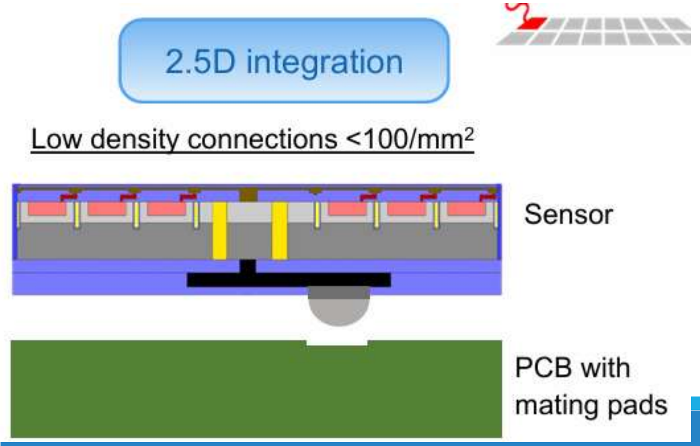
Integrate SiPM with readout electronics method: hybridization

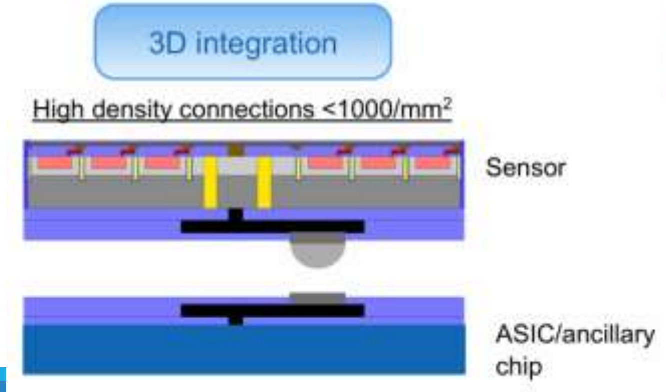
Alberto Gola's talk

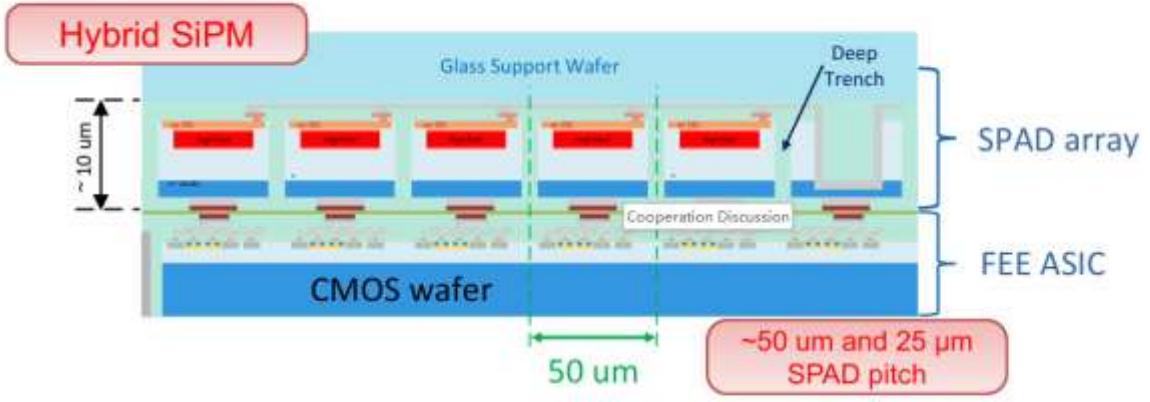


high-density interconnections to the front-end and high-segmentation

Interposer, TSV, bump bonding







Technologies: SPAD and Digital SiPM

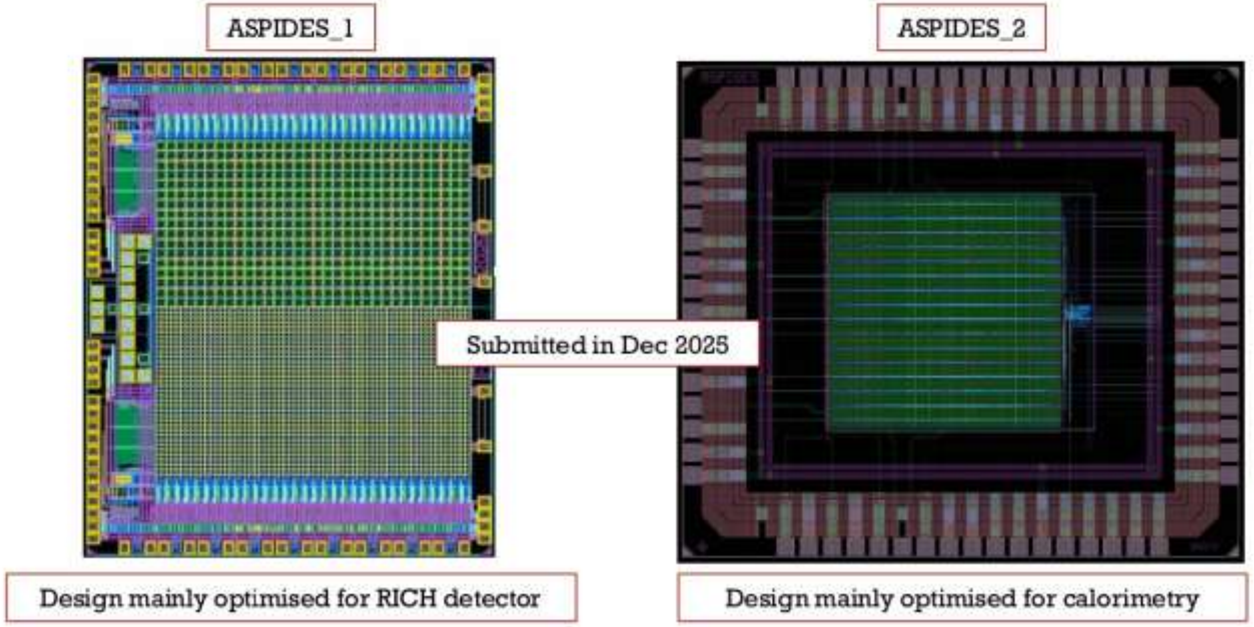
Integrate SiPM with readout electronics method: monolithic

Fill factor is affected by the readout electronics around the SPAD cell in one pixel

- INFN: CMOS SPAD and Digital SiPM Romualdo Santoro

  Lfoundry 110 nm CIS technology

A INFN-funded project to develop dSiPMs with single-photon sensitivity and embedded functionalities to meet the energy physics requirements


ASPIDES_1

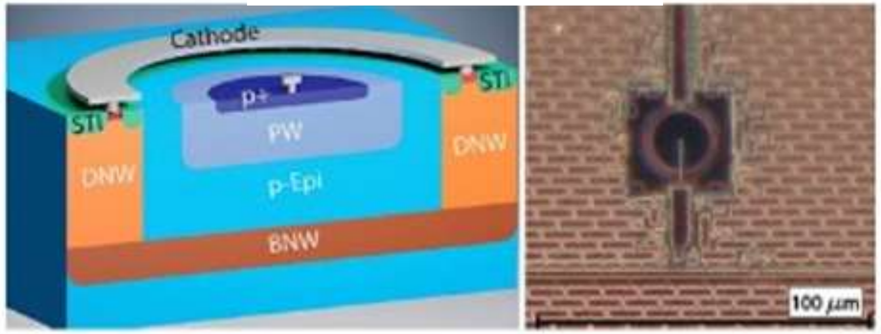
ASPIDES_2

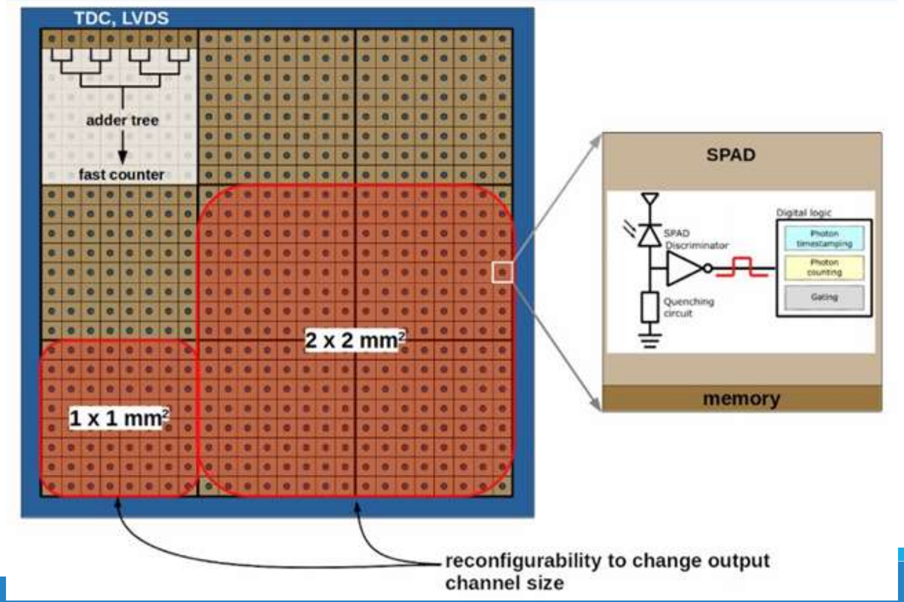
Submitted in Dec 2025

Design mainly optimised for RICH detector

Design mainly optimised for calorimetry

Rok Pestotnik's talk





reconfigurability to change output channel size

Cooperation Discussion

Discussion meeting on 9th April.

Participants: Alberto Gola(FBK), Romualdo Santoro(INFN)

IHEP: Miao He, Yong Liu, Zhonghua Qin, Zhijun Liang, Mei Zhao

FBK has 5-6m^2 Production ability

1、SiPM 2.5D/3D integration with ASIC

FBK is seeking opportunities to cooperate with institutions and industry in China on the sensor-chip integration

2、SiPM radiation performance study

【Micro-Lens, cooling, Electrical field optimization, thermal treatment/annealing】

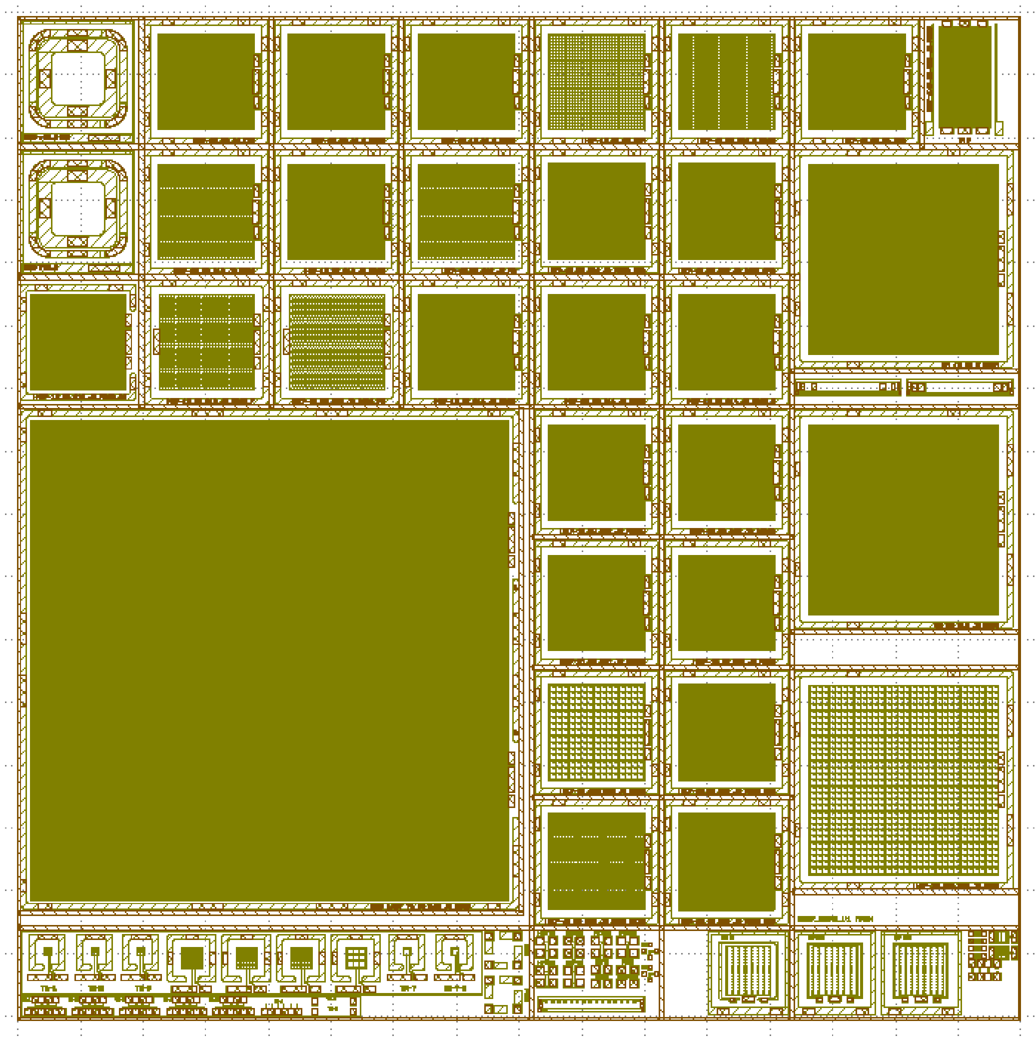
3、Towards small pixel: BSI-SiPM with 8um pixel, 40% crosstalk: metal trench method to improve this

4、Discuss about SiPM non-Linearity, Position sensitive SiPM, “niose free” SiPM, Non-uniformity of irradiation damage

5、Program/funding: Exchange student to work together for SiPM development

FBK and IHEP teams are interested in exploration of student exchange programs and funding support, like joint funding between Italy and China

IHEP SiPM development



- ◆IHEP SiPM design
  - ➢SiPM size: 1*1mm, 3*3mm, 5*5mm
  - ➢Pixel size: 10um, 20um, 50um

- ➢Masks fabricated in last year
- ➢**Poly-silicon quenching resistors: fabrication on dummy wafer ongoing**
- ➢**Gain layer process parameters: more simulation needed**
- ➢Plan to use SOI wafer to isolate the dark current from bulk damage
- ➢Poly-silicon resistors are on top, which will affect the fill factor, and also the inter-pixel structure[JTE, Pstop]
- ➢**In the early stages**

Summary and next

1、 SiPM requirement for CEPC detector is clear.

2、 SiPM candidates from HPK, NDL are tested for ECAL and HCAL detector.

SiPM R&D , improvement and more testing are needed for CEPC detector

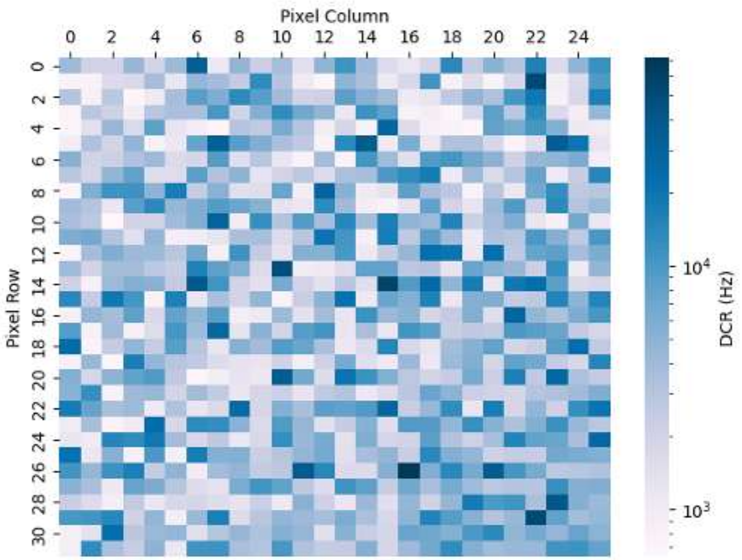
3、How to go ahead with SiPM R&D for CEPC detector?

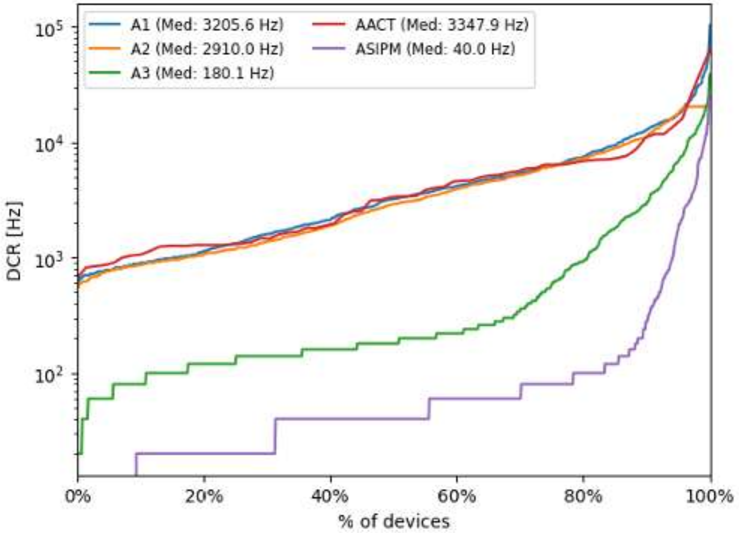
- Cooperation with DRD4, FBK, NDL for SiPM development
  - FBK has demonstrated a very cooperative attitude, but further discussions are needed regarding more details of the cooperation, like if they will optimize the sensor to fill our requirement
  - NDL, Some prototype suitable for ECAL, HCAL requirement, optimization is also needed.
  - What about HPK? Cooperation for custom-made sensor
- IHEP SiPM development at domestic factory

In the early stages.

Several fabrications submissions are needed to firstly fabricate a working SiPM, and then optimize the performance.

Funding and manpower are needed. Timeline will be 3-5 years.





DCR characterization @ 25° and Vov = 2V

- ❑ DCR seems pretty uniform along the sensor array
- ❑ Average DCR for A1 (100 µm pitch) ~5.5 kHz, for A3 (50 µm pitch) is ~1.3 kHz