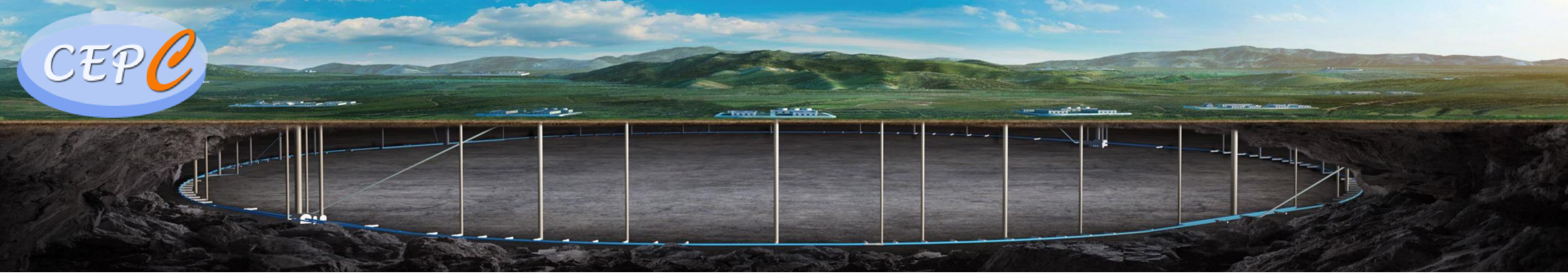


ASIC development plan and status

Wei Wei

On behalf of the CEPC Electronics study team

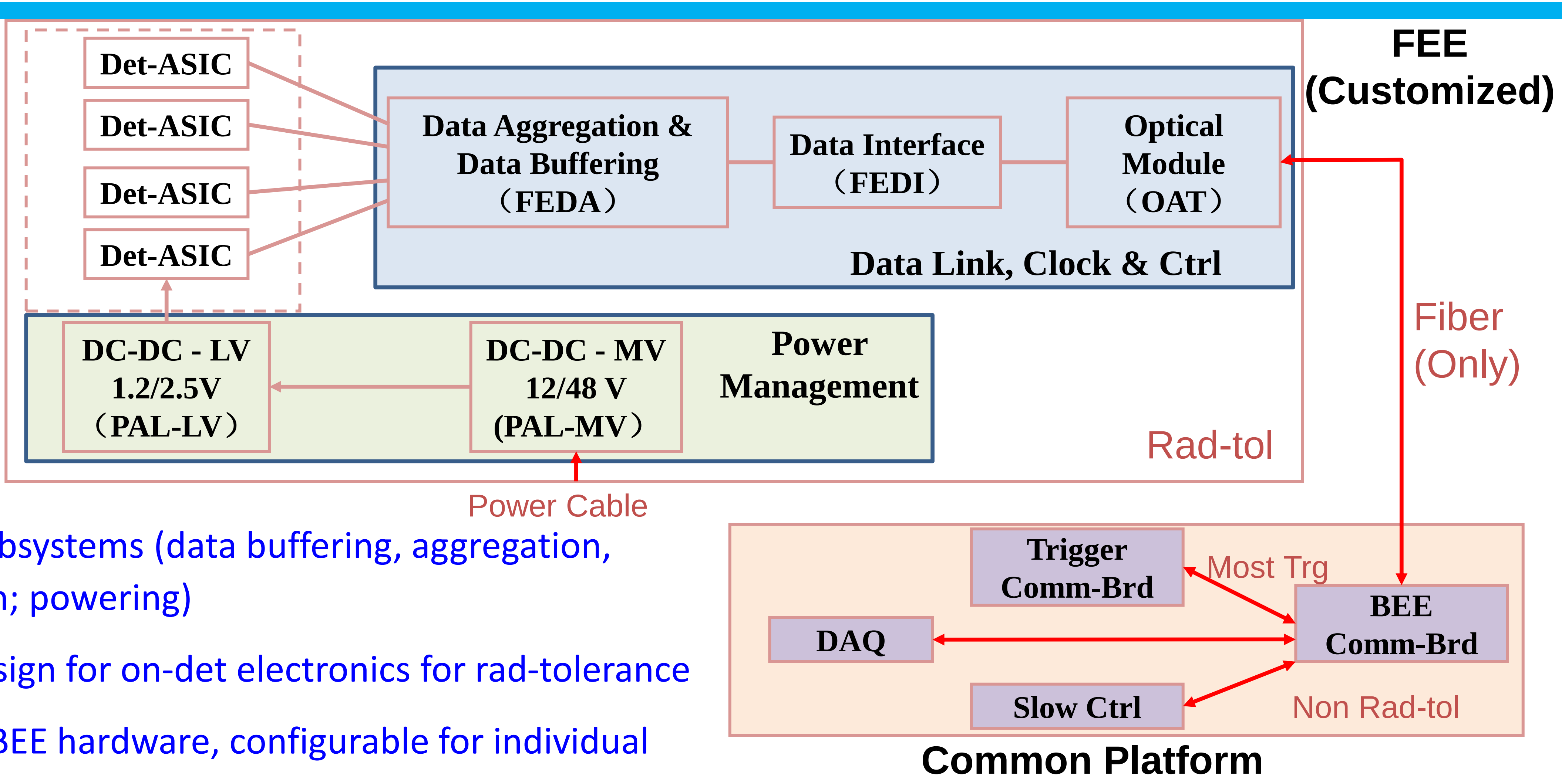
中国科学院高能物理研究所
Institute of High Energy Physics
Chinese Academy of Sciences

March. 25th, 2026, CEPC Detector and Physics Plenary Meeting

Content

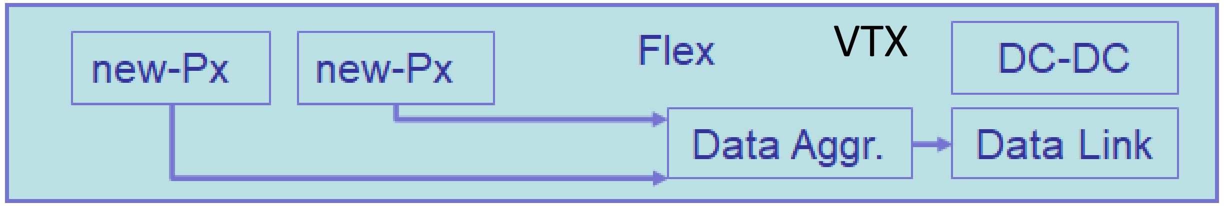
- Overview status of the ASIC development
- Plan updates
- Updates for the data interface development
- Updates for the DC-DC controller development

Reminder of the Overall framework

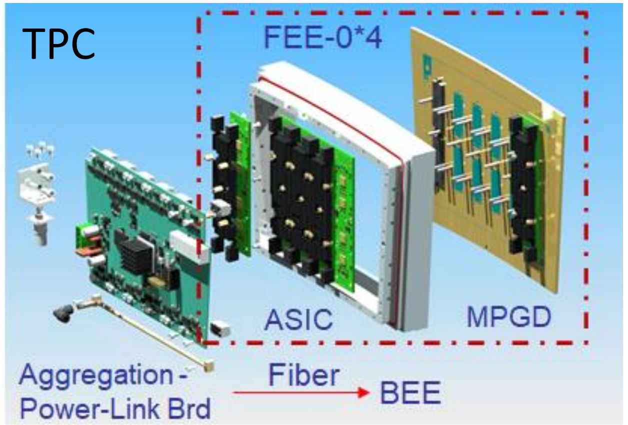


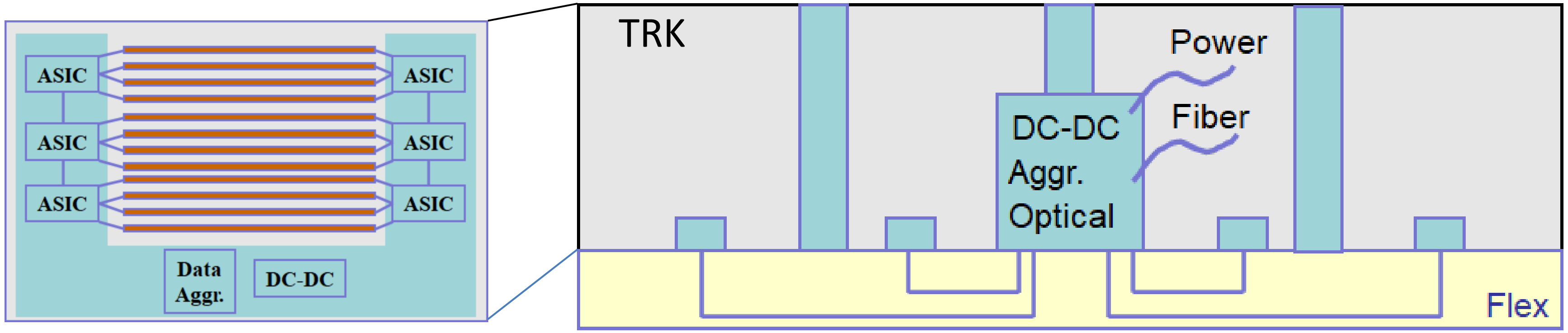
- Common subsystems (data buffering, aggregation, transmission; powering)
- Full ASIC design for on-det electronics for rad-tolerance
- A common BEE hardware, configurable for individual subsystems.
- TDAQ interface is (probably) only on BEE

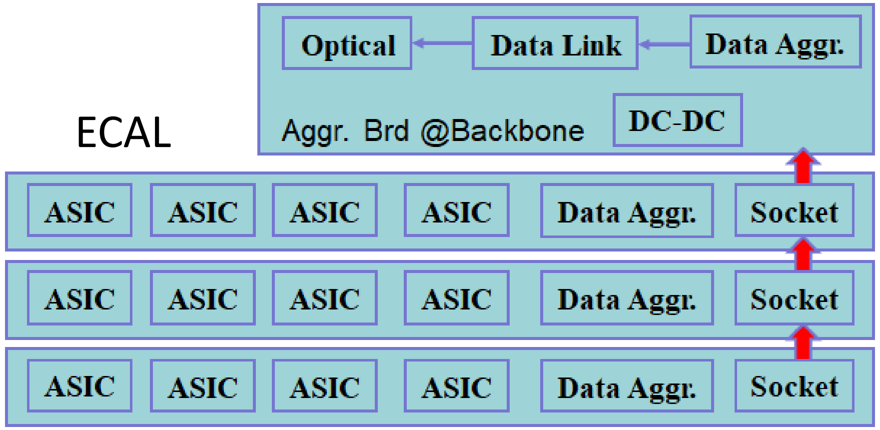
Reminder of the Sub-Det readout Elec.

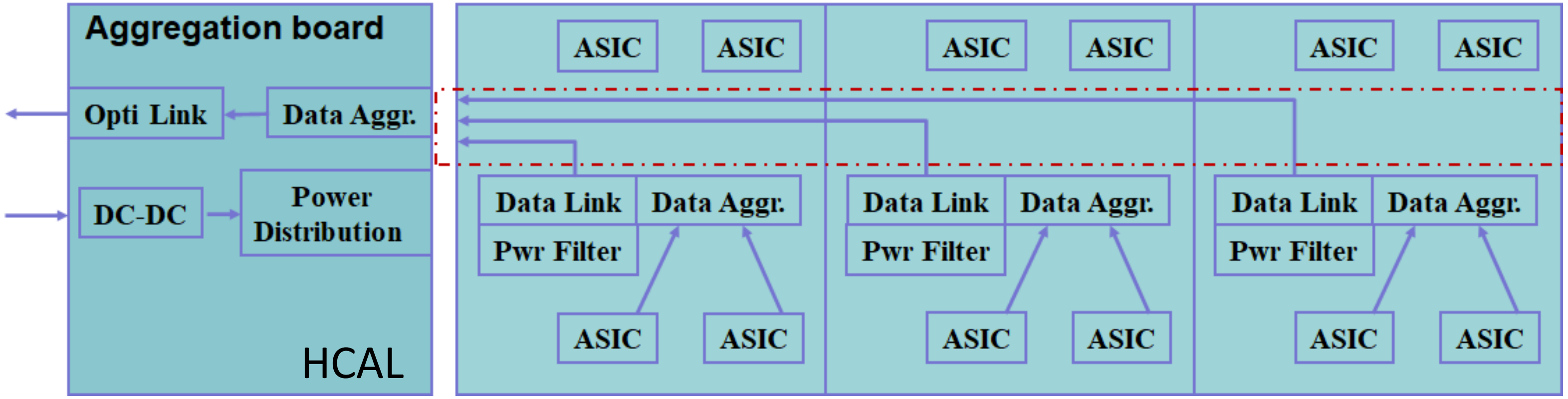


- All sub-det readout electronics were proposed based on this unified framework, maximizing the possibility of common design usage.



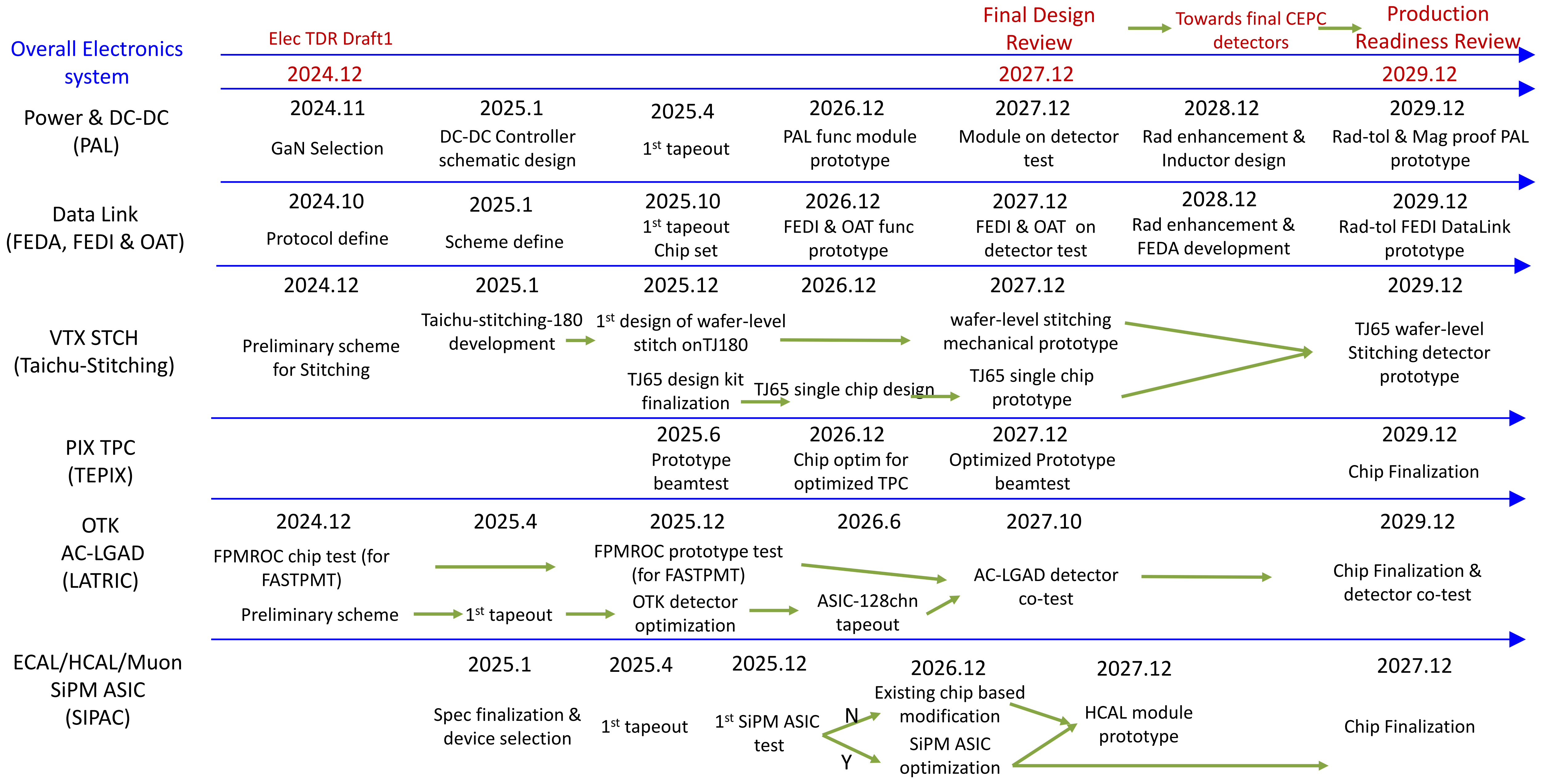






ASIC development & teams

Name	Application	Functional	Foundry & technology	Similar chips	Leading person	Development team	Headcounts	Past tapeout times
Taichu	VTX	VTX-Stitching	Towerjazz 180nm (65nm)	MOSAIX	Wei Wei (IHEP)	NPU, CCNU, SDU, NJU	18	3
TEPIX	TPC	Pixel TPC	TSMC 180nm (65nm)	Timepix3/4	Zhi Deng (THU)	IHEP	5	2
COFFEE	ITK	HVCMOS	SMIC 55nm HV	MightyPix	Yiming Li (IHEP)	ZJU, NPU, DMU，SDU, NJU	20	3
LATRIC	OTK	LGAD-TOF	SMIC 55nm	ALTIROC	Xiongbo Yan (IHEP)	CCNU, WTU, HPU	19	1
SIPAC	SiPM ASIC	ECAL, HCAL, Muon	SMIC 55nm	HGCROC、SPIROC	Huaishen Li (IHEP)	CCNU, NPU	11	1
FEDI	Common Elec	Data Link	SMIC 55nm	lpGBT	Di Guo (CCNU)	IHEP, NPU, USTC, WTU, HPU	25	1
OAT	Common Elec	Optical	SMIC 55nm	VTRx+	Di Guo (CCNU)	IPAS, IHEP	6	0
FEDA	Common Elec	Data Aggr.	SMIC 55nm	lpGBT	Di Guo (CCNU)	IHEP, NPU	6	0
PAL	Common Elec	DC-DC	SMIC 180nm HV	bPolx	Jia Wang (NPU)	IHEP, USTC, TECHORILUX	10	1



Overall Electronics system

Elec TDR Draft1 2024.12

Final Design Review 2027.12 → Towards final CEPC detectors → Production Readiness Review 2029.12

Power & DC-DC (PAL)

2024.11 GaN Selection

2025.1 DC-DC Controller schematic design

2025.4 1st tapeout

2026.12 PAL func module prototype

2027.12 Module on detector test

2028.12 Rad enhancement & Inductor design

2029.12 Rad-tol & Mag proof PAL prototype

Data Link (FEDA, FEDI & OAT)

2024.10 Protocol define

2025.1 Scheme define

2025.10 1st tapeout Chip set

2026.12 FEDI & OAT func prototype

2027.12 FEDI & OAT on detector test

2028.12 Rad enhancement & FEDA development

2029.12 Rad-tol FEDI DataLink prototype

VTX STCH (Taichu-Stitching)

2024.12 Preliminary scheme for Stitching

2025.1 Taichu-stitching-180 development → 1st design of wafer-level stitch onTJ180 →

2025.12 TJ65 design kit finalization → TJ65 single chip design →

2026.12

2027.12 wafer-level stitching mechanical prototype; TJ65 single chip prototype →

2029.12 TJ65 wafer-level Stitching detector prototype

PIX TPC (TEPIX)

2025.6 Prototype beamtest

2026.12 Chip optim for optimized TPC

2027.12 Optimized Prototype beamtest

2029.12 Chip Finalization

OTK AC-LGAD (LATRIC)

2024.12 FPMROC chip test (for FASTPMT) → 2025.12 FPMROC prototype test (for FASTPMT) →

Preliminary scheme → 2025.4 1st tapeout → OTK detector optimization → 2026.6 ASIC-128chn tapeout →

2027.10 AC-LGAD detector co-test →

2029.12 Chip Finalization & detector co-test

ECAL/HCAL/Muon SiPM ASIC (SIPAC)

2025.1 Spec finalization & device selection

2025.4 1st tapeout

2025.12 1st SiPM ASIC test

N → 2026.12 Existing chip based modification

Y → SiPM ASIC optimization

2027.12 HCAL module prototype

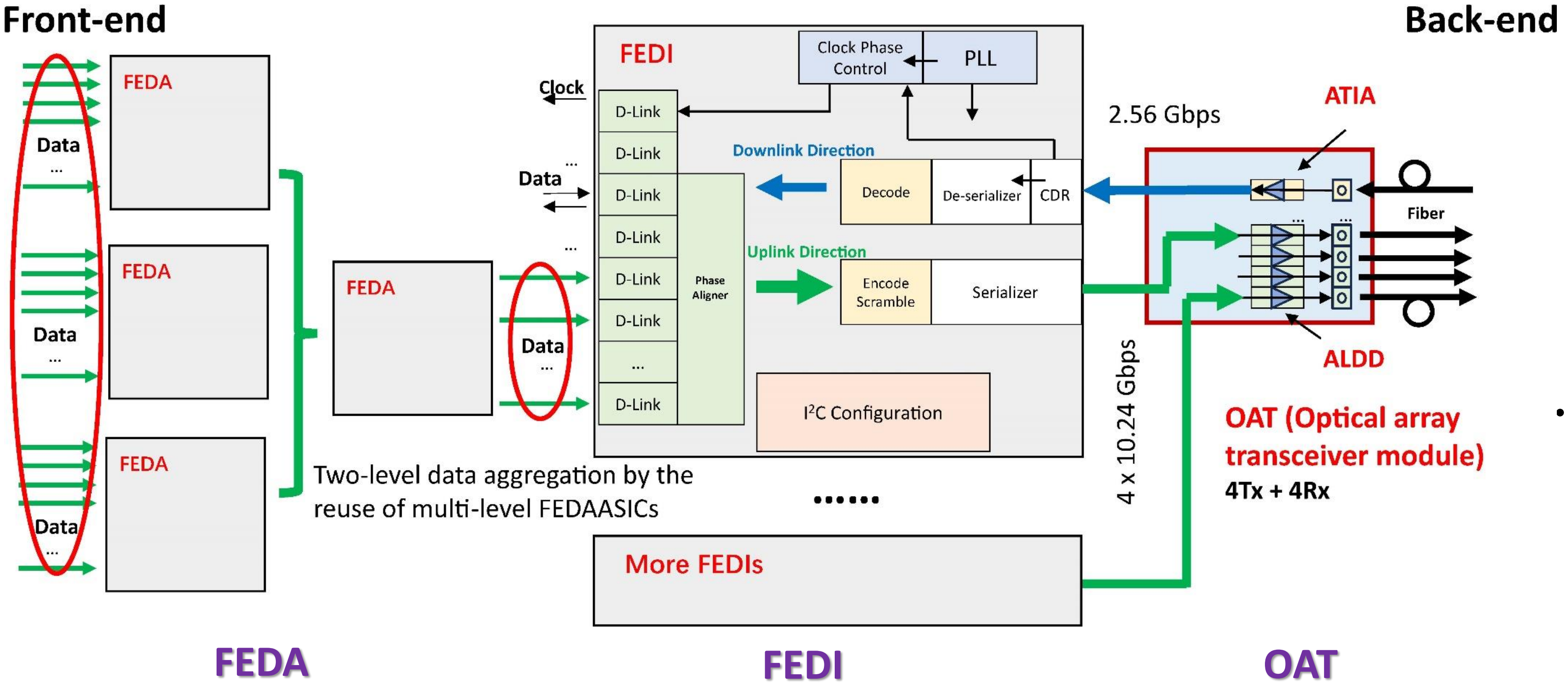
2027.12 Chip Finalization

Plan updates

- The “new” chips：
  - Tapeout with 2 MPWs （V0, V1), with channel functionality in current ver.
  - Following exactly the TDR schedule for the development, no modification
    - LATRIC(OTK)
    - SIPAC(SiPM)
  - Tapeout with 1 MPW, another in manufacture, bugs understood
    - PAL (DC-DC convertor)
  - Main chip in design, to be tapeout in July, delayed due to complexity
    - FEDI (Data Interface)
    - FEDA (Data Aggregation) and OAT (Opto- module) prototype version tapeout, to be tested

Detailed design on Data Transmission

Figure 11.2



Two-level data aggregation by the reuse of multi-level FEDAASICs

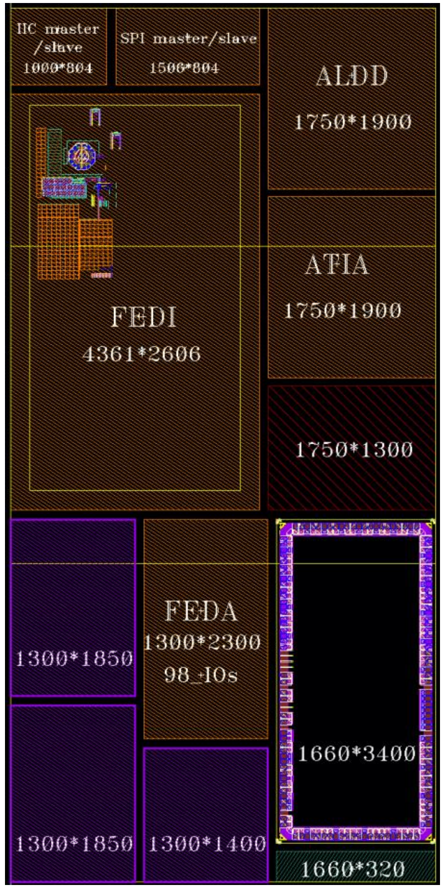
- **Design Team**
  IHEP:3 + 3
  CCNU:2+8
  NPU:2+2
  USTC:1+2
  WTU:2+2
  IPAS:1+1
  HPU:1+2

- Pre-Aggregation ASIC (FEDA): Intend to fit with different front-end detector (different data rates/channels)
- GBTx-like Data Link ASIC (FEDI): Bidirectional serdes ASIC including ser/des, PLL, CDR, code/decode …
- Array Laser Driver ASIC (ALDD) + TIA ASIC (ATIA) + Customized Optical module (OAT)

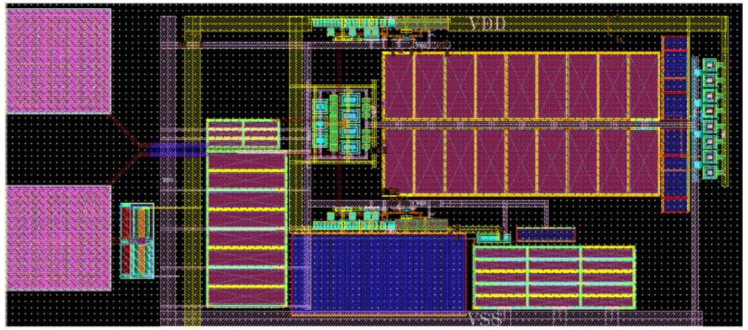
Recent tapeout for the data interface

❖ ASIC Design Status

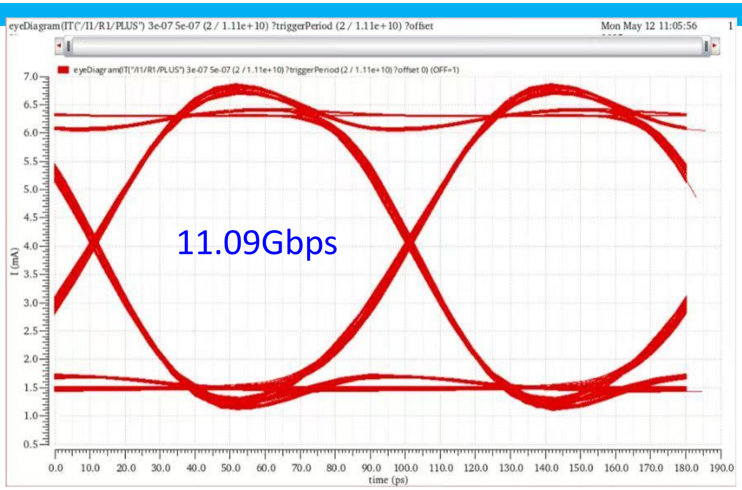
- FEDA： Full digital flow design with added receiver, driver, and IO
- ALDD： 4-channel VCSEL Array driver
- ATIA： 4-channel PD Array reciever



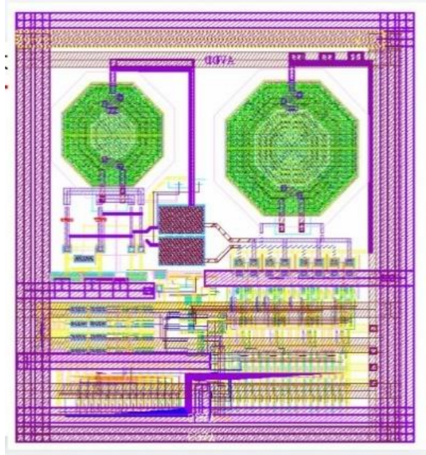
Overall layout for the October tapeout （about 2.75 blocks）



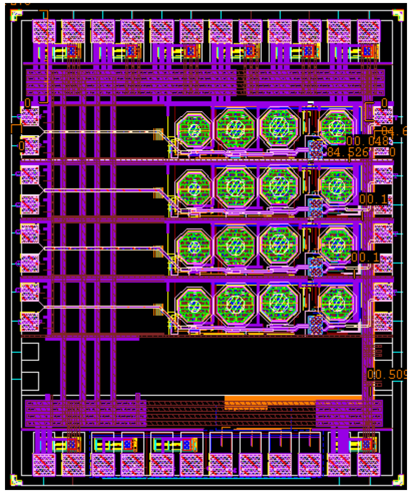
Layout of one channel of ATIA



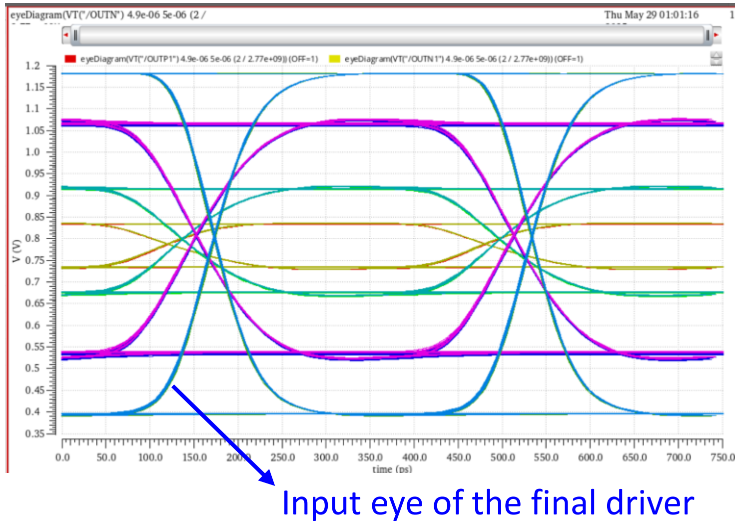
Simulated eye diagram of a single channel in ALDD



Top layout of the serializer (optimizing)



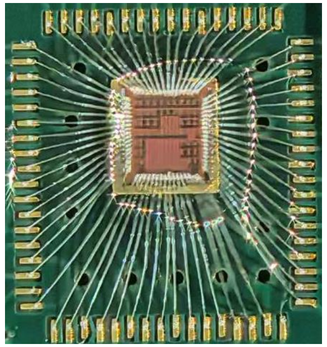
Top layout of ALDD

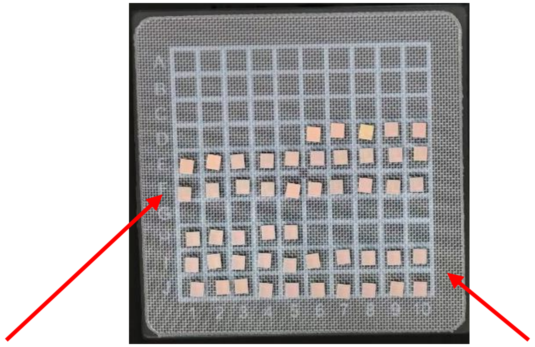


Simulated eye diagram (outputs of the LAs) of a single channel in ATIA at 2.77 Gbps

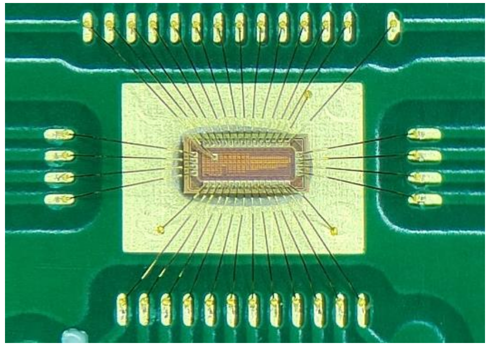
ASICs Design and Test Status of Data Link

ASICs or modules	Status	Results
Front-End Data Interface (FEDI)	Design ongoing (2026.7.7)	Sub-modules are almost done; careful verification is ongoing.
Front-End Data Aggregator (FEDA)	Preparing for testing: wire bonding	
Array Laser Diode Driver (ALDD)	Preparing for testing (module fabrication)	
Array TransImpedance Amplifier (ATIA)		
IIC master and salve	Preparing for testing: wire bonding (in FEDA)	The slave module has already been verified in the previous version.
SPI master and salve	Testing	The slave module works normally, while the master is in testing.


FEDA chip
$1.3\times1.4\text{mm}^2$


ALDD chip
$1.75\times1.9\text{mm}^2$

ATIA chip
$1.75\times1.9\text{mm}^2$

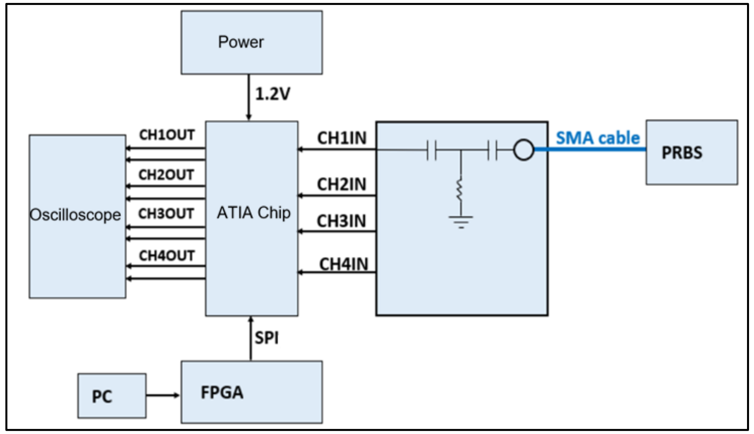

SPI master and slave chip

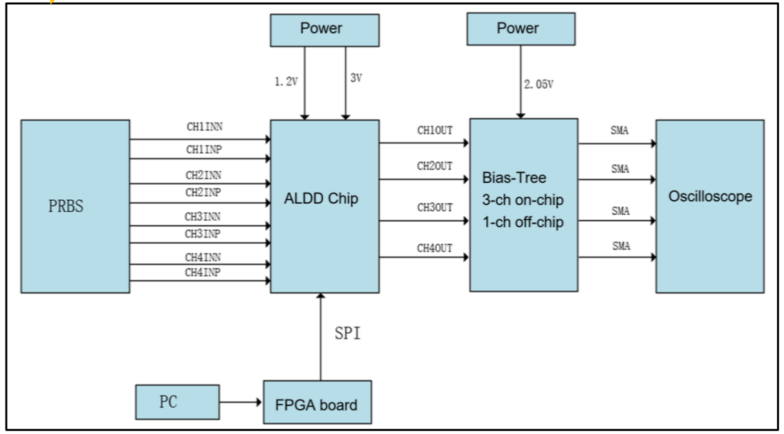
ASICs Test Status of Data Link

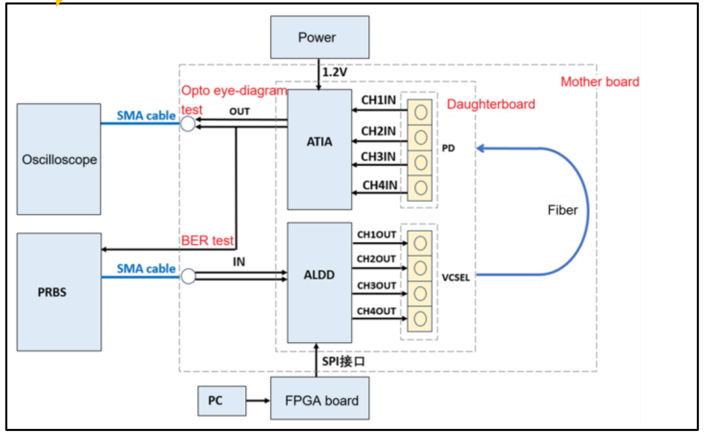
❖ ALDD-ATIA test plan

- Two steps: electrical tests of ATIA and ALDD, followed by an optical test.

Electrical test of ATIA Chip ⇨ **Electrical test of ALDD Chip** ⇨ **Opto-module test**

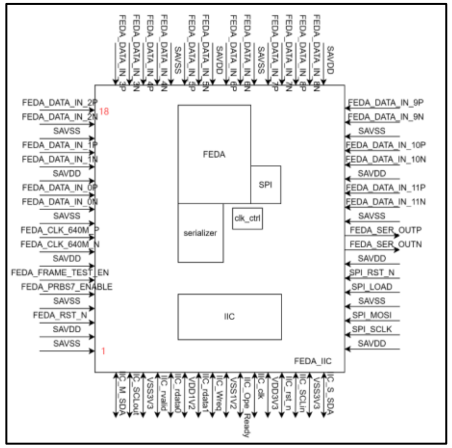




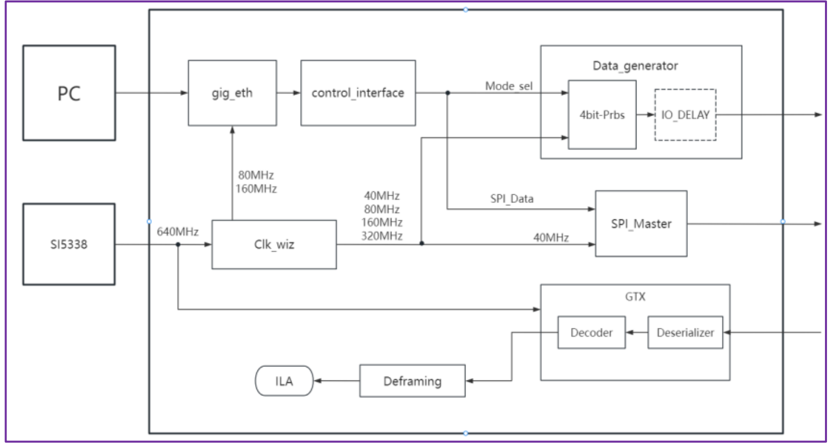


❖ FEDA test plan

FEDA IOs

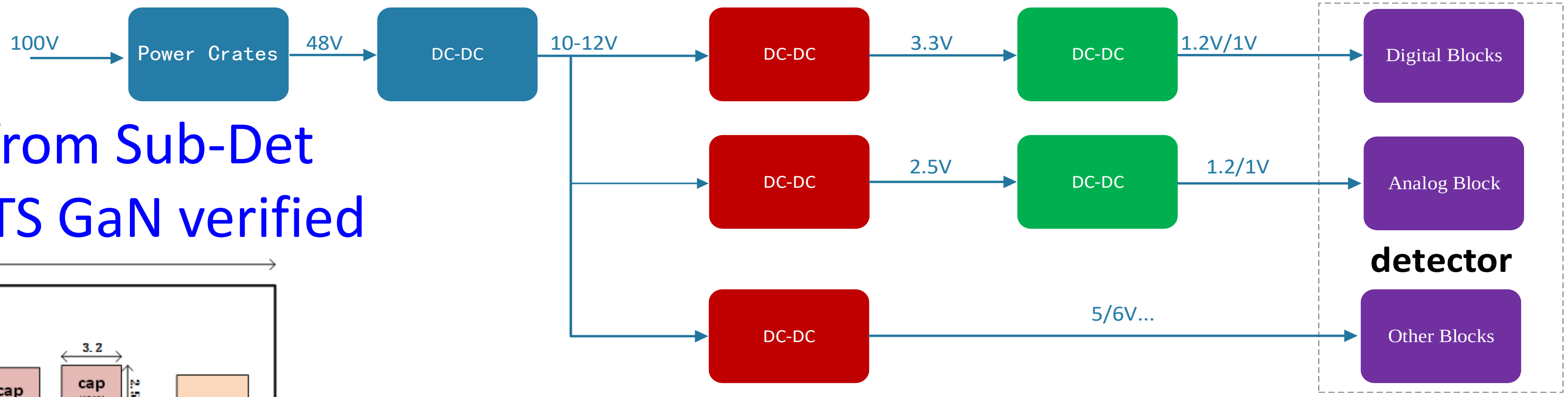


Test Firmware Block Diagram of FEDA



Design on powering distribution and module

- Structure of the power distribution system



100V
Power Crates
48V
DC-DC
10-12V
DC-DC
3.3V
DC-DC
1.2V/1V
Digital Blocks
DC-DC
2.5V
DC-DC
1.2/1V
Analog Block
detector
DC-DC
5/6V...
Other Blocks

- Design spec summarized from Sub-Det
- Preliminary rad-tol. of COTS GaN verified

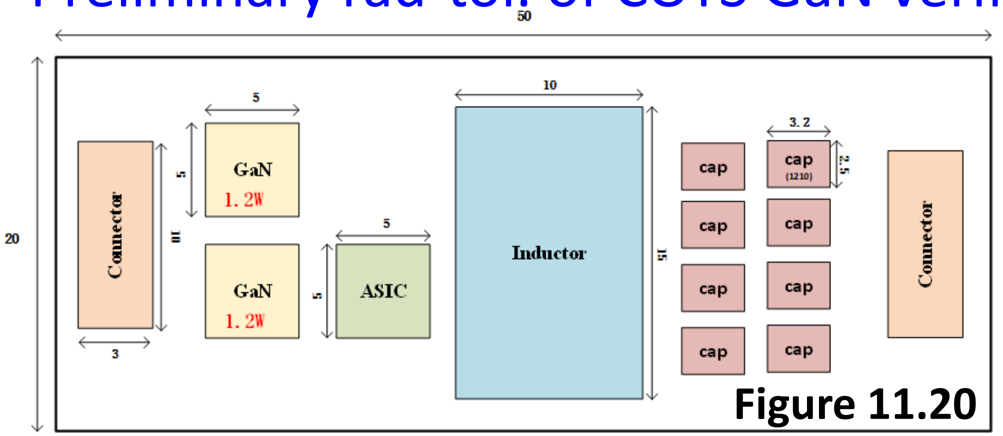


Figure 11.20

Table 11.11

	Nominal	Range
Input V	48V	36V-48V
Output V	1.2V	1.2V、3.3V
Output Current	10A	
Output ripple	10mVpp	
Efficiency	85%	80%-85%-80%（light-nom -heavy）
Dimension	50mmX20mmX6.7mm	Including cooling & shielding
TID	5 Mrad（Si）	
Magnet	3T	

- Proposed design of BUCK DC-DC convertor

PAL Series

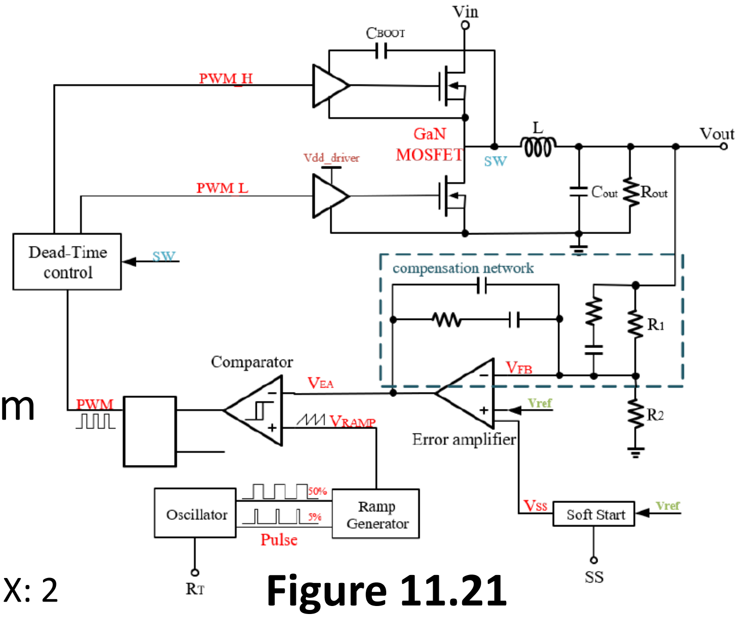
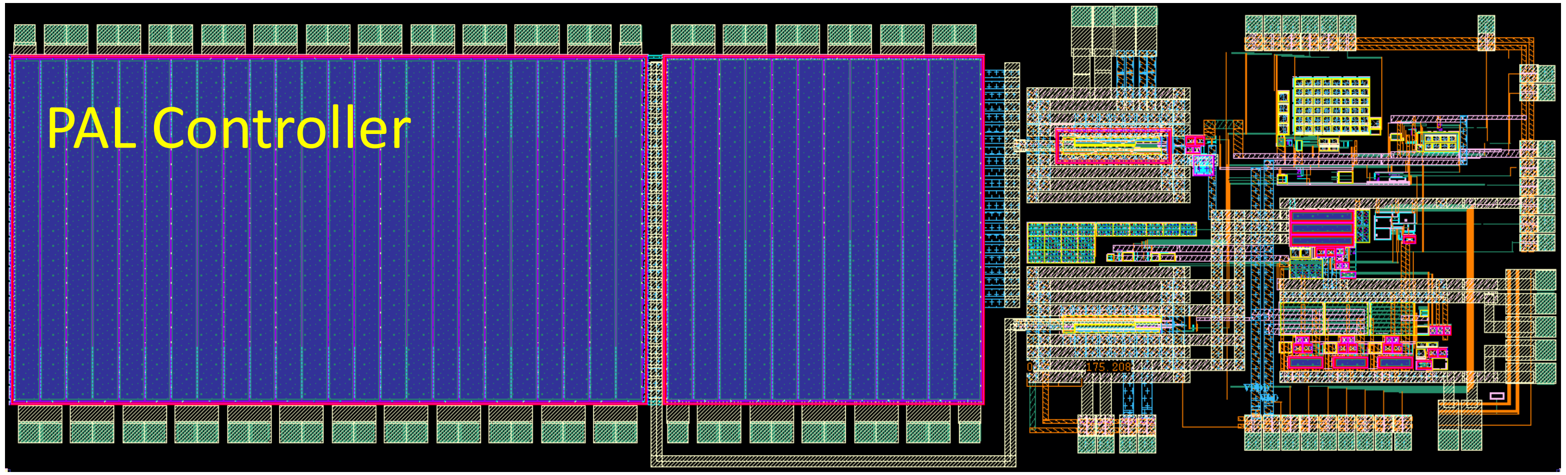


Figure 11.21

- Design team
  - IHEP: 3
  - NPU: 1+2
  - USTC: 1+1
  - TECHORILUX: 2

DC-DC controller development in 2025

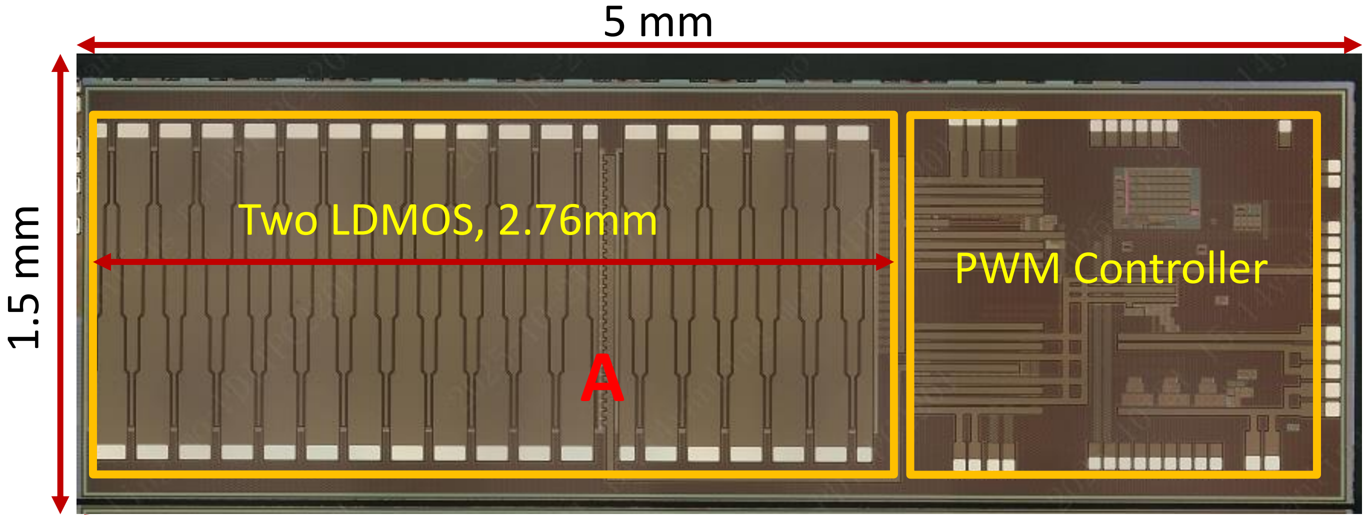


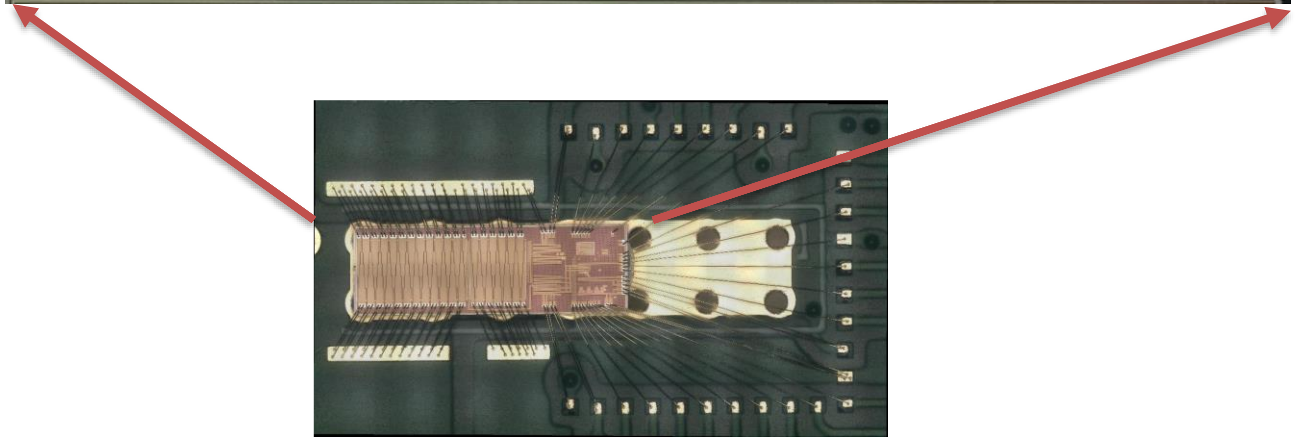
R&D new progress
Not in TDR

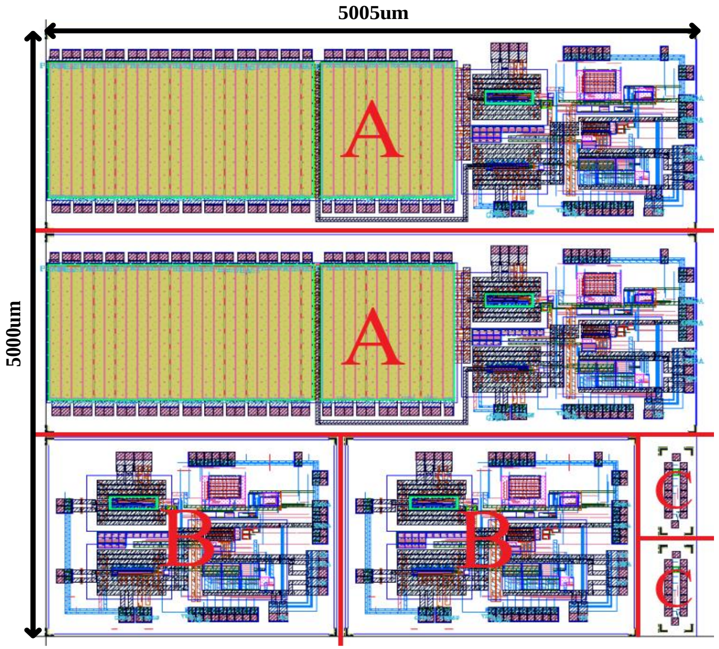
- 1st version of PAL (DC-DC controller) taped out on April 1st , SMIC 180nm 40V-HV
  - – Received in Oct.
- The power module design (by using COTS) parallelly in progress
  - – Magnet proof, compact size is the main constraint
  - – However, suspended due to the lack of budget

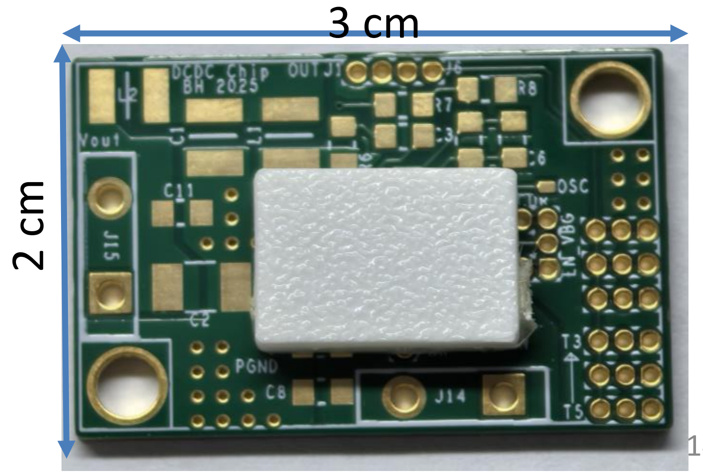
Tapeout in 2025 with on-chip power transistor

- Micro-photo of chip and testing board



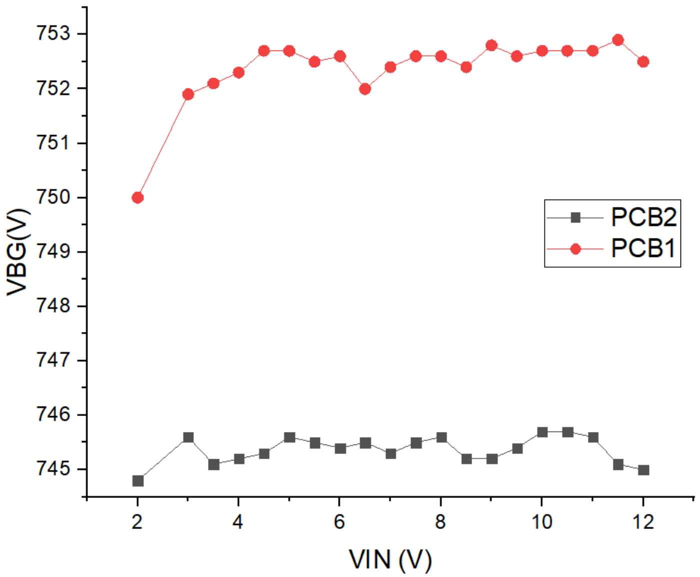




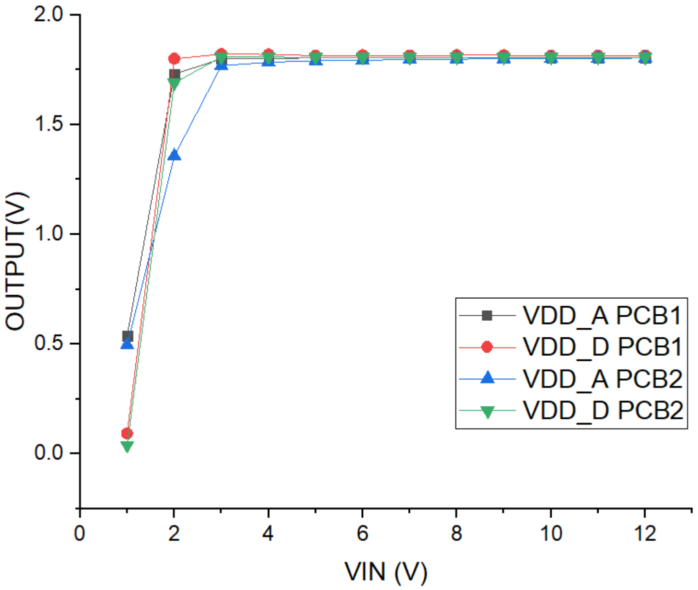


DC/DC convertor test with onchip LDMOS

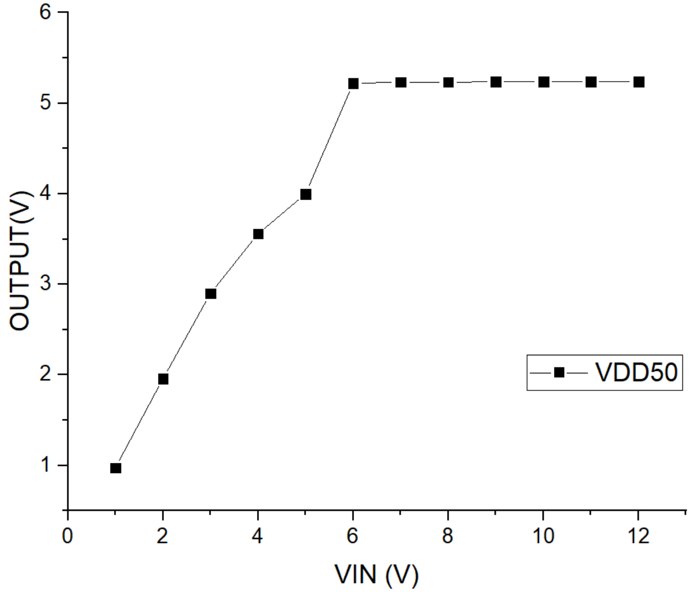
- Measurement results of the built-in bandgap and regulators



Reference voltage (750mV)



Supply analogue/digital power for controller (1.8V)

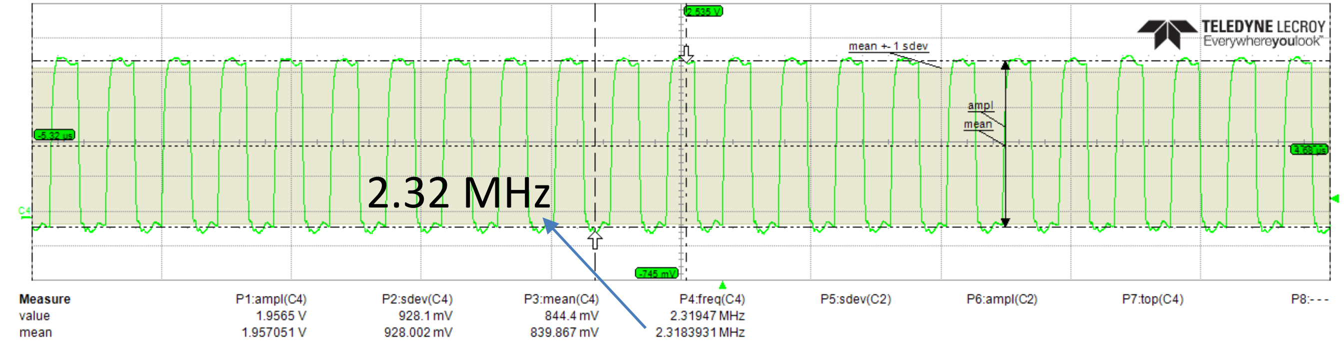


Supply power for the LDMOS driver (5V)

- A bandgap reference circuit can provide a stable reference voltagewith various input voltages.
- Due to limitations in the all-MOS bandgap architecture, variations exist between different circuit boards, which can be addressed through board-level trimming.
- Measured results demonstrate the built-in bandgap and regulators can work well.
- However, large leakage current detected, while the bug was understood later related to the LDMOS cell

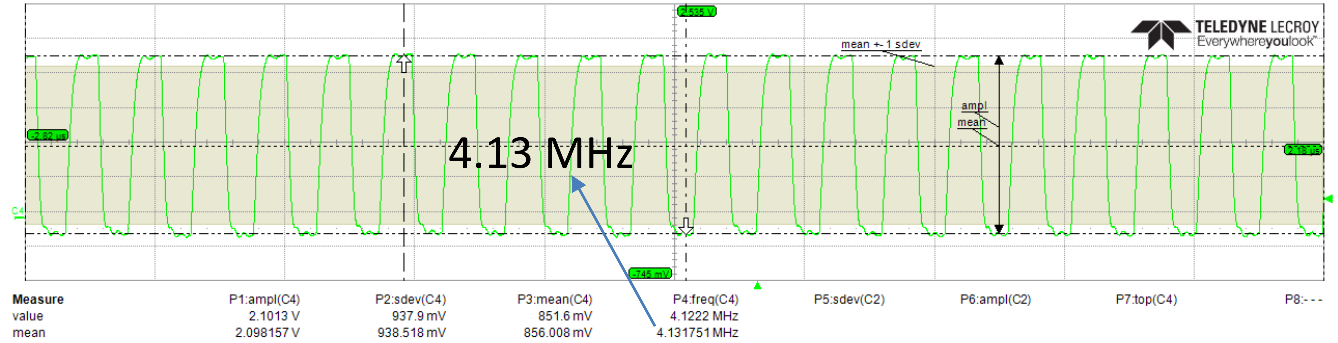
DC/DC convertor test with onchip LDMOS

- Measured frequency of the built-in oscillator



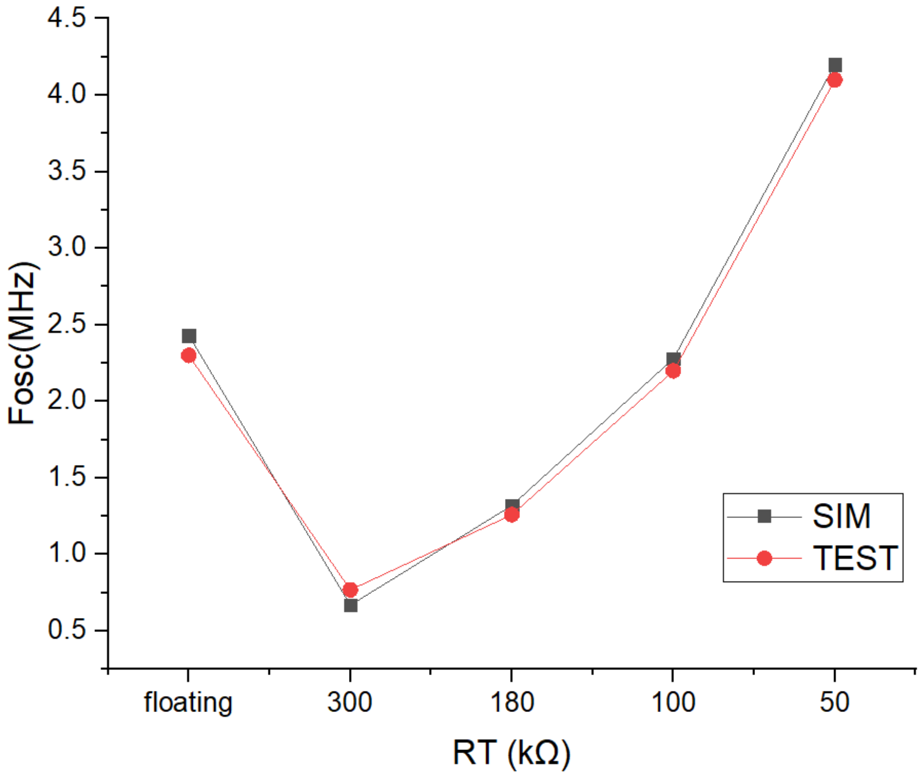
Measure	P1:ampl(C4)	P2:sdev(C4)	P3:mean(C4)	P4:freq(C4)	P5:sdev(C2)	P6:ampl(C2)	P7:top(C4)	P8:- - -
value	1.9565 V	928.1 mV	844.4 mV	2.31947 MHz				
mean	1.957051 V	928.002 mV	839.867 mV	2.3183931 MHz				

Works with internal current source, when RT is floating.



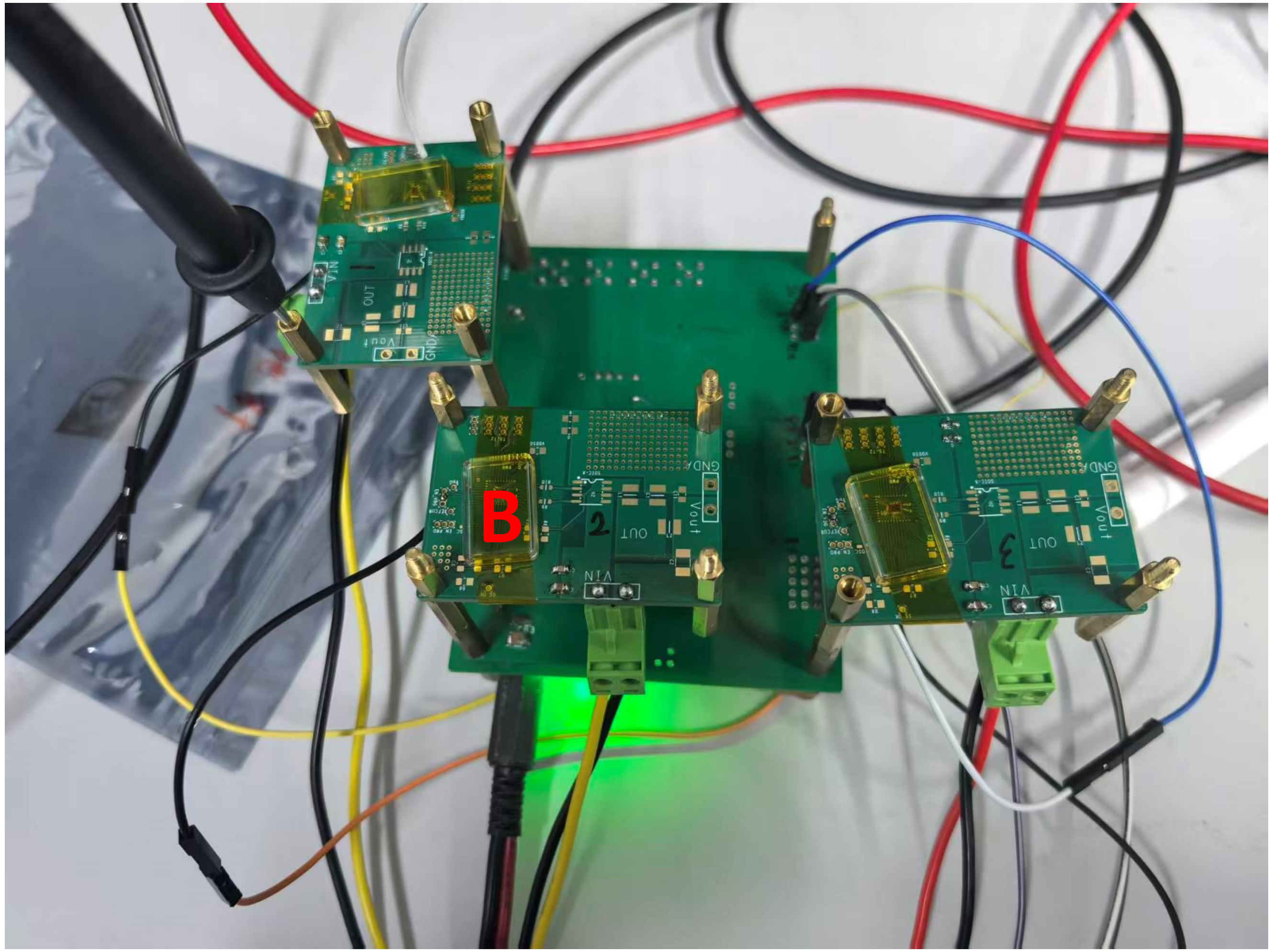
Measure	P1:ampl(C4)	P2:sdev(C4)	P3:mean(C4)	P4:freq(C4)	P5:sdev(C2)	P6:ampl(C2)	P7:top(C4)	P8:- - -
value	2.1013 V	937.9 mV	851.6 mV	4.1222 MHz				
mean	2.098157 V	938.518 mV	856.008 mV	4.131751 MHz				

Works with external current source, when RT is 50kΩ

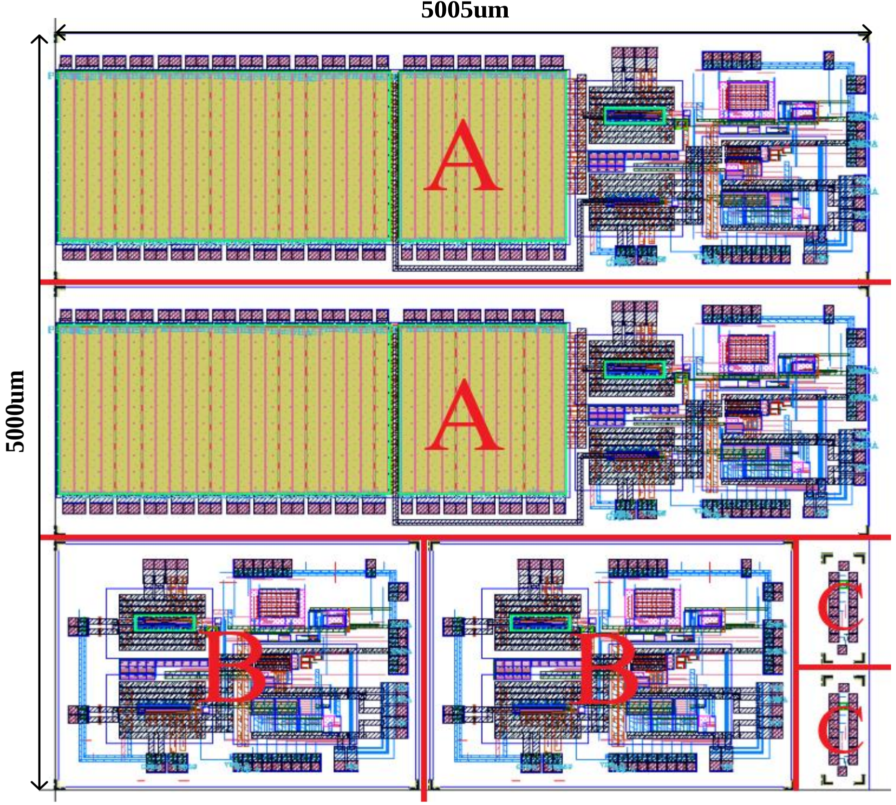


- ➢ Frequency changes linearly with the value of RT(0.5-4MHz)
- ➢ Test results are consistent with simulation results

Controller with external power transistor@Si



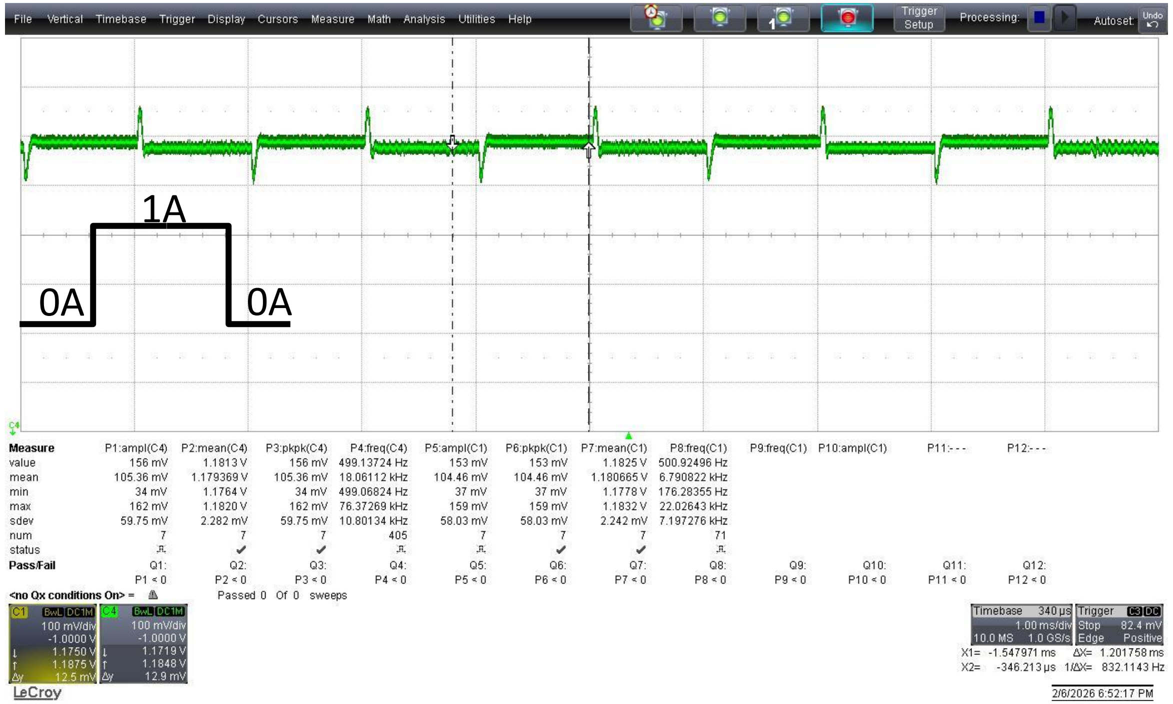
□ 2025年流片



- ➢ Block B for the external power MOS

Controller with external power transistor@Si

Transient response with load



Measure	P1:ampl(C4)	P2:mean(C4)	P3:pkpk(C4)	P4:freq(C4)	P5:ampl(C1)	P6:pkpk(C1)	P7:mean(C1)	P8:freq(C1)	P9:freq(C1)	P10:ampl(C1)	P11:- - -	P12:- - -
value	156 mV	1.1813 V	156 mV	499.13724 Hz	153 mV	153 mV	1.1825 V	500.92496 Hz				
mean	105.36 mV	1.179369 V	105.36 mV	18.06112 kHz	104.46 mV	104.46 mV	1.180665 V	6.790822 kHz				
min	34 mV	1.1764 V	34 mV	499.06824 Hz	37 mV	37 mV	1.1778 V	176.28355 Hz				
max	162 mV	1.1820 V	162 mV	76.37269 kHz	159 mV	159 mV	1.1832 V	22.02643 kHz				
sdev	59.75 mV	2.282 mV	59.75 mV	10.80134 kHz	58.03 mV	58.03 mV	2.242 mV	7.197276 kHz				
num	7	7	7	405	7	7	7	71				
status	⎍	✓	✓	⎍	⎍	✓	✓	⎍				
Pass/Fail	Q1:	Q2:	Q3:	Q4:	Q5:	Q6:	Q7:	Q8:	Q9:	Q10:	Q11:	Q12:
	P1 < 0	P2 < 0	P3 < 0	P4 < 0	P5 < 0	P6 < 0	P7 < 0	P8 < 0	P9 < 0	P10 < 0	P11 < 0	P12 < 0

<no Qx conditions On> = ⚠ Passed 0 Of 0 sweeps

C1 BwL DC1M 100 mV/div -1.0000 V ↓ 1.1750 V ↑ 1.1875 V Δy 12.5 mV

C4 BwL DC1M 100 mV/div -1.0000 V ↓ 1.1719 V ↑ 1.1848 V Δy 12.9 mV

Timebase 340 µs 1.00 ms/div 10.0 MS 1.0 GS/s

Trigger C3 DC Stop 82.4 mV Edge Positive

X1= -1.547971 ms ΔX= 1.201758 ms

X2= -346.213 µs 1/ΔX= 832.1143 Hz

2/6/2026 6:52:17 PM

Measure	P1:ampl(C4)	P2:mean(C4)	P3:pkpk(C4)	P4:freq(C4)	P5:ampl(C1)	P6:pkpk(C1)	P7:mean(C1)	P8:freq(C1)	P9:freq(C1)	P10:ampl(C1)	P11:- - -	P12:- - -
value	359 mV	1.1817 V	359 mV	500.01325 Hz	363 mV	363 mV	1.1831 V	499.96650 Hz				
mean	359.38 mV	1.181678 V	359.38 mV	500.01976 Hz	362.50 mV	362.50 mV	1.183148 V	500.00225 Hz				
min	359 mV	1.1817 V	359 mV	499.93676 Hz	363 mV	363 mV	1.1831 V	499.96650 Hz				
max	359 mV	1.1817 V	359 mV	500.13228 Hz	363 mV	363 mV	1.1831 V	500.03525 Hz				
sdev	---	---	---	70.92785 mHz	---	---	---	25.14152 mHz				
num	1	1	1	4	1	1	1	4				
status	⎍	✓	✓	⎍	⎍	✓	✓	⎍				
Pass/Fail	Q1:	Q2:	Q3:	Q4:	Q5:	Q6:	Q7:	Q8:	Q9:	Q10:	Q11:	Q12:
	P1 < 0	P2 < 0	P3 < 0	P4 < 0	P5 < 0	P6 < 0	P7 < 0	P8 < 0	P9 < 0	P10 < 0	P11 < 0	P12 < 0

<no Qx conditions On> = ⚠ Passed 0 Of 0 sweeps

C4 BwL DC1M 100 mV/div -1.0000 V ↓ 1.1836 V ↑ 1.1723 V Δy -11.3 mV

Timebase -80 µs 1.00 ms/div 10.0 MS 1.0 GS/s

Trigger C3 DC Stop 82.4 mV Edge Positive

X1= -289.377 µs ΔX= 992.164 µs

X2= 702.787 µs 1/ΔX= 1.007898 kHz

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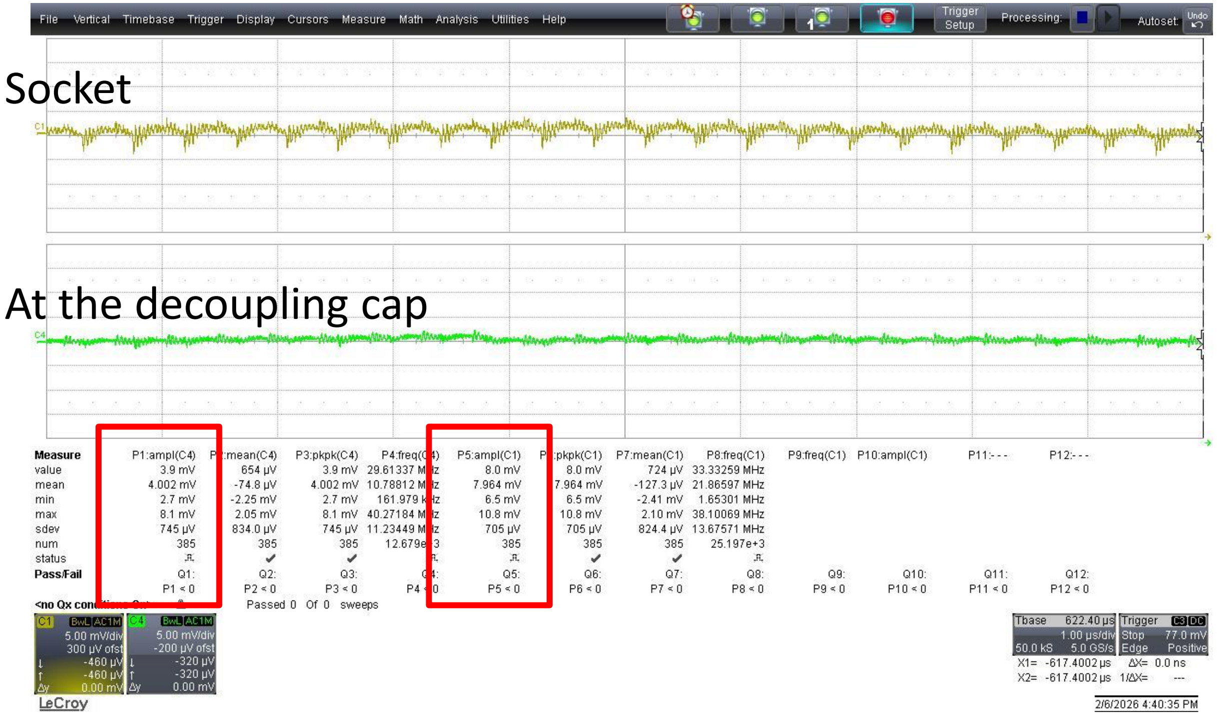
- △Vout=80mV@T_r=1ns
- Recovery time:50us、65us

- △Vout=170mV@T_r=1ns
- Recovery time: 80us、100us

Controller with external power transistor@Si

- Output ripple



Measure	P1:ampl(C4)	P :mean(C4)	P3:pkpk(C4)	P4:freq(C 4)	P5:ampl(C1)	P :pkpk(C1)	P7:mean(C1)	P8:freq(C1)	P9:freq(C1)	P10:ampl(C1)	P11:- - -	P12:- - -
value	3.9 mV	654 μV	3.9 mV	29.61337 M z	8.0 mV	8.0 mV	724 μV	33.33259 MHz				
mean	4.002 mV	-74.8 μV	4.002 mV	10.78812 M z	7.964 mV	7.964 mV	-127.3 μV	21.86597 MHz				
min	2.7 mV	-2.25 mV	2.7 mV	161.979 k z	6.5 mV	6.5 mV	-2.41 mV	1.65301 MHz				
max	8.1 mV	2.05 mV	8.1 mV	40.27184 M z	10.8 mV	10.8 mV	2.10 mV	38.10069 MHz				
sdev	745 μV	834.0 μV	745 μV	11.23449 M z	705 μV	705 μV	824.4 μV	13.67571 MHz				
num	385	385	385	12.679e 3	385	385	385	25.197e+3				
status	⎍	✓	✓	⎍	⎍	✓	✓	⎍				
Pass/Fail	Q1:	Q2:	Q3:	Q 4:	Q5:	Q6:	Q7:	Q8:	Q9:	Q10:	Q11:	Q12:
	P1 < 0	P2 < 0	P3 < 0	P4 0	P5 < 0	P6 < 0	P7 < 0	P8 < 0	P9 < 0	P10 < 0	P11 < 0	P12 < 0

<no Qx cond   Passed 0 Of 0 sweeps

C1 BwL AC1M 5.00 mV/div 300 μV ofst ↓ -460 μV ↑ -460 μV Δy 0.00 mV

C4 BwL AC1M 5.00 mV/div -200 μV ofst ↓ -320 μV ↑ -320 μV Δy 0.00 mV

Tbase 622.40 μs 1.00 μs/div 50.0 kS 5.0 GS/s

Trigger C3 DC Stop 77.0 mV Edge Positive

X1= -617.4002 μs ΔX= 0.0 ns

X2= -617.4002 μs 1/ΔX= ---

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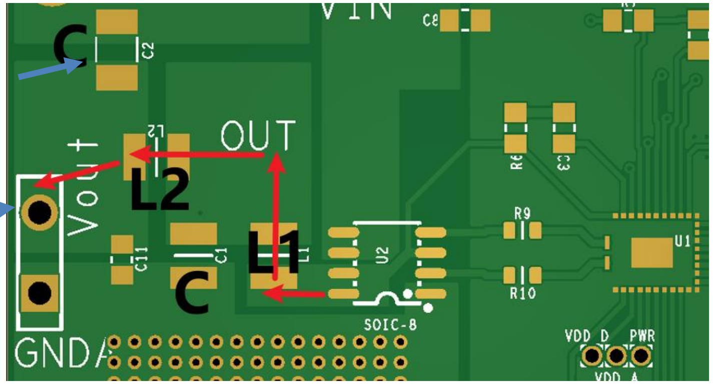
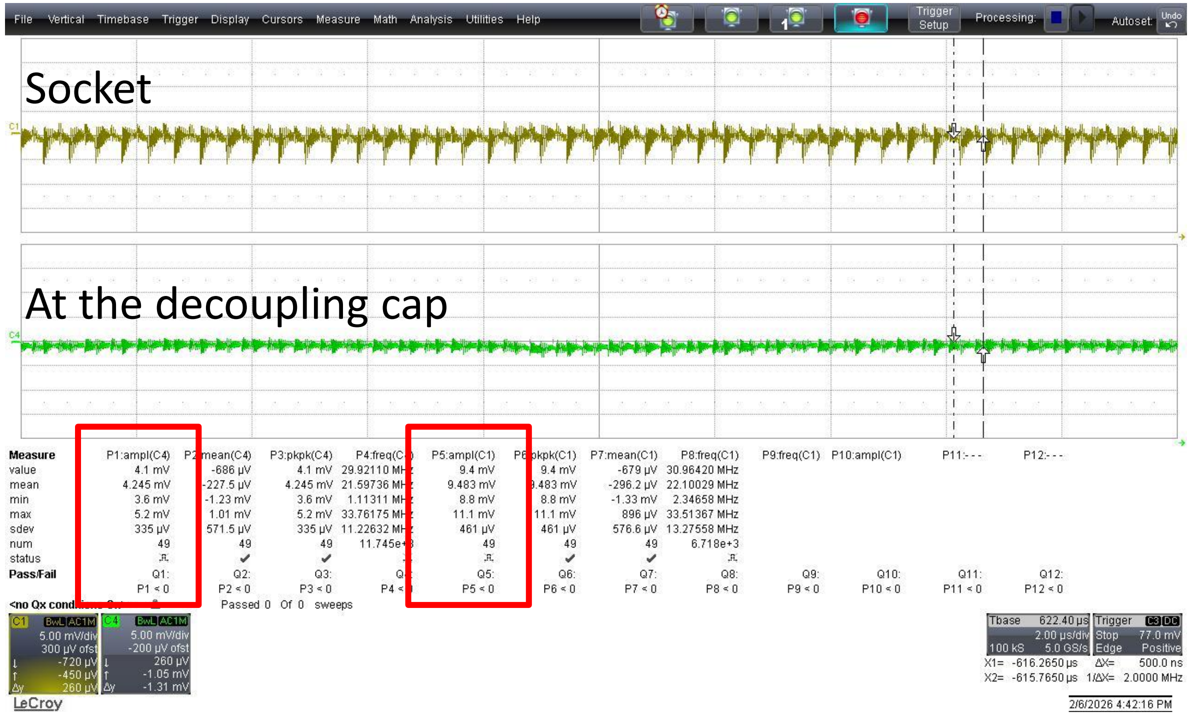
Vout ripple@VIN=5V，Iout=2A

At the decoupling cap

Socket





Measure	P1:ampl(C4)	P2 mean(C4)	P3:pkpk(C4)	P4:freq(C)	P5:ampl(C1)	P6 pkpk(C1)	P7:mean(C1)	P8:freq(C1)	P9:freq(C1)	P10:ampl(C1)	P11:- - -	P12:- - -
value	4.1 mV	-686 μV	4.1 mV	29.92110 MH	9.4 mV	9.4 mV	-679 μV	30.96420 MHz				
mean	4.245 mV	-227.5 μV	4.245 mV	21.59736 MH	9.483 mV	.483 mV	-296.2 μV	22.10029 MHz				
min	3.6 mV	-1.23 mV	3.6 mV	1.11311 MH	8.8 mV	8.8 mV	-1.33 mV	2.34658 MHz				
max	5.2 mV	1.01 mV	5.2 mV	33.76175 MH	11.1 mV	11.1 mV	896 μV	33.51367 MHz				
sdev	335 μV	571.5 μV	335 μV	11.22632 MH	461 μV	461 μV	576.6 μV	13.27558 MHz				
num	49	49	49	11.745e+	49	49	49	6.718e+3				
status	⎍	✓	✓		⎍	✓	✓	⎍				
Pass/Fail	Q1:	Q2:	Q3:	Q	Q5:	Q6:	Q7:	Q8:	Q9:	Q10:	Q11:	Q12:
	P1 < 0	P2 < 0	P3 < 0	P4 <	P5 < 0	P6 < 0	P7 < 0	P8 < 0	P9 < 0	P10 < 0	P11 < 0	P12 < 0

<no Qx cond   Passed 0 Of 0 sweeps

C1 BwL AC1M 5.00 mV/div 300 μV ofst ↓ -720 μV ↑ -450 μV Δy 260 μV

C4 BwL AC1M 5.00 mV/div -200 μV ofst ↓ 260 μV ↑ -1.05 mV Δy -1.31 mV

Tbase 622.40 μs 2.00 μs/div 100 kS 5.0 GS/s

Trigger C3 DC Stop 77.0 mV Edge Positive

X1= -616.2650 μs ΔX= 500.0 ns

X2= -615.7650 μs 1/ΔX= 2.0000 MHz

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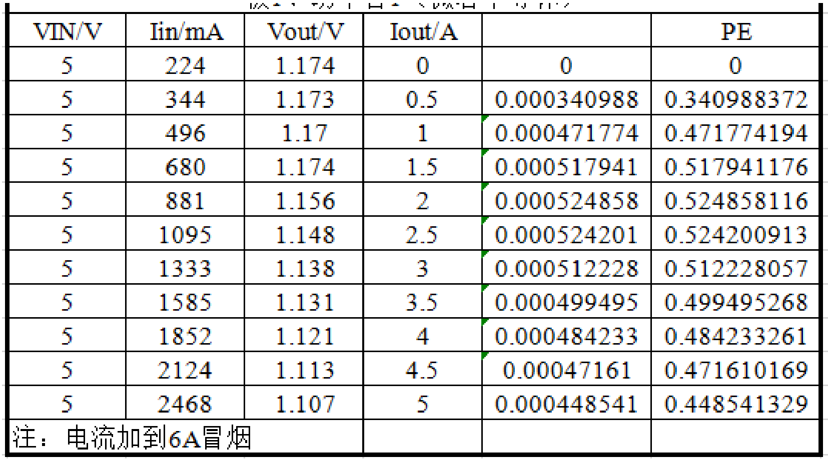
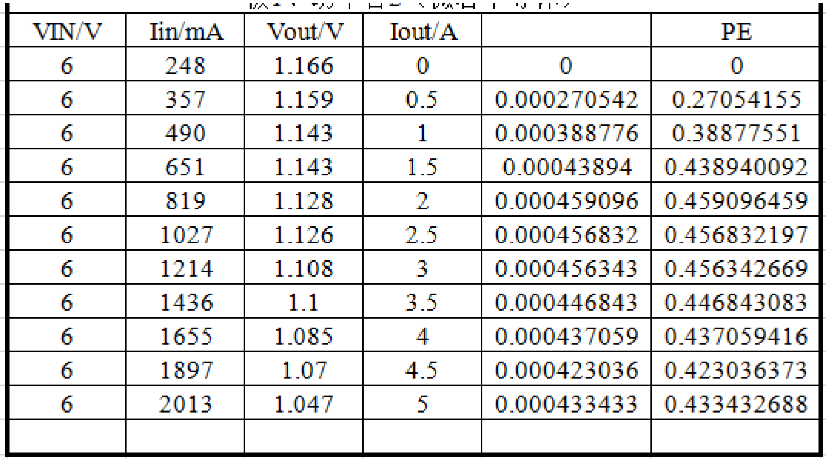
Vout ripple@VIN=5V，Iout=4A

Controller with external power transistor@Si

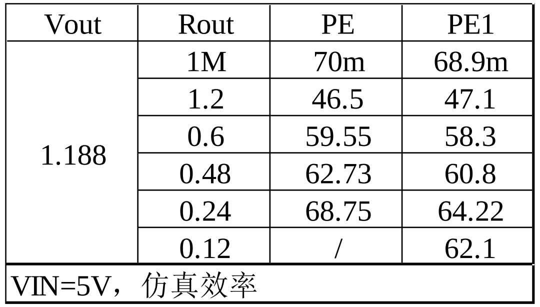
Power efficiency



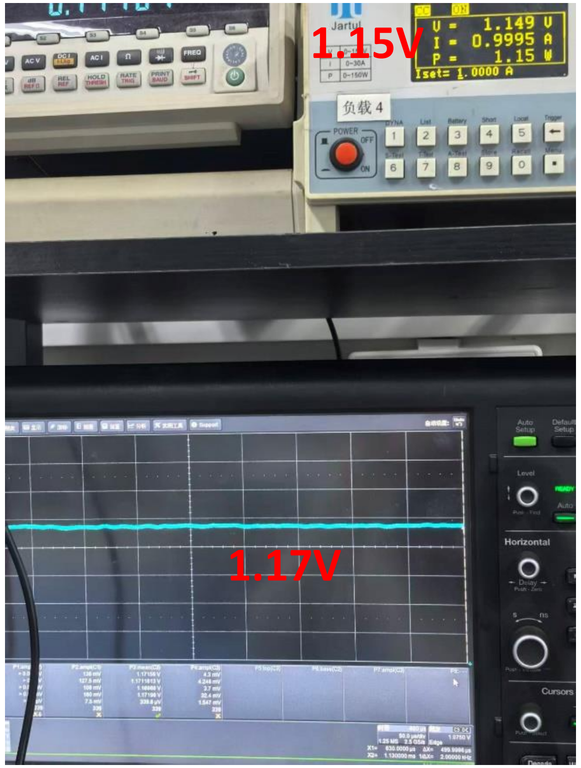
VIN/V	Iin/mA	Vout/V	Iout/A		PE
5	224	1.174	0	0	0
5	344	1.173	0.5	0.000340988	0.340988372
5	496	1.17	1	0.000471774	0.471774194
5	680	1.174	1.5	0.000517941	0.517941176
5	881	1.156	2	0.000524858	0.524858116
5	1095	1.148	2.5	0.000524201	0.524200913
5	1333	1.138	3	0.000512228	0.512228057
5	1585	1.131	3.5	0.000499495	0.499495268
5	1852	1.121	4	0.000484233	0.484233261
5	2124	1.113	4.5	0.00047161	0.471610169
5	2468	1.107	5	0.000448541	0.448541329
注：电流加到6A冒烟					



VIN/V	Iin/mA	Vout/V	Iout/A		PE
6	248	1.166	0	0	0
6	357	1.159	0.5	0.000270542	0.27054155
6	490	1.143	1	0.000388776	0.38877551
6	651	1.143	1.5	0.00043894	0.438940092
6	819	1.128	2	0.000459096	0.459096459
6	1027	1.126	2.5	0.000456832	0.456832197
6	1214	1.108	3	0.000456343	0.456342669
6	1436	1.1	3.5	0.000446843	0.446843083
6	1655	1.085	4	0.000437059	0.437059416
6	1897	1.07	4.5	0.000423036	0.423036373
6	2013	1.047	5	0.000433433	0.433432688



Vout	Rout	PE	PE1
1.188	1M	70m	68.9m
	1.2	46.5	47.1
	0.6	59.55	58.3
	0.48	62.73	60.8
	0.24	68.75	64.22
	0.12	/	62.1
VIN=5V，仿真效率			



- ➢ Bug detected: current consuming due to the ESD problem
- ➢ Test efficiency 50%， while in simulation (with ESD) 60%
- ➢ Possible power loss at

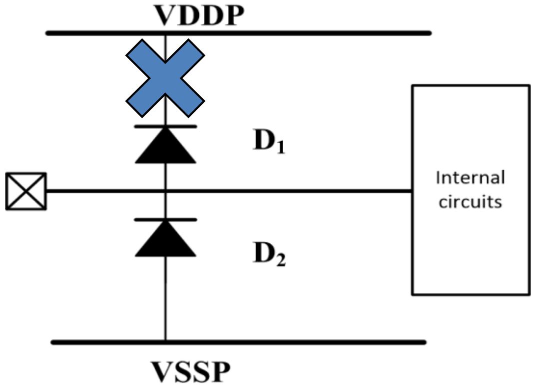
①Ron=30mΩ②output DCR=6mΩ×2③conductor DCR=6.6mΩ×2

Revision tapeout in January

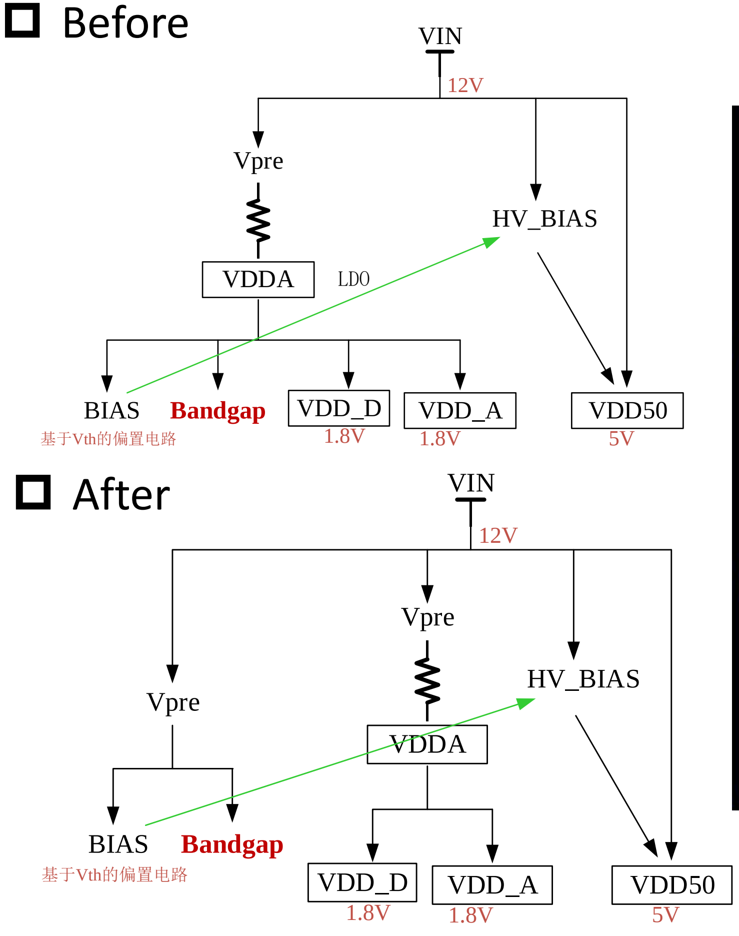
SMIC MPW shuttle on Jan.6

Modifications：

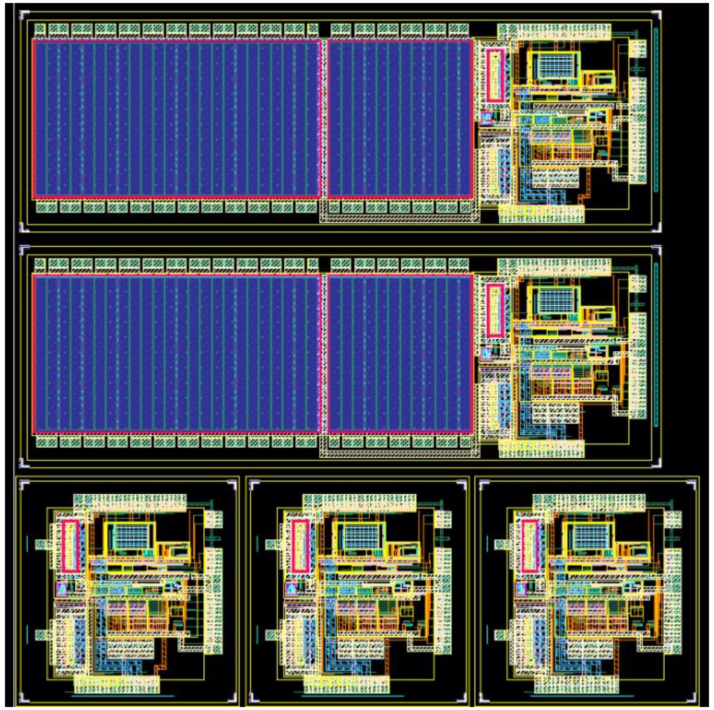
1. Connection of the LDMOS to avoid leakage
2. Correction of the ESD design
3. Improvement of the timing for the power-up
4. Improvement of the layout (2.17*1.48 mm^2 —> 1.38*1.42 mm^2)
5. Reserve for a non-esd version, preparing for the irradiation test



ESD modification



Timing modification of the power-up



Summary and plan for DC-DC convertor

☐ **Test summary**

Design is functional while performance needs further Improvement

Output ripple：3-5mV@light load, 10-20mV@heavy load

Output current：Max 6A

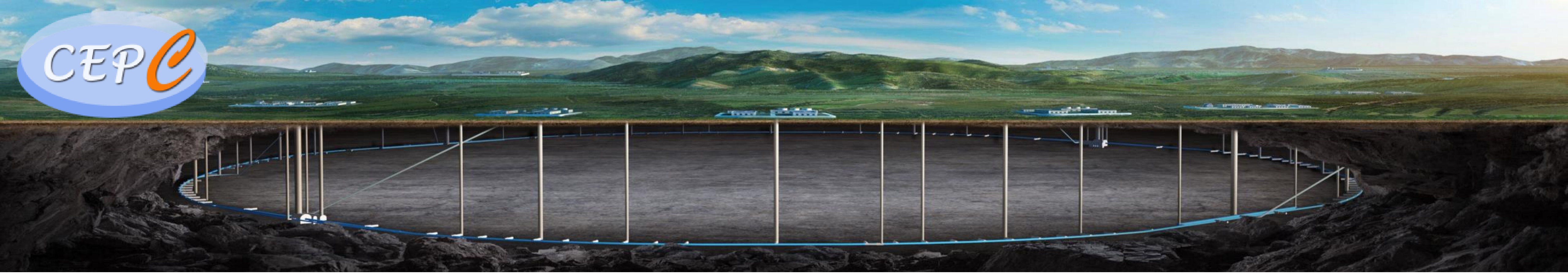
Efficiency：~50%

☐ **Recent plan**

- Using FIB to cut esd for debugging
- Debugging for the crosstalk problem
- Further test with external GaN transistor with designed controller

Summary

- Most new ASICs is progressing with the 1st/2nd tapeout and preparing for the tested and debugging
- Overall schedule currently unchanged, some chip delayed due to the complexity
- Further development may face some difficulties from the budget, especially for collaborators outside IHEP
  - Should find a solution for the shared budget, including not only tapeout, but also man power



Thank you for your attention!

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Institute of High Energy Physics
Chinese Academy of Sciences