SIPAC: A SiPM Readout ASIC for the CEPC Detector

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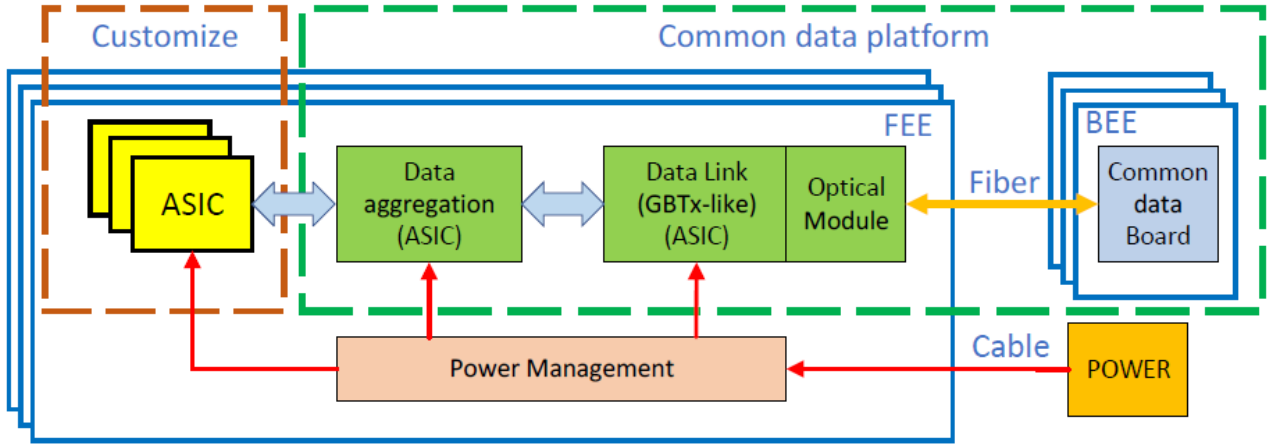
ECAL/HCAL/Muon requirements



- Schematics of the ECAL readout electronics with the modular design for the SiPM readout
- SIPAC is used for the readout of SiPMs

Table 7.3: Requirements of ECAL front-end electronics

Parameters	Requirements
Charge Range	0.128 pC~ 3.84 nC (0.1~3000 MIP)
Charge Resolution	10 % (1.0 MIP), 1 % (100 MIP)
Timing Resolution	200 ps (1 MIP), 100 ps (12 MIP)
Integral Non-linearity	< 1 %
Average Event Rate/channel	13 kHz
Max Event Rate/channel	230 kHz
Typical Signal Rising Edge	40 ns
Typical Signal Width	~ 1 μs

ECAL

SiPM characteristics that drive the requirements for the readout electronics design.

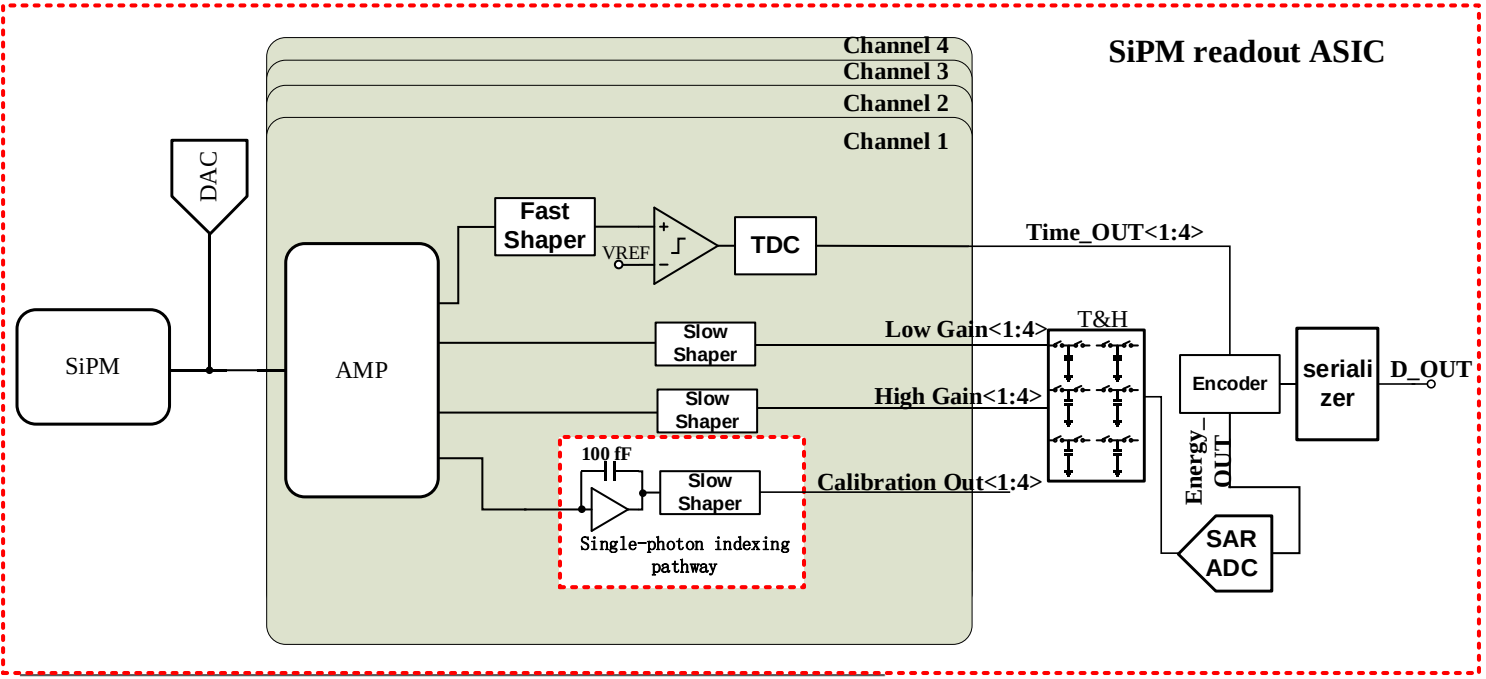
Item	Requirement
Charge dynamic range	0.8 pC~800 pC (0.1~100 MIPs)
Charge resolution	10% of 1.0 MIP
SiPM capacitance	≤ 100 pF
SiPM gain	≥ 5×10^5
Average event rate/channel	2 kHz
Max event rate/channel	50 kHz
Typical signal	2~3 mV/p.e.

HCAL

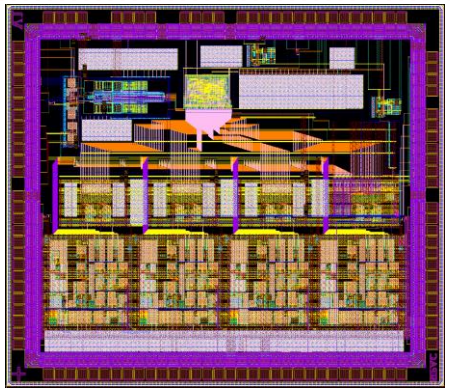
MUON requirement

- Readout design for ECAL and HCAL covers the requirements of Muon detector $N_{pe} < 100, \sigma_T < 0.5ns$
- Use the ASIC scheme from ECAL or HCAL, and customize the FEE based on ASIC.
- Revise according to the constraints from cooling and mechanical structure of the detector

SIPAC0 Design

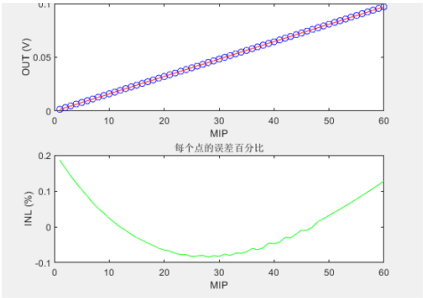


Characteristics	Value
Charge Dynamic Range	1.28 pC~3.84 nC
Charge resolution	10%@1.28pC, 1%@128pC 1%@100 MIPS
Time resolution(RMS)	200 ps @1.28pC, 100 ps @12.8pC
Detector Capacitance	$\leq$ 100 pF
Max signal rate/channel	500 kHz/ch
ADC	10-bit
TDC resolution	8-bit
TDC bin width	100 ps
Power consumption	15mW/channel
Num. of channels	4

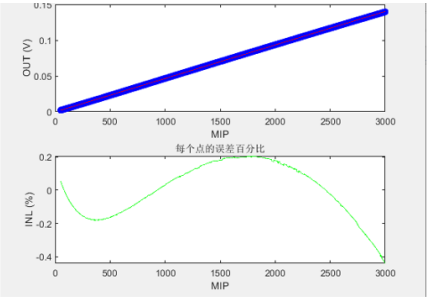


Layout size:2.0mm x 2.3mm
55nm CMOS process, TO April 2025

- ECAL and HCAL in CEPC detector require a large dynamic range, with integrated TDC and ADC, and a dedicated chip for fully digital readout.
- Voltage preamplifier, fast/slow shaper, discriminator, TDC, switched-capacitor-array(SCA), SAR-ADC, serializer, DAC
- high/low gain shpaer for large dynamic range, and fast shaper for timing

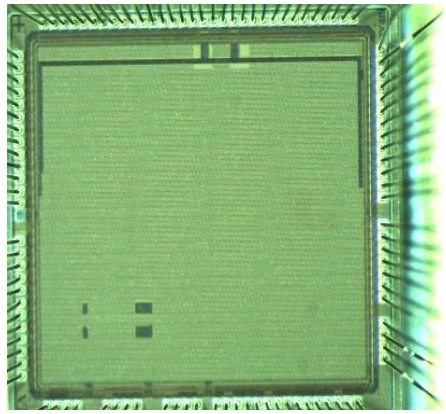


1-60MIPs, INL<0.2%

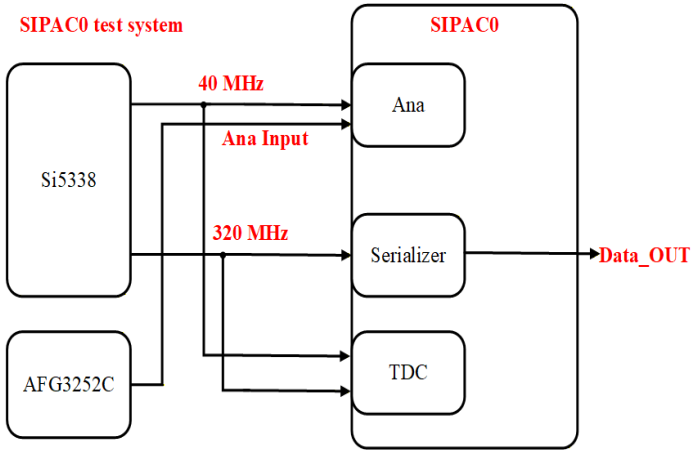


50-3000MIPs, INL<0.4%

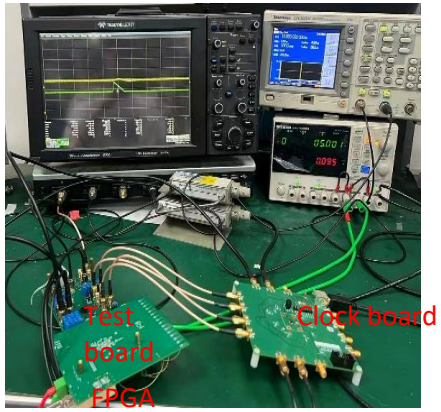
SIPAC0 Test setup



SIPAC0



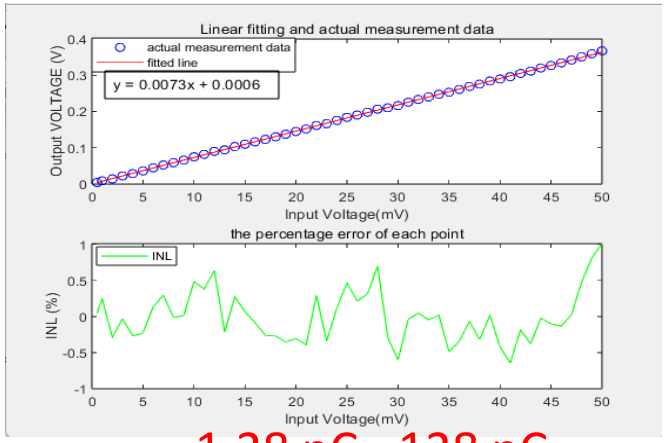
Test setup



Test System

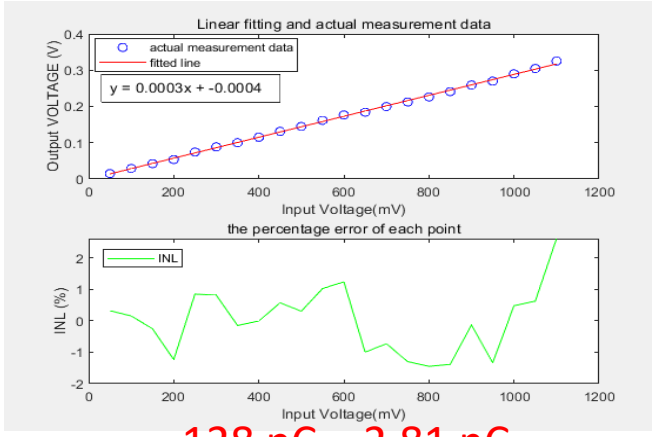
- *The Si5338 clock board generates a 320 MHz clock for both serialization and TOA measurement. The clock from the same PLL is divided down to 40 MHz which serves both the analog circuitry and the TDC's coarse counter.*
- *To characterize the TDC core, a 1 MHz clock from the Si5338 is used to trigger a pulse/pattern generator (81130A) and The Time of Arrival (TOA) is measured by sweeping the clock phase.*

SIPAC0 Test results



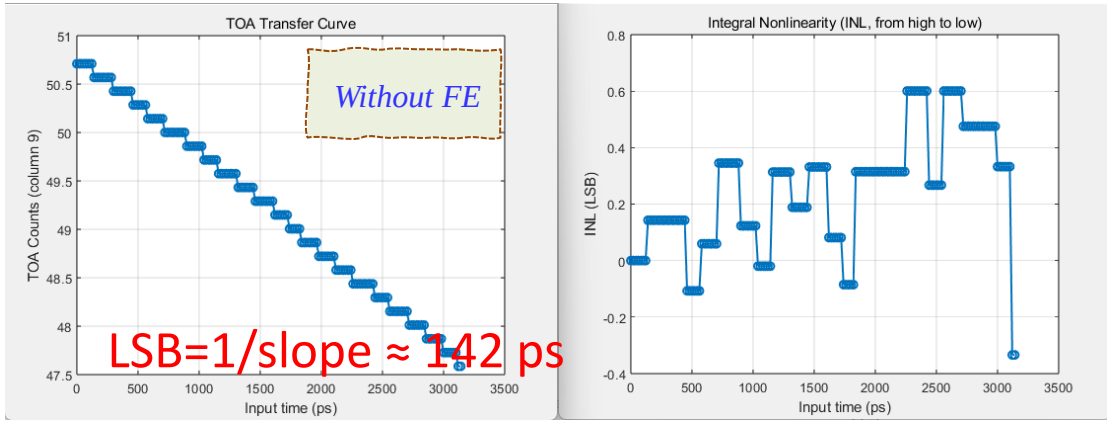
1.28 pC - 128 pC

High-gain path INL



128 pC – 2.81 nC

Low-gain path INL

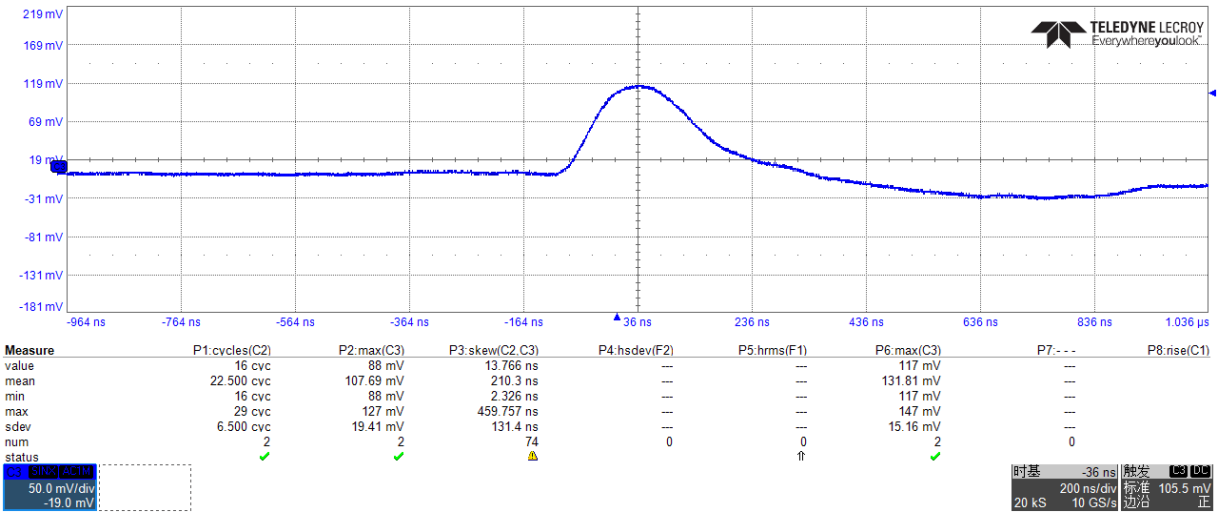


TDC transfer curve

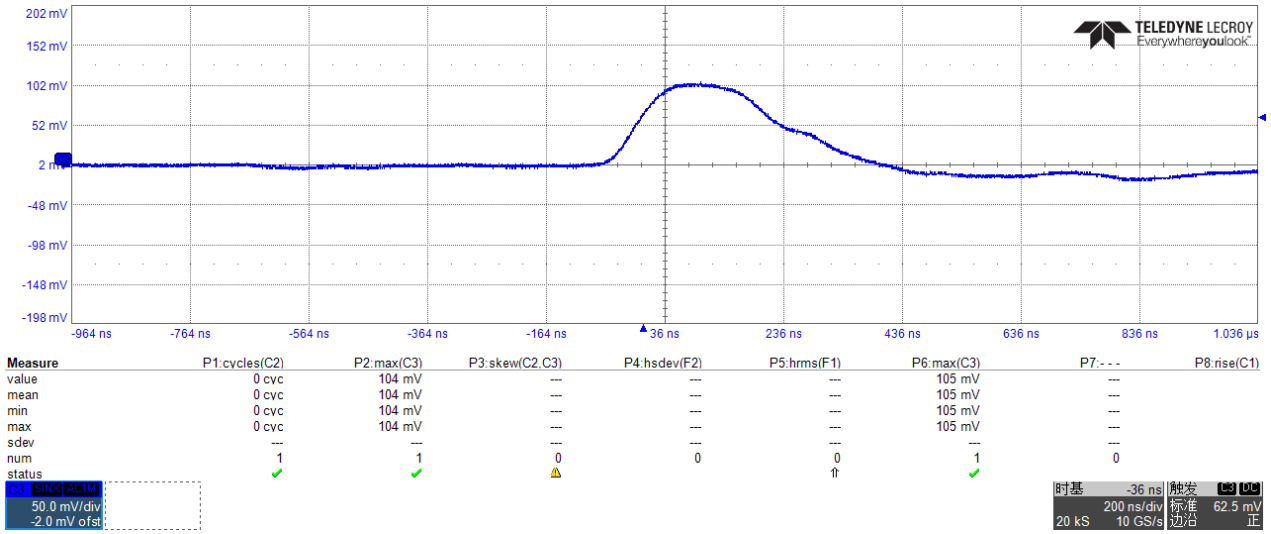
Post-Simulation result		Test result
Input dynamic range	1.28 pC - 3.84 nC	1.28 pC – 2.81 nC
High gain path gain	8	7.3
Low gain path gain	0.5	0.3
SNR	5	4.3
TDC resolution	100 ps	142 ps
ADC resolution	ENOB 10bit	~8bit

- *The chip achieves a dynamic range of 1.28 pC to 2.81 nC with nonlinearity below 3%. The TDC provides a timing precision of 142 ps.*
- *The TOA INL without FE are measured less than ± 1 LSB.*
- *During testing, several issues were identified. The dynamic range limitation is likely caused by MOS transistors entering the linear region, the TDC delay may result from the slow–slow (SS) process corner, and the ADC sampling error is attributed to charge redistribution. All these issues have been corrected in SIPAC1, which was submitted for fabrication in October.*

SIPAC0 test with SiPM



SIPAC0+SiPM+BGO



SIPAC0+SiPM+Glass

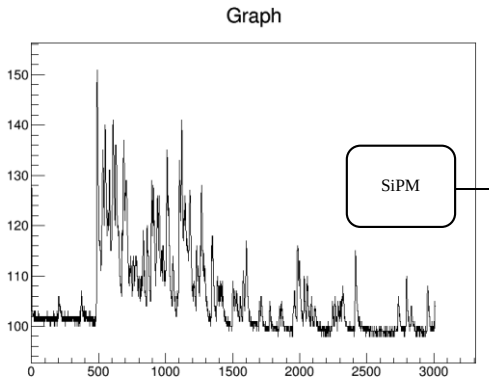
SiPM： NDL EQR20-3030

Glass 4*4 & BGO 3*3

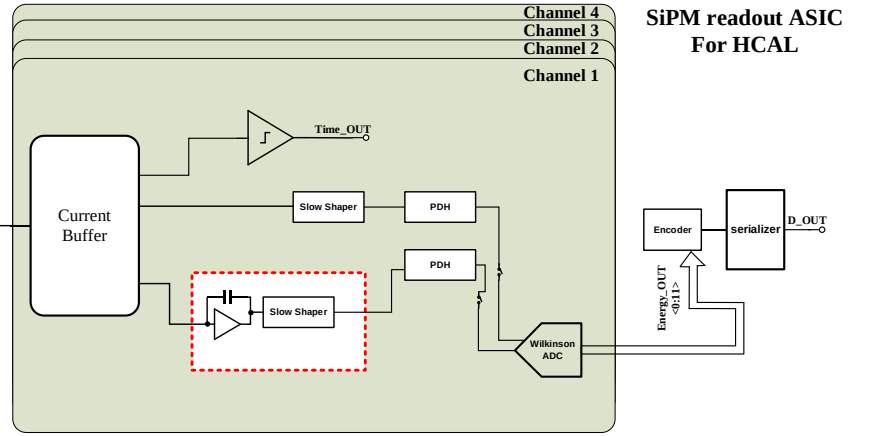
Cosmic Ray test

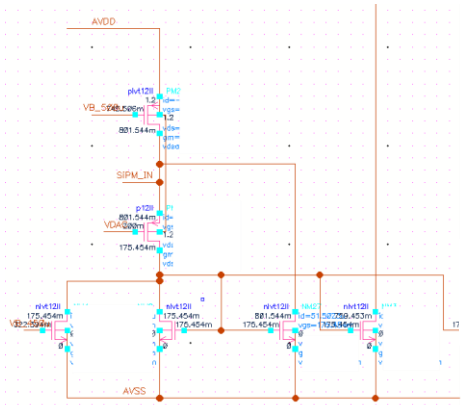
SIPAC_H: for HCAL

- ECAL uses BGO, while HCAL uses glass coupled SiPM, and glass has a longer decay time (500ns), resulting in more discontinuous waveforms for small signal at the MIP level, and requires an integrating preamplifer
- For HCAL version of SIPAC_H, the front end adopts a current-mode preamplifier, combined with a back-end integrating circuit, to process discontinuous small signal

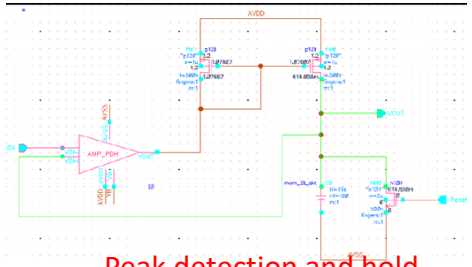


HCAL SiPM Small signal

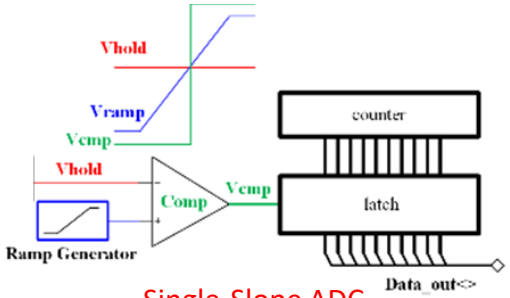




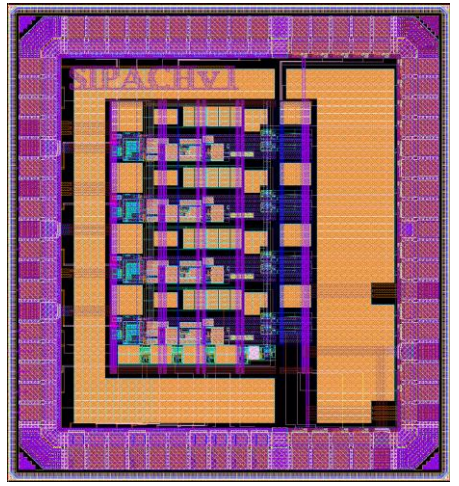
Current buffer amp.



Peak detection and hold



Single-Slope ADC



Layout size:1.3mm x 1.4mm
55nm CMOS process, TO Oct.2025

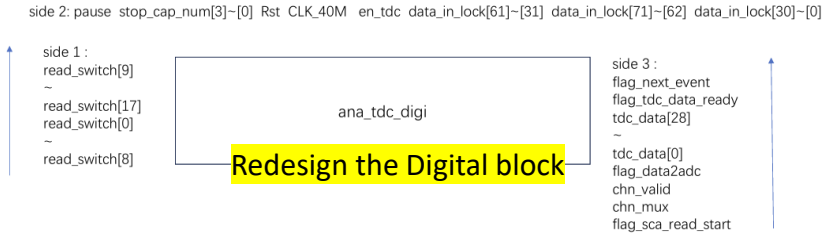
Table 8.5: SiPM characteristics that drive the requirements for the readout electronics design.

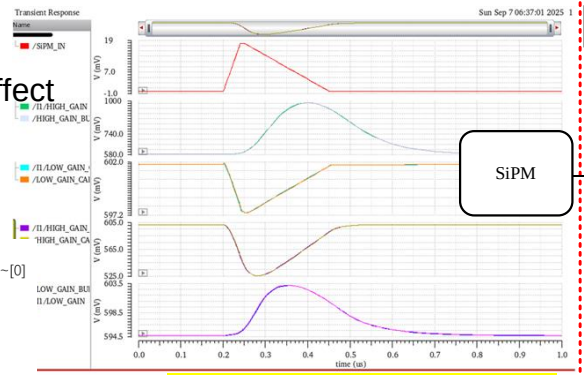
Item	Requirement
Charge dynamic range	0.8 pC~800 pC (0.1~100 MIPs)
Charge resolution	10% of 1.0 MIP
SiPM capacitance	≤ 100 pF
SiPM gain	≥ 5×10^5
Average event rate/channel	2 kHz
Max event rate/channel	50 kHz
Typical signal	2~3 mV/p.e.

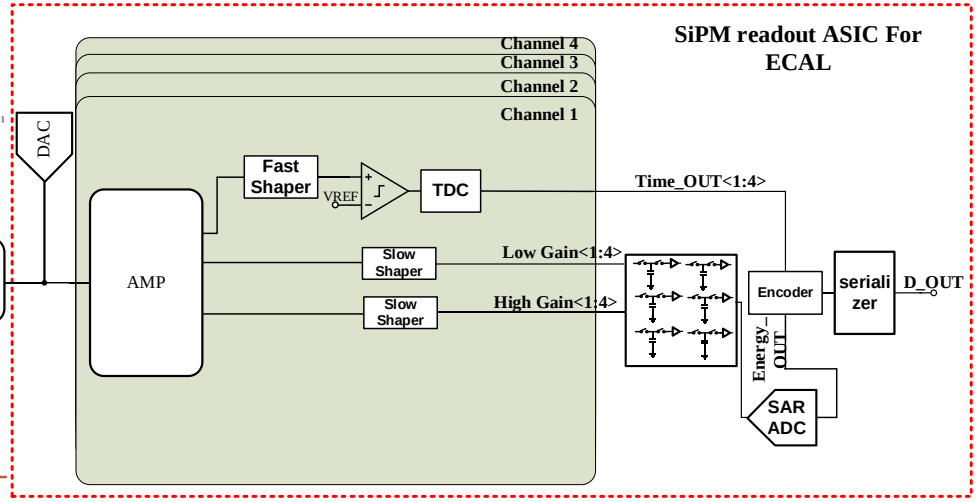
- SIPAC HCAL
  - Based on SIPACv0，using current buffer to replace voltage amp as the preamplifier
  - Remove TDC module，and issues encountered in SIPAC0 have been fixed
  - Using single-slope ADC to replace SAR ADC
  - Smaller layout area：1.3mm x 1.4mm

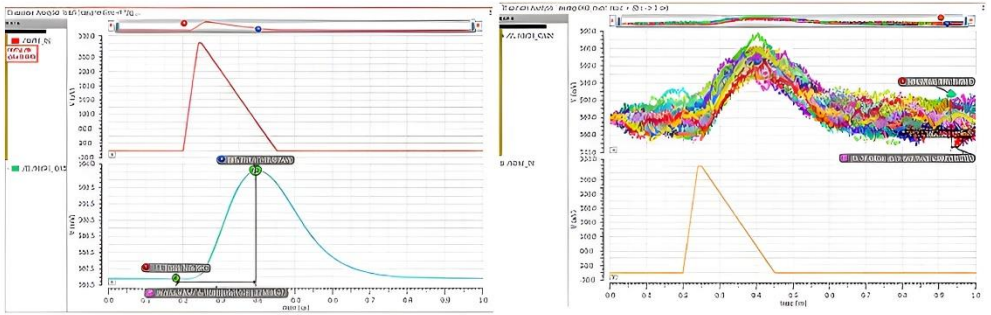
SIPAC_E: for ECAL

- SIPAC_E main revision
  - Fix the issues in SIPAC0
  - Modification and optimization of the shaper
  - Optimization of the SCA, to improve the charge sharing effect
  - Optimization of the control logic
  - Optimization of the test-point buffer
  - Smaller area: from 2.0mm x 2.3mm, to 1.3mm x 1.9mm



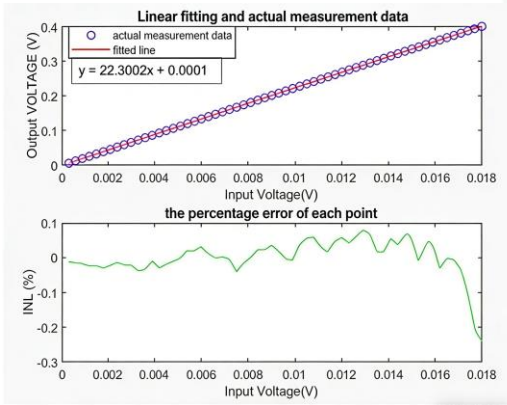






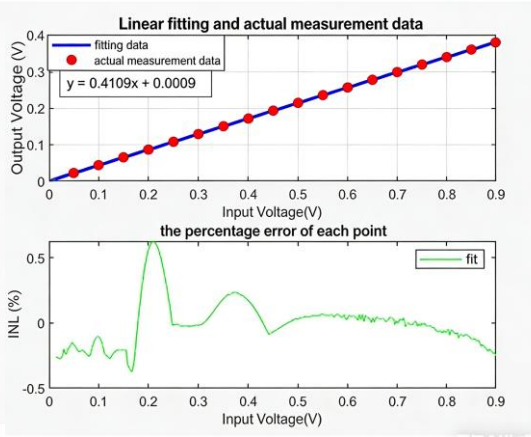
Output of High-Gain Gear at 300 uV Input

When 1 MIPS input, i.e., 300 uV, is applied, the output of the high-gain gear is 6.7 mV with an amplification factor of about 22 times. After adding transient noise with a maximum noise frequency of 1 GHz, the simulated RMS noise is 947 uV, and the system's signal-to-noise ratio is 7.07.



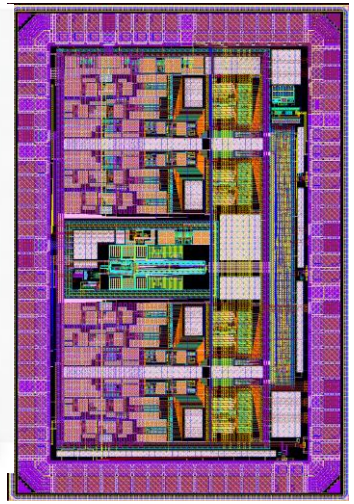
Linearity of Buffer Output Node in High-gain Gear

1-60MIPs, INL<0.3%



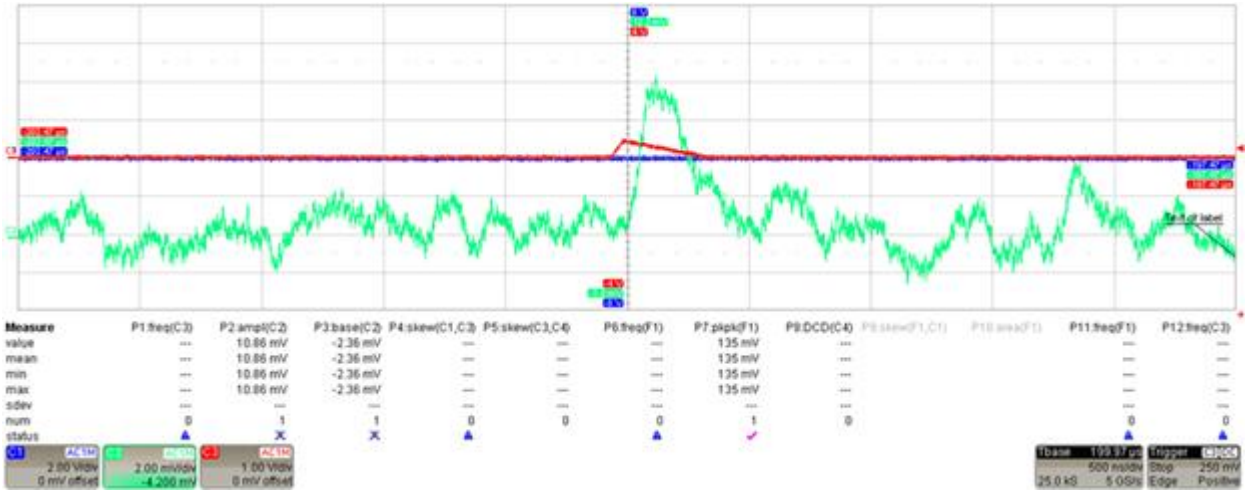
Linearity of Buffer Output Node in Low-Gain Gear

50-3000MIPs, INL<0.6%

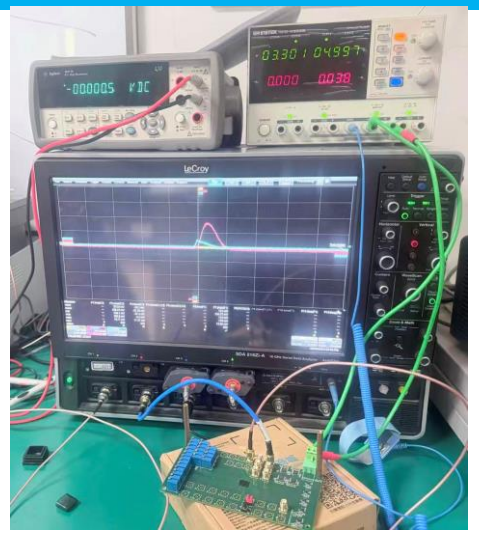


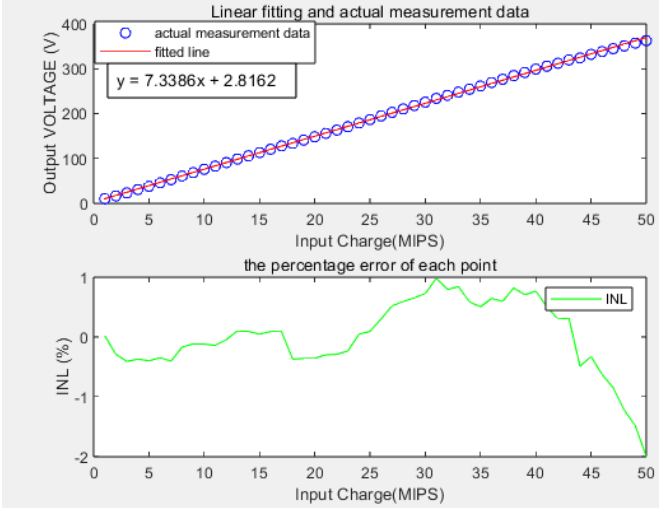
Layout size:1.3mm x 1.9mm
55nm CMOS process, Oct.2025

SIPAC_E test(Preliminary, 2026.3.24)



SNR =4 @1MIP of high-gain shaper



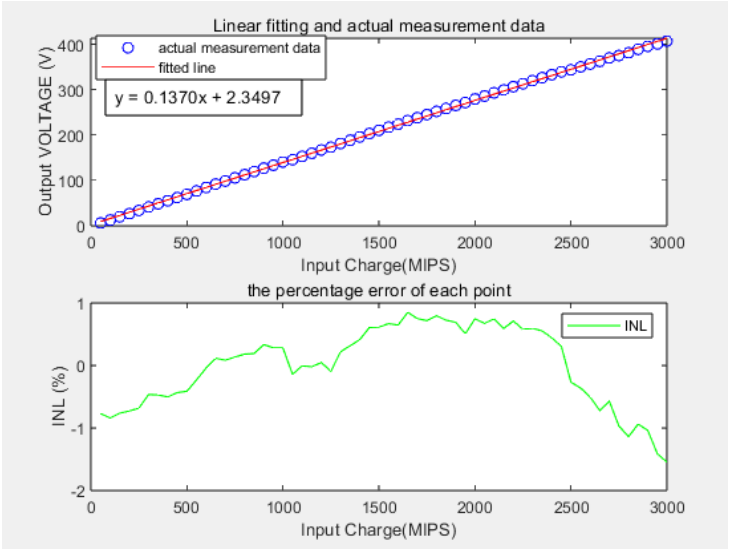


1-50MIPs, INL<1%

Dynamic range: 1 MIP – 3000 MIPS
(300 μV – 900 mV)

Equivalent input noise: 75 μV

Gain: 22 @ High Gain,
0.41 @ Low Gain
(Close to simulation values)



50-3000MIPs, INL<1.6%

Summary

- SIPAC_E & SIPAC_H testing is ongoing, more detailed test results will be available in the coming weeks.
- The time-line of SIPAC
  - SIPAC design starting from the end of 2024
  - 1st Tape-out: April 2025, SIPAC0, validation of the key block
  - 2nd Tape-out: Oct. 2025, SIPAC_E & SIPAC_H, revision of the chip
  - Next step, aiming to practical ASIC