A Low-Power Timing Chip Prototype for Strip LGAD Readout

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on behalf of Elec and OTK

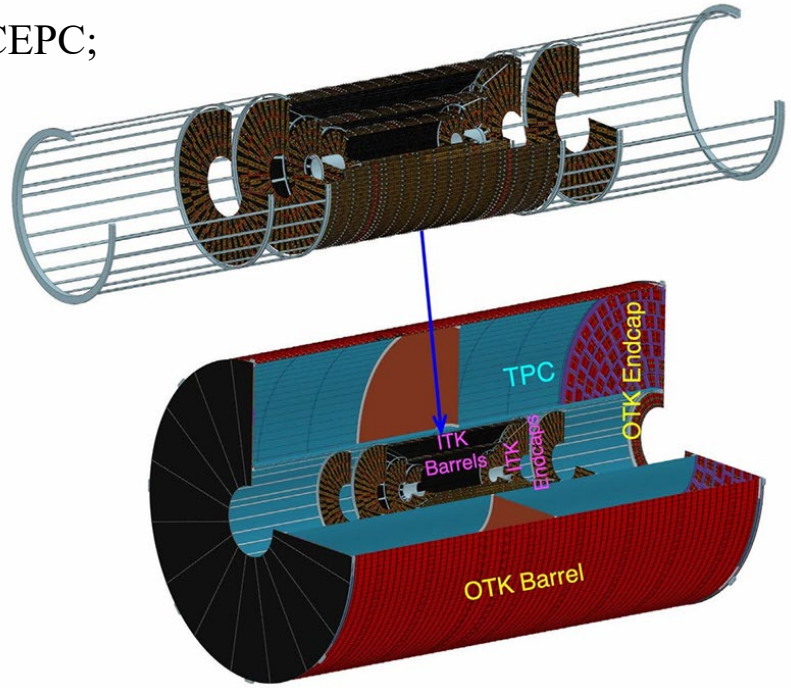
Outline

- Introduction
- LATRIC0 & Test
- LATRIC1 & Test
- Conclusion

Introduction

◆ OTK

- The outermost detector of the tracking system in the reference detector of the CEPC;
- Uses AC-LGAD microstrip sensors;
- Provides both high spatial resolution (10 μm) and high time resolution (50 ps).



◆ ASIC specification in TDR

Table 5.12: Configuration for the LATRIC ASIC (assuming a detector capacitance C_d = 8 pF)

Parameter	Value
Voltage	1.2 V
Number of channels	128
Channel pitch	< 100 μm
Single channel noise (ENC)	< 10,000 e^- (1.6 fC)
Cross-talk	< 10%
Maximum jitter	30 ps at 16 fC
Minimum threshold	4 fC
Dynamic range	8 fC–50 fC
TDC conversion time	< 23 ns
Power dissipation per ASIC	1.5 W (for occupancy < 1%)
Data size per fired channel	48 bits
e-link driver bandwidth	43.33 Mbps or 86.67 Mbps

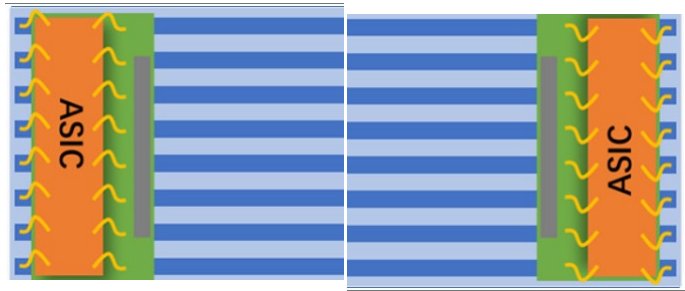
→ (Wire bonding channel to channel)

→ (Assume LGAD contributs 40 ps)

$$\sigma_{hit}^2 = \sigma_{Landau}^2 + \sigma_{clock}^2 + \sigma_{elec}^2$$

→ (Large cap leads to high consumption)

$$\sigma_{\text{jitter}} = \frac{e_n C_d}{Q_{in}} \sqrt{t_d} \propto \frac{C_d \sqrt{t_d}}{Q_{in} \sqrt{I}}$$

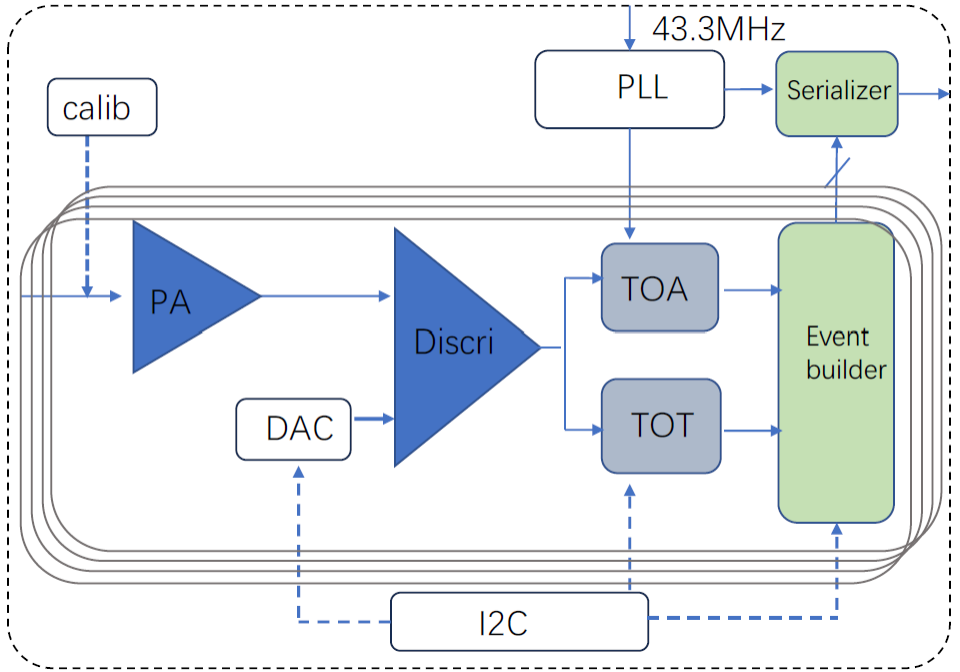


Layout of module

LATRIC

◆ **LATRIC（LGAD Timing and Readout Integrated Chip）**

- ➢ Front –end
  - Preamplifier and Discriminator
  - Threshold DAC for each channel
- ➢ TDC
  - Time of Arival (TOA) for arrival time
  - Time over Threshold (ToT) for signal charge
- ➢ Event builder: Data arrangement, scrambling, and packing
- ➢ PLL: Clock management
- ➢ Serializer: Data output and transmission
- ➢ I2C: Configuration of control bits



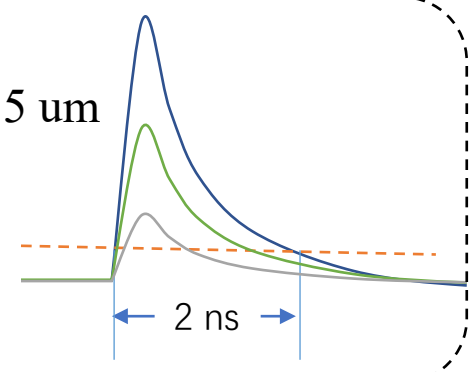
■ LATRIC0 (single-channel, April, 2025)

- ■ Front-end, TDC, Serializer（720MHz）

■ LATRIC1 (8-channel, October, 2025)

- ■ Front-end, TDC (improved), Event builder, Serializer（40 MHz）
- ■ 4 channel with Front-end, 4 channel without.

Spacial resolution:
50 ps/2 ns*100 um=2.5 um



LATRIC0 Circuit Design

◆Architecture

- Front-End (FE)
  - An amplification and a discrimination.
- TDC core
  - *Timing controller;*
  - *Event-Driven RO & Quantization logic;*
  - Encoder.
- Output logic
  - Output the Measured CAL, TOT, TOA codes;
  - 128-bit Serializer for 111-bit raw data;
  - 40-bit Serializer for 36-bit encoded data;

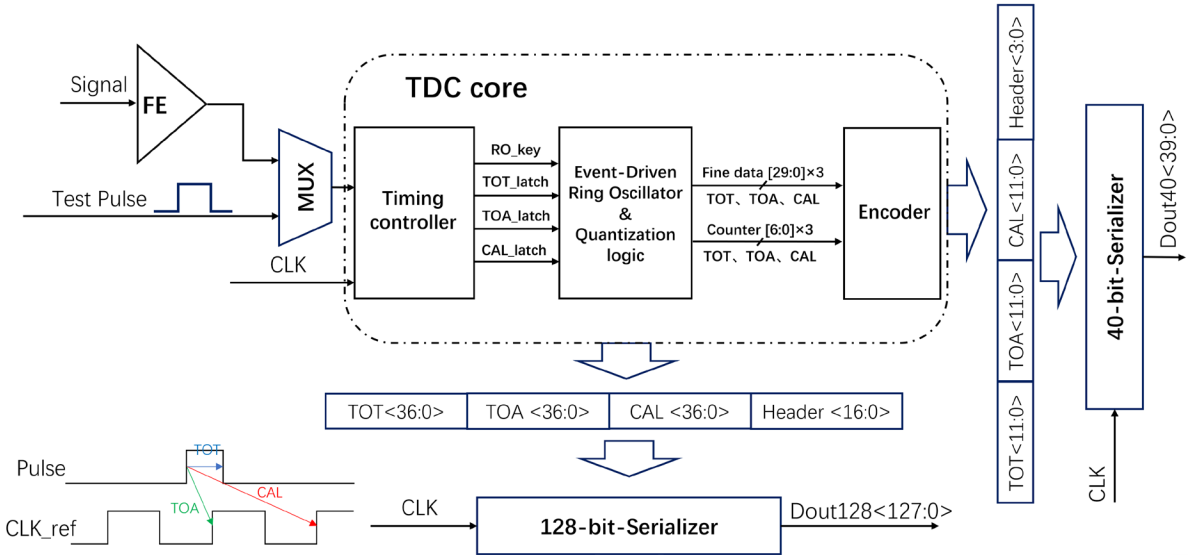


Fig 2. The overall block diagram

■ Self-calibration

- An additional period of CLK_ref is measured for calibration: $LSB_{Cal} = T_{CLK\_ref} / (CAL_{code} - TOA_{code})$;
- $TOA_{time} = LSB_{Cal} * TOA_{code}$;
- $TOT_{time} = LSB_{Cal} * TOT_{code}$.

Circuit Design

TDC core

- Ring Oscillator (RO)& Quantization logic
  - The RO employs 15 NAND-based delay cells, each providing an average delay of about 30 ps;
  - The 15 S2D converters transform both the rising and falling edges into **differential** signals for the three groups of SR latches;
  - The **symmetric** structure of SR latch ensures a consistent response to both rising and falling edges from the delay cells.

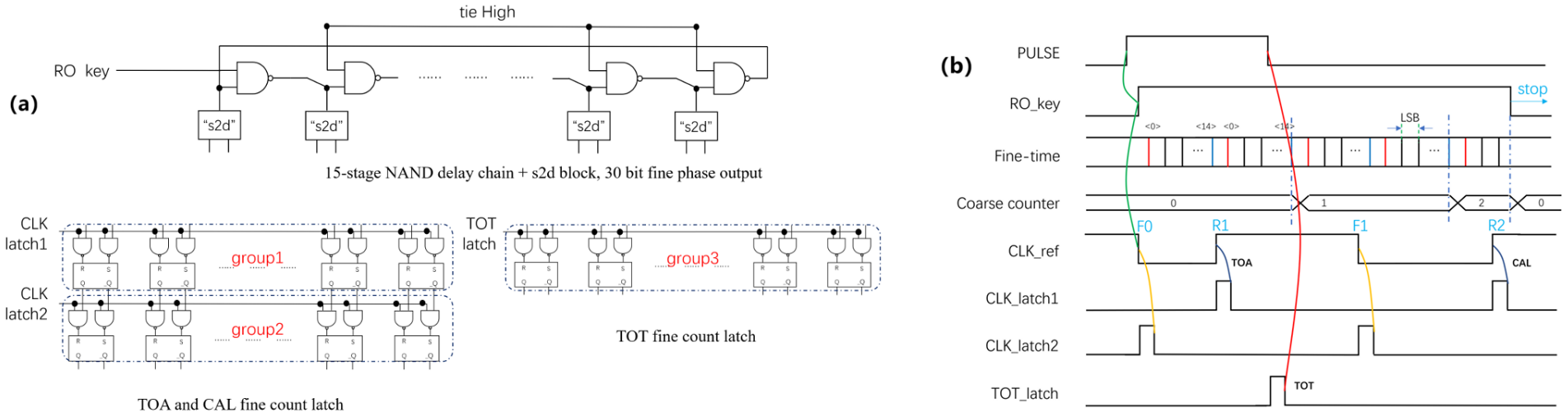
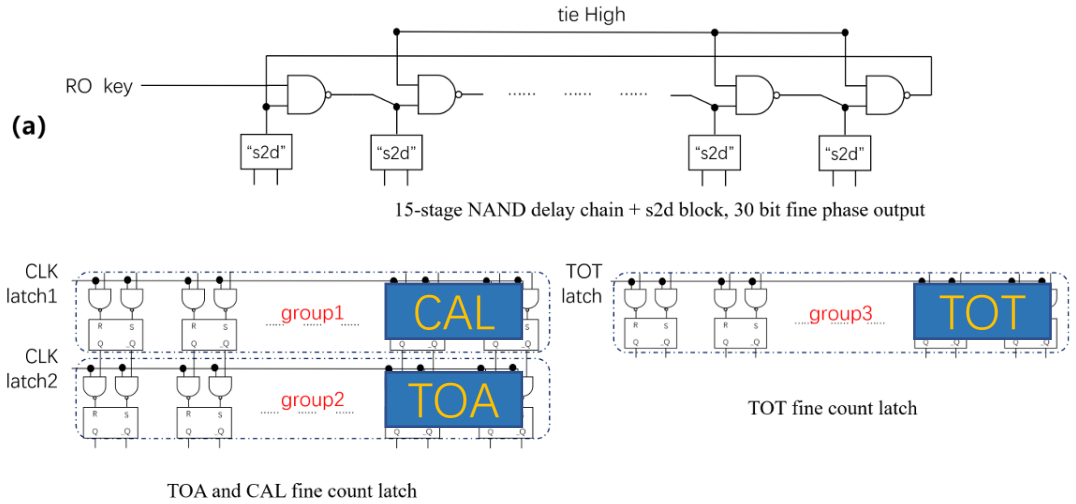


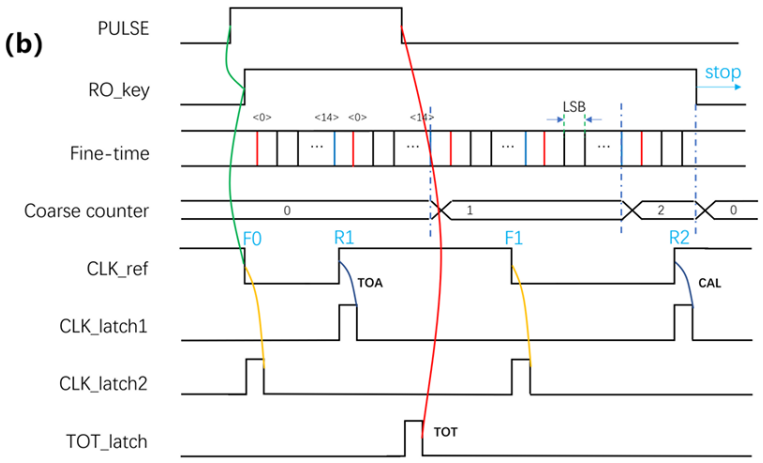
Fig 3. (a) Event-Driven RO & Quantization logic; (b) Quantization timing

Quantization logic

TDC core Quantization timing

1. When the leading edge of the PULSE signal arrives, the RO is activated, the CLK_ref is enabled, coarse count starts;
2. The first rising edge (R1) of CLK_ref generates the CLK_latch1, which captures the TOA information in the latch group1;
3. The falling edge (F1) generates CLK_latch2, transferring the TOA codes to the latch group2;
4. The rising edge (R2) of CLK_ref generates the second CLK_latch1 pulse, which latches the CAL information into the latch group1, overwriting the previous TOA codes;
5. The trailing edge of the PULSE signal generates the TOT_latch signal to capture the TOT information in the latch group3;



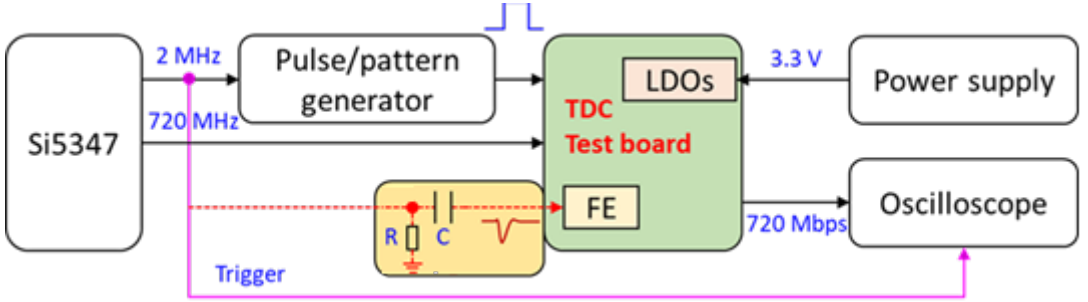


(a) Event-Driven RO & Quantization logic; (b) Quantization timing

LATRIC0 Test Results

Test Setup

- Test-pulse mode
  - A 720-MHz clock (Si5347) for both serializer and TDC. Inside the TDC, the 720-MHz clock is divided down to 18 MHz and used as the reference clock for TOA measurement.
  - A 2-MHz clock (Si5347) to trigger a pulse/pattern generator (81130A). Both the pulse width and relative delay of pulse signal are independently adjustable. This function enables scanning of TOT and TOA transfer curves.
  - The averaged and rounded TDC output code from repeated measurements are used to plot the transfer curve.
- FE-mode
  - For functional verification of the FE-TDC integration, a calibration cap of 1 pF is used as input of FE.



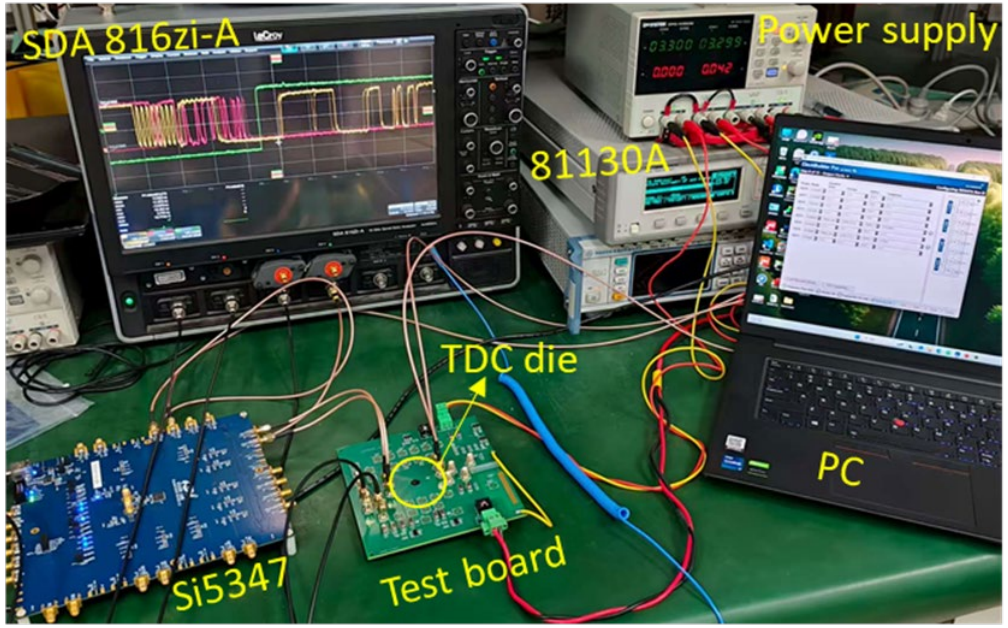


Fig 3. Test setup

LATRIC0 Test Results

Timing performance (test-pulse mode)

- LSB $_{toa} \approx 31.1$ ps;
- The TOA DNL and INL without FE : less than ± 1 LSB;
- LSB $_{tot} \approx 31.0$ ps ;
- The TOT DNL and INL without FE : less than ± 1 LSB;

- LSB $_{cal} \approx 31.1$ps ;
- These three LSB are very close, indicating the effectiveness of the self-calibration.

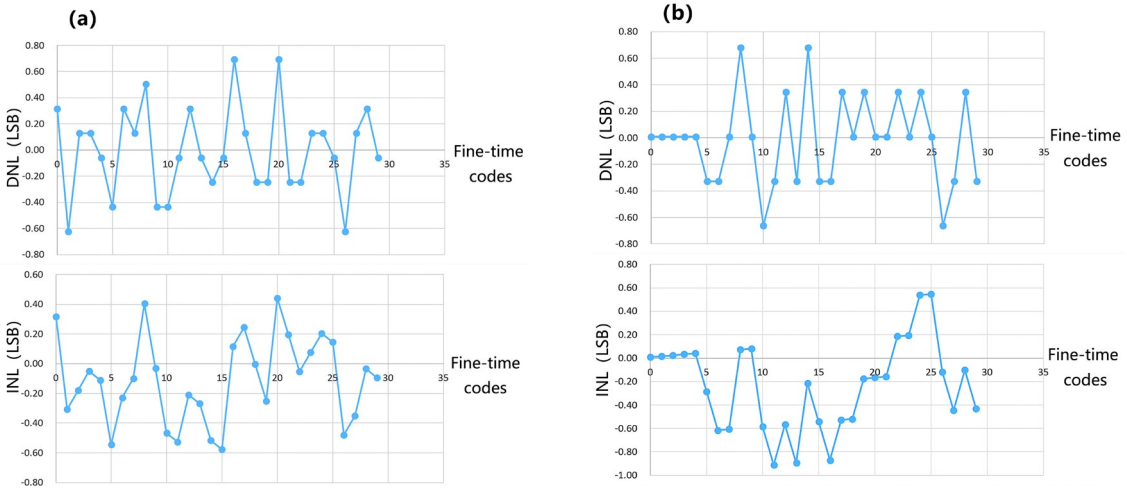
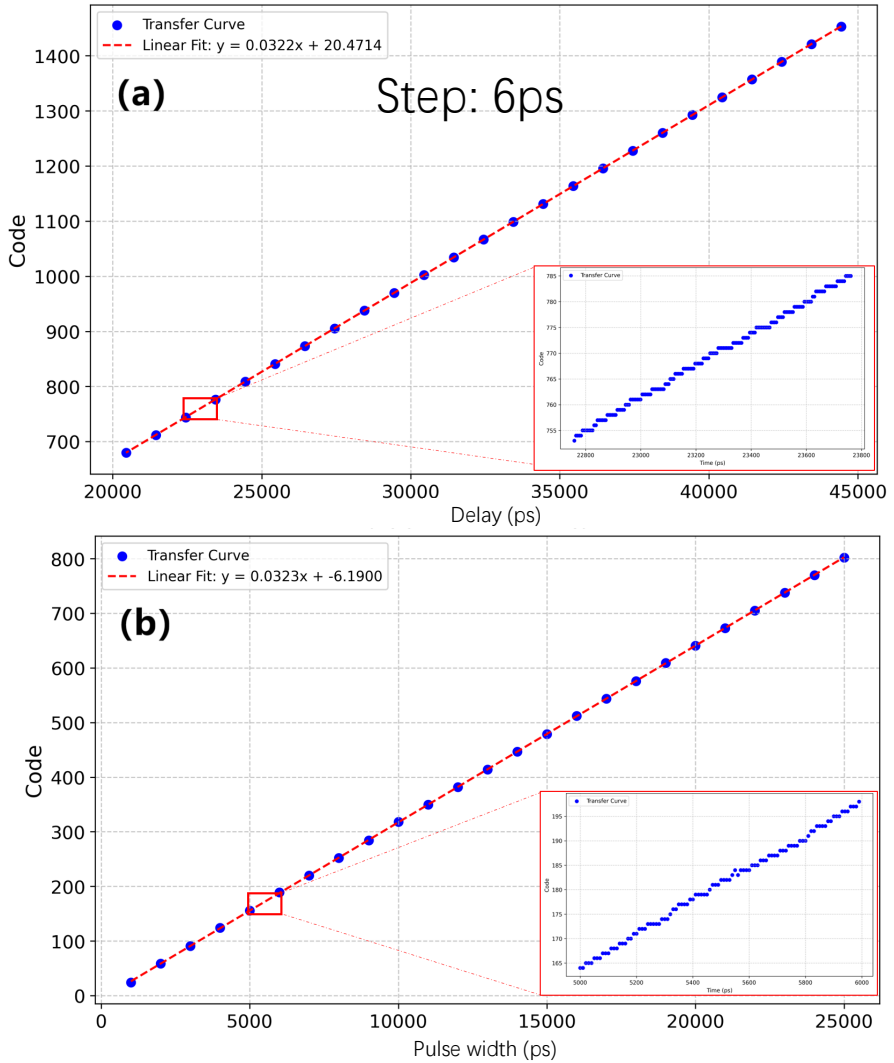


Fig 4. DNL & INL of: (a) TOA; (b) TOT

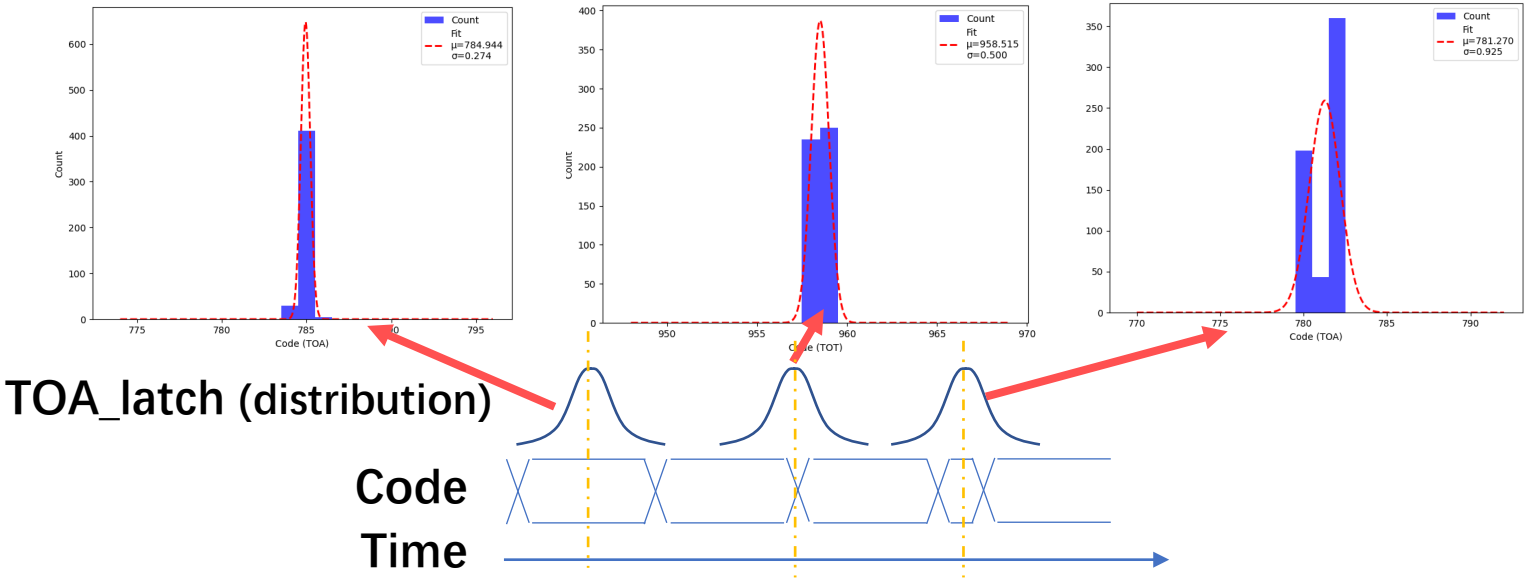


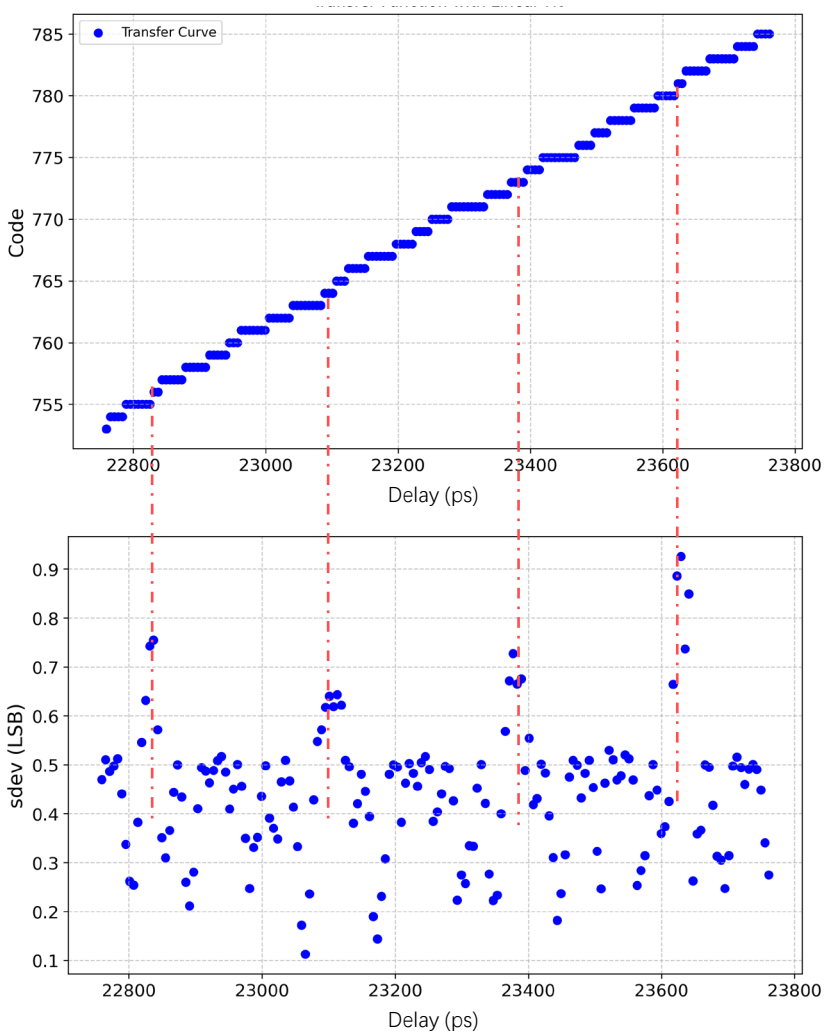
Measured transfer curves of: (a) TOA; (b) TOT

LATRIC0 Test Results

Timing performance (test-pulse mode)

- σ < 0.5 LSB for most steps
- For σ > 0.5 LSB:
  - It happens at place with smaller bin width.
  - The code varies more to the jitter of the input for smaller bin width.





The standard deviation of Single Shot Precision

LATRIC0 Test Results

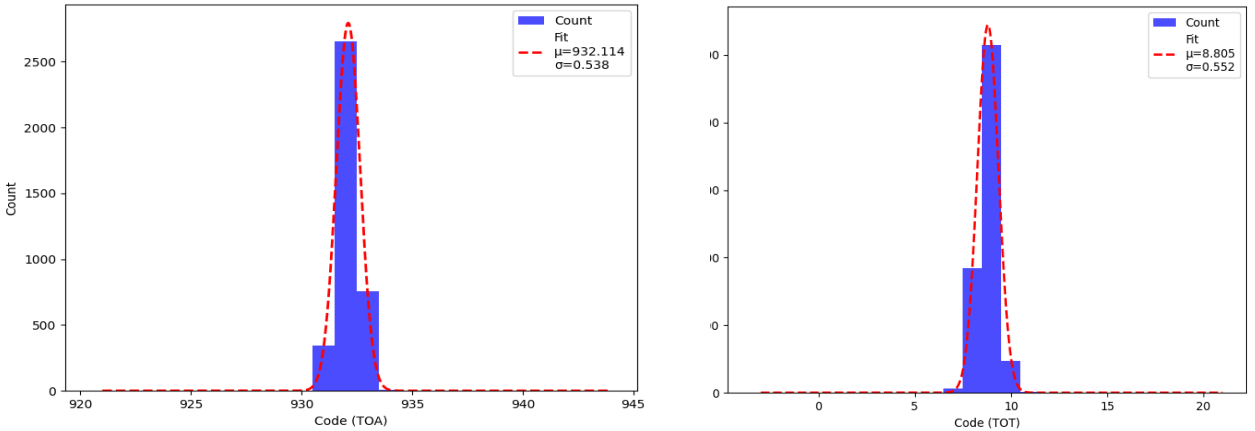
Timing performance (FE-mode)

- $\sigma_{FE\text{-}TOA}$ and $\sigma_{FE\text{-}TOT}$ distributions <0.55 LSB for a 8.0 mV （8fC） input signal.

Power consumption

- The FE consumes 4.9 mA (1.2V).
- The power consumption of the TDC core varies with event rate.
- The total power consumption is measured to be 6.24 mW at an event rate of 1 MHz.

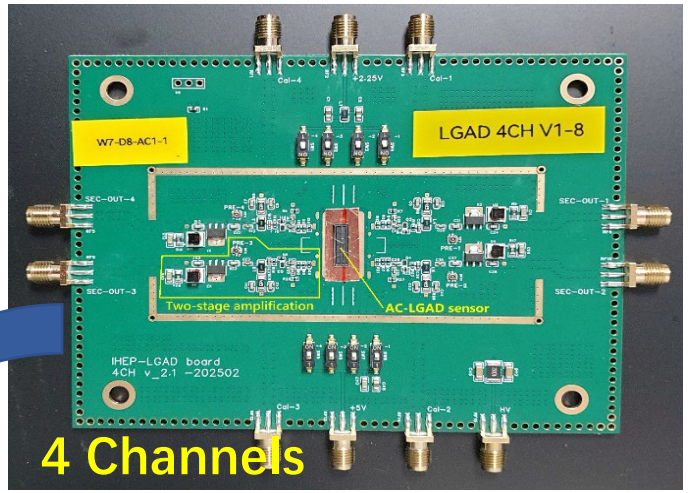
Blocks	Event rate	Operating current
TDC part	2 MHz	~ 0.5 mA
	1 MHz	~ 0.3 mA
	500 kHz	~ 0.1 mA
Pre-amplifier		~4.9 mA

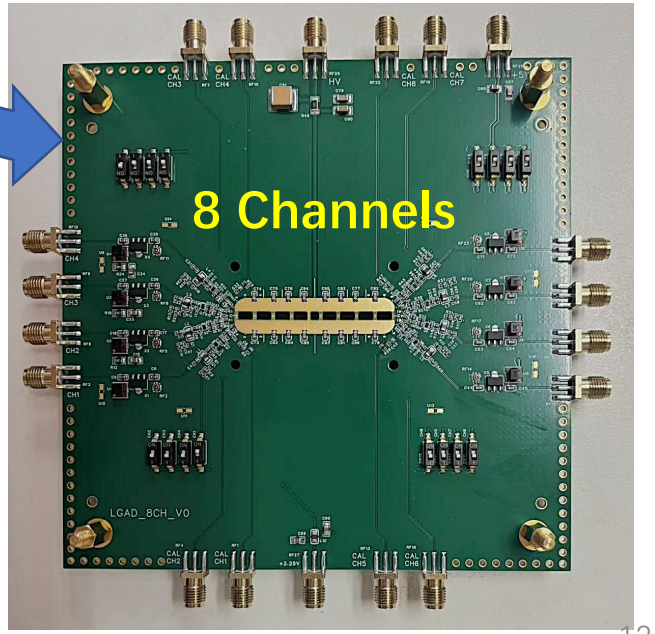


The statistical standard deviation for single shot
（input 8fC， Vth=830mV）

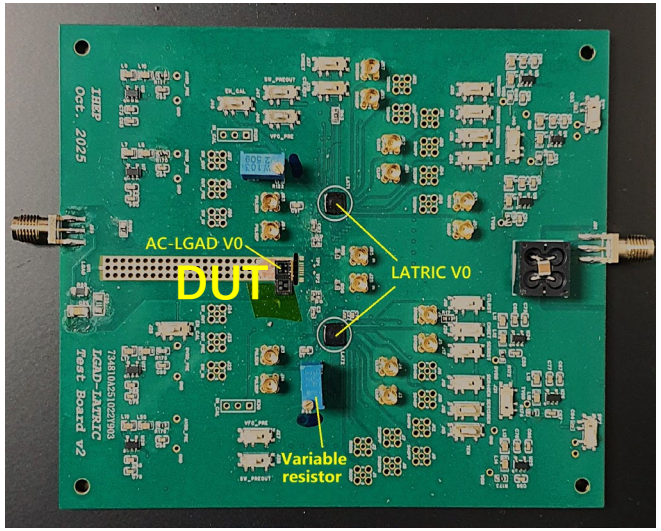
LGAD test board

- For spatial resolution measurement, new test board for LGAD：
  - Increase channels: 4 CHs → 8 CHs;
  - Improve the stability of circuit；
  - Reduce the bonding wire: 5.4 mm →1.1 mm；
  - Increase slots for β test;
  - Match 4 cm LGAD strip.



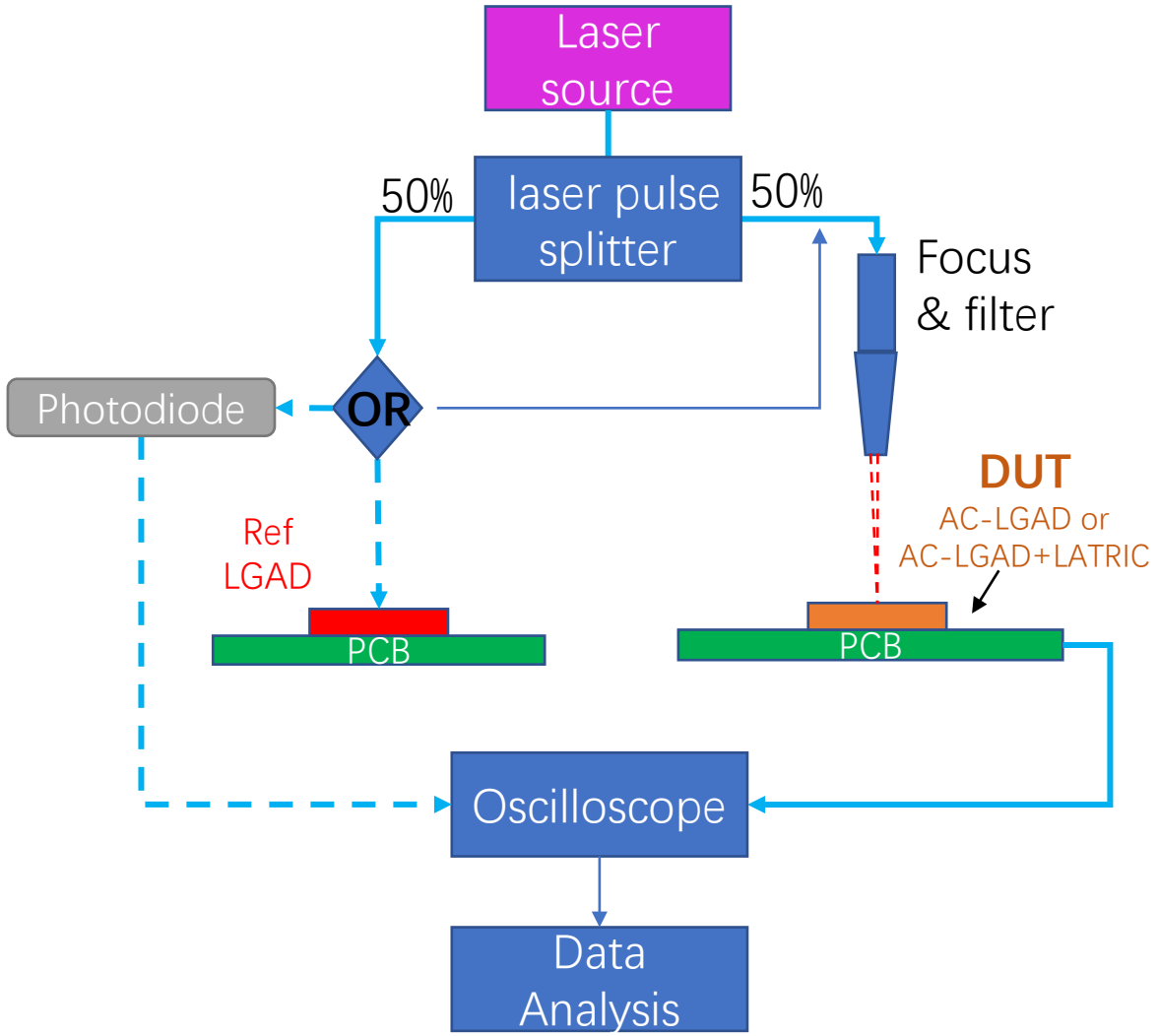


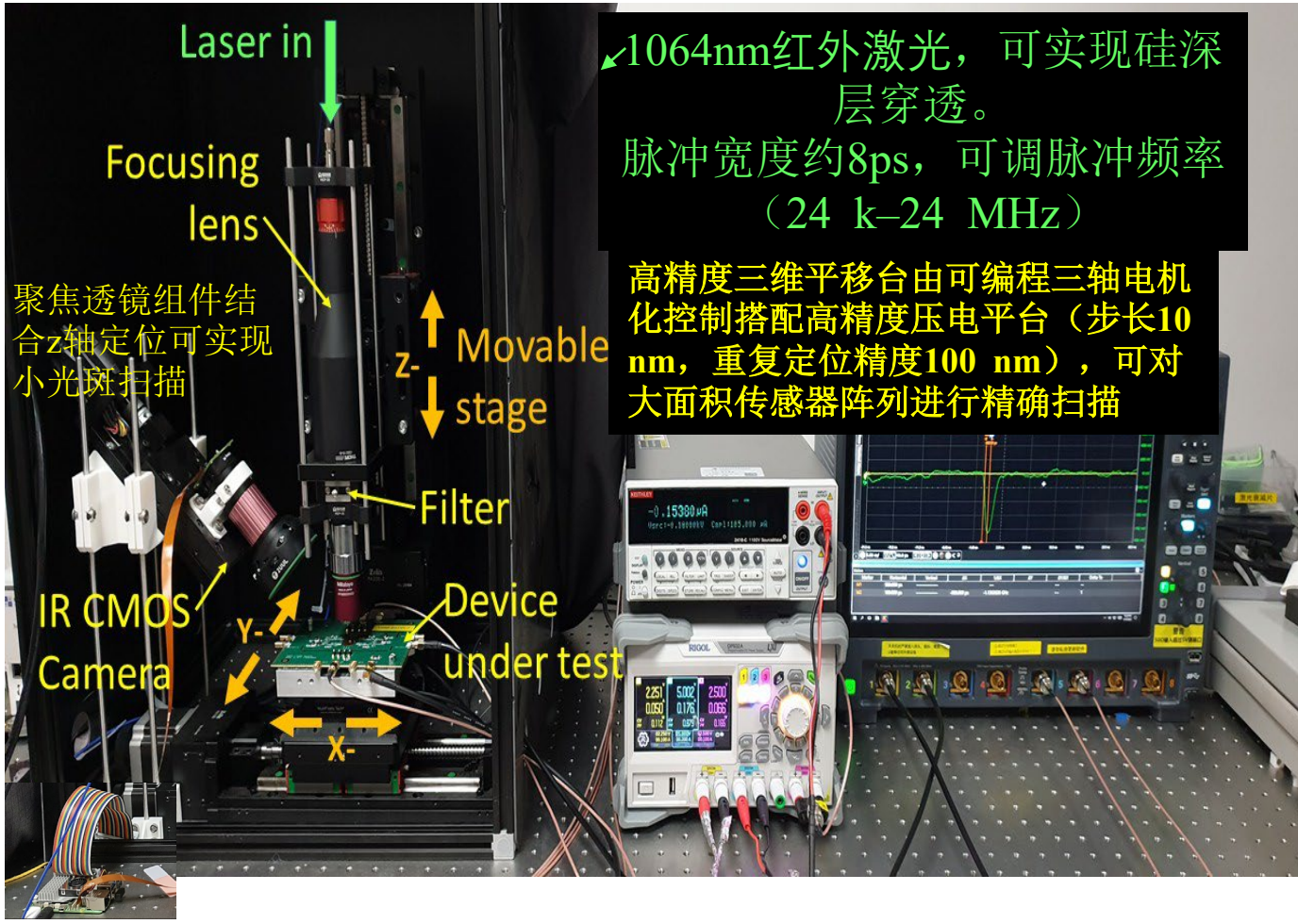
- LGAD+LATRIC0 joint test：
  - 2 LATRIC0s;
  - Match 4 cm LGAD strip;
  - 2 LGAD pixel 2.5mm* 2.5mm.



Time measurement step up

Transient Current Technique, TCT

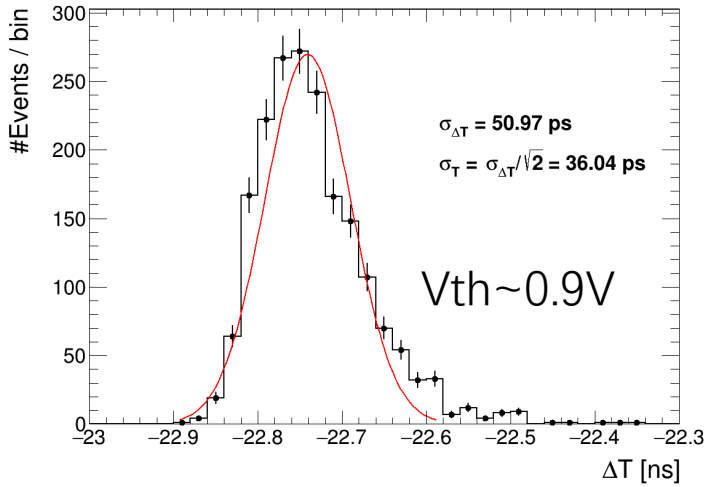




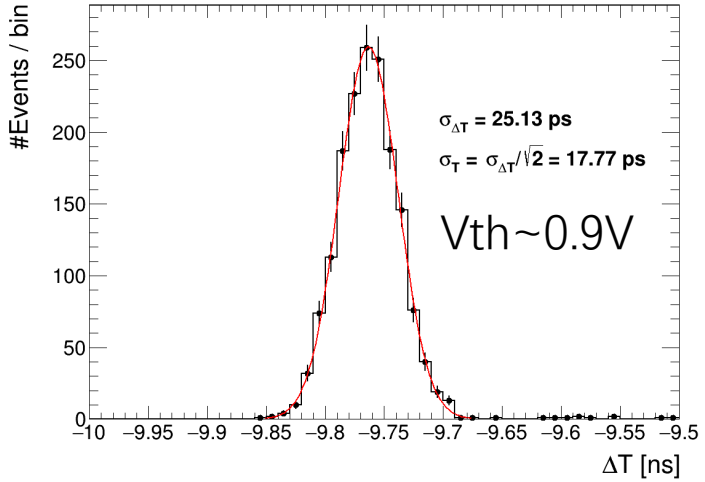
↙1064nm红外激光，可实现硅深层穿透。
脉冲宽度约8ps，可调脉冲频率（24 k–24 MHz）

高精度三维平移台由可编程三轴电机化控制搭配高精度压电平台（步长10 nm，重复定位精度100 nm），可对大面积传感器阵列进行精确扫描

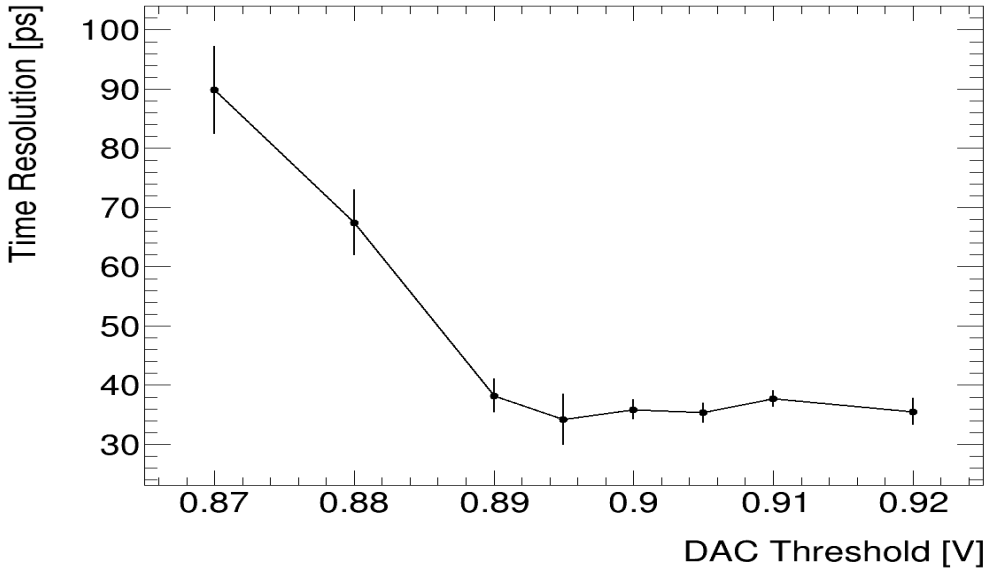
Coincidence test (LGAD+LATRIC0)



TOA coincidence time resolution @ Laser intensity equivalent to MIP



TOA coincidence time resolution @ 100% laser intensity

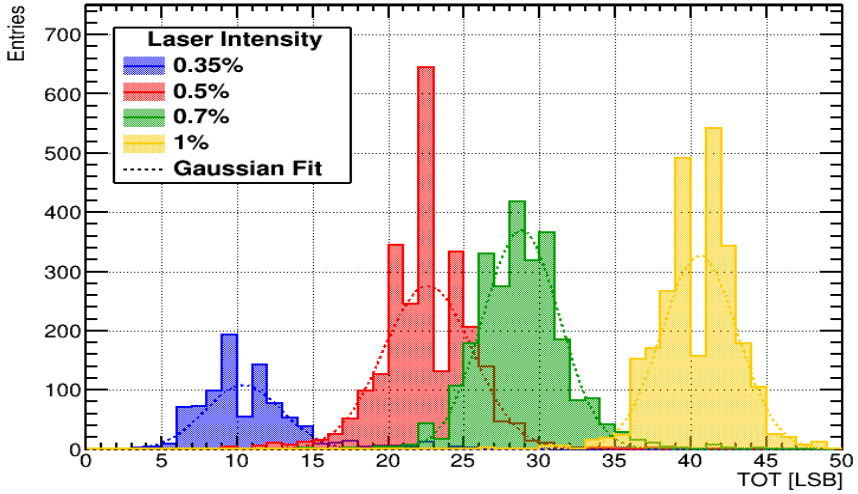


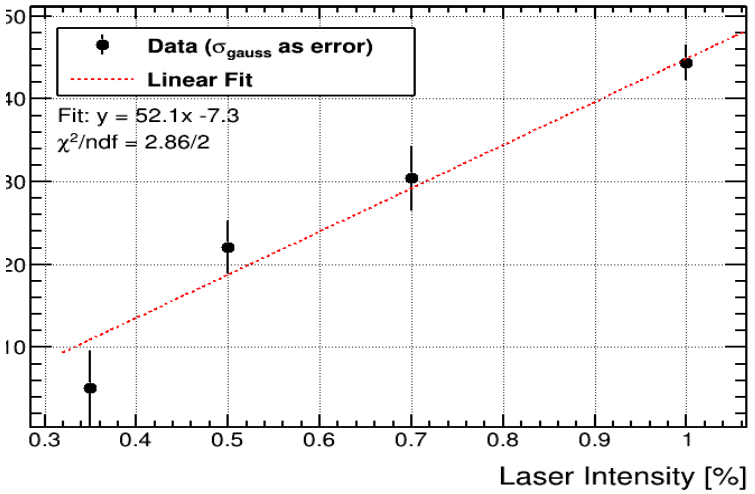
- The resolution deceases with threshold with an equivalent MIP laser.

TOT with different Laser intensity

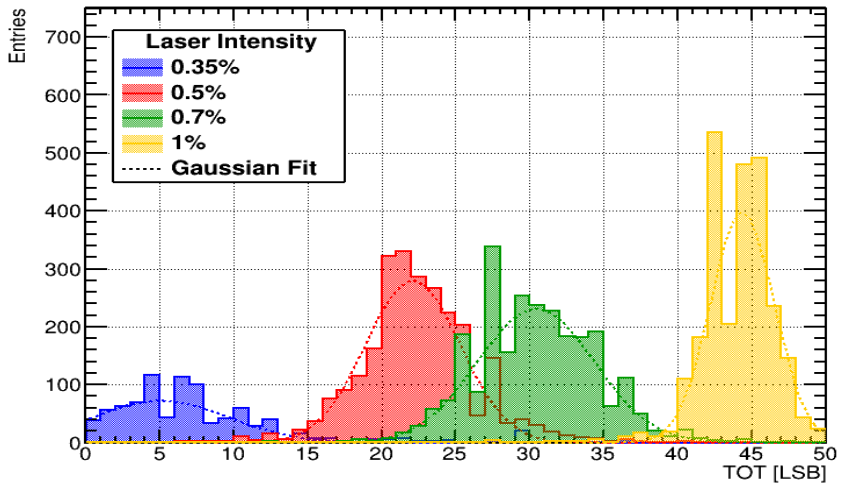
- TOT changes with the laser intensity, more study needed

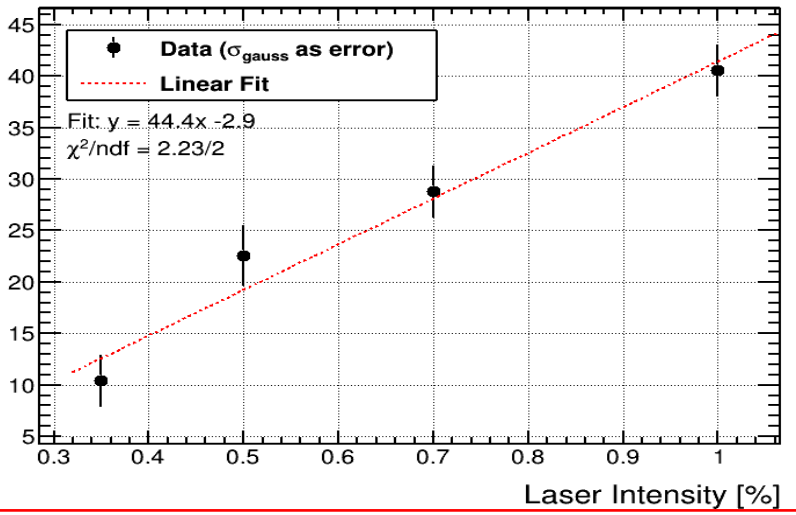
LATRIC-1





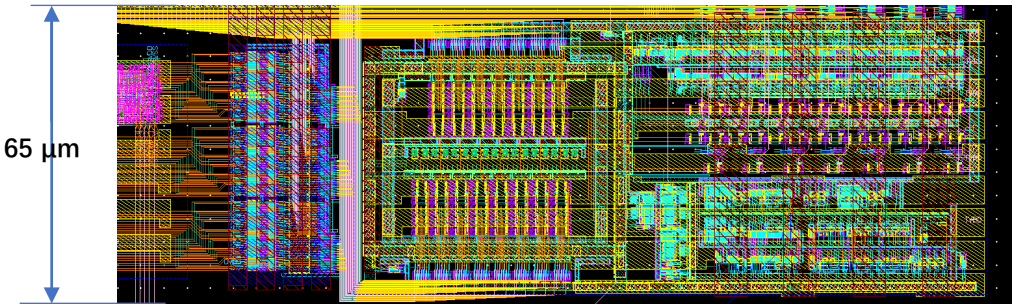
LATRIC-2

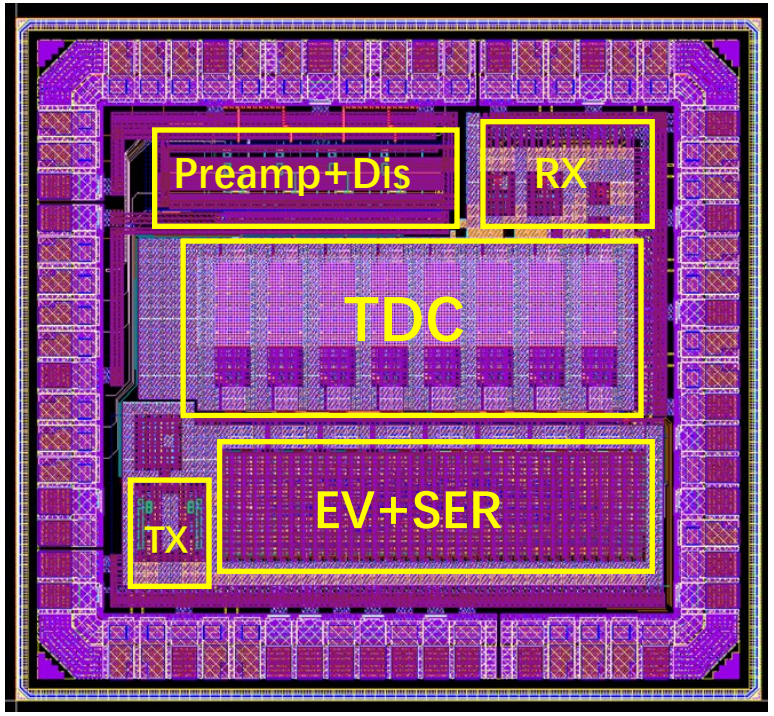




LATRIC1

- LATRIC0
  - Successful integration of FE and TDC in LATRIC0
  - High timing precision with low power consumption
  - Effective self-calibration with consistent LSB values
  - Meets CEPC requirements for OTK readout , including the height constrain of layout.
- LATRIC1
  - Submitted for tape-out in October 2025, received in Feb, 2026
  - 8 channels TDC; 4 channels with front-end;
  - Increase the gain of preamplifier;
  - Improve the encoder logic;
  - Add event builder and timestamp;
  - 100 μm channel pitch match the LGAD.



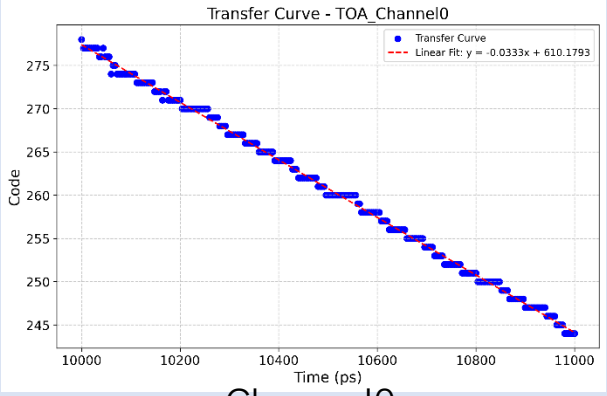


LATRIC1 layout

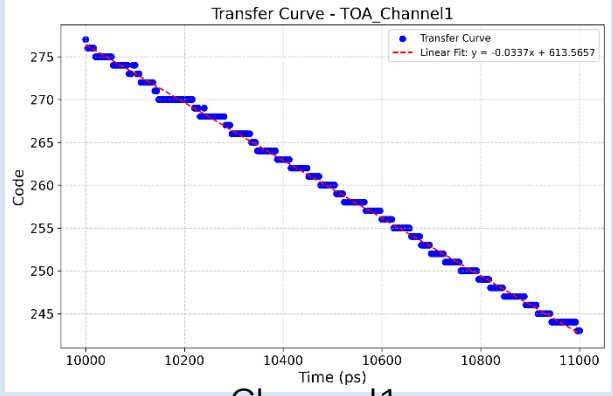
LATRIC1 Test -Transfer Curve

◆Resolution(LSB): CH0 ~29.80 ps , CH1~ 29.44 ps, CH2 ~ 27.09 ps, CH3~ 27.58 ps (step: 4ps)

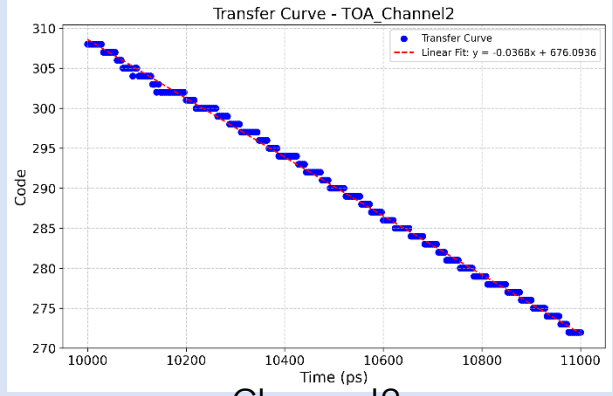
TOA (step: 4ps)



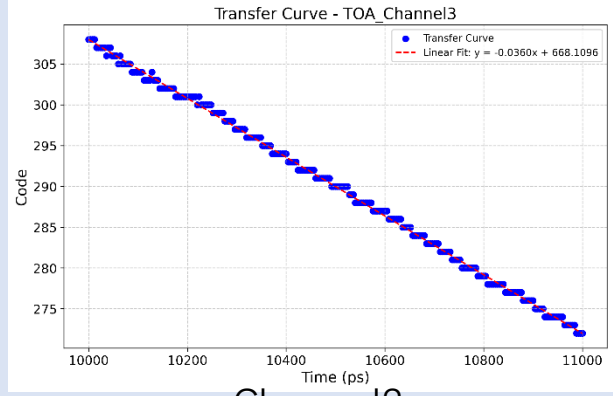
Channel0



Channel1

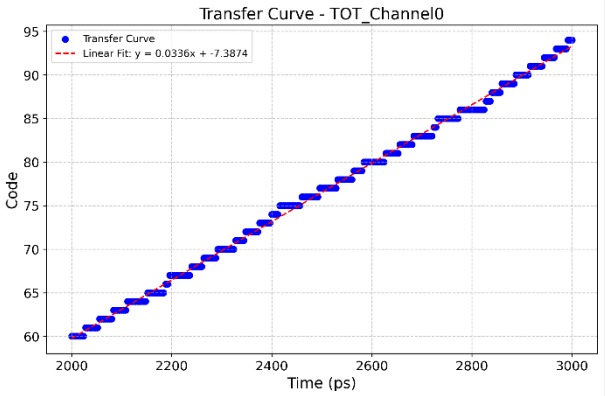


Channel2

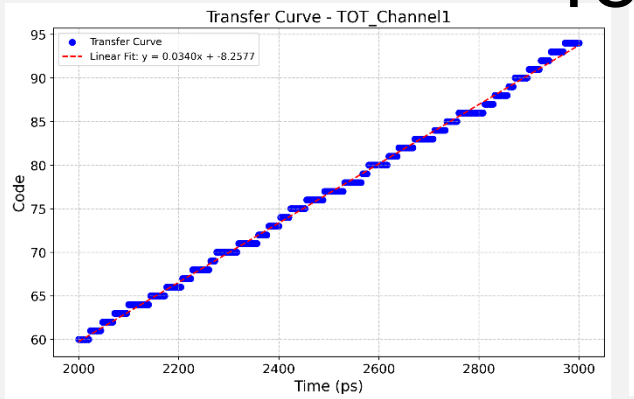


Channel3

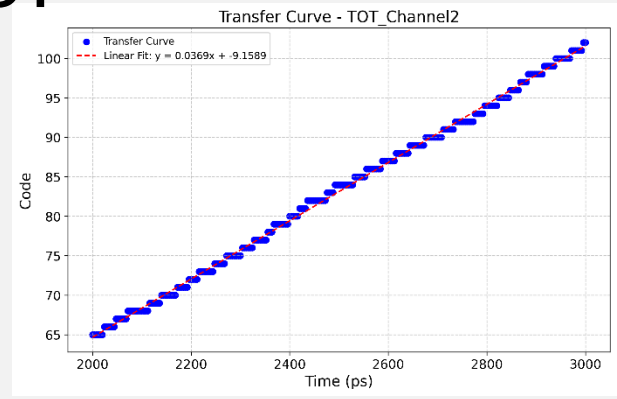
TOT



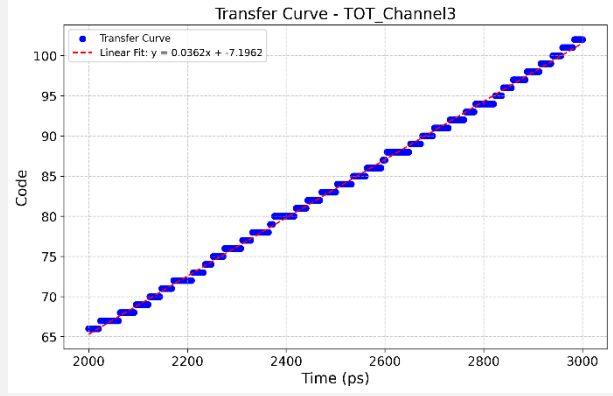
Channel0



Channel1



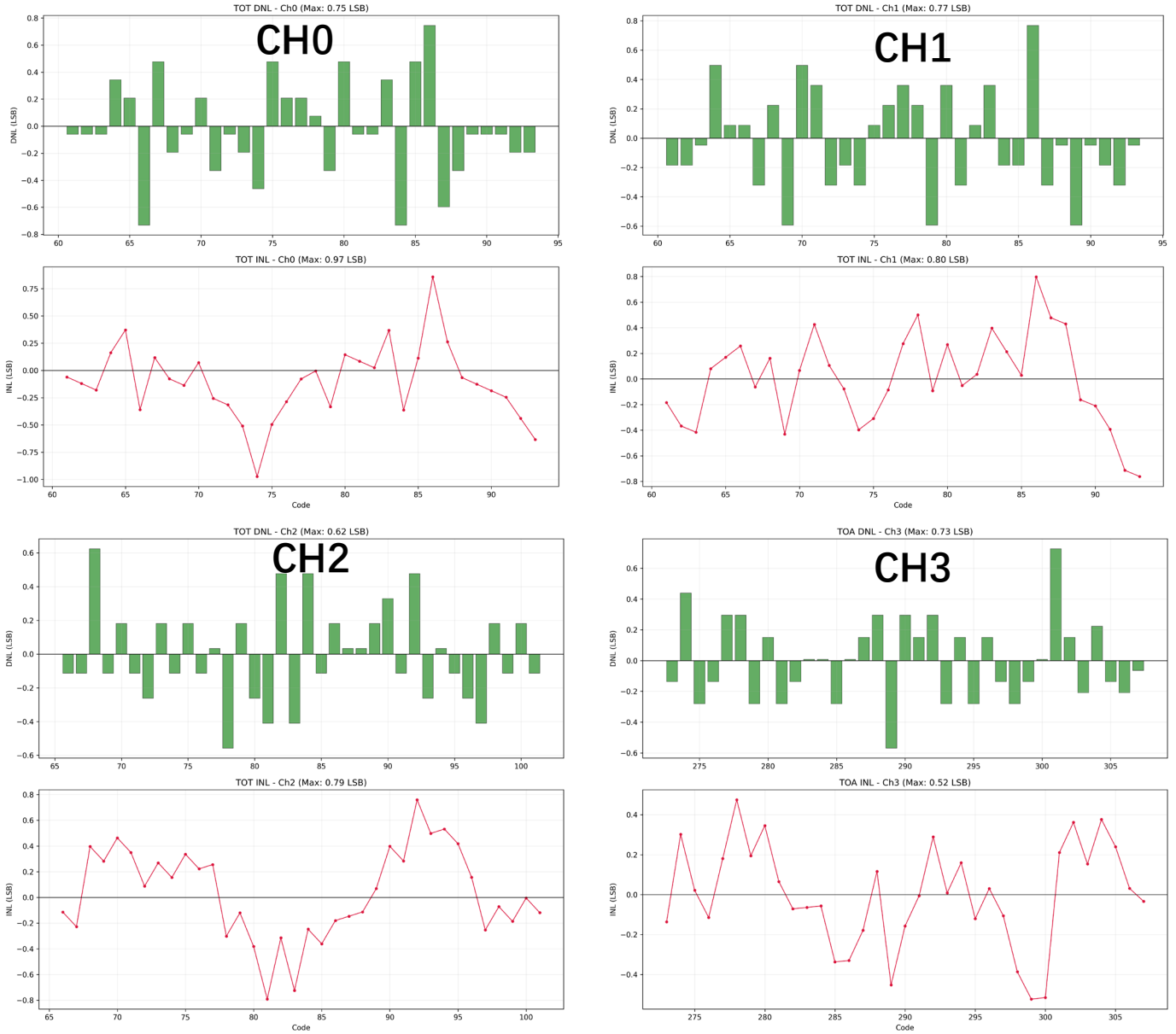
Channel2



Channel3

LATRIC1 Test -Linearity

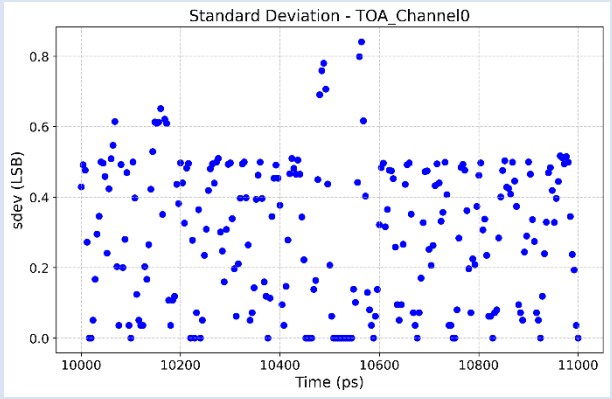
- CH0
  - INL: ±0.97 LSB
  - DNL: ±0.75 LSB
- CH1
  - INL: ±0.77 LSB
  - DNL: ±0.80 LSB
- CH2
  - INL: ±0.79 LSB
  - DNL: ±0.62 LSB
- CH3
  - INL: ±0.52 LSB
  - DNL: ±0.73 LSB



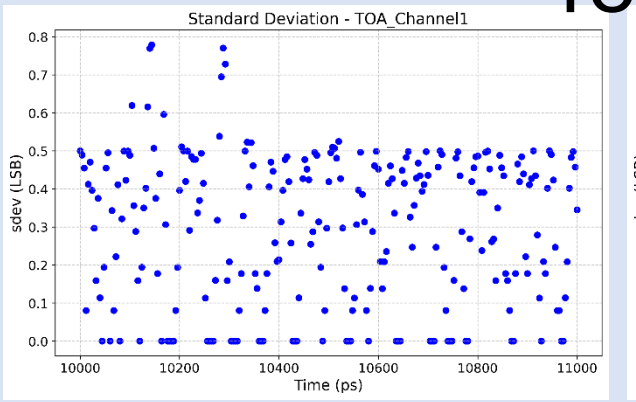
LATRIC1 Test -Single Shot Precision

◆ σ_{TOA}~ 0.5 LSB, σ_{TOT}~ 0.5 LSB

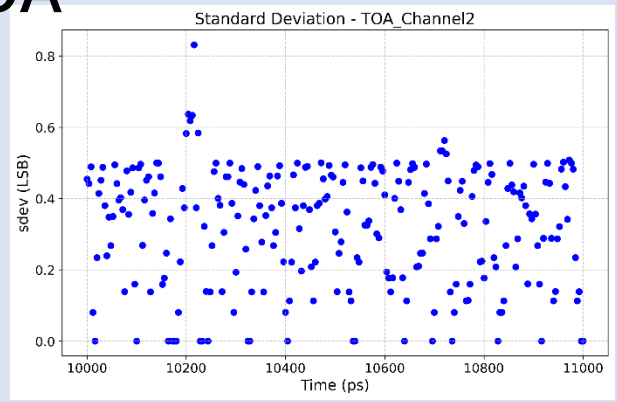
TOA



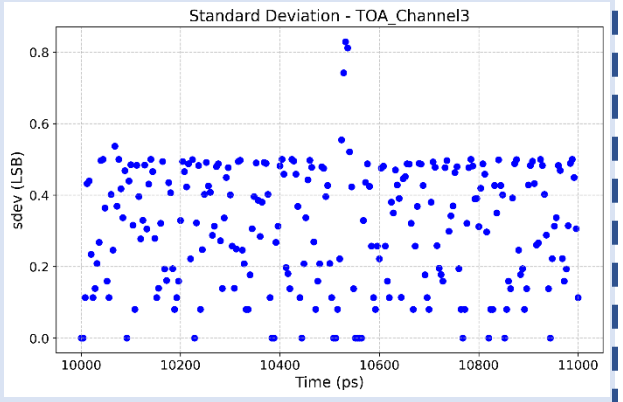
Channel0



Channel1

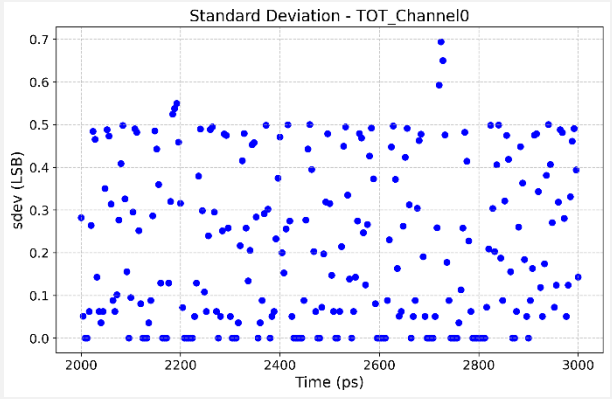


Channel2

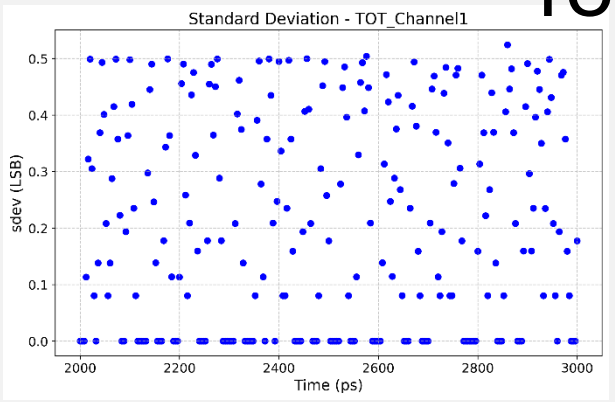


Channel3

TOT



Channel0



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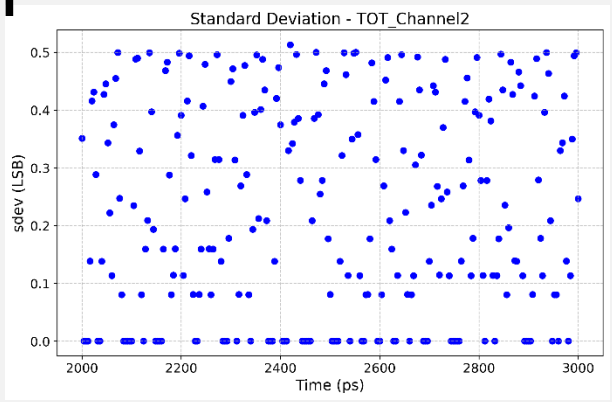

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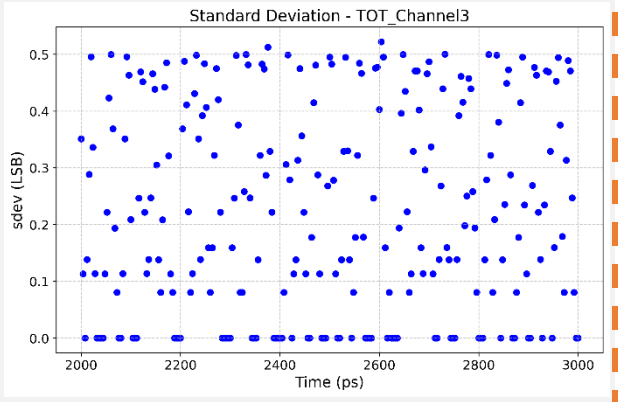
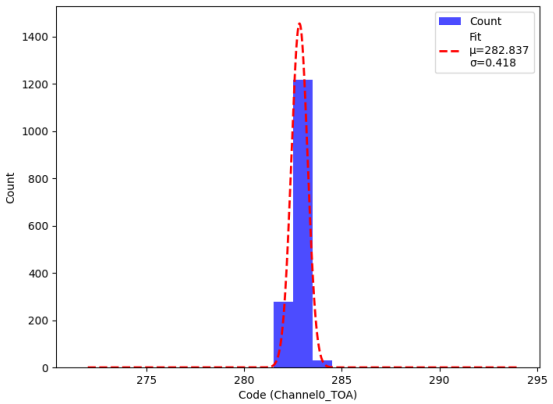


Channel3

LATRIC1- Single Shot Precision

- Precision measurement Details



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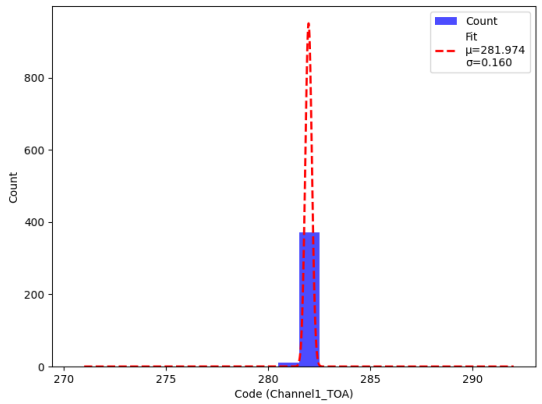
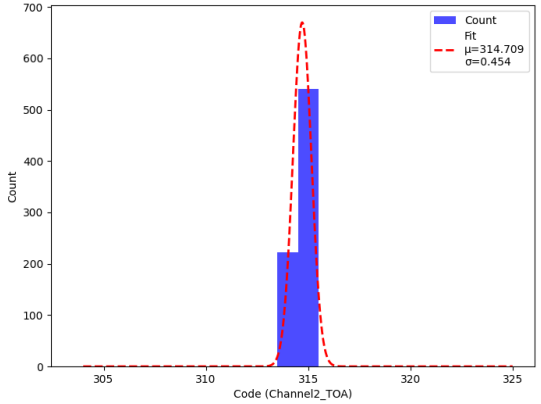


CH1



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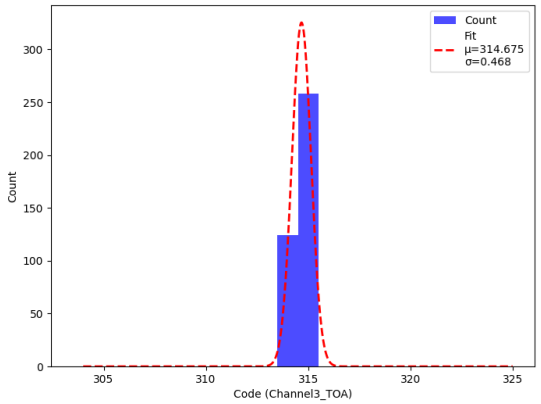
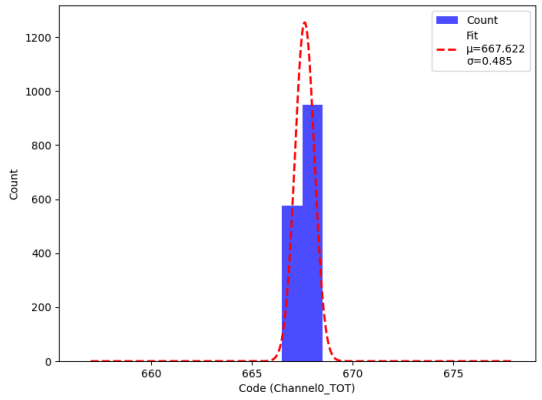
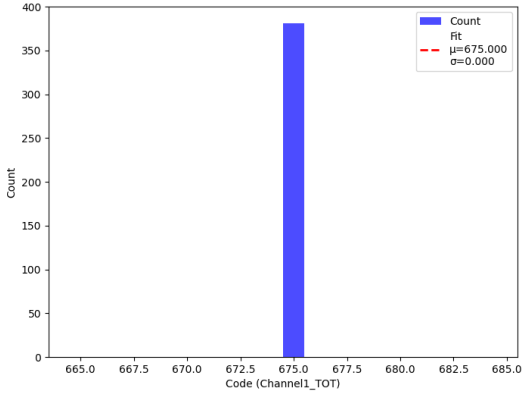


CH3

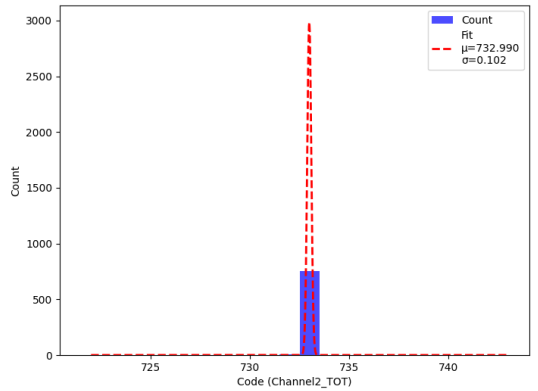
TOA resolution



CH0



CH1



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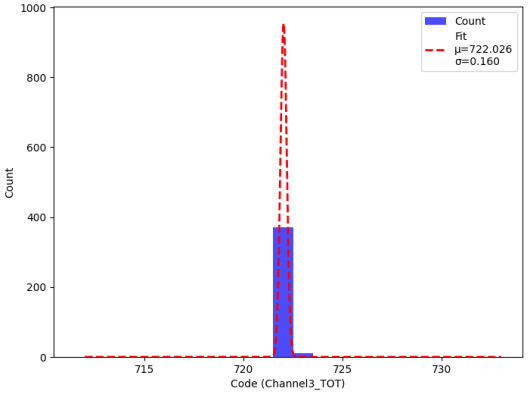
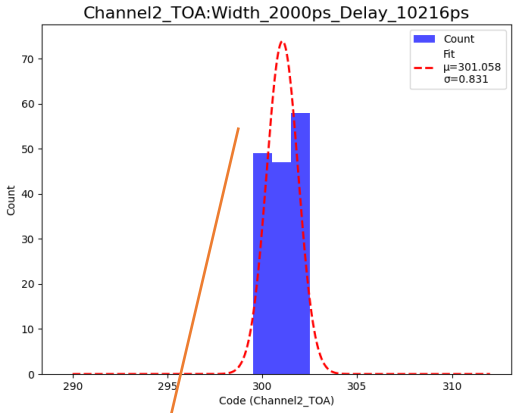


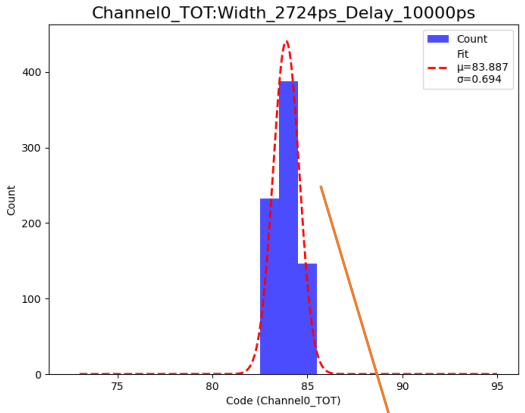
CH3

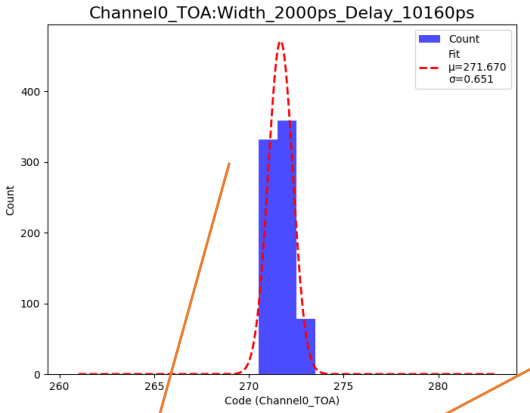
TOT resolution

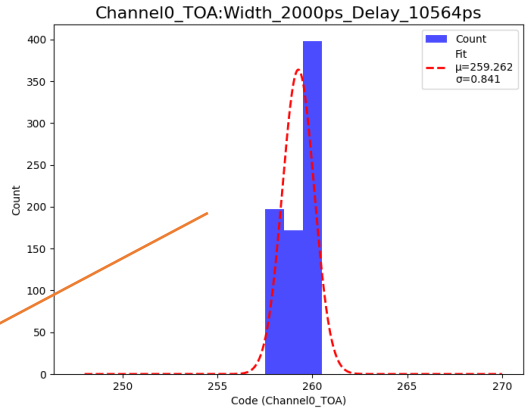
LATRIC1- Single Shot Precision

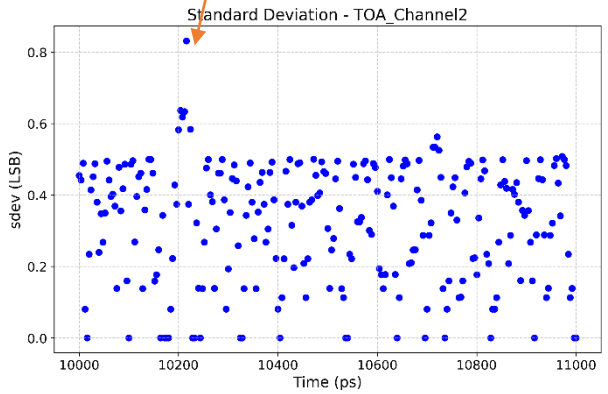
◆ Details for Precision exceptions

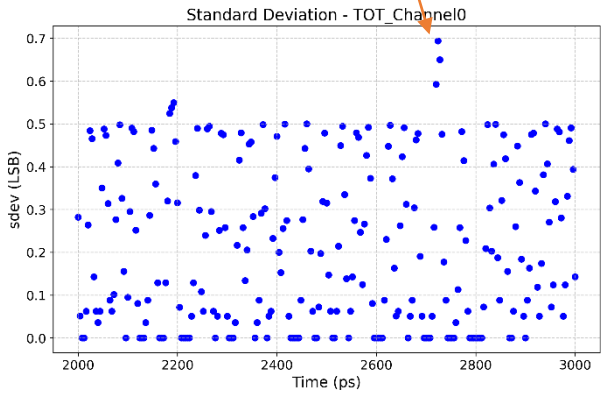


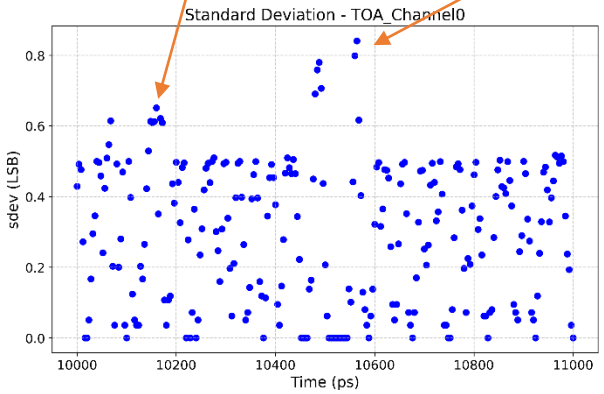






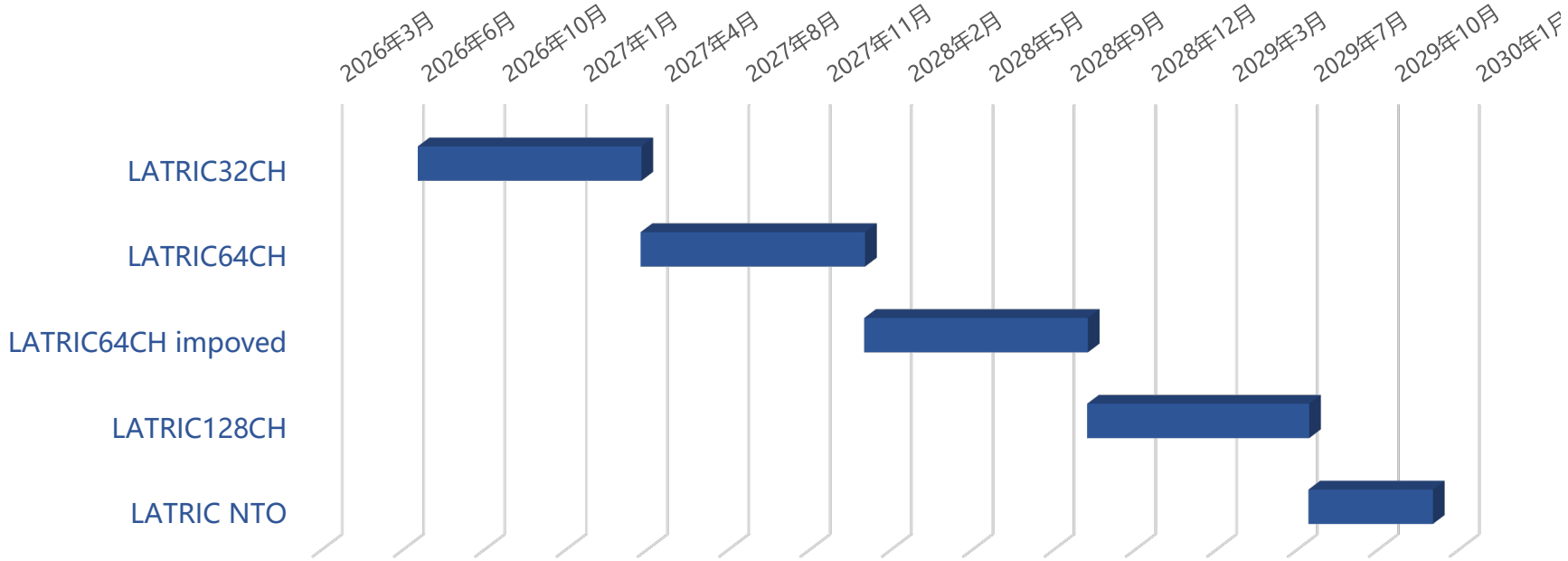






Conclusion

- LATRIC0 time resolution is proved with pixel LGAD by Laser, while performace test by β is ongoing.
- Spatial test system is debugging.
- LATRIC1 time performance is proved preliminarily, need more time.



Thank you!