清華大學 工程物理系
Department of Engineering Physics, Tsinghua University

用于暗物质和中微子实验的低温低本底低噪声高纯锗探测器读出电子学研制

刘灿文，邓智，叶祥柯，罗海波，郝嘉俊，何力

2026-08

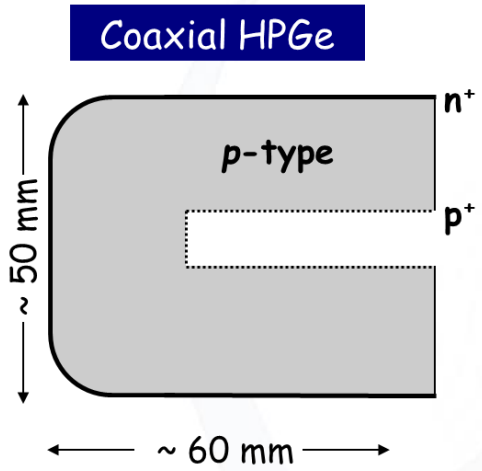
河南-登封

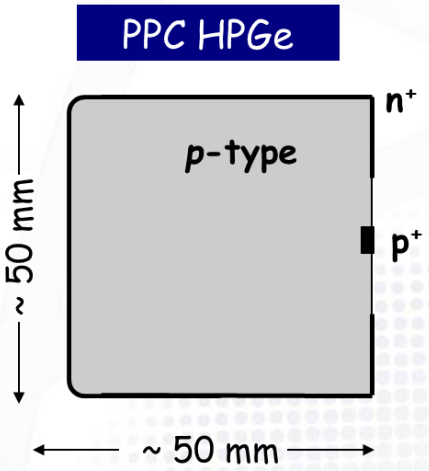
NED2026

CONTENTS

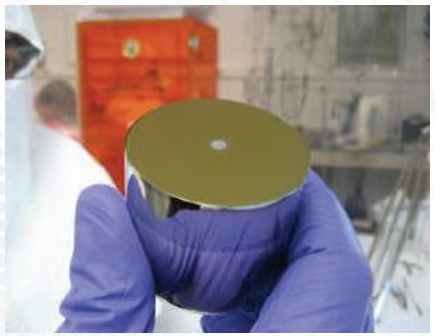
点电极高纯锗探测器用于低本底实验

- PC-HPGe detector
  - 低输入电容 ~ 1 pF
  - 高能量分辨
  - 低本底





P.N. Luke, et. al. TNS 1989



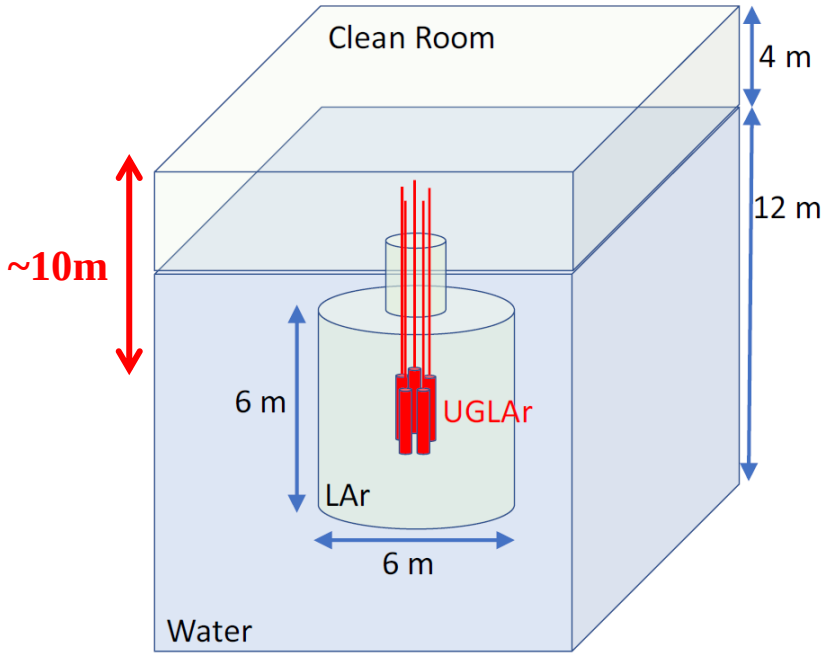
- 用于低本底实验
  - Neutrinoless double-beta decay（0νββ）：GERDA， Majorana
    - GERDA: half-life time of 0νββ 8.0×10^{25} y with the lowest background.
  - Direct Dark Matter Detection：CoGeNT，CDEX
    - CDEX: 160eV energy threshold in 2018，the most sensitive result in 4~5 GeV.

点电极高纯锗探测器用于低本底实验

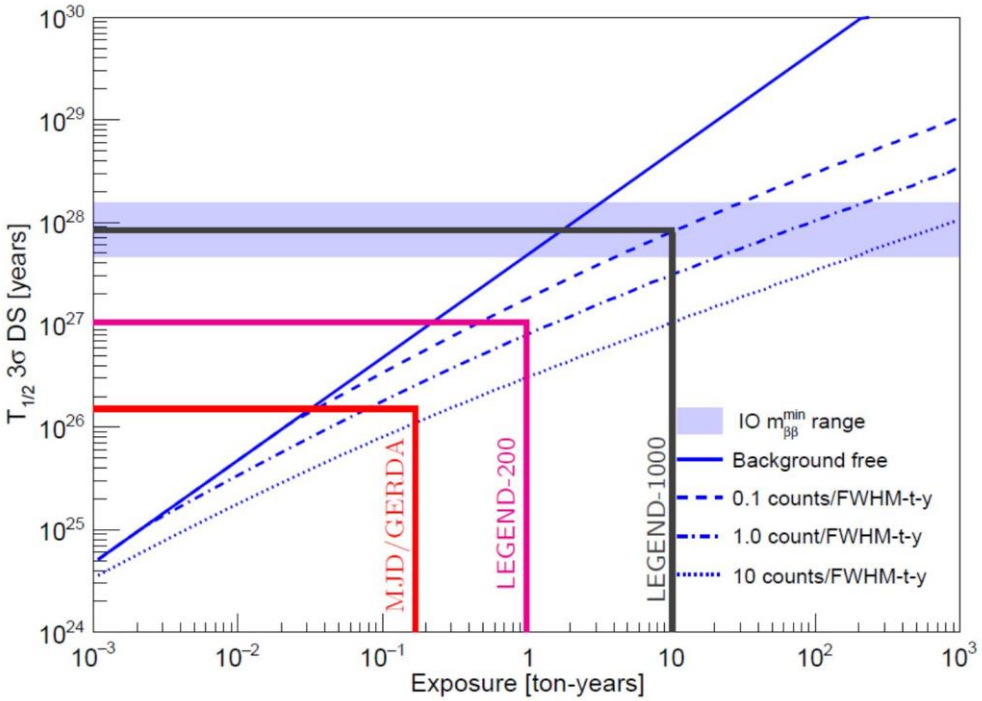
- 使用吨级高纯锗探测器实现更高的灵敏度
- LEGEND-1000
  - Large detector mass
  - Low background
  - Low temperature

50 kg ⟶ 1000 kg

3 c/(FWHM·t·yr) ⟶ 0.1 c/(FWHM·t·yr)



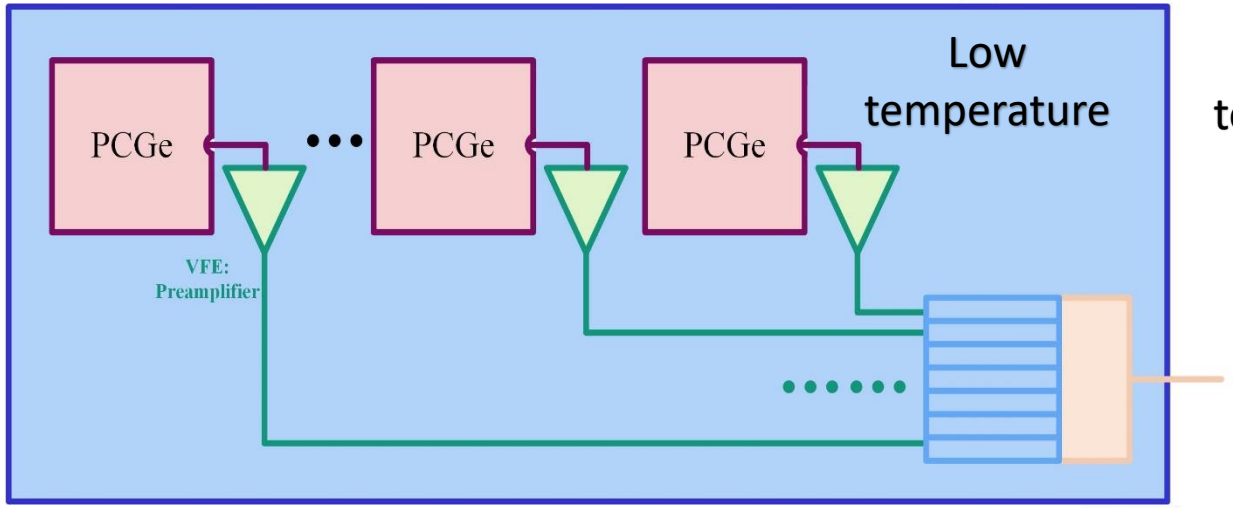
LEGEND-1000

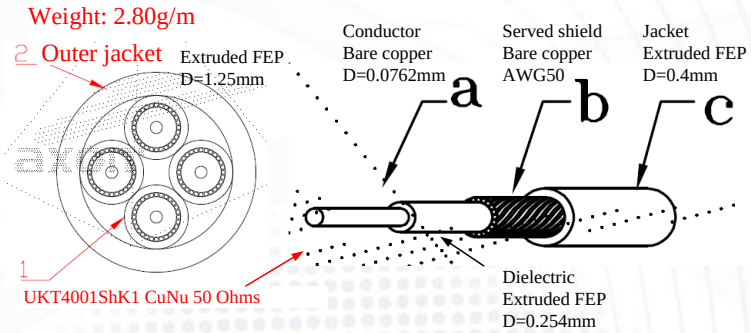


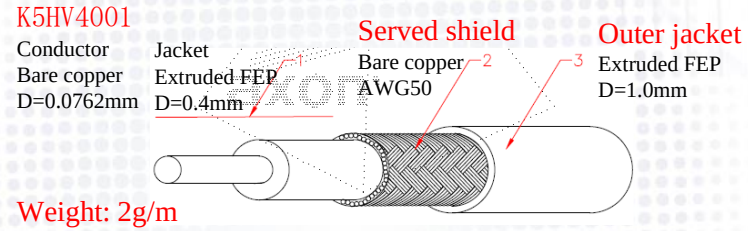
0νββ half-life versus exposure curve LEGEND,TAUP 2017

读出电子学方案

- 低温前端电子学方案——低温、低本底、低噪声







- 优势
  - 更少的同轴连接线/连接器
  - 更好的信号完整性
- 挑战
  - 低温CMOS器件模型
  - 串扰/干扰
  - 低本底、低功耗、低噪声需求

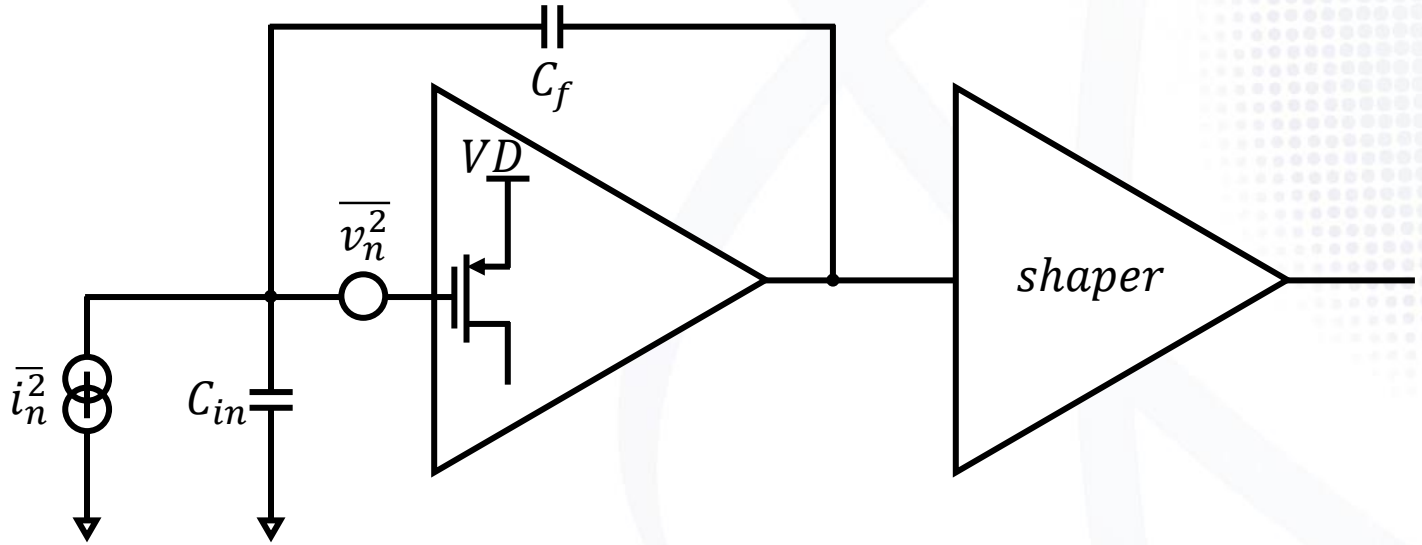
CONTENTS

低噪声前放ASIC芯片——噪声来源

电子学噪声：输入晶体管（Cg，W，L等），探测器（Cin，Sin等）

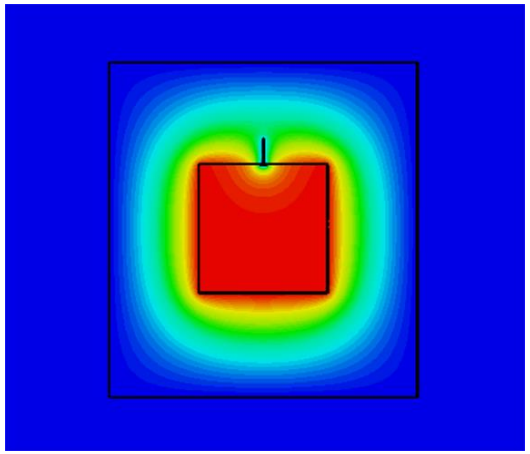
$$ENC^2 = \frac{\int_0^{\infty}[S_{in}|H(j\omega)|^2 + (C_{in}+C_g)^2\omega^2 S_{vn}|H(j\omega)|^2]d\omega}{2\pi h(t)^2_{\max}}$$

$$= (C_{in}+C_g)^2[\frac{1}{\tau_p}\frac{4kT\alpha_w n\gamma}{g_{mw}(J_D,L)W} + (2\pi\tau_p)^{\alpha_f-1}a_f\frac{2\pi K_f}{C_{ox}WL}] + a_p S_{in}\tau_p$$

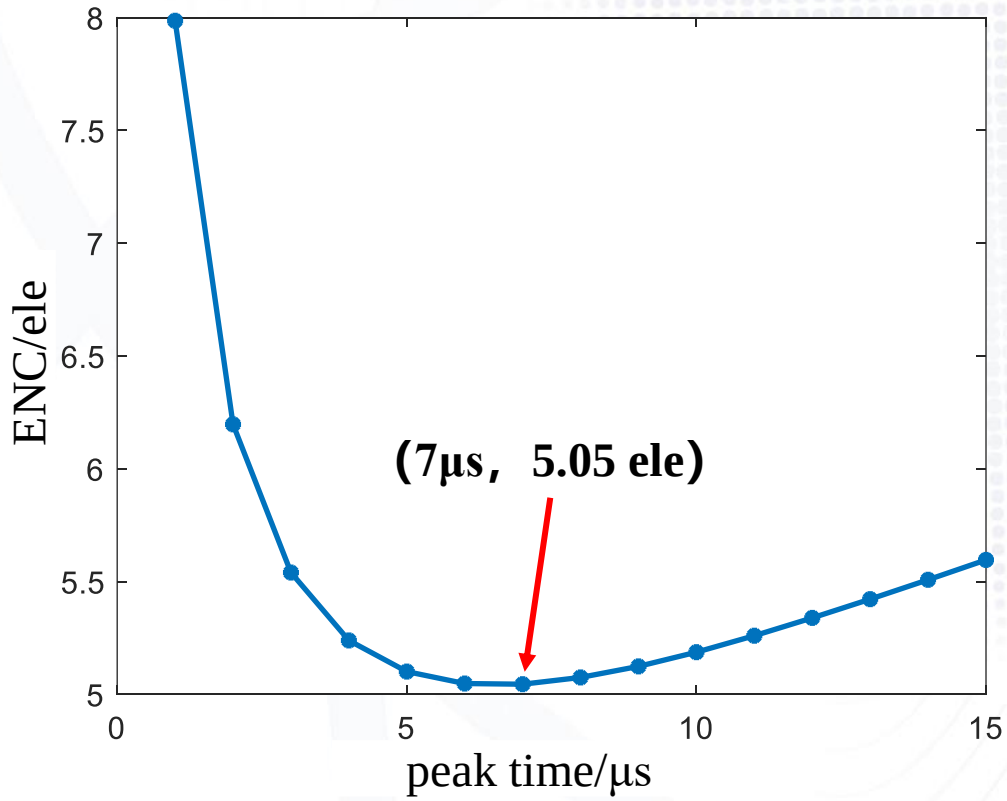


低噪声前放ASIC芯片——探测器参数估算

- HPGe detector
  - Simulation setting
    - 0.5 kg
    - 50 mm diameter and height
    - 3 mm electrode diameter
  - $C_d \approx 1.1$ pF，$C_{in} \approx 2$ pF

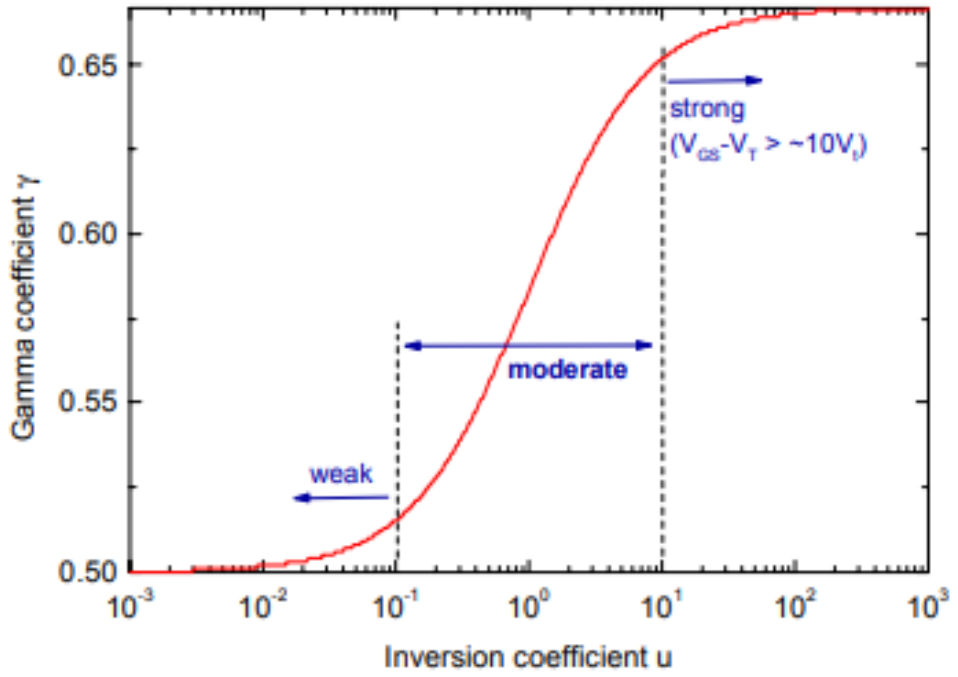


- Optimal peak time
  - Detector leakage current~1 pA
  - Optimal peak time ~10 μs



低噪声前放ASIC芯片——输入晶体管优化

- Input stage transistors
  - Gate capacitance $C_g = C_{gs} + C_{gd} + C_{gb}$
  - C_{gs} is related to the working status of MOSFET

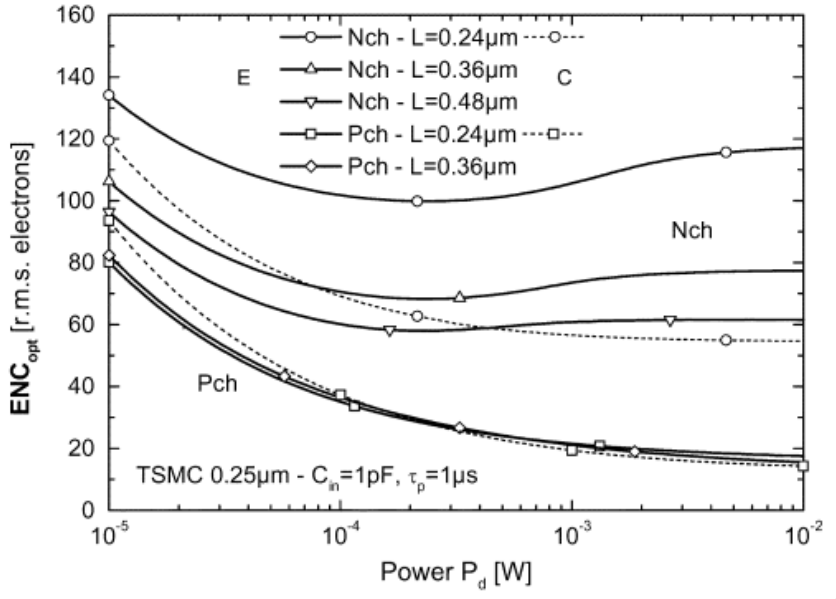


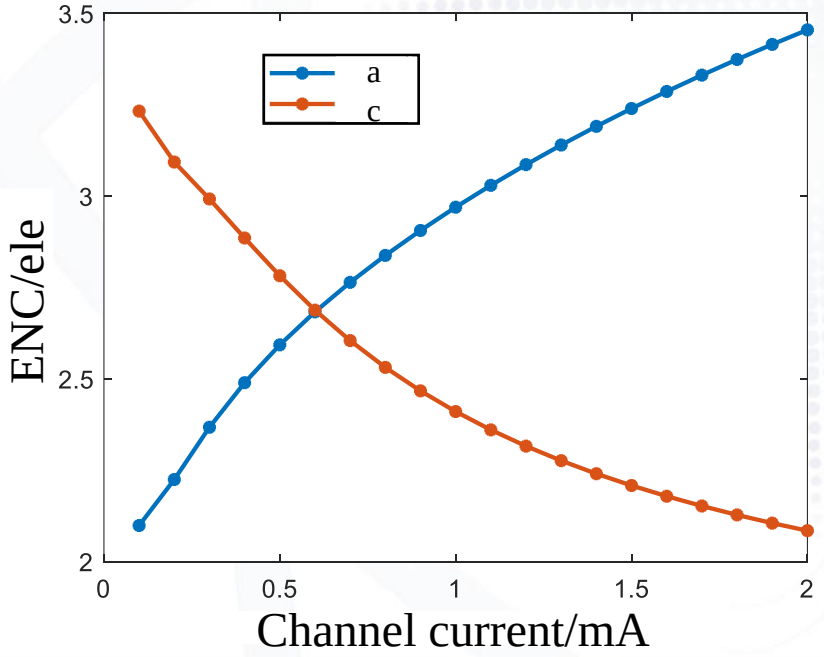
$$C_g = WLC_{ox}/(\frac{3}{2} + \frac{f(u)}{u}) + 2C_{ov}W + C_{gbw}W$$

De Geronimo G, O'Connor P. MOSFET Optimization in Deep Submicron Technology for Charge Amplifiers. IEEE TNS,2005,52(6):3223.

低噪声前放ASIC芯片——输入晶体管优化

- Input stage transistors
  - The greater the channel current I_d, the lower the PMOS transistor 1/f noise;
  - The greater the channel current I_d the greater the PMOS transistor thermal noise;
  - The channel current design value is 1 mA (transition region)





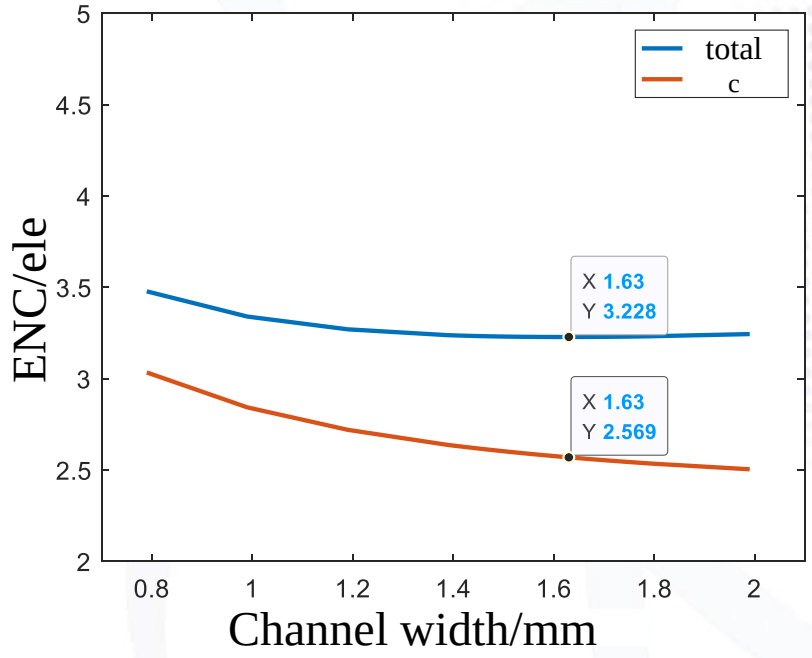
低噪声前放ASIC芯片——输入晶体管优化

- 尺寸&沟道电流

$$W_{opt} \approx \frac{C_{in}}{0.47C_{ox}L + 2C_{ov} + C_{gbw}} \approx 1.5\ \text{mm}$$

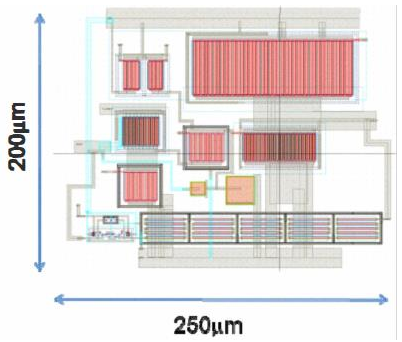
$$ENC_c \approx 2.57\ e^-$$

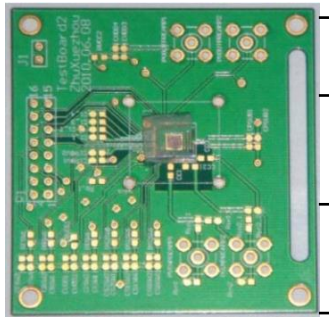
- 板图寄生参数优化
  - 输入节点寄生电容



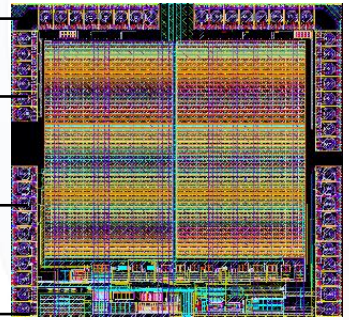
低噪声前放ASIC芯片——研制历史

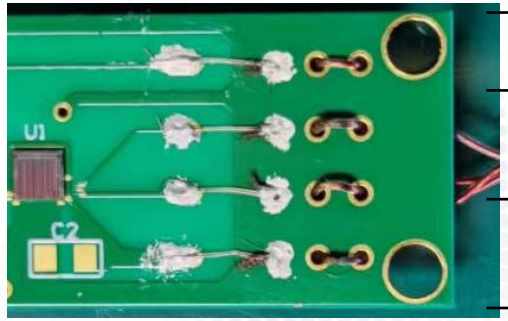
- L3GeRO (Low temperature, Low noise and Low background Germanium detector ReadOut)





process	GF 350nm
ENC	6.5 e⁻ @ 213K 12μs
energy resolution	3.9 keV @ 662 keV





process	XFAB 350nm
ENC	8.9 e⁻ @ 77K 12μs
energy resolution	600 eV @ 122 keV

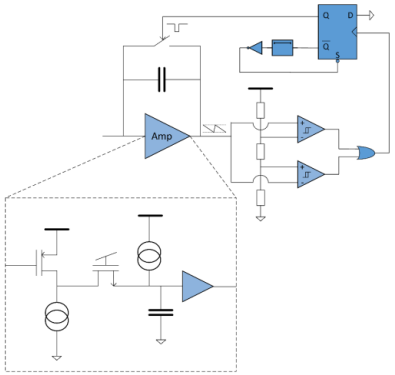
L3GeRO-2011

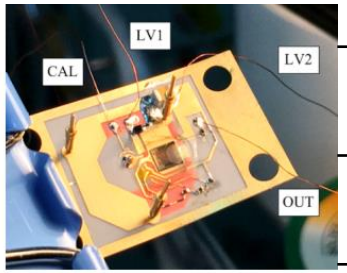
L3GeRO-2021

2011 — 2018 — 2021 — 2023 — 2024-2025

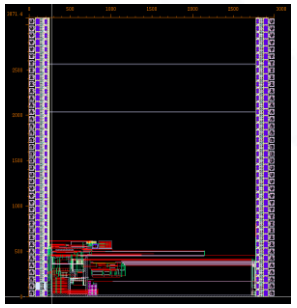
L3GeRO-2018

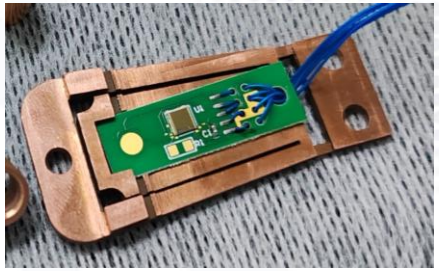
L3GeRO-2023





process	GF 350nm
ENC	9.7 e⁻ @ 77K 12μs
energy resolution	640 eV @ 122 keV

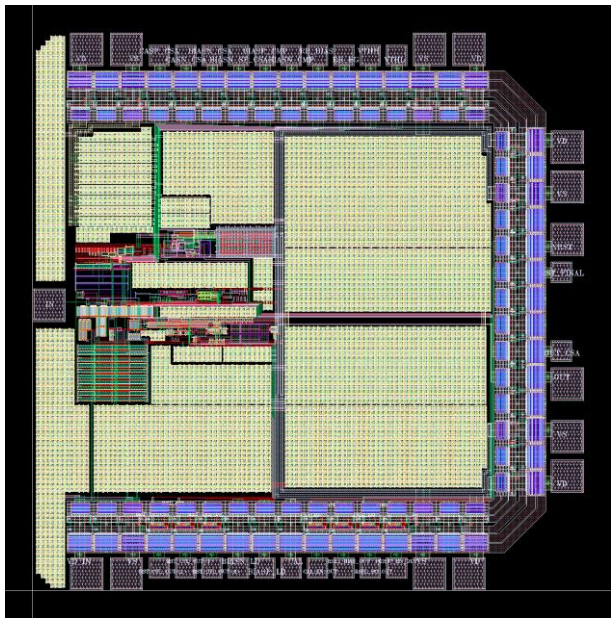


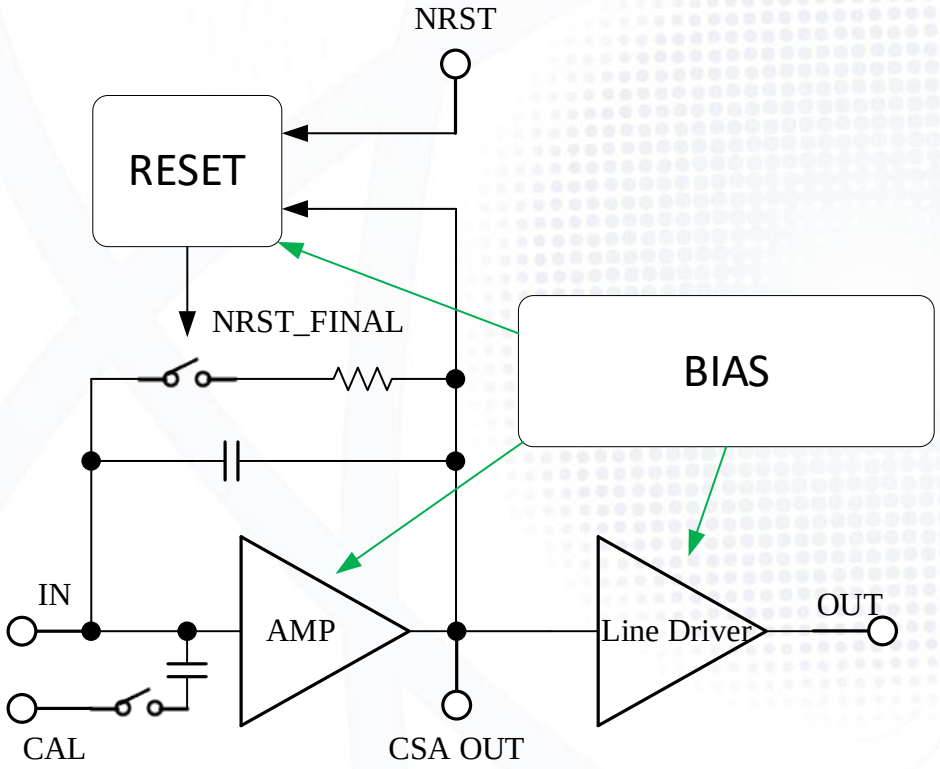


process	GF 180nm
ENC	3.0 e⁻ @ 77K 12μs
energy resolution	-

低噪声前放ASIC芯片——芯片结构

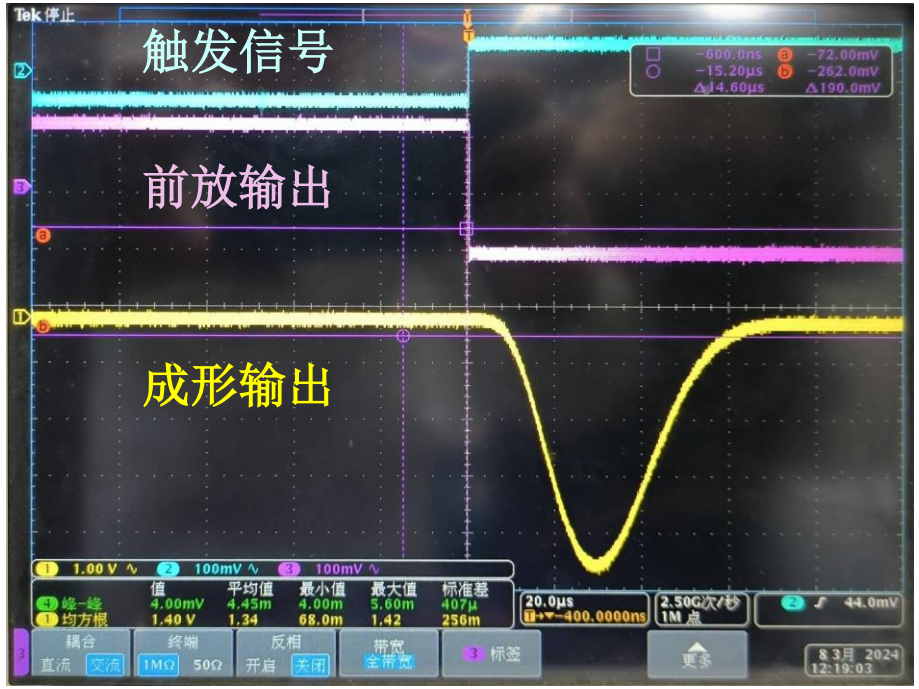
- L3GeRO
  - 无需外部器件
  - 脉冲复位/内部集成复位逻辑
  - CSA输出经过驱动级后输出
  - 仿真ENC：<3 e @ 2pF, 77K

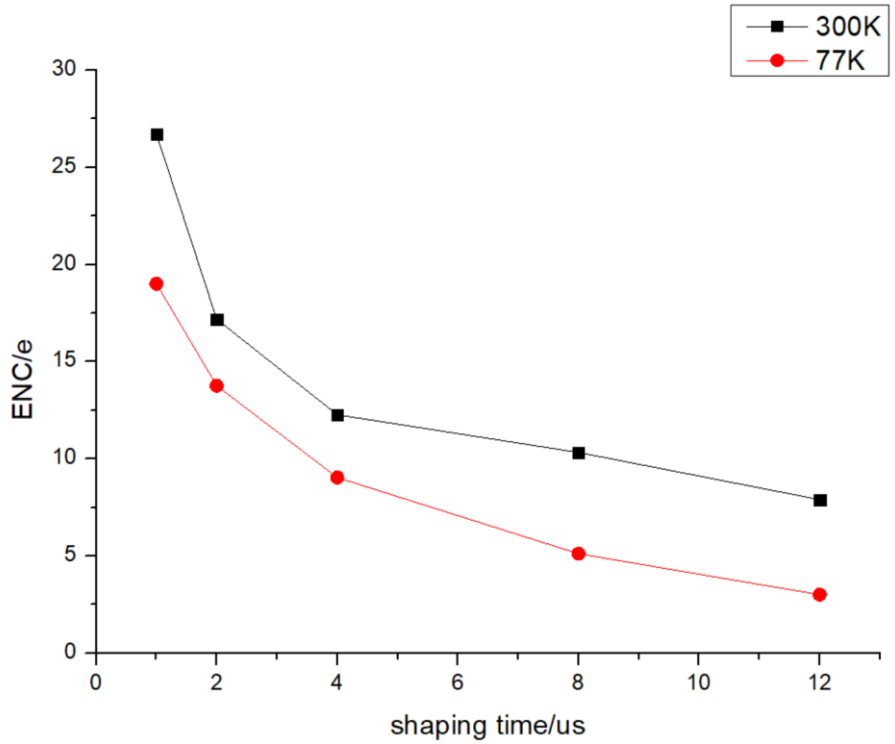




低噪声前放ASIC芯片——芯片性能测试

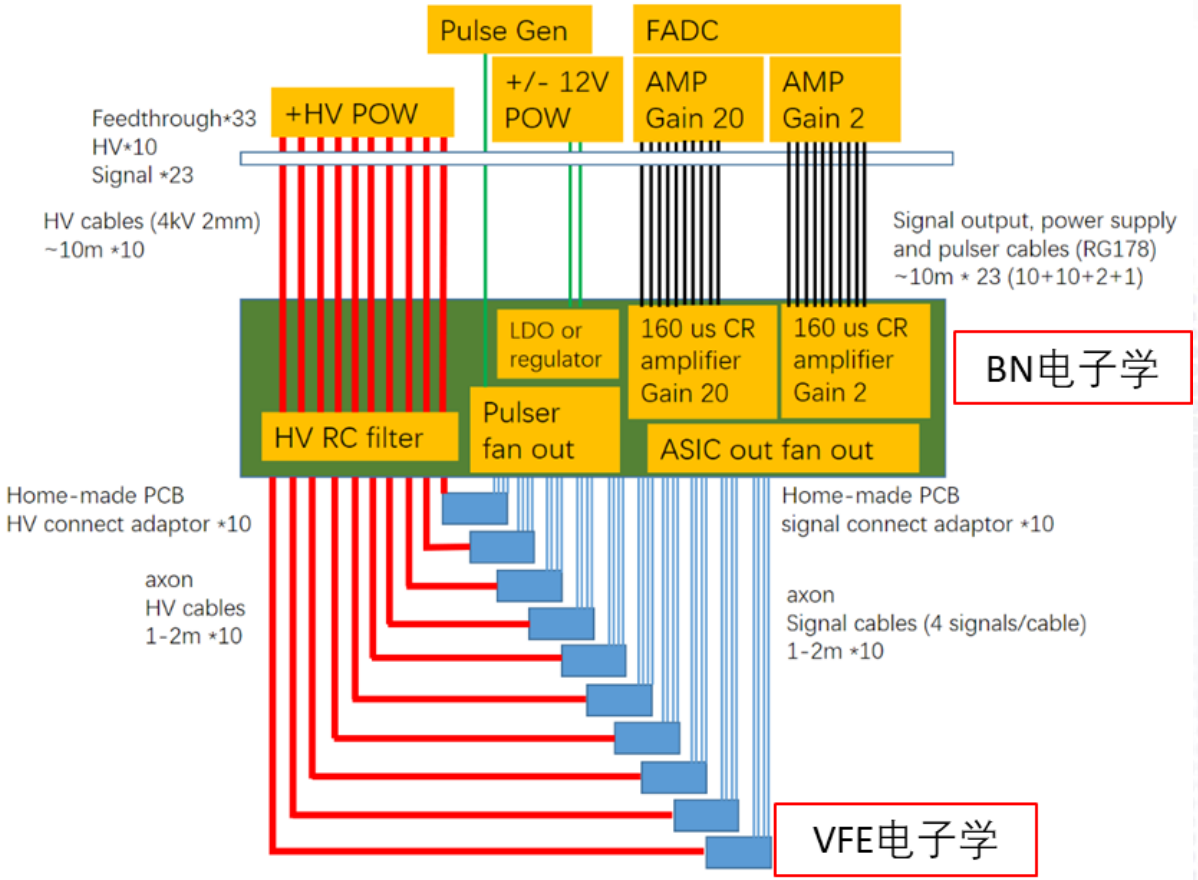
- 瞬态波形
- 零电容噪声——3e@77K 12us



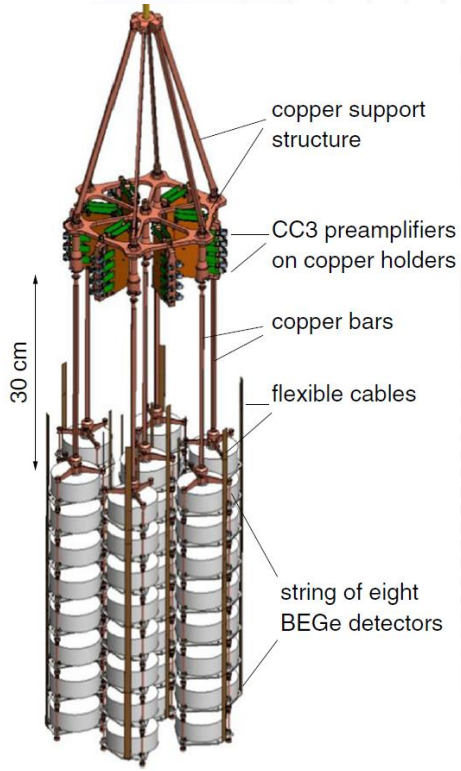


读出电子学研制——方案设计

- 低温读出电子学方案
  - 近前端电路板（VFE）
    - 前放：CMOS ASIC
  - 信号综合处理板（BN）
    - 电源滤波
    - 双增益+信号驱动
    - 校准信号扇出
    - HV滤波

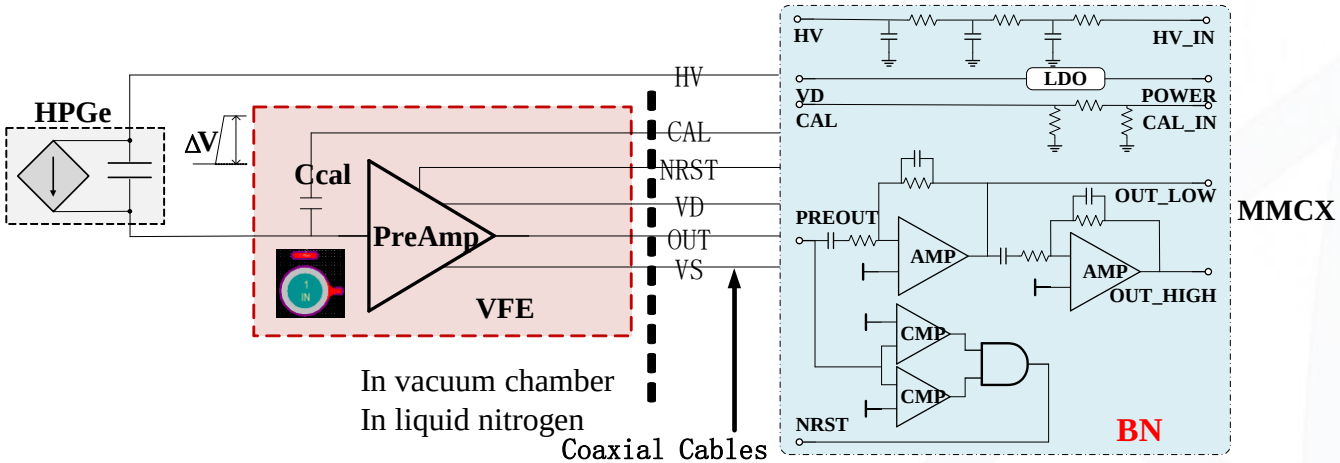


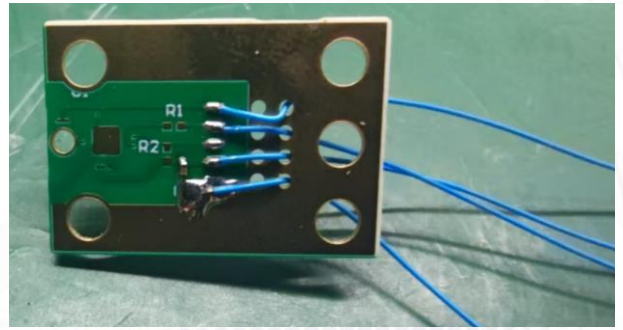
探测器阵列



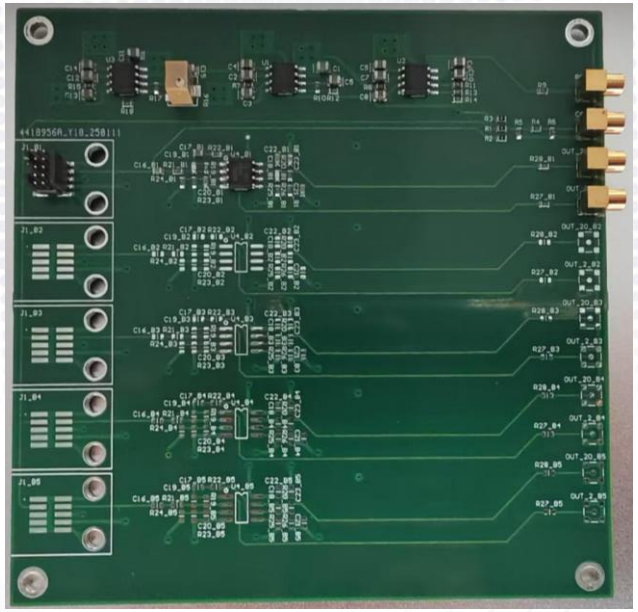
读出电子学研制——框图与实物

- L3GeRO in CDEX
  - HPGe探测器 + 近前端电路板VFE + 信号综合处理板BN
  - 同轴电缆链接VFE 和 BN——信号线/高压线

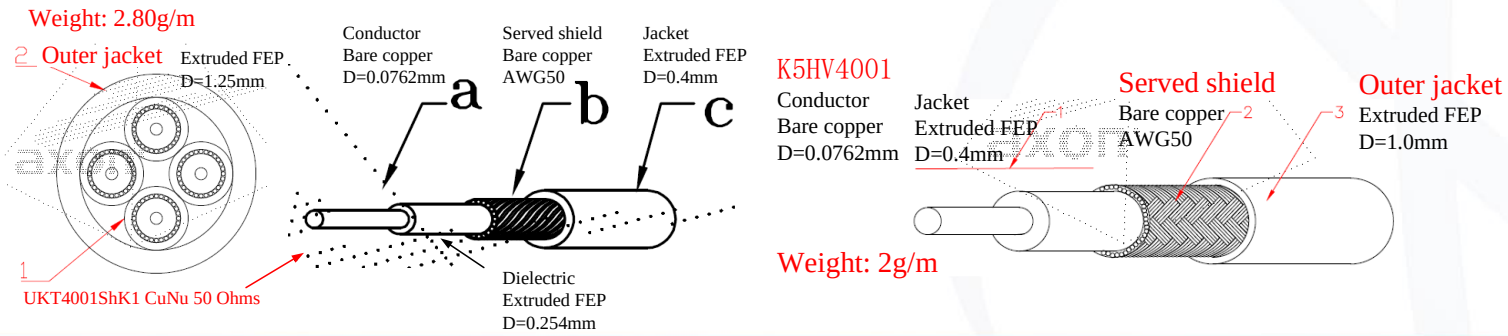




近前端电路板VFE

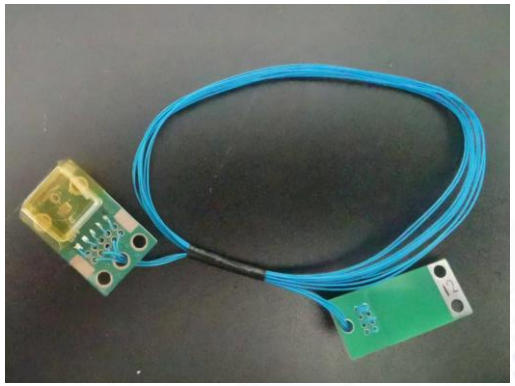


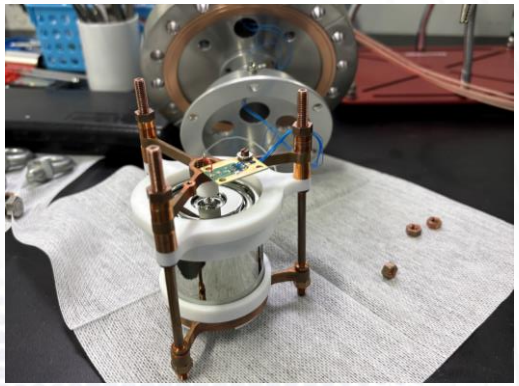
信号综合处理板BN

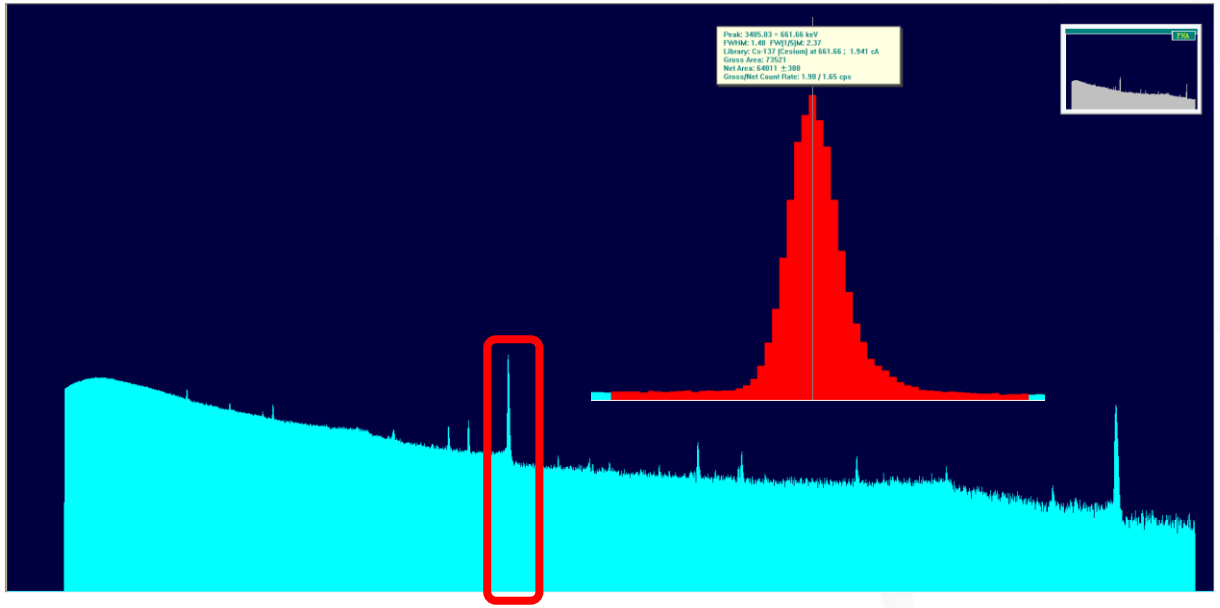


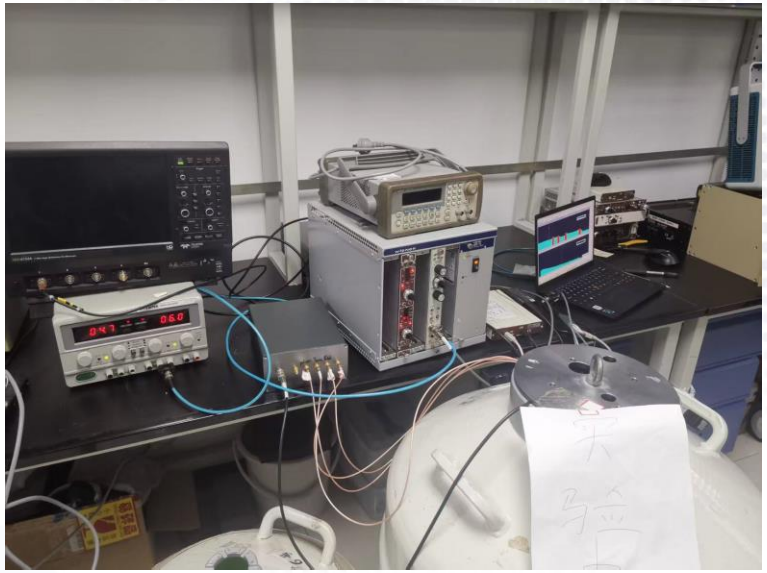
读出电子学研制——连探测器测试

- L3GeRO in CDEX
  - HPGe和VFE 置于真空罐中
  - 真空罐浸泡到液氮中
  - FWHM=1.5 keV @ 662 keV(Cs-137)



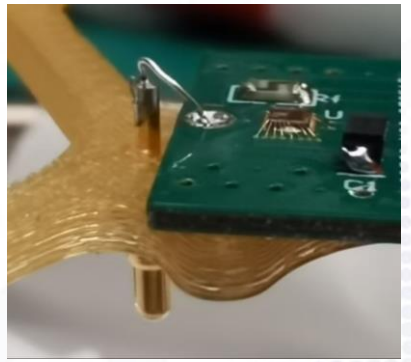


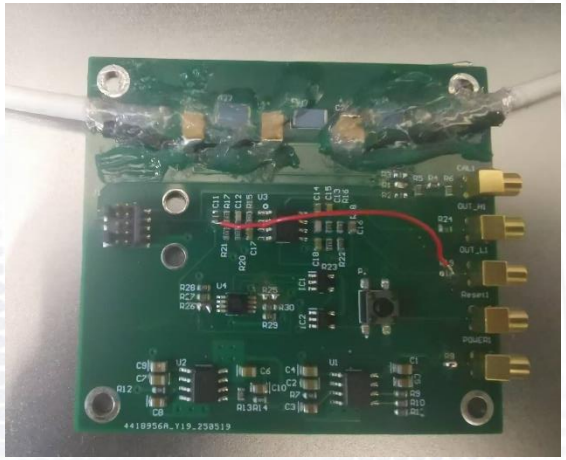


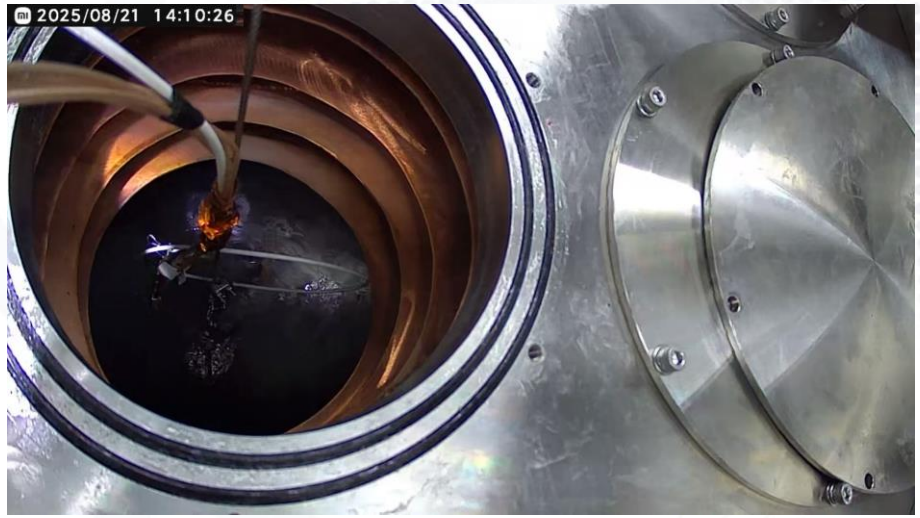


读出电子学研制——裸泡测试

- L3GeRO in CDEX
  - HPGe + VFE + BN
  - HPGe和VFE直接浸泡到液氮中
  - 实验正在进行







CONTENTS

总结与展望

- 总结
  - 低噪声前放ASIC芯片设计方法——输入管参数优化、输入节点寄生参数优化
  - 用于CDEX实验的低温低本底低噪声高纯锗探测器读出前放ASIC芯片
  - 基于L3GeRO的读出电子学及相关测试情况

- 展望
  - ASIC噪声性能及低温工作稳定性的进一步优化
  - 低本底实验推进