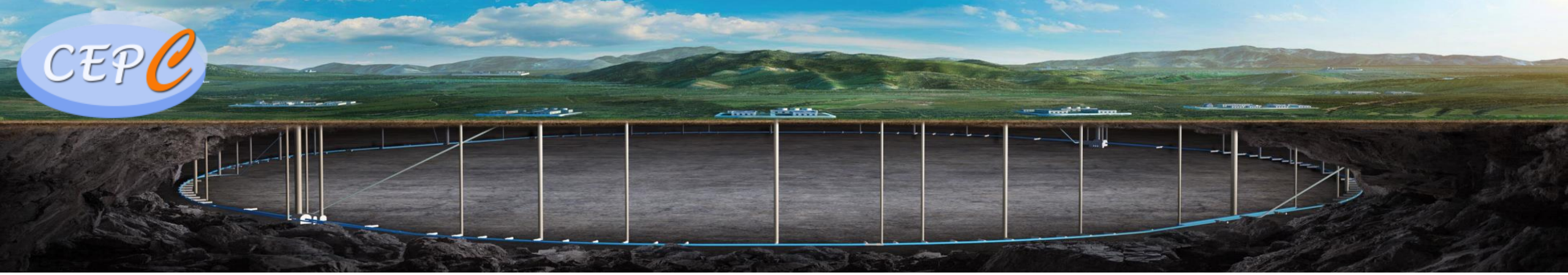


CEPC顶点探测器研发进展

张 颖

代表CEPC顶点探测器研发团队

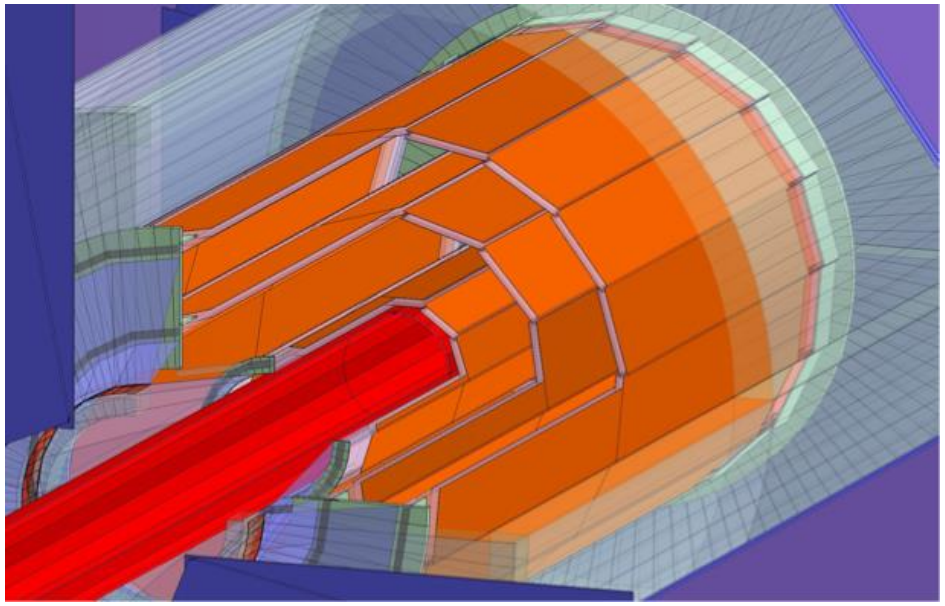
中国科学院高能物理研究所
Institute of High Energy Physics
Chinese Academy of Sciences

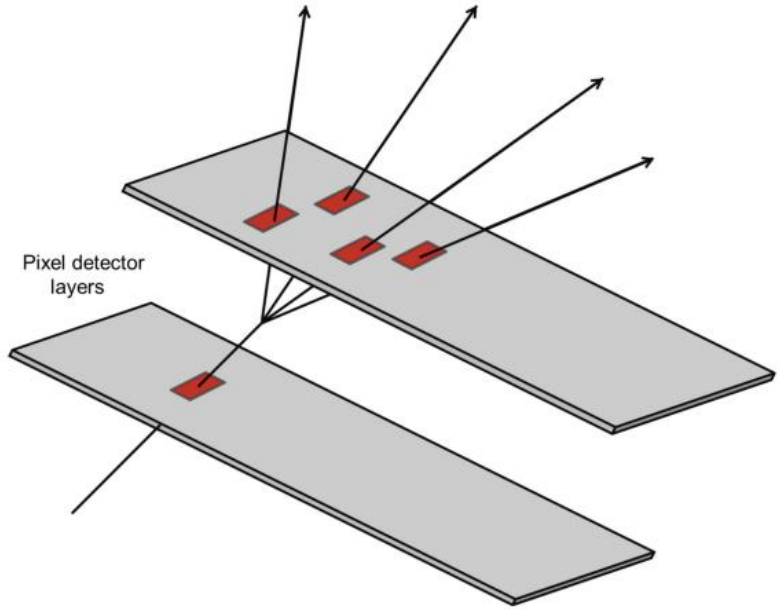
报告内容

- 顶点探测器设计目标
- 技术方案
- 研发状态
- 未来规划

Introduction: vertex detector

- Vertex detector optimized for first 10 years of operation (ZH, low lumi-Z)
- Motivation:
  - Aim to optimize impact parameter resolution and vertexing capability
  - Key detector for H → bb/cc and H → light quark or gluons physics
  - The observation H → cc or H → gg is important goal for CEPC





Vertex Requirement

- Inner most layer (b-layer) need to be positioned as close to beam pipe as possible
  - Challenges: Radius (11.1 mm) is smaller compared with ALICE ITS3 (18 mm)

Table 4.2: Vertex Detector Design Parameters

Parameter	Design
Spatial Resolution	~ 5 μm
Detector material budget	$\sim 0.8\% X_0$
First layer radius	11.1 mm
Power Consumption	< 40 mW/cm^2 (air cooling requirement)
Time stamp precision	100 ns
Fluence	$\sim 2 \times 10^{14}$ Neq/cm^2 (for first 10 years)
Operation Temperature	~ 5 °C to 30 °C
Readout Electronics	Fast, low-noise, low-power
Mechanical Support	Ultralight structures
Angular Coverage	$\lvert \cos\theta \rvert < 0.99$

TDR. arXiv:2510.05260

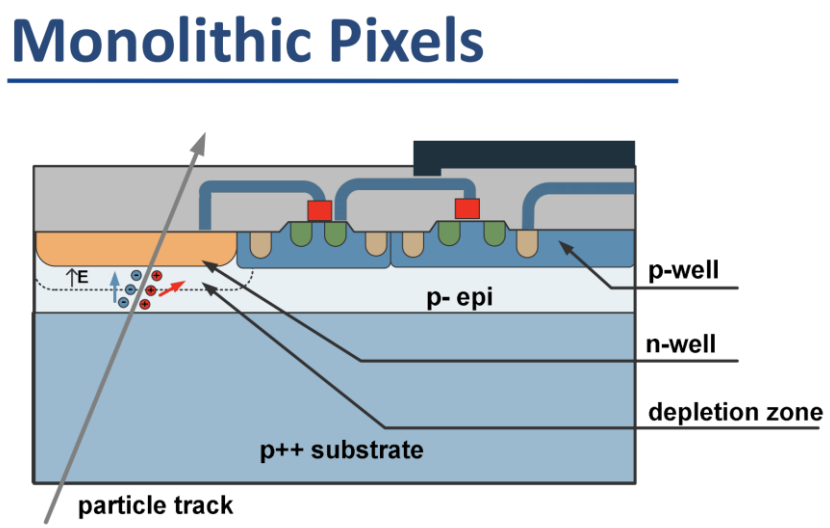
Technology for CEPC Reference TDR

- Vertex detector technology selection

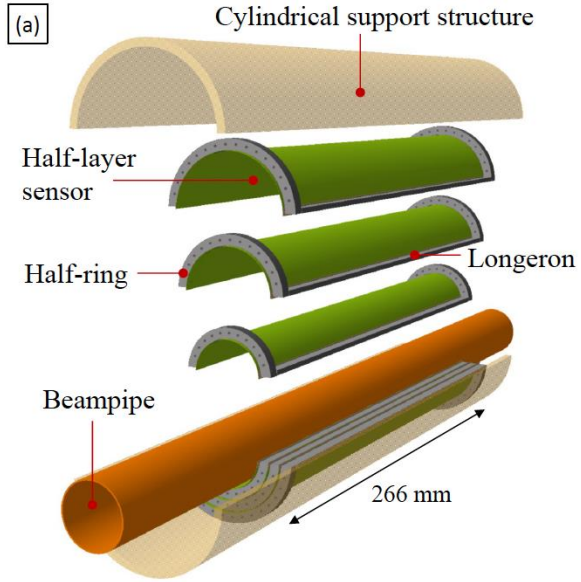
TDR. arXiv:2510.05260

  - Baseline: based on curved CMOS MAPS (Inspired by ALICE ITS3 design [1])
    - Advantage: 2~3 times smaller material budget compared to alternative (ladder)
  - Alternative: Ladder design based on CMOS MAPS

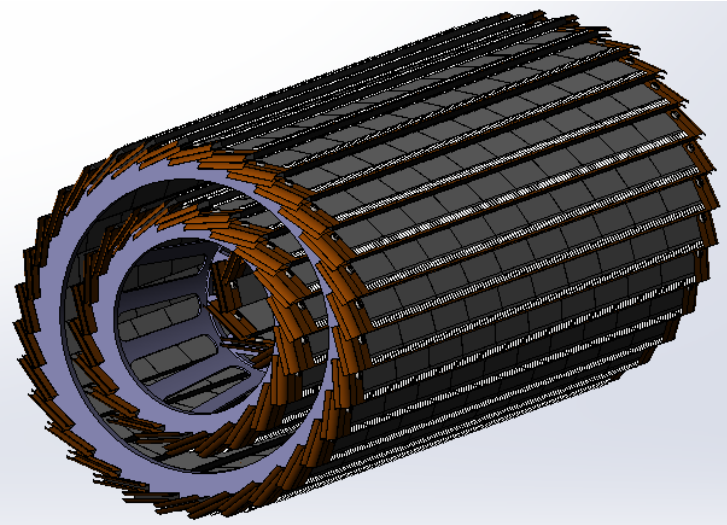
Monolithic active Pixel Sensor (MAPS)



Baseline: curved MAPS

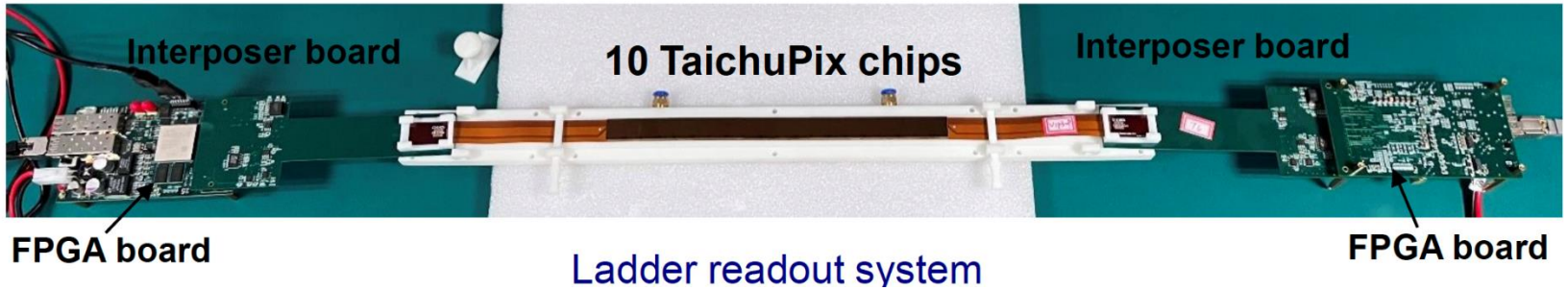


Alternative: ladder based MAPS



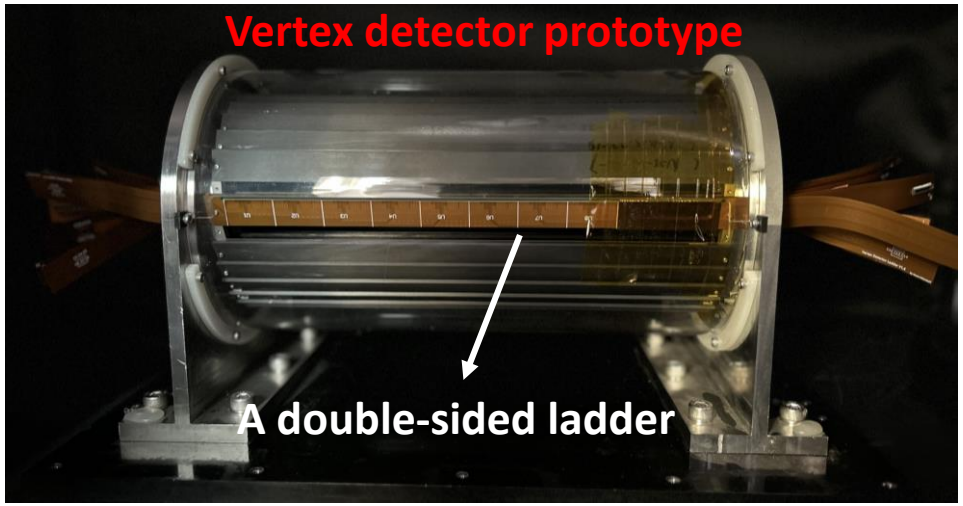
[1] ALICE ITS3 TDR: https://cds.cern.ch/record/2890181

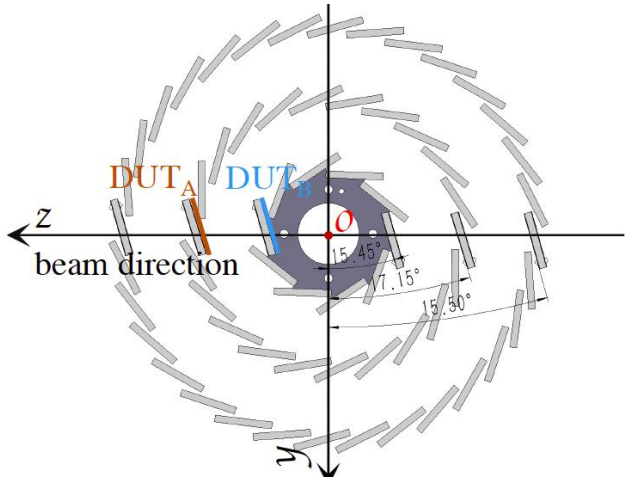
R&D effort: vertex detector prototype

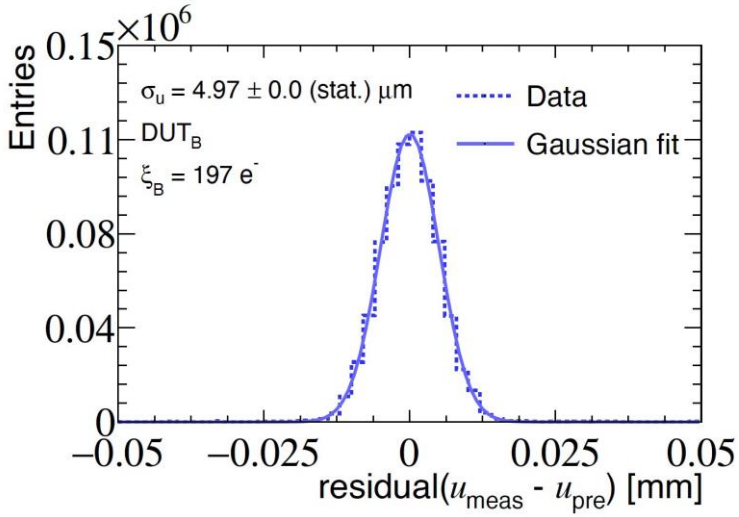


Ladder readout system

TaichuPix-based prototype detector tested at DESY in April 2023
Spatial resolution ~ **4.9 µm**
@ Detection efficiency > 99%



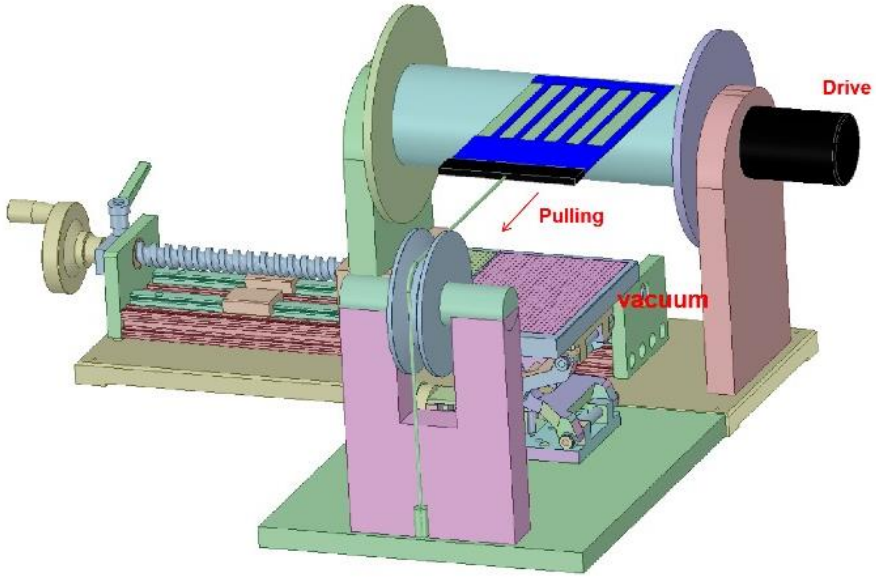


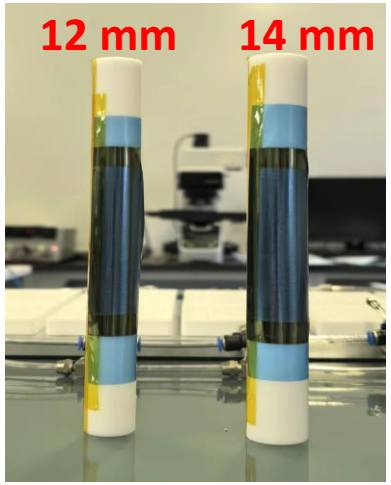


	Status	CEPC Final goal
Detector integration	Detector prototype with ladder design	Detector with bent silicon design

R&D efforts curved MAPS

- CEPC b-layer radius (11 mm) smaller compared with ALICE ITS3 (radius = 18 mm)
- Feasibility : Mechanical prototype with dummy wafer can curved to a radius of 12 mm
  - The dummy wafer has been thinned to 40 µm





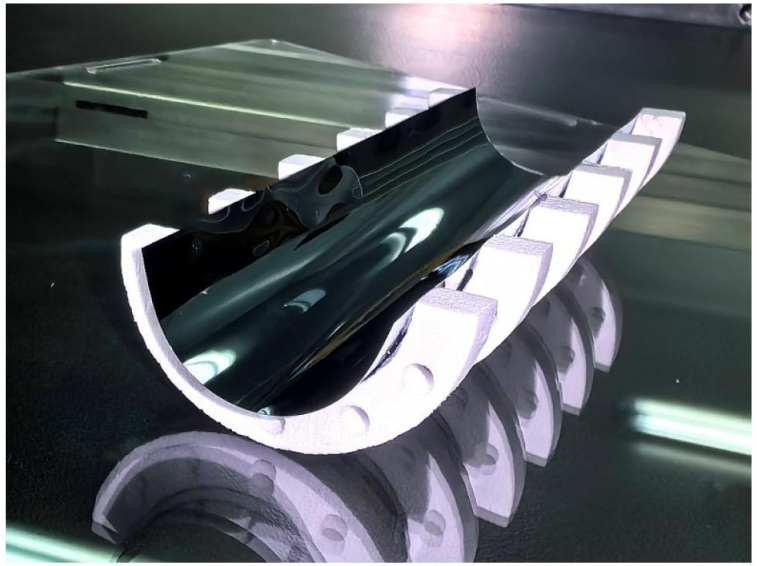
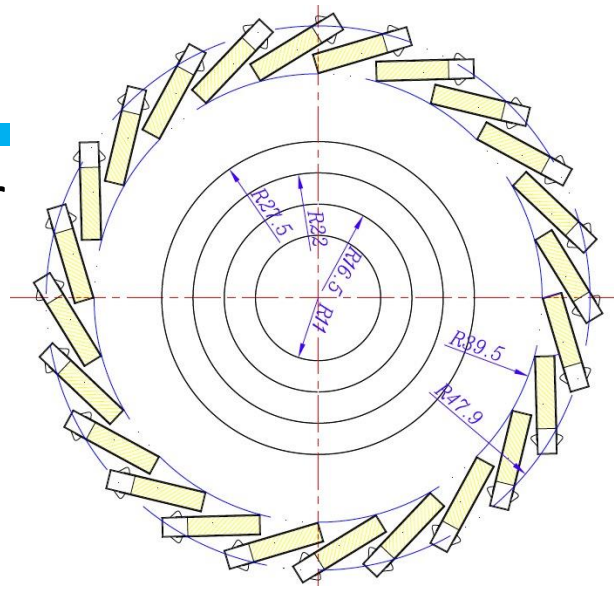


Figure 4.26: 12 mm bending radius.

	Status	CEPC Final goal
Bent silicon with radius	Bent Dummy wafer radius ~12 mm	Bent final wafer with radius ~11 mm

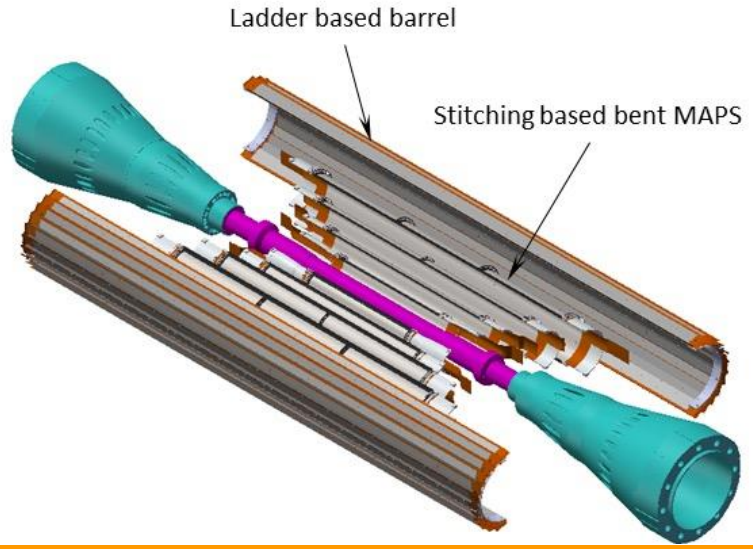
Baseline layout in Ref-TDR

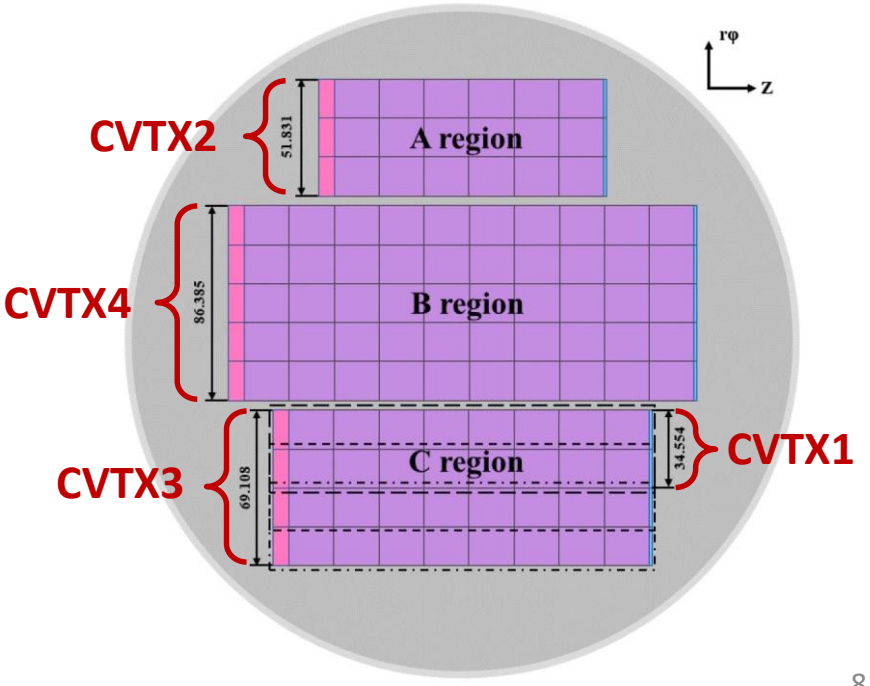


- Baseline: 4 single layer of bent MAPS + 1 double-sided ladder layer
  - Alternative option: 3 double layer ladders
- Inner layer: using single bent MAPS (~0.15 m^2)
  - Low material budget 0.06% X_0 per layer
  - Different rotation angle in each layer to reduce dead area
- Outer layer: using double layer ladder (~0.3% X_0/layer)

CVTX/ PVTX X	radius mm	length mm
CVTX 1	11.1	161.4
CVTX 2	16.6	242.2
CVTX 3	22.1	323.0
CVTX 4	27.6	403.8
PVTX 5	39.5	682.0
PVTX 6	47.9	682.0

Long barrel layout (no endcap disk)





Data rate estimation of vertex detector

- Various sources of beam-induced backgrounds are simulated
  - Data rate is dominated by pair production
  - Data rate at low-lumi Z pole is about ~Gbps per chip for triggerless readout

Background rate for Higgs and low-lumi Z runs

Layer	Ave. Hit Rate (MHz/cm^2)	Max. Hit Rate (MHz/cm^2)	Ave. Data Rate (Mbps/cm^2)	Max. Data Rate (Mbps/cm^2)
Higgs mode: Bunch Spacing: 277 ns, 63% Gap				
1	6.2	12	760	1500
2	0.84	1.6	87	160
3	0.17	0.36	19	38
4	0.067	0.16	8.4	19
5	0.017	0.037	2.1	4.2
6	0.013	0.026	1.6	3.7
Low-luminosity Z mode: Bunch Spacing: 69 ns, 17% Gap				
1	15	39	2700	8100
2	1.7	2.6	240	400
3	0.72	1.2	110	240
4	0.43	0.94	70	210
5	0.10	0.19	14	31
6	0.078	0.15	11	23

Electronics

- Inner layers (L1-L4): stitching and RDL metal layers on wafer to transfer signal and power
  - Flexible Printed Circuit (FPC) connecting stitched sensors and Front-end Electronics Board (FEE)
  - FEE is installed in the service area outside of fast-LumiCal
- Outer layers (L5-L6): ladder on FPCs (also used in alternative design)
  - Signal, clock, control, power, ground will be handled by control board through FPCs

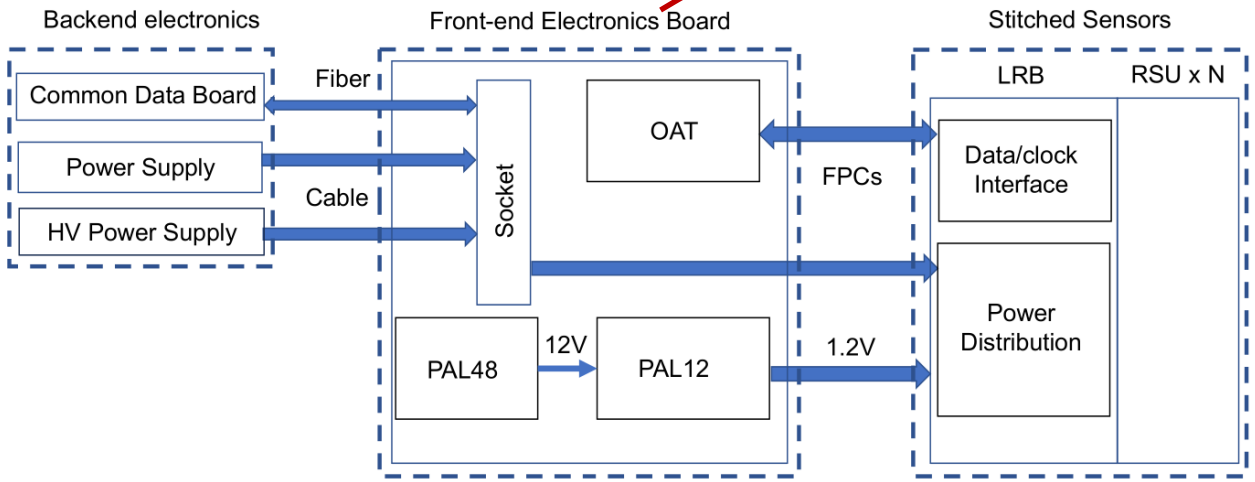
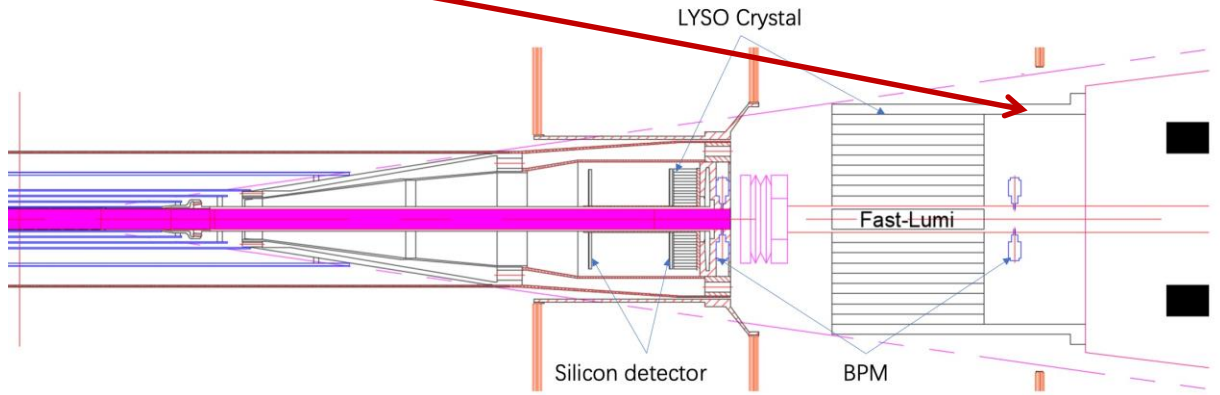


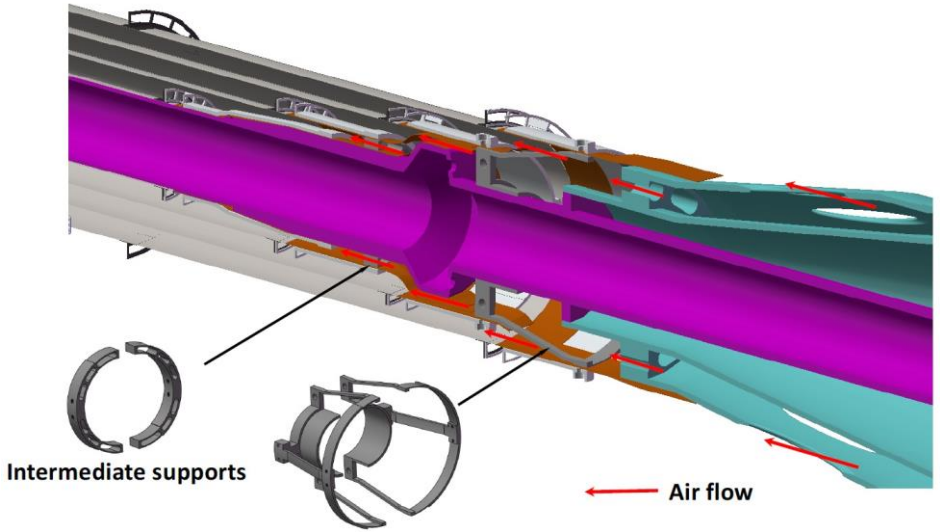
Diagram of the VTX readout electronics



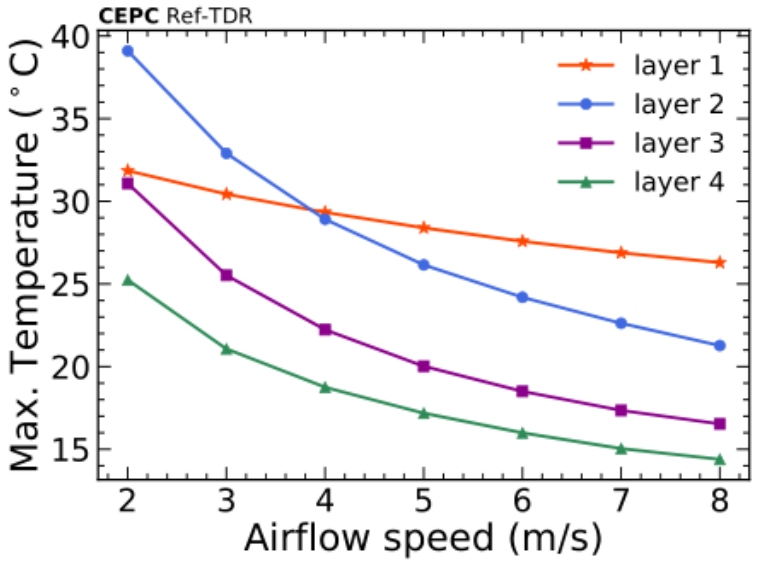
Location of the VTX service area

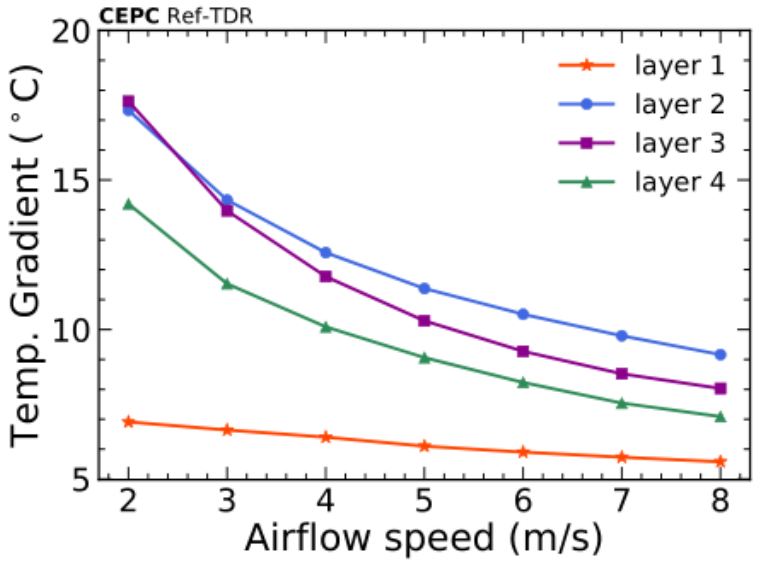
Mechanics and cooling

- For the sensitive area of stitched sensor, power consumption estimated to ~40 mW/cm^2
- Air cooling feasibility study
  - Effective airflow cross section of 12.6 cm^2
  - Baseline layout can be cooled down below 30 ℃ with 7 m/s air speed for stitching layers



Installation of the half layers and intermediate support

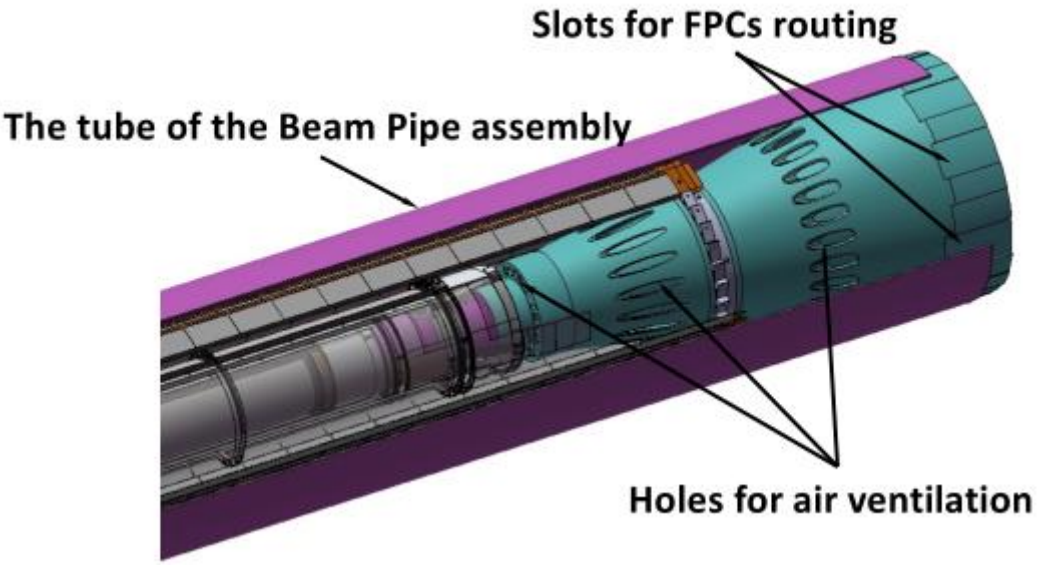




Thermal simulation results for the curved layers

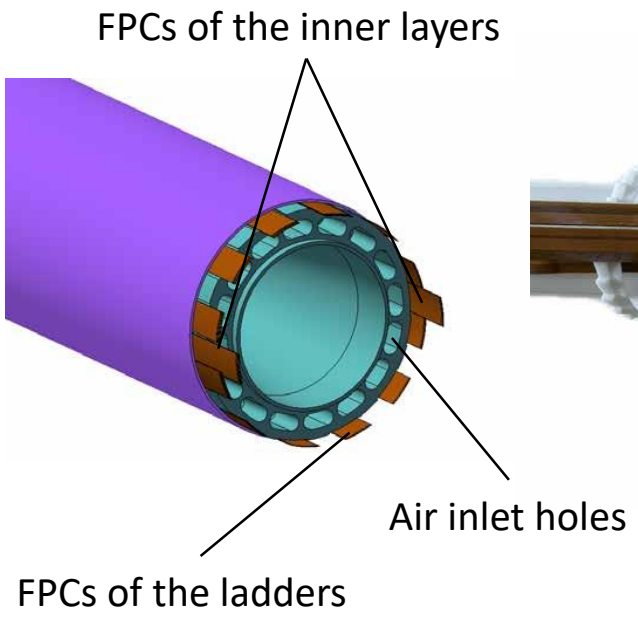
Vertex technologies: cables and services

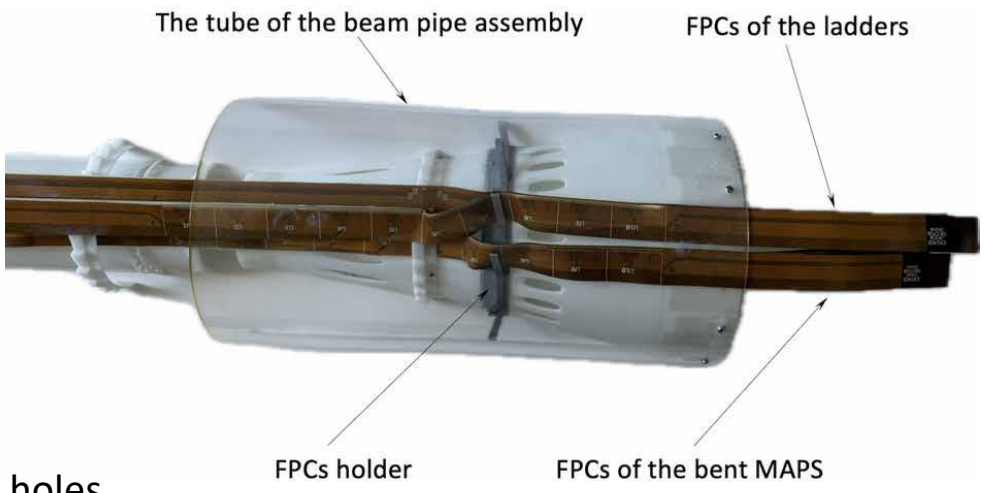
- A hollow conical structure integrated into the beam pipe assembly to serves as air distributor.
- A half-dummy 3D printed mechanical mockup was constructed
  - Validated there is enough space for cable routing and air cooling channel
  - The effective area for air cooling is 12.6 cm^2 (stitching layers)+ 28 cm^2 (between L4/L5)



Cross-sectional view of the full assembly

Dummy mockup of the VTX structure

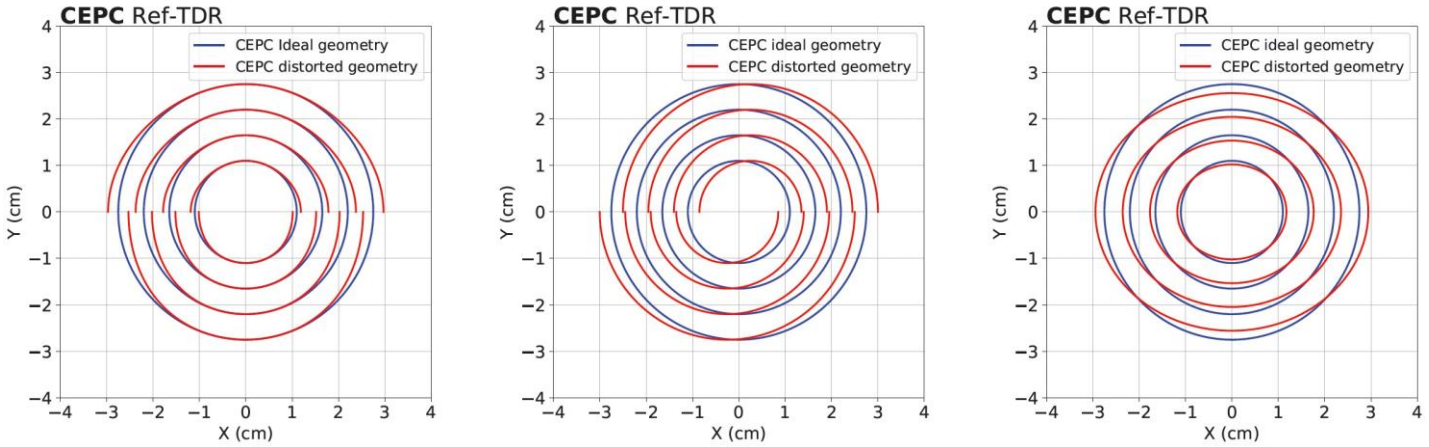




Alignment in stitching layer

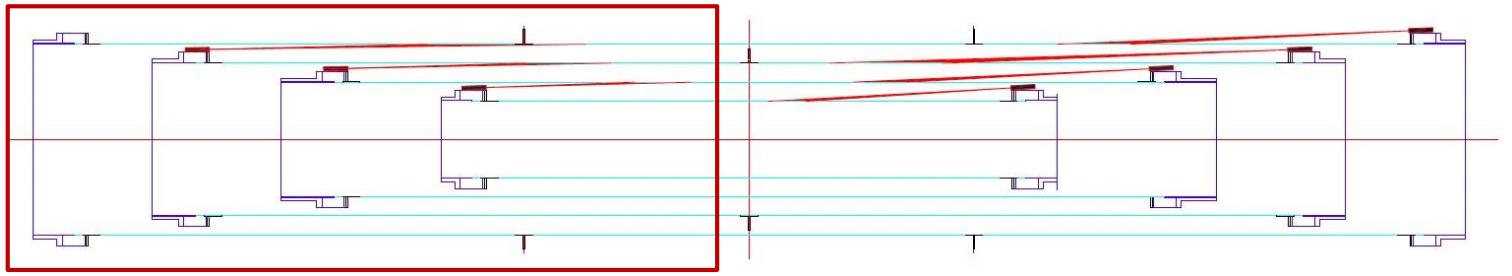
- Deformation modes simulated by FEA

Hit positions with three deformed geometries

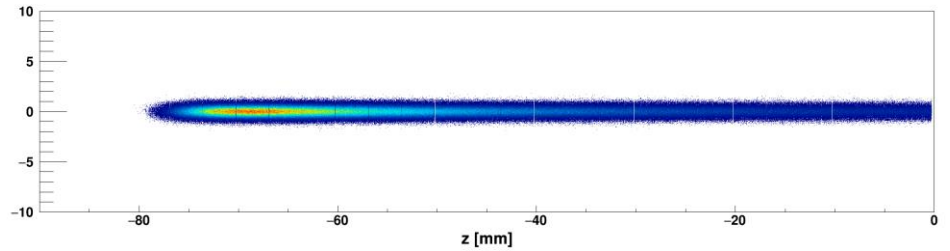


- Real time deformation monitoring by a infrared laser alignment system
  - laser sources are placed at both sides of the inner three layers and right side of the Layer 4

Back-side illuminations

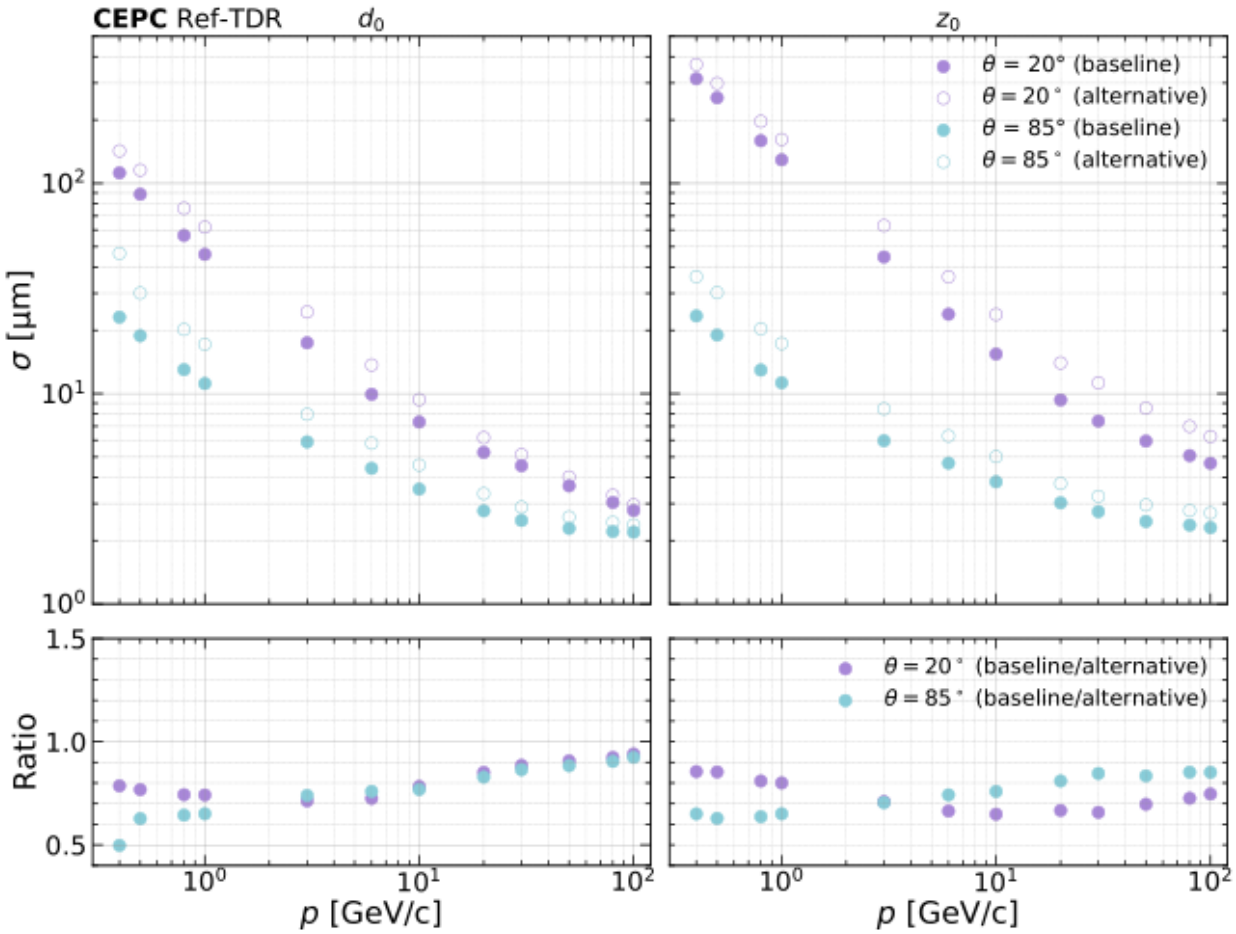


Laser beam spot on the Layer2 from (13 mm, 0, -85 mm)

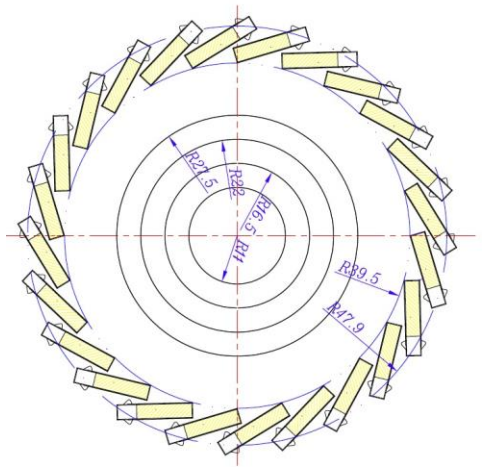


Performance: impact parameter resolution

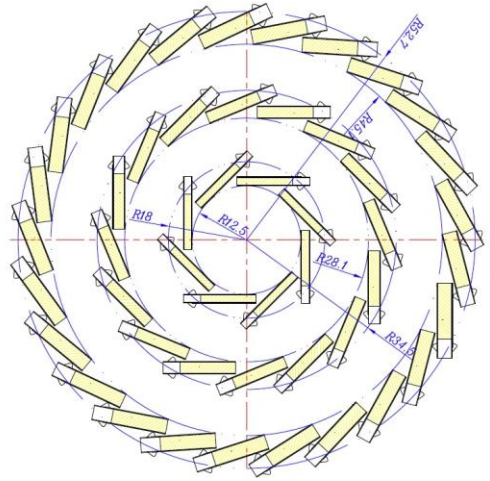
- Baseline has better resolution than alternative (ladder) (10-40%) in 0.4 GeV to 100 GeV



Baseline scheme
4 stitched curved sensor +
1 double layer ladders



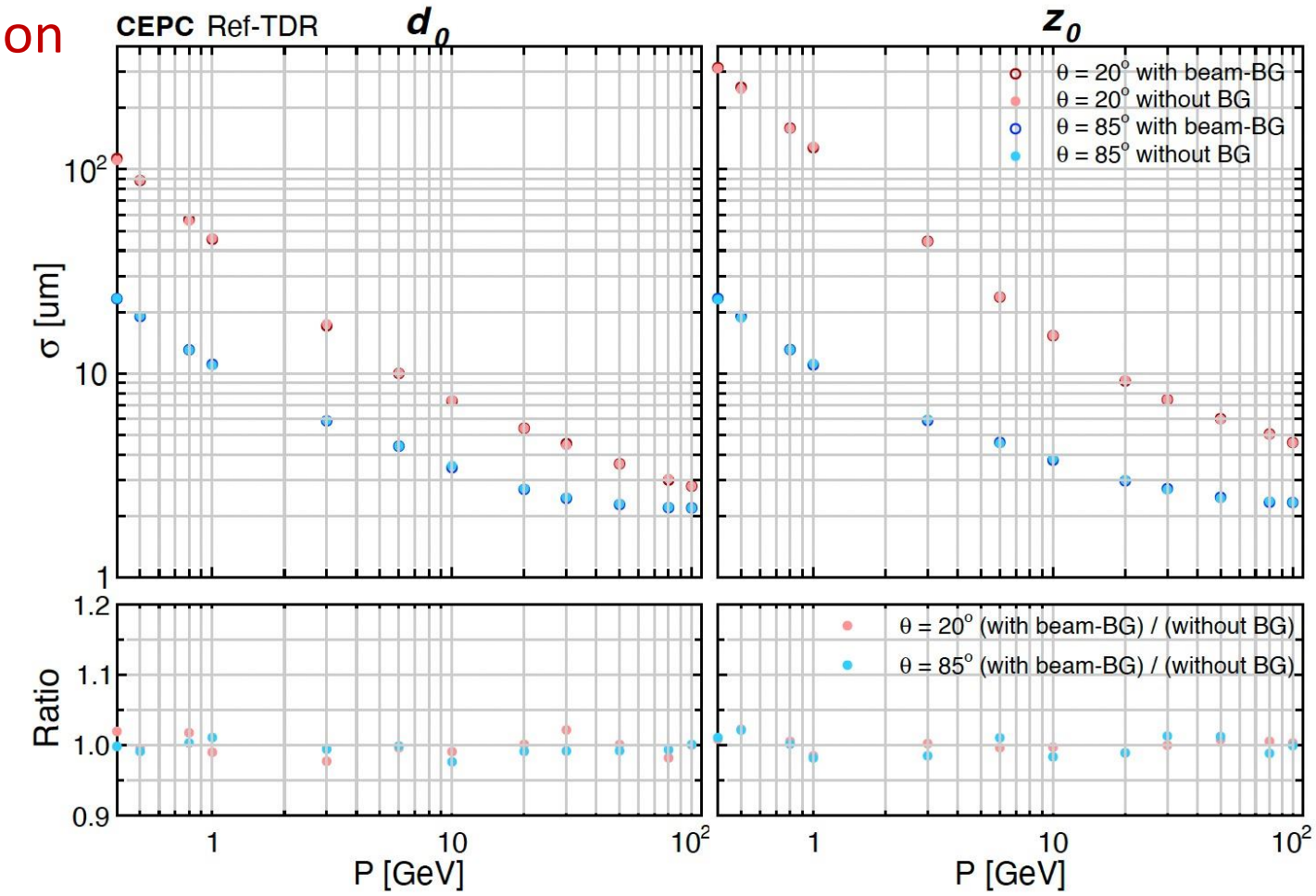
Alternative scheme
3 double layer ladders



Impact parameter resolutions of d_0 and z_0 for the baseline and alternative

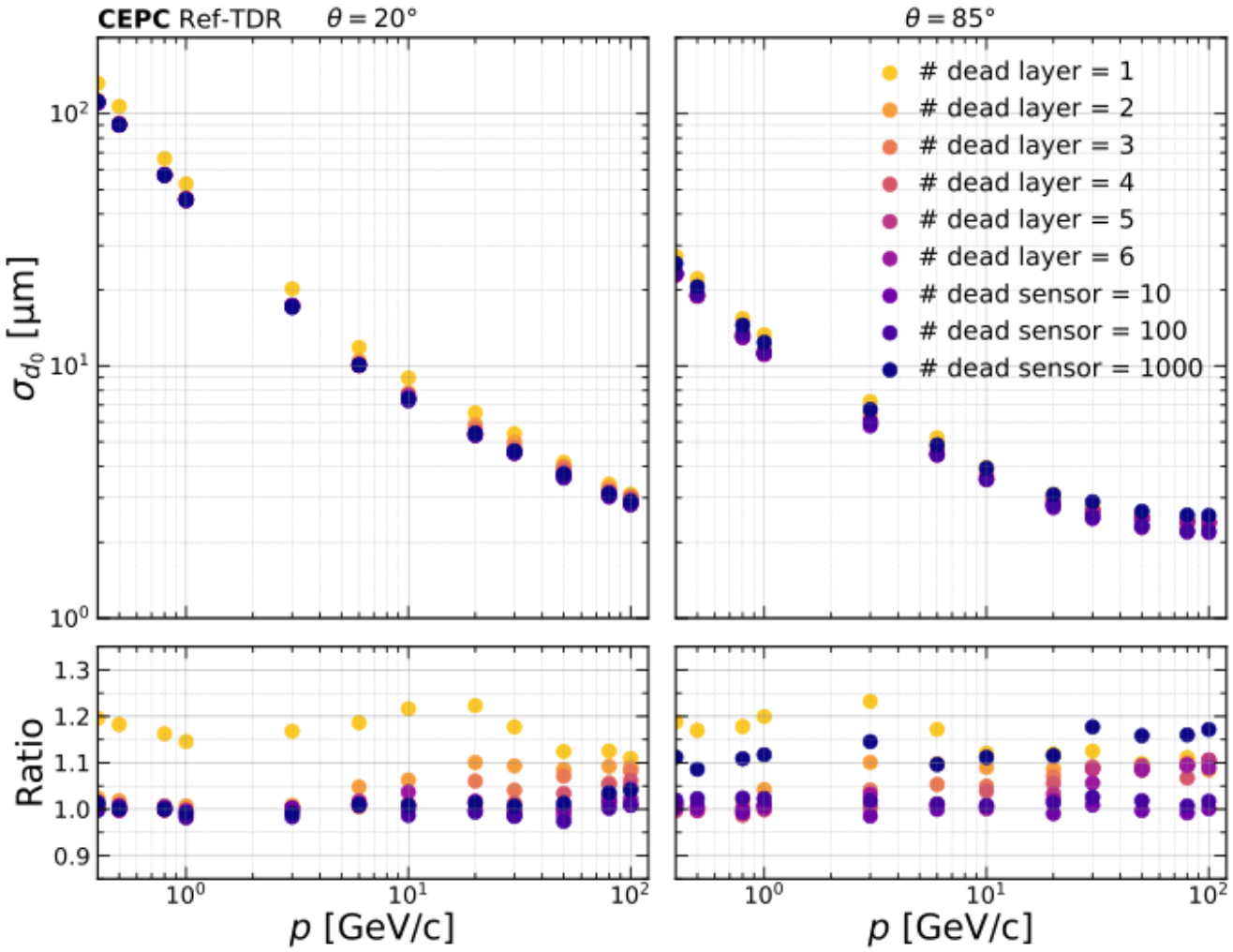
Performance with beam background

- The impact of beam background to performance has been studied.
  - No visible effect in d_0/Z_0 resolution
  - SR photons not accounted yet
    - Expected to be negligible



Performance: Efficiency

- Simulations assuming the complete loss of signal from one layer at a time.
- Any single layer loss leads to performance drop <= 25%, with the innermost layer contributing the most.
- VTX expected to maintain stable performance.

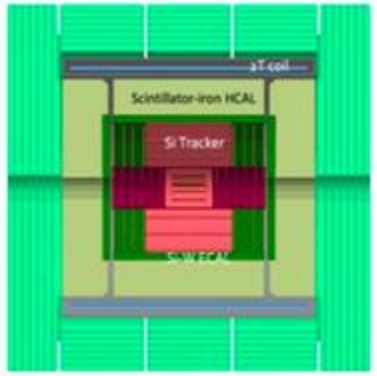


Detector concept: AGORA

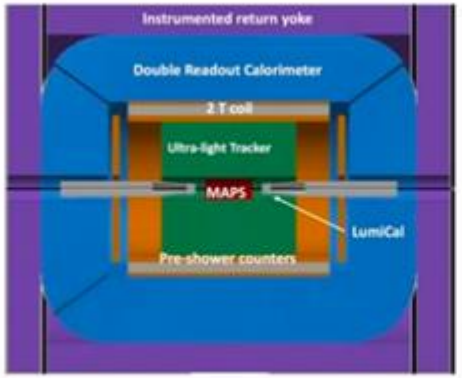
- AGORA: Advanced Glass Optimized Research Apparatus, originated from the CEPC Reference Detector, has been adopted as the 6th detector concept for FCC-ee in June.

Collider	FCC-ee				CEPC	
Detector Concept	ILD	CLD	FCC-ee IDEA	ALLEGRO	AGORA	CEPC IDEA
B-field [T]	2	2	2	2	3	2
Vertex inner radius [mm]	13	13	14	14	11	11
Vertex	Si-pixel	Si-pixel	Si-pixel	Si-pixel	Si-pixel	Si-pixel

Ref: Projects for FCC-ee Vertex Detectors, FCC-week 2026



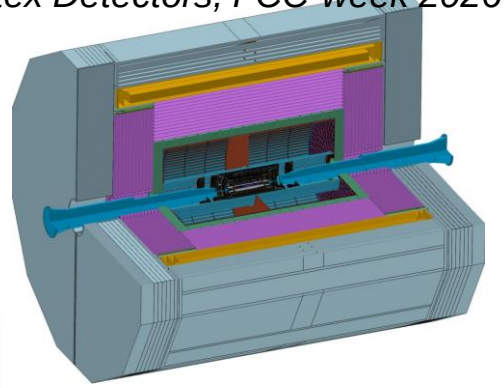
CLD



IDEA


ALLEGRO

ILD


AGORA

Choice of technology for next R&D

- Next step foundry: SK Hynix system fab in Wuxi China (90 nm CIS with Stitching feasibility)

	Requirements	TPSCo 65 nm	HLMC 55 nm	HC90L
Feature size	55 – 90 nm	65 nm	55 nm	90 nm
Epitaxial layer thickness	10 - 25 µm	10 µm	3-5 µm	4 – 8.5 µm (default) Can be changed to ~20 µm
Resistivity of epi-layer	> 1 kΩ•cm	~130 Ω•cm	Low resistivity ~10 Ω•cm	30-50 Ω•cm (default) Can upgraded to 5 kΩ•cm
Availability of deep N-well	Yes	Yes	Yes	Yes
Availability of deep P-well	Yes	Yes	Yes	Yes
Numbers of metal layers	> 6	Max. 7	Max. 5	Max. 5 (6^{th} metal in development)
Availability of stitching	Yes	Yes	Yes	Yes
Cost (NRE)		~7.0 M RMB	~6.0 M RMB	2-3 M RMB

Vertex detector working plan

- Development of 1st engineering run MAPS with HC90L technology.
  - Prototype full size RSU-like sensor
  - Validate sensor and electronics performance without stitching
  - Expect to finalize the design by Q1 2027
- Work together with mechanics group on thermal mockup
  - Test air cooling and the vibration
- Longer term: explore stitched MAPS prototypes with HC90L process
- Final goal: built detector prototype close to AGORA baseline design

Summary

- Curved MAPS option chosen as baseline for Reference detector TDR. （arXiv:2510.05260）
- We active expanding international collaboration and explore synergies with other projects
  - We are members of ECFA DRD3 collaboration
  - We are now working to integrate AGORA into the FCC-ee project.
  - Plan to propose HC90L MAPS R & D project to DRD3 in near future.

Research team

- IHEP: 8 faculty, 2 postdoc, 5 students
- IPHC/CNRS: collaboration in framework of FCPPL and DRD3
  - CEPC Jadepix design, ALICE/BELLE2 upgrade (especially on MAPS design, stitching)
- IFAE: Chip design , Sebastian Grinstein et al
  - CEPC TaichuPix chip design, ATLAS upgrade
- CERN: Joint R&D collaboration, in ALICE3 upgrade framework
- ShanDong U.: Stitching chip design
- CCNU: Chip design, ladder assembly
- Northwestern Polytechnical U. : Chip design
- Nanchang U. : Chip design
- Nanjing U.: Irradiation study, chip design
- NanKai U.: Physics performance

感谢各位聆听！

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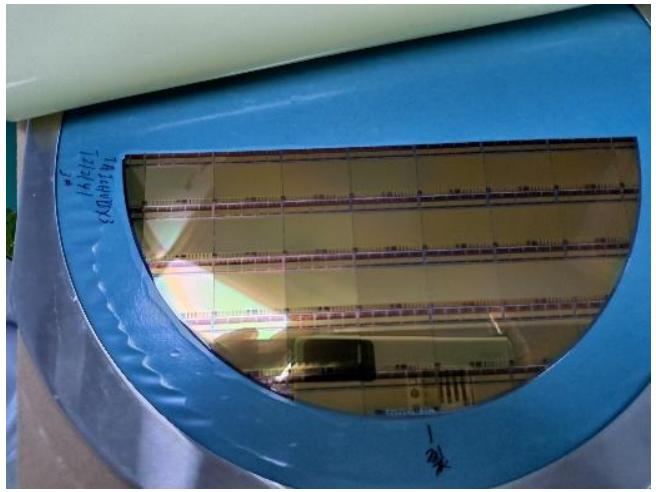
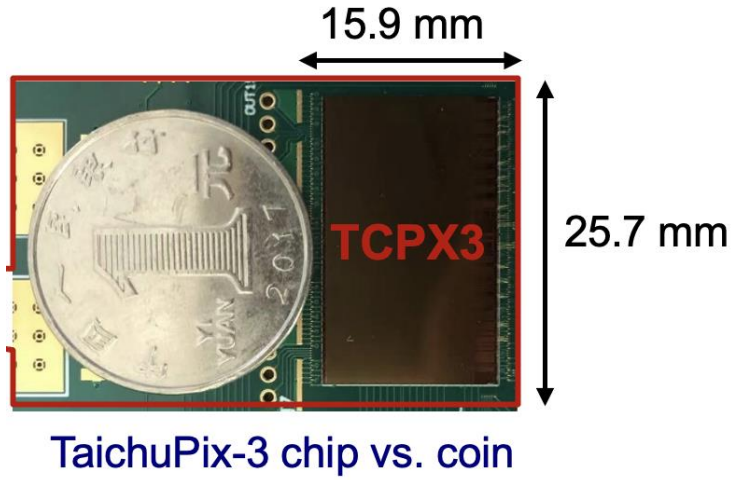
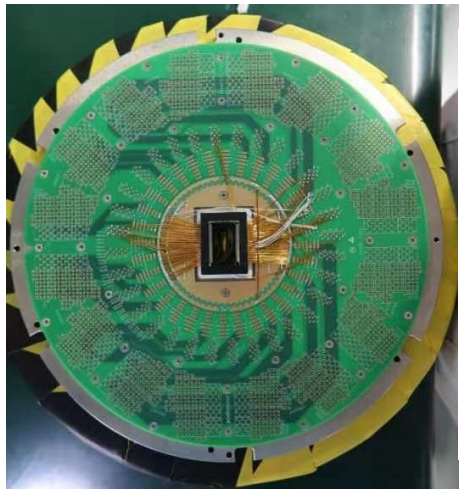
R&D efforts: Full-size TaichuPix3

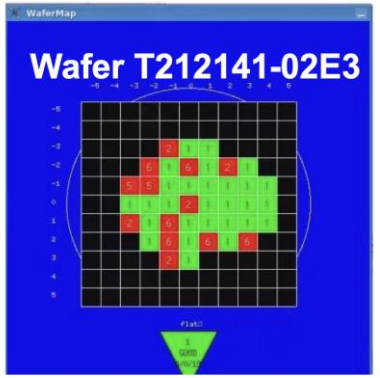
- Full reticle-size CMOS chip developed, 1st engineering run
  - 1024×512 Pixel array, Chip Size： 15.9 mm×25.7 mm
  - 25 μm×25 μm pixel size with high spatial resolution < 5 μm (@ detection eff. > 99%)
  - Process: 180 nm CIS process
  - Fast data-driven readout (50 ns/pixel) to cope with all operation modes in CDR
    - Dead time < 500 ns, Max. hit rate 36 MHz/cm^2





TaichuPix-3 chip vs. coin



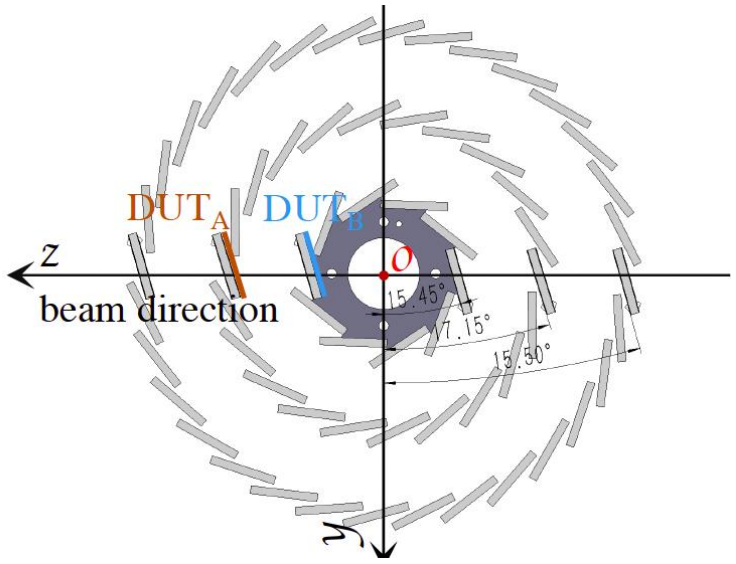


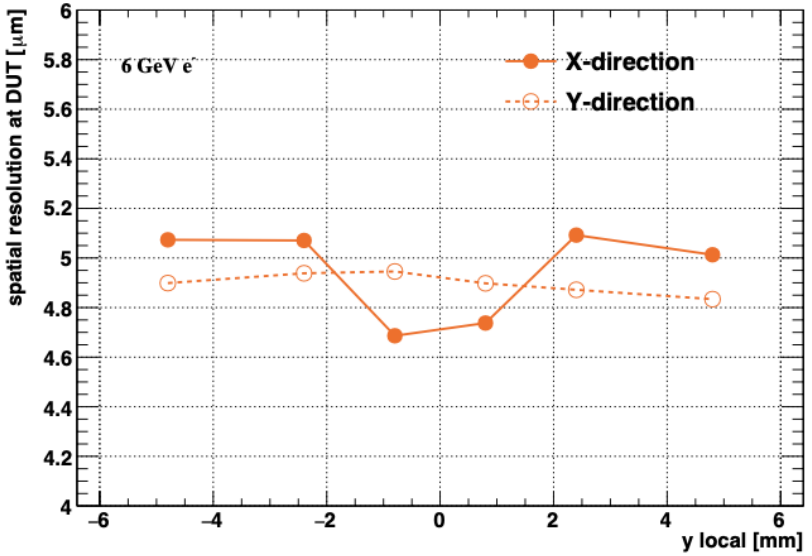
An example of wafer test result

	Status	CEPC Final goal
CMOS chip technology	Full-size chip with 180 nm CIS	65nm CIS

R&D efforts and results: vertex detector prototype beam test

Spatial resolution ~5 μm **Efficiency >99%**

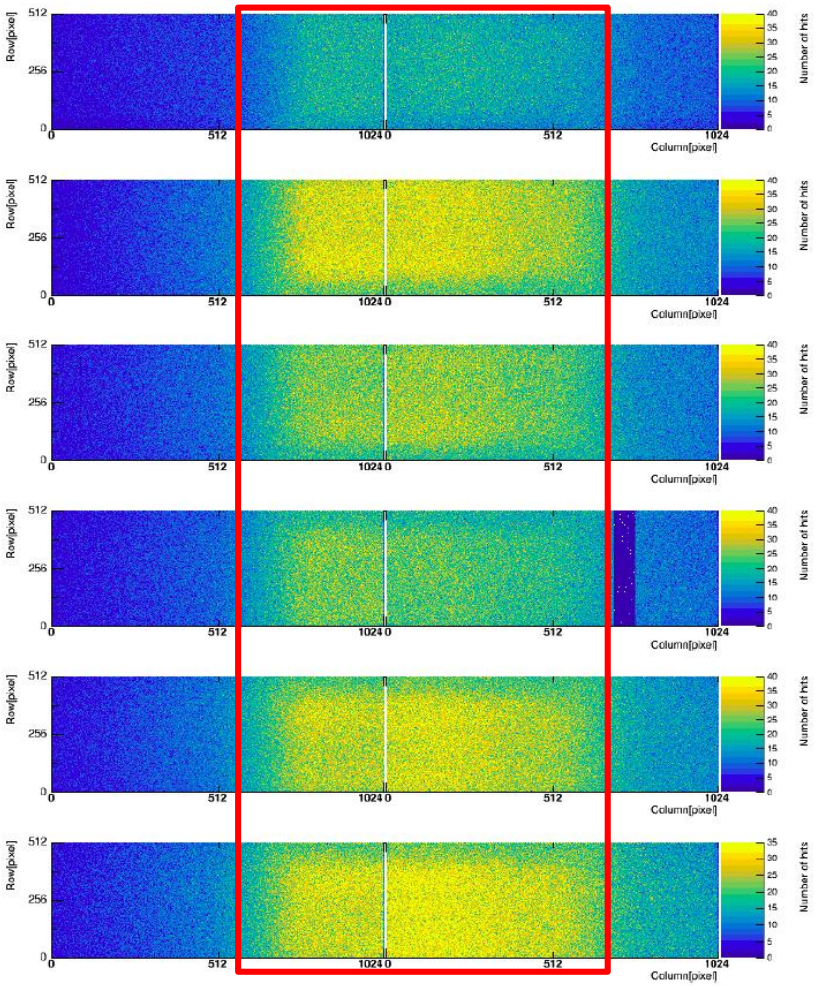




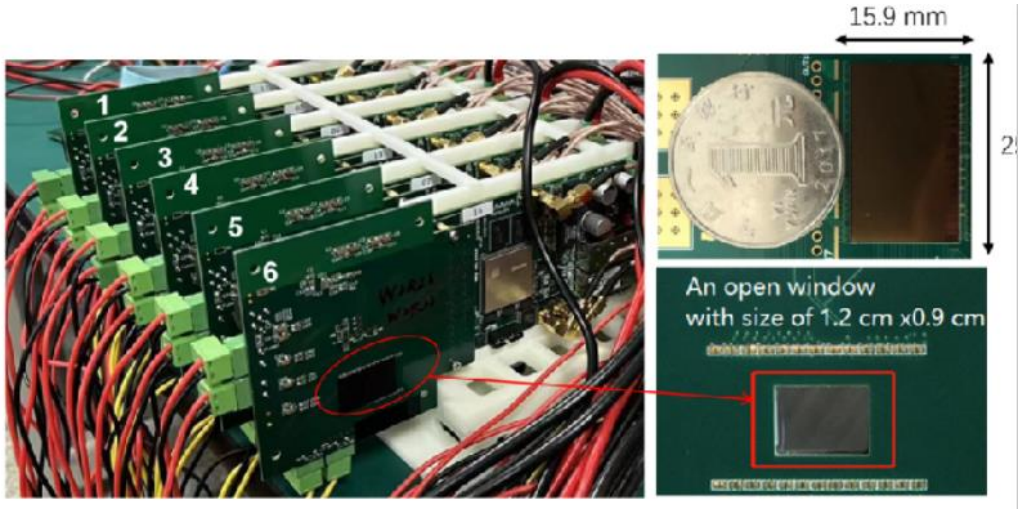
	Status	CEPC Final goal
Spatial resolution	4.9 μm	3-5 μm

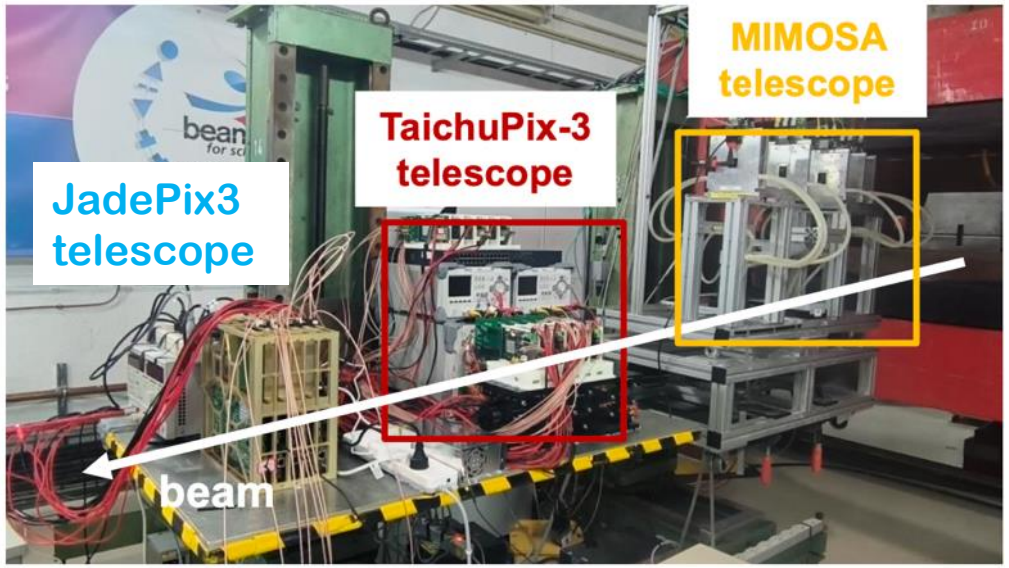
Hit maps of multiple layers of vertex detector

Beam spot



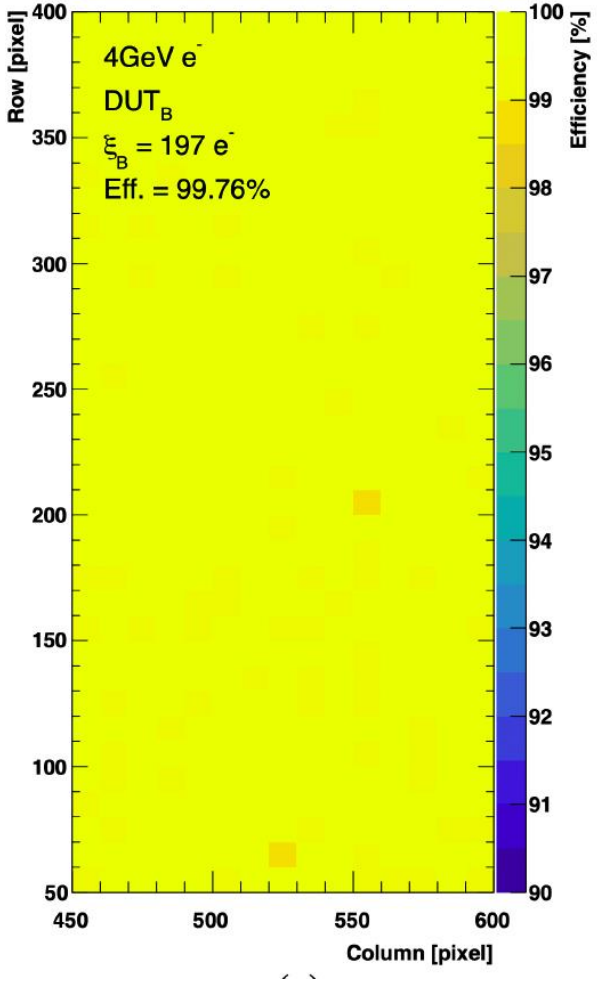
R&D efforts and results: Jadepix3/TaichuPix3 beam test @ DESY



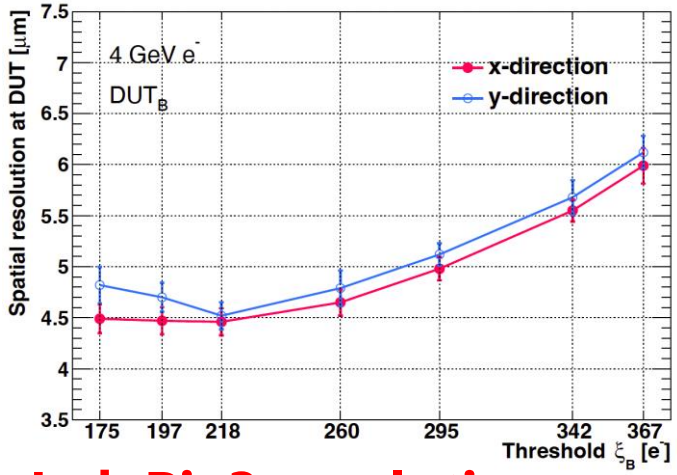


Spatial resolution 4~5um, Efficiency >99%

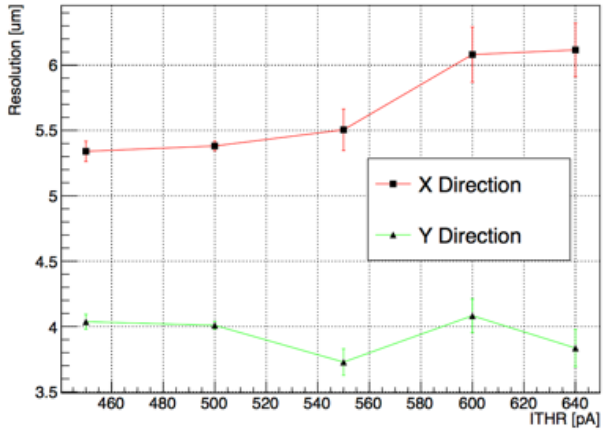
TaichuPix3 efficiency



TaichuPix3 resolution



JadePix3 resolution



Collaboration with CNRS and IFAE in Jadepix/TaichuPix R & D