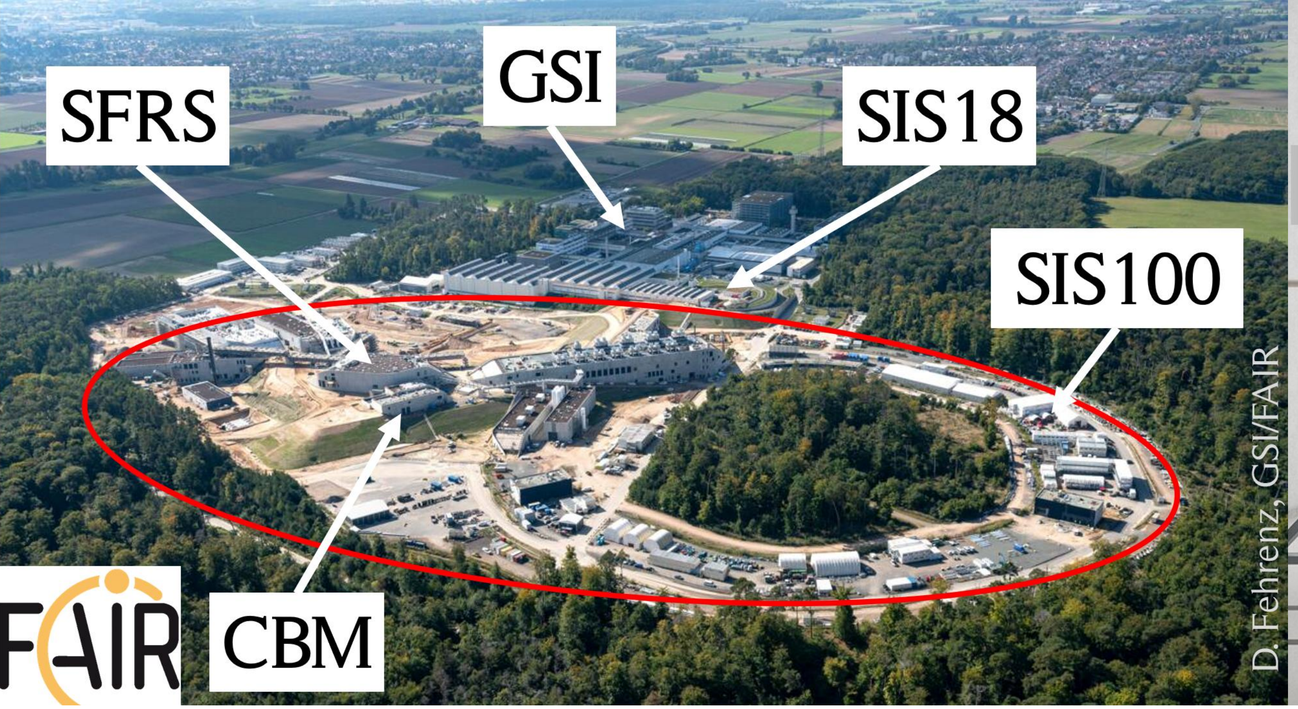
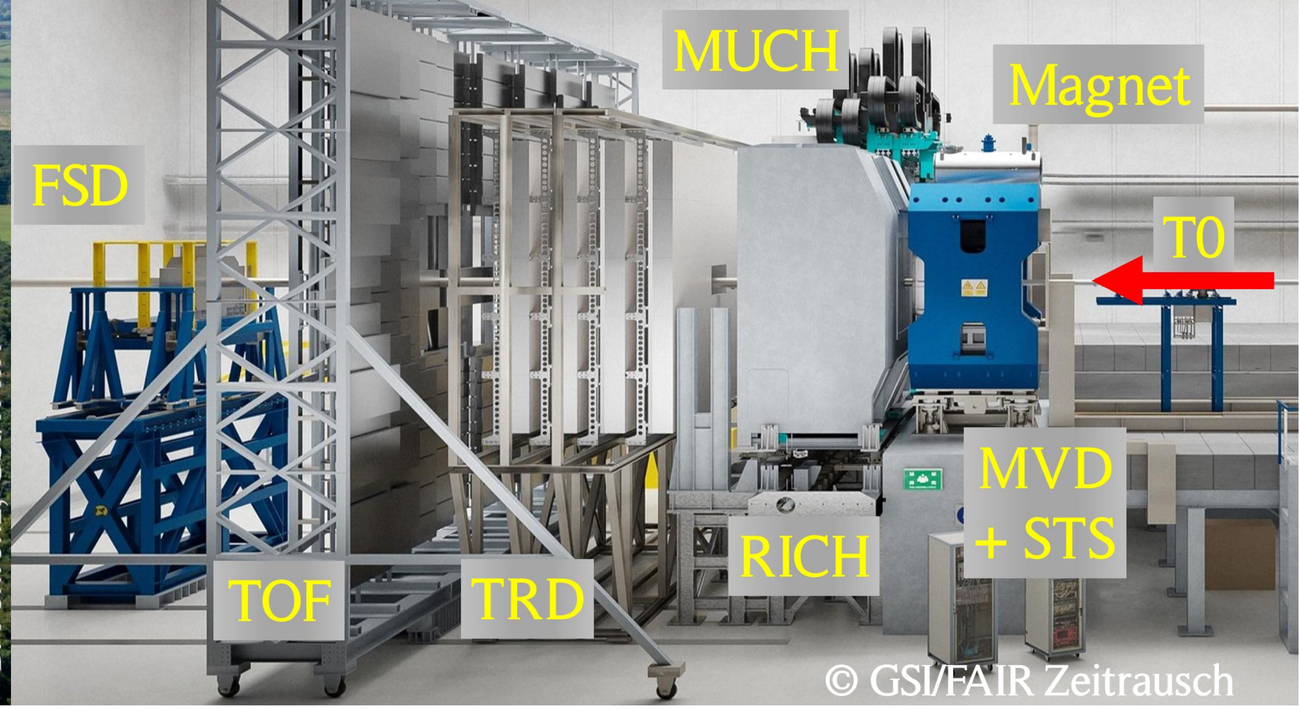
Status of the CBM Micro Vertex Detector

Franz A. Matejcek

AC-LGAD workshop Dalian, 10.11.2026



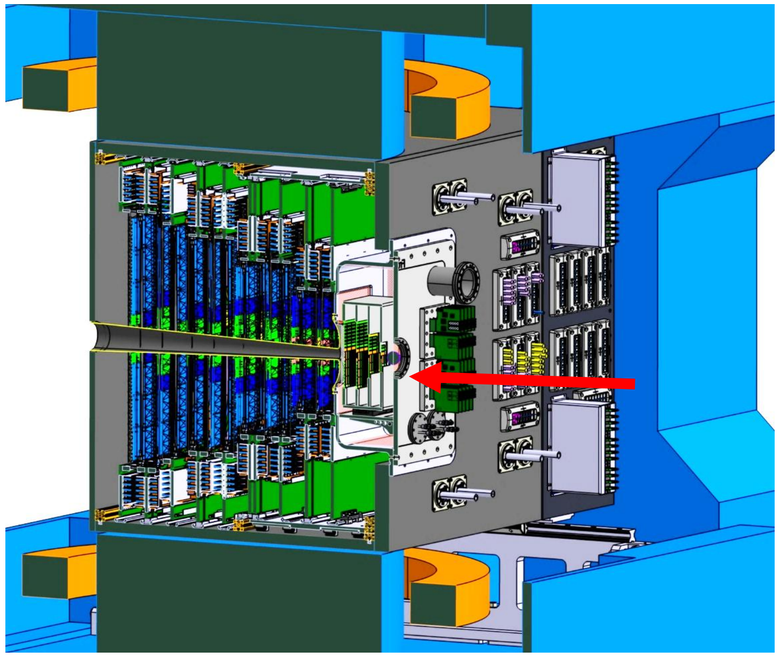


Compressed Baryonic Matter Experiment

→ Facility for Antiproton and Ion Research

→ Darmstadt, Germany

→ Fixed Target A-A at $\sqrt{s_{NN}} = 2.9, \ldots, 4.9$ GeV



The Inner Tracker

Inside 1 T·m magnet dipole field

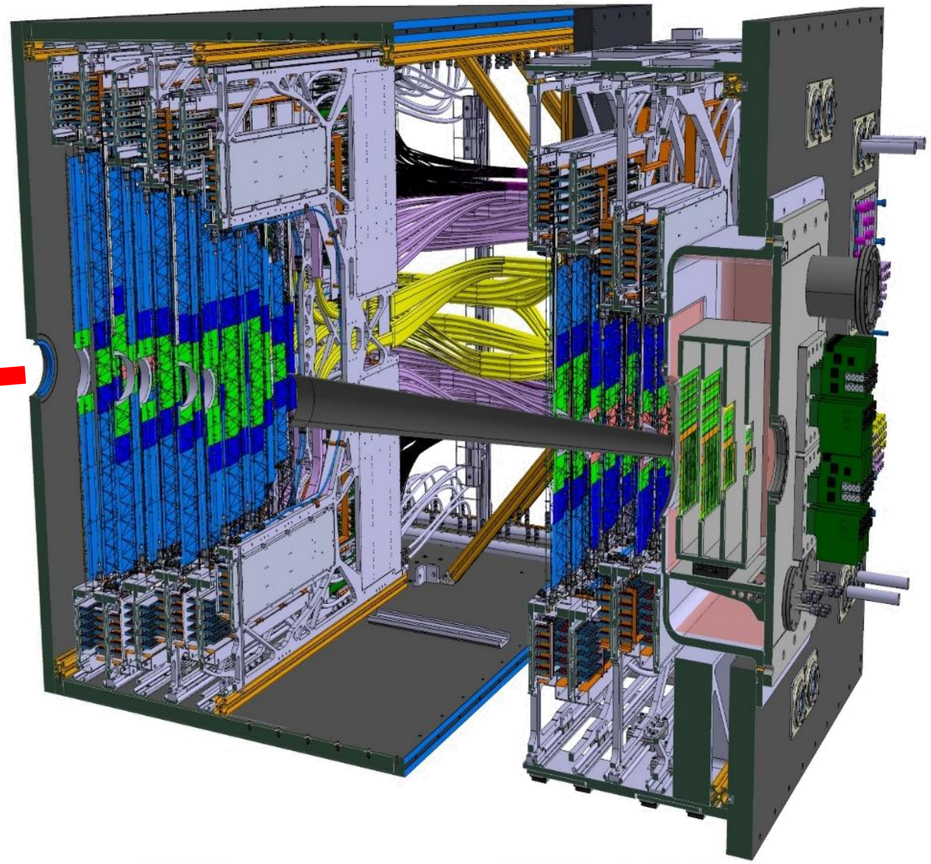
2.5 – 25° polar acceptance (full azimuth)

MVD: 4 layers CMOS MAPS

STS: 8 layers Si-strips

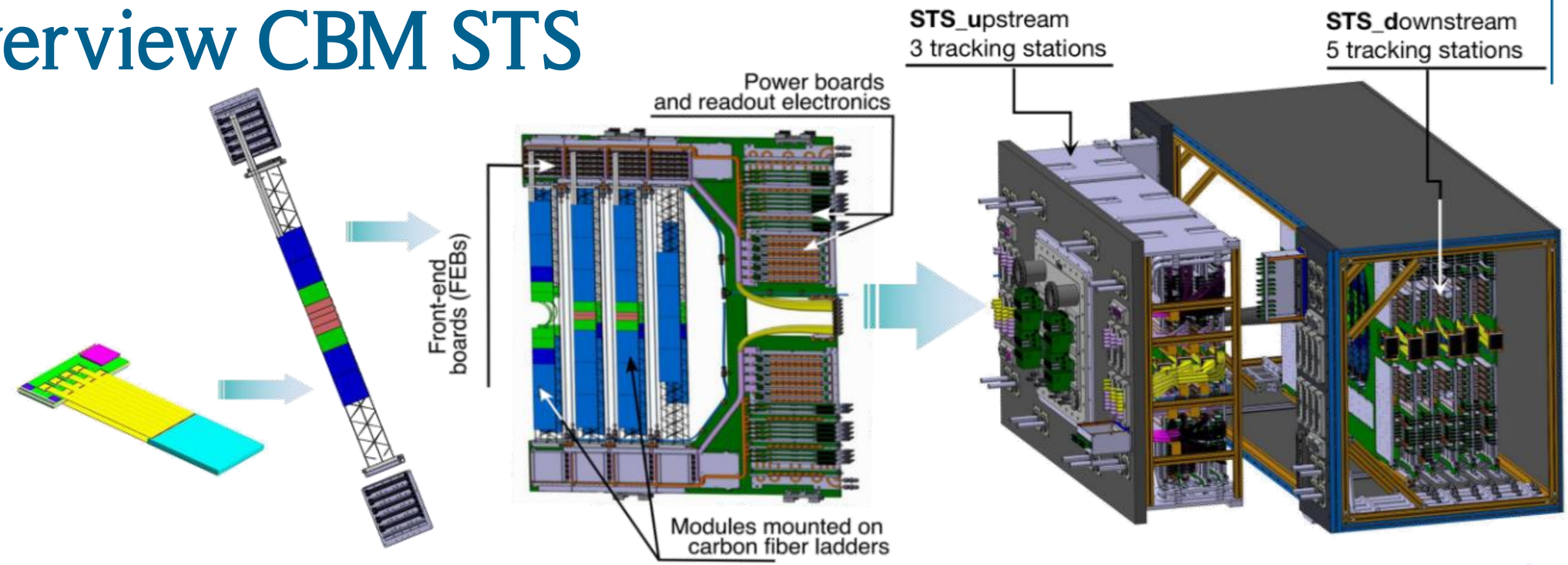
The CBM Inner Tracker





STS5 STS3+MVD

Overview CBM STS



876 modules
160 different modules
~1.8 million channels

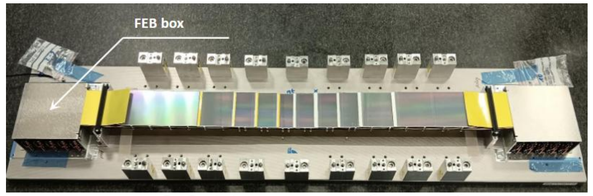
106 ladders
41 different form factors
2 - 10 modules

20 half-units

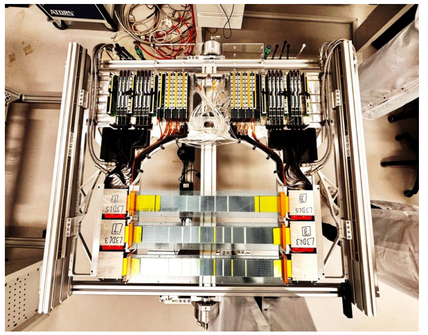
STS: 8 Tracking stations
3 **STS_u** + 5 **STS_d**



100% completed
(July ’26)



~80% completed
(Oct ’26)



1st HU assembled

Overview Micro Vertex Detector

4 planar tracking stations

→ 8 – 20 cm downstream of target

→ ~300 CMOS MAPS (0.15 m^2)

→ Interaction rate 100 kHz Au+Au (10 MHz pp)

Key challenges:

→ Radiation (EOL: 5 Mrad, 10^{14} n_{eq}/cm^2 peak)

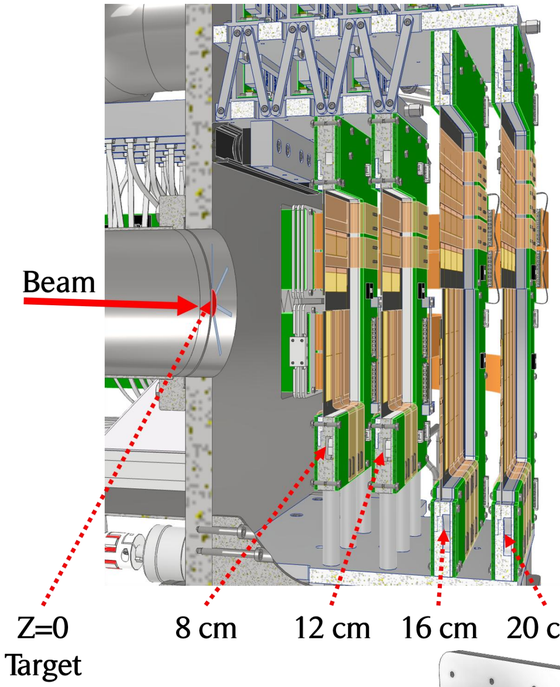
→ Magnetic field (1 Tm)

→ Moderate vacuum (10^{-4} mbar)

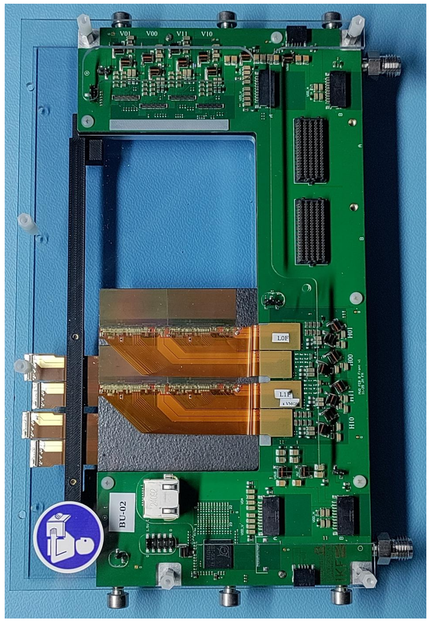
→ 0.3% – 0.5% X_0 per station

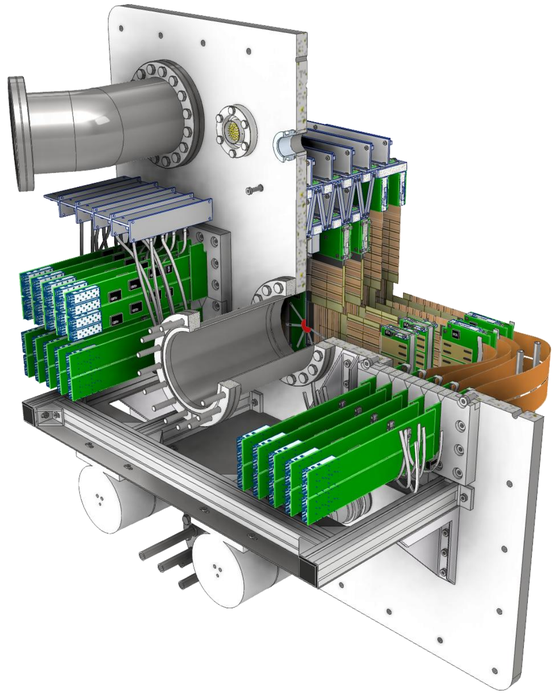
Passive cooling inside acceptance

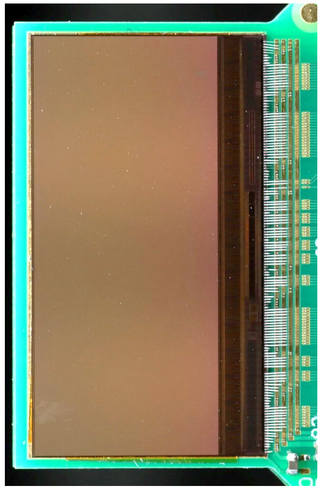
Double-sided sensor integration



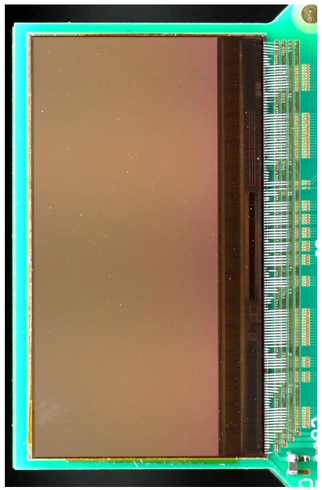




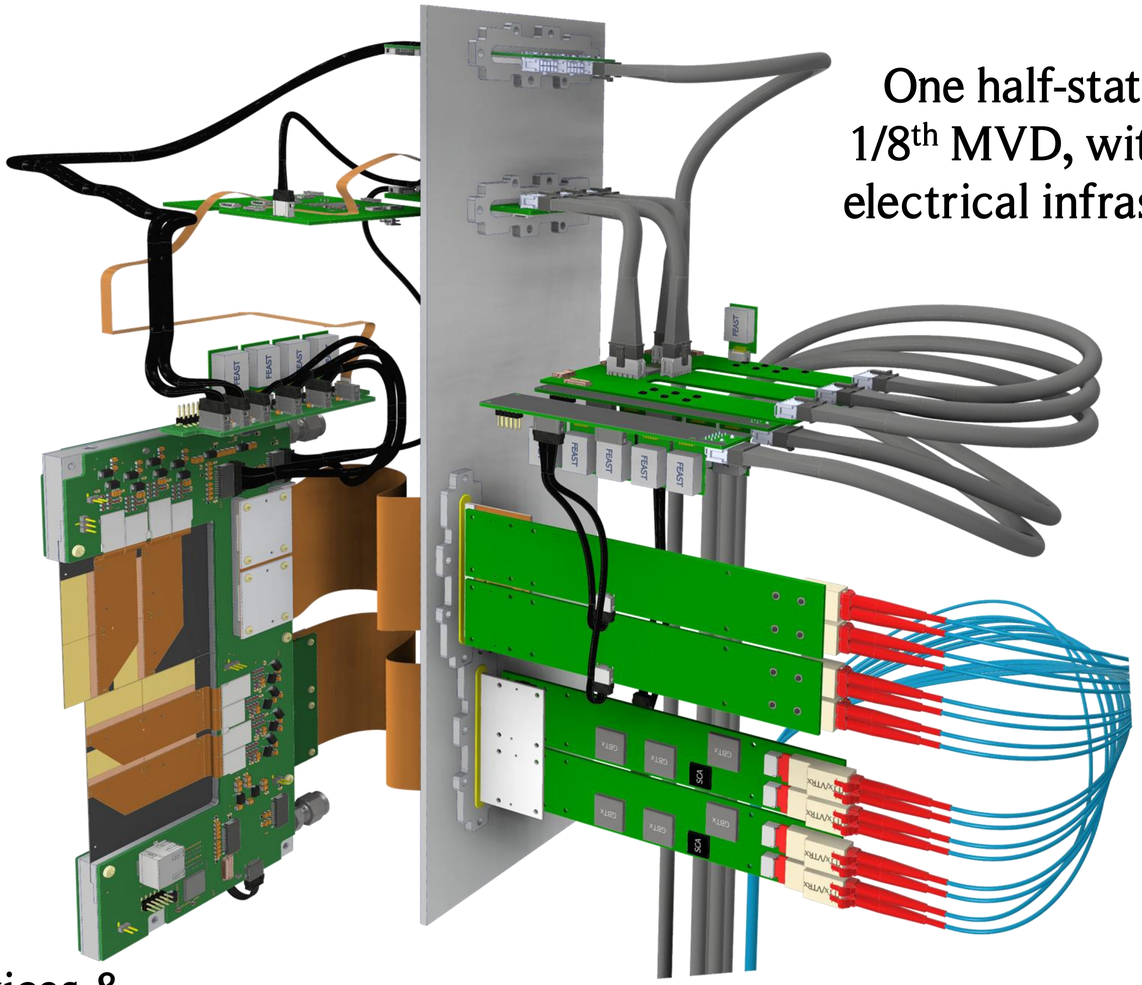




Not just x300 …

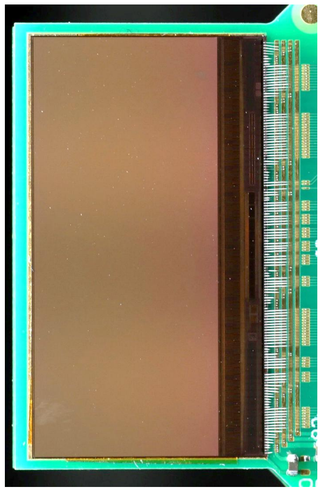


Not just x300 …

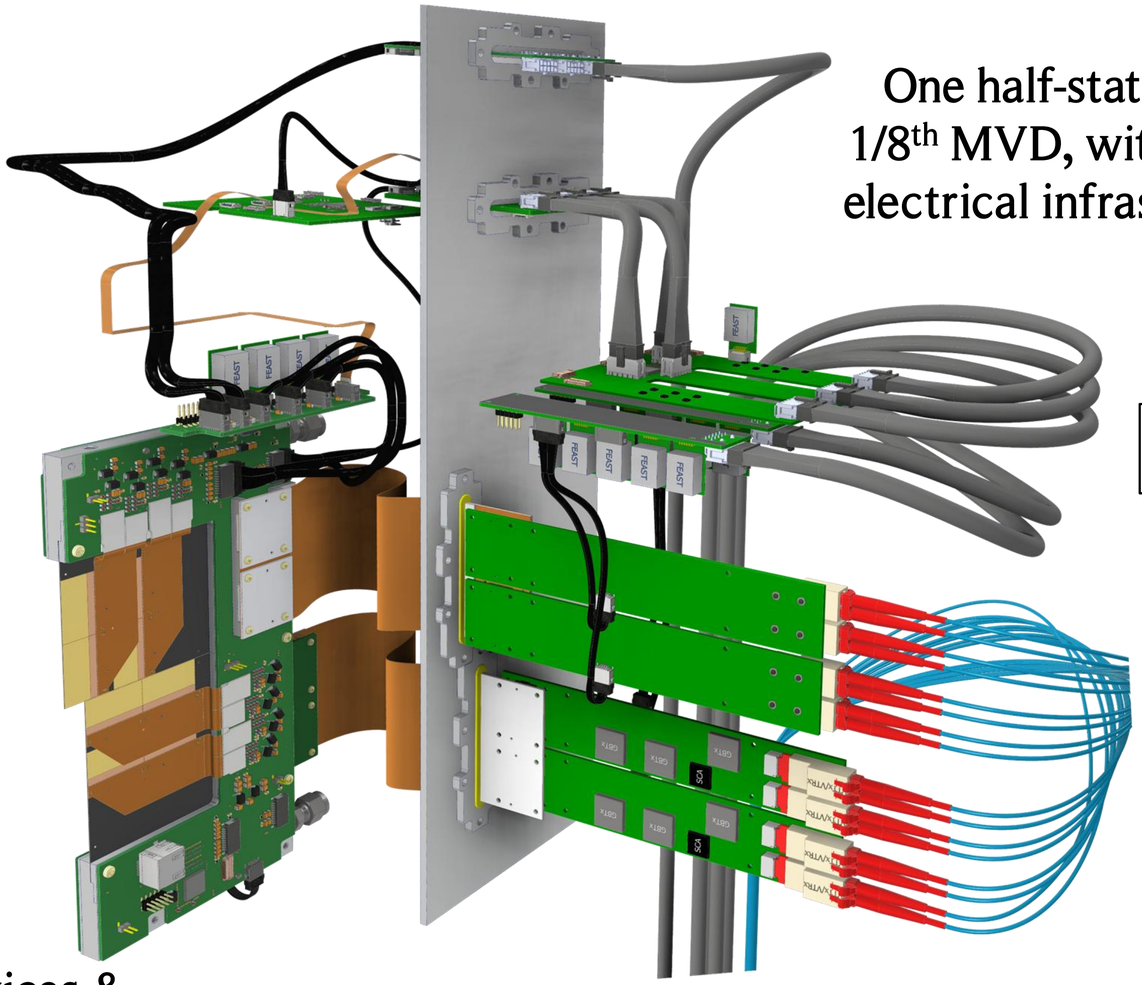


One half-station, i.e. 1/8th MVD, with its full electrical infrastructure

But many services & interfaces



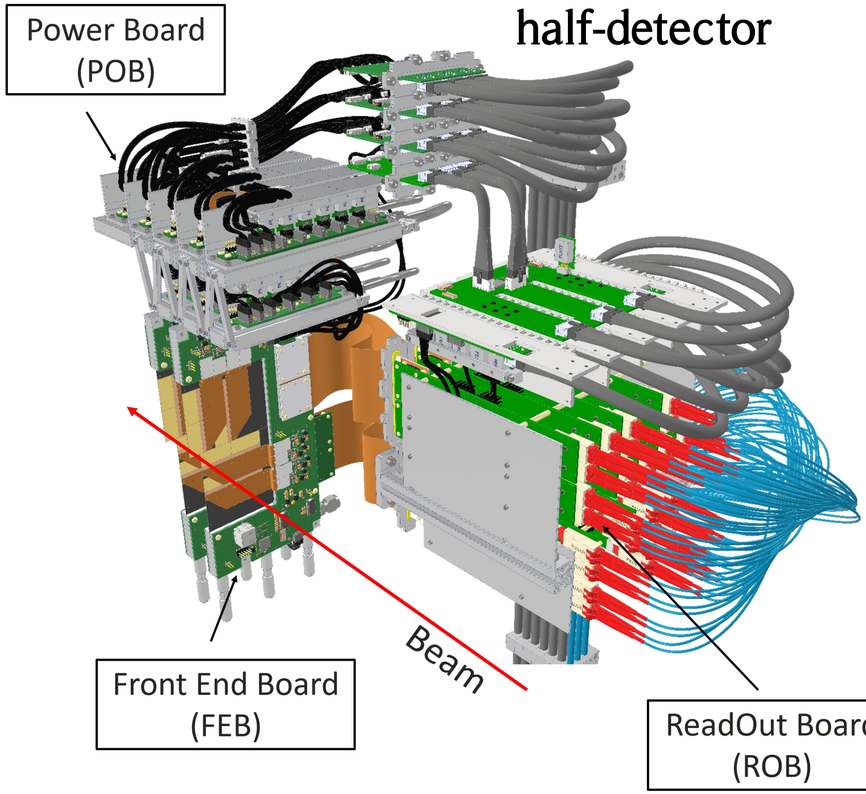
Not just x300 …



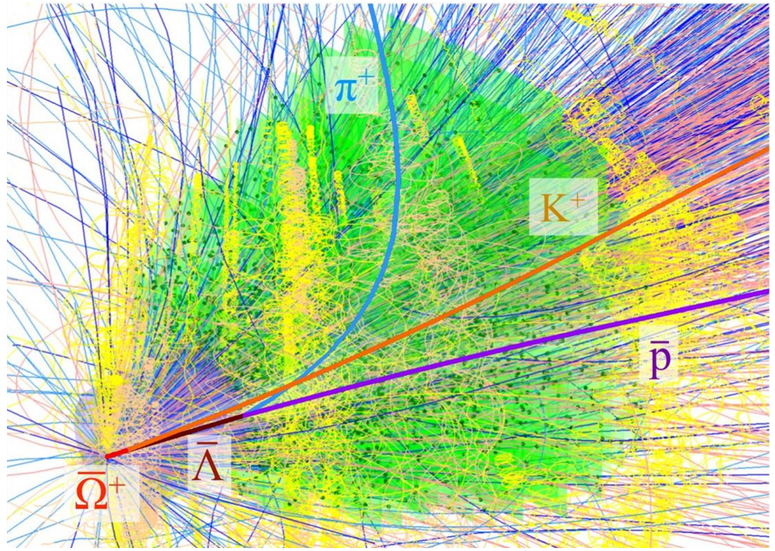
One half-station, i.e. 1/8th MVD, with its full electrical infrastructure

But many services & interfaces

Electrical services half-detector



MIMOSIS (TJ180)

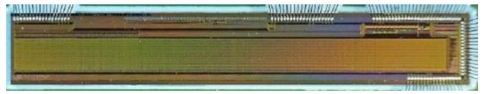


"The needle in the haystack"
Anti-Ω in12 *A*GeV Au-Au collisions
in the Inner Tracker

	Requirement
Spatial precision	~5 µm
Time resolution	~5 µs
Thickness	~50 µm
Power dissipation	< 100 mW/cm²
Radiation doses (non-ionizing)	**> 7x10^{13} n$_{eq}$/cm²**
Radiation doses (ionizing)	**> 5 Mrad**
Radiation gradient on chip	**~100%**
Rate capability avg. (peak)	**20 (80) MHz/cm²**
HI-tolerance	10 Hz/mm²

~10x ALPIDE (ALICE ITS2)

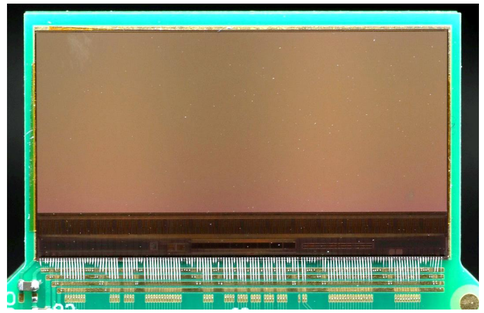
~20x ALPIDE (ALICE ITS2)



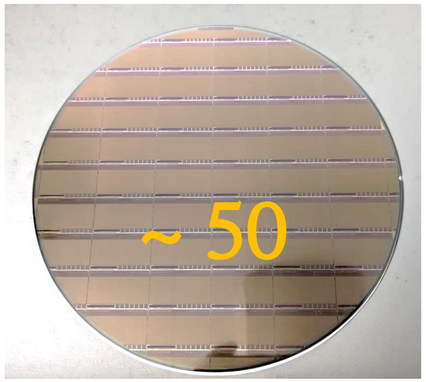
MIMOSIS-0 (2018)



MIMOSIS-1 (2020)



MIMOSIS-2/2.1 (2024)



MIMOSIS-3 (2027)

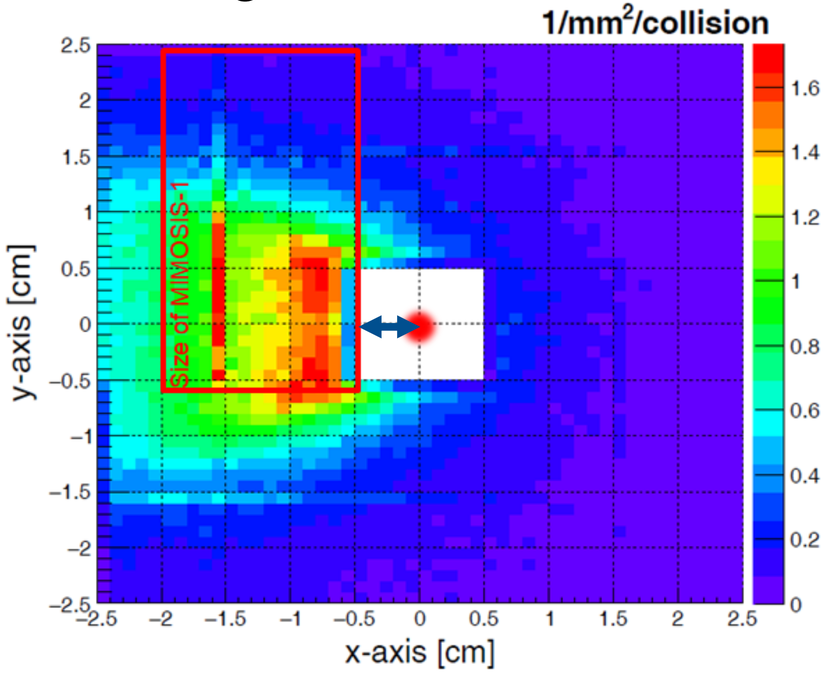
Challenge: Fixed Target

δ-e⁻ (+ dipole field: irradiation gradient)

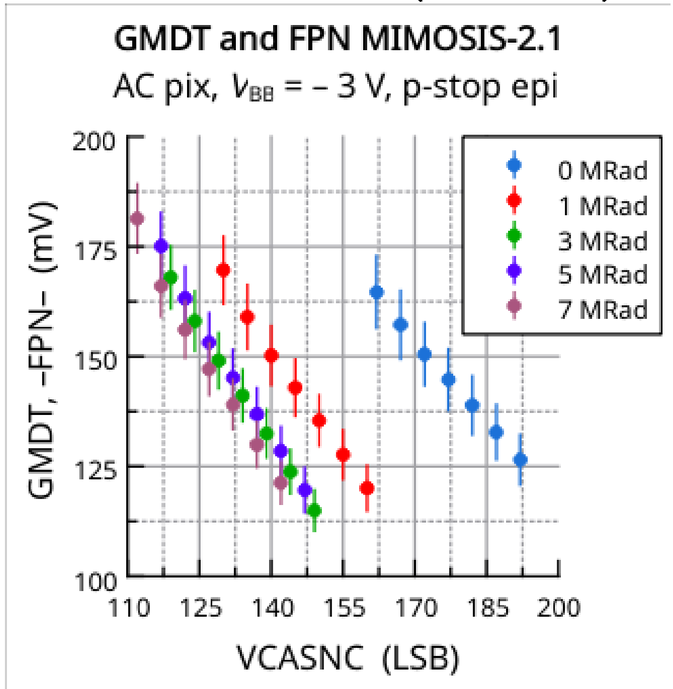
→ Threshold shift

→ Pre-irradiation to saturate effect (^{60}Co γ)

Hit gradient 1st MVD station



Threshold shift M2 (unbiased)

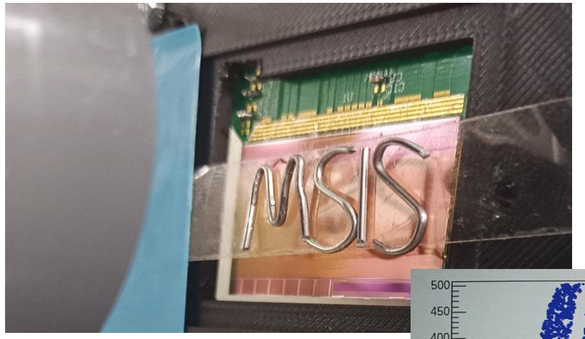


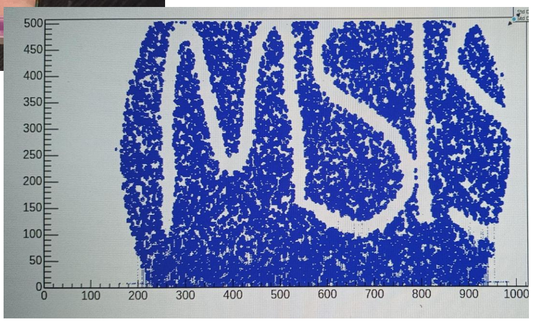
Challenge: Fixed Target

δ-e⁻ (+ dipole field: irradiation gradient)

→ Threshold shift

→ Pre-irradiation to saturate effect (^{60}Co γ)



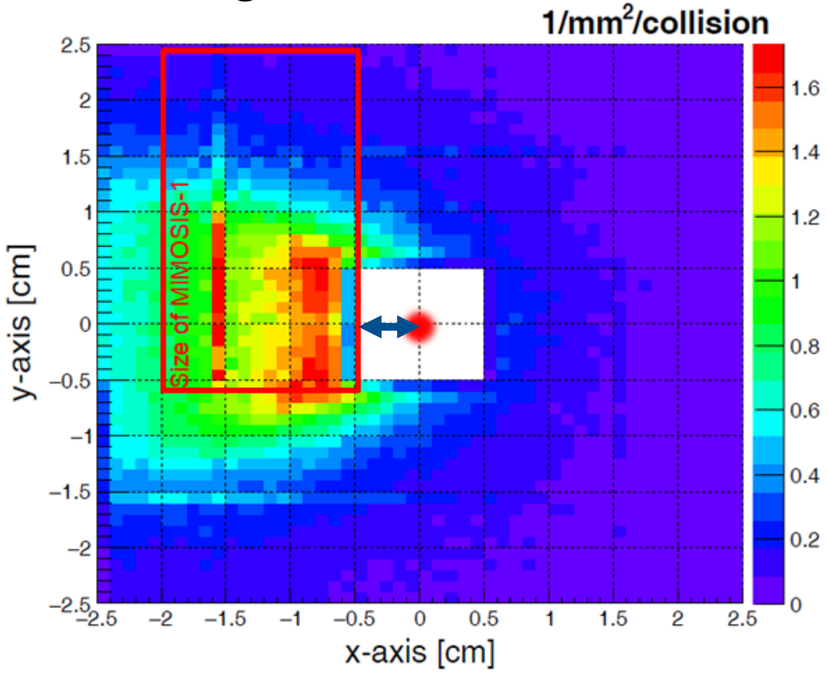


Single Event Effects from beam halo, target fragments, direct beam impact

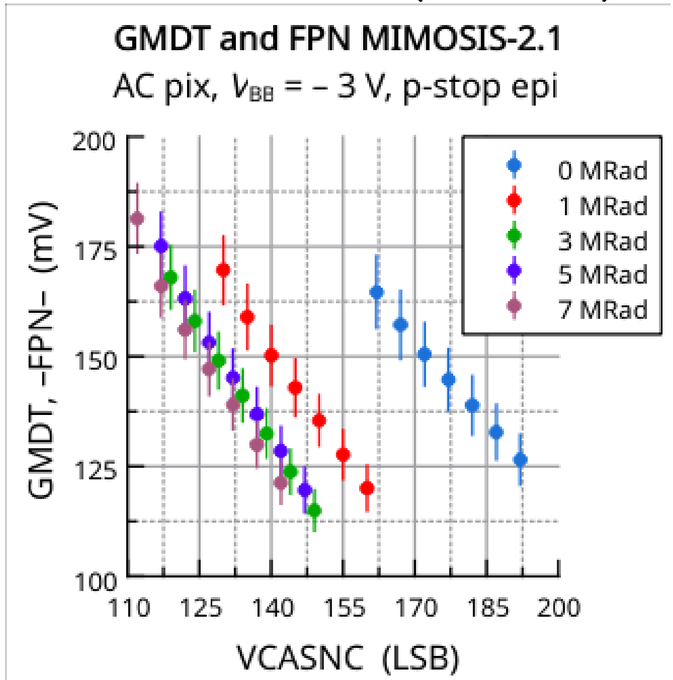
→ 5.4 mm next to the beam!

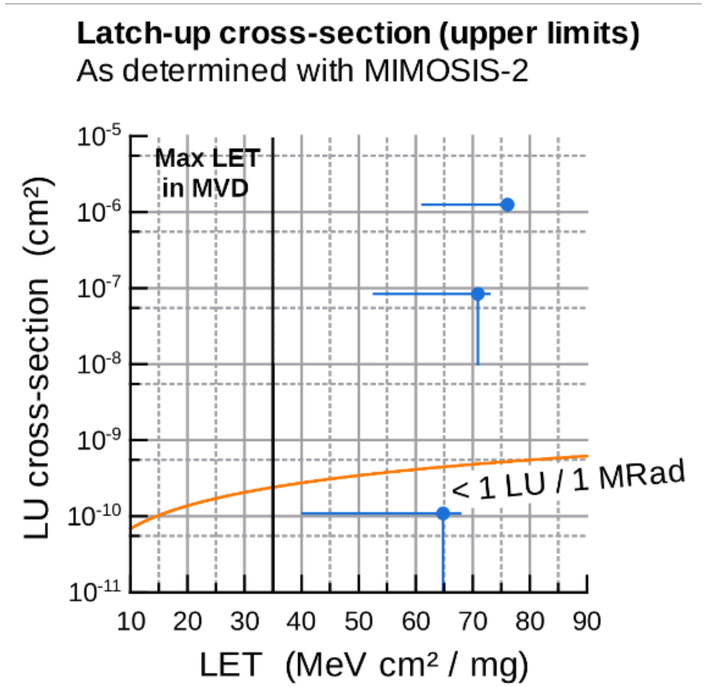
→ Validate with ~4 *A*MeV Au @GSI

Hit gradient 1st MVD station



Threshold shift M2 (unbiased)





First results: B. Arnoldi-Meadows et al.

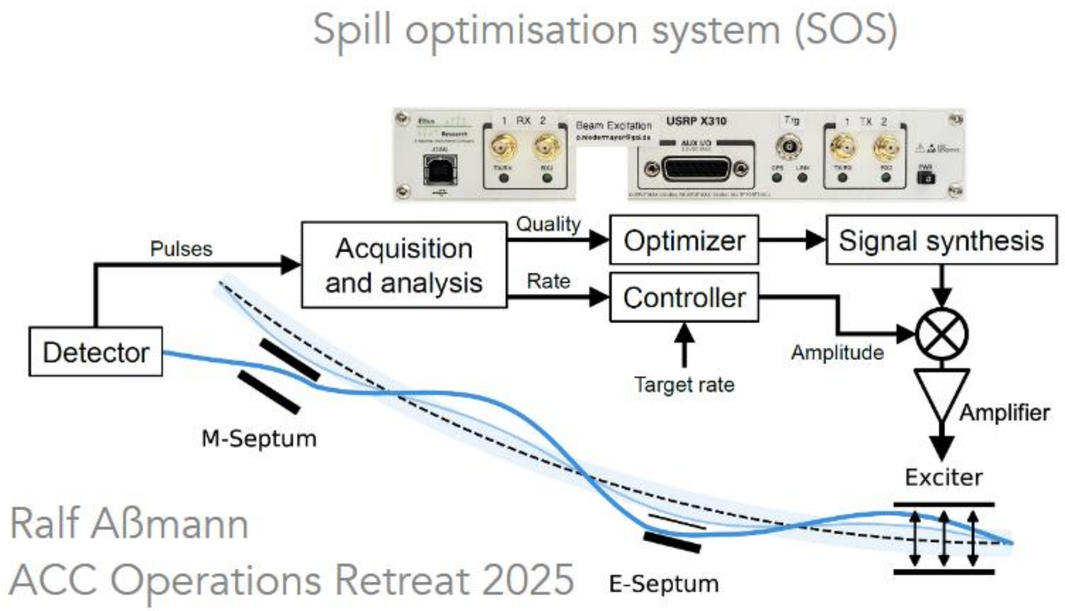
Challenge: Intensitiy Fluctuations

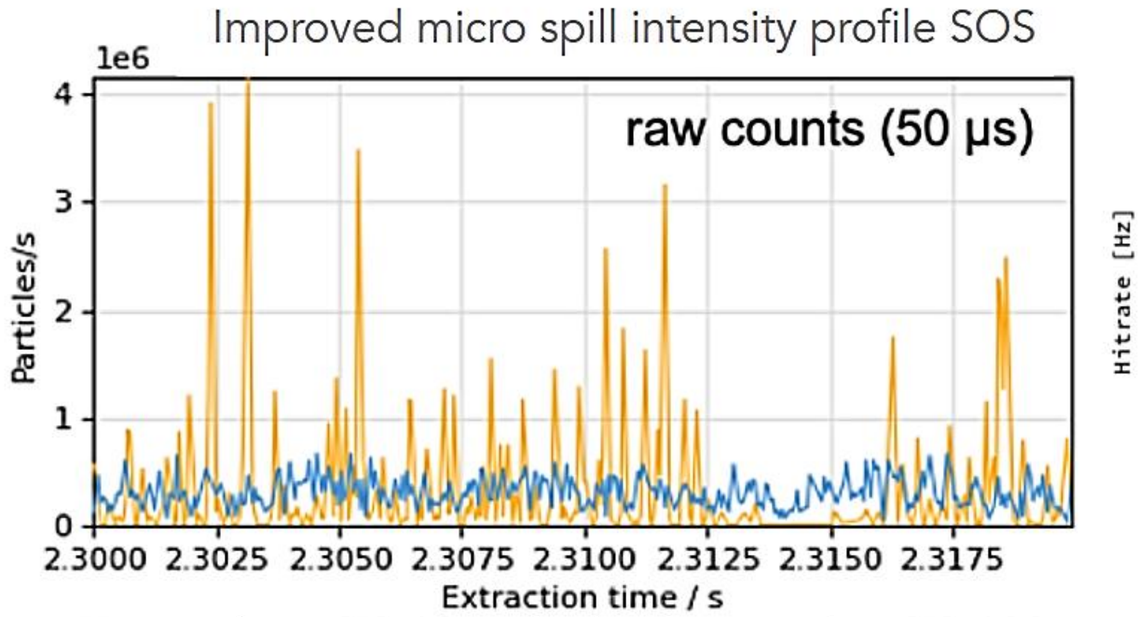
Non-ideal spills in realistic accelerators (SIS100)

→ Global spill: 0.5 s synchrotron refill, 10 s slow extraction

→ μ-spill structure (known from SIS18)

→ Substantially improved with Spill Optimization System (SOS)





Known from SIS-18, to be implemented at SIS-100.

Challenge: Intensitiy Fluctuations

Non-ideal spills in realistic accelerators (SIS100)

→ Global spill: 0.5 s synchrotron refill, 10 s slow extraction

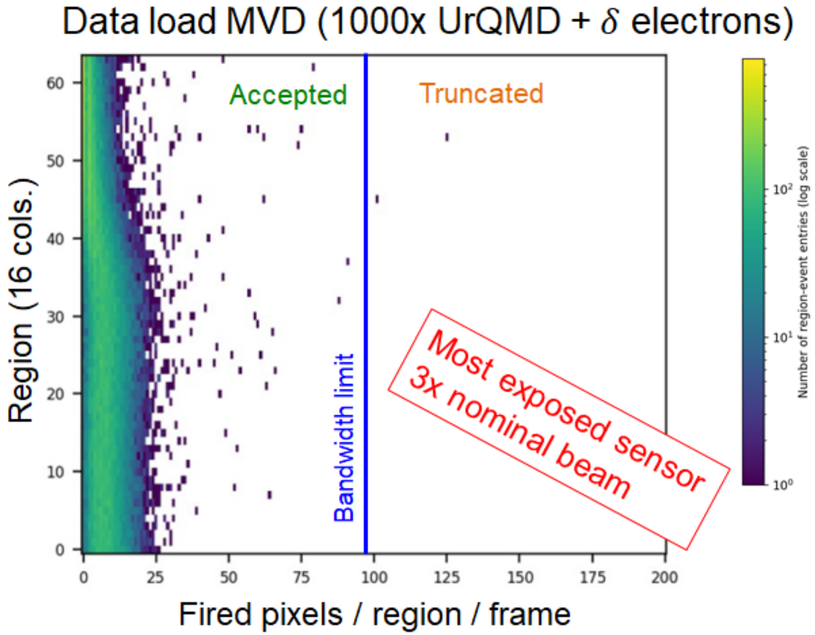
→ μ-spill structure (known from SIS18)

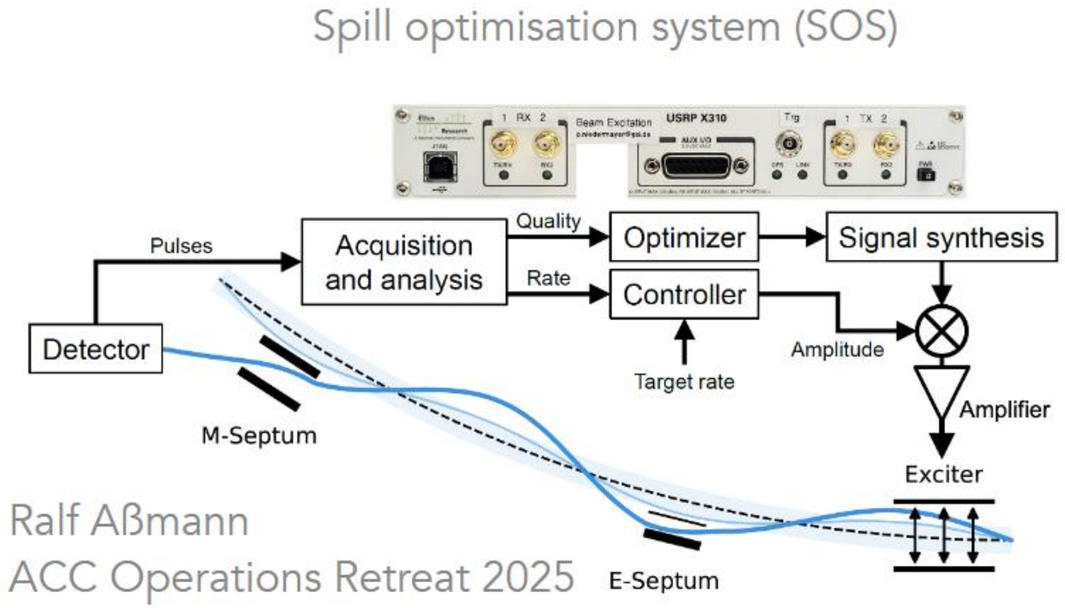
→ Substantially improved with Spill Optimization System (SOS)

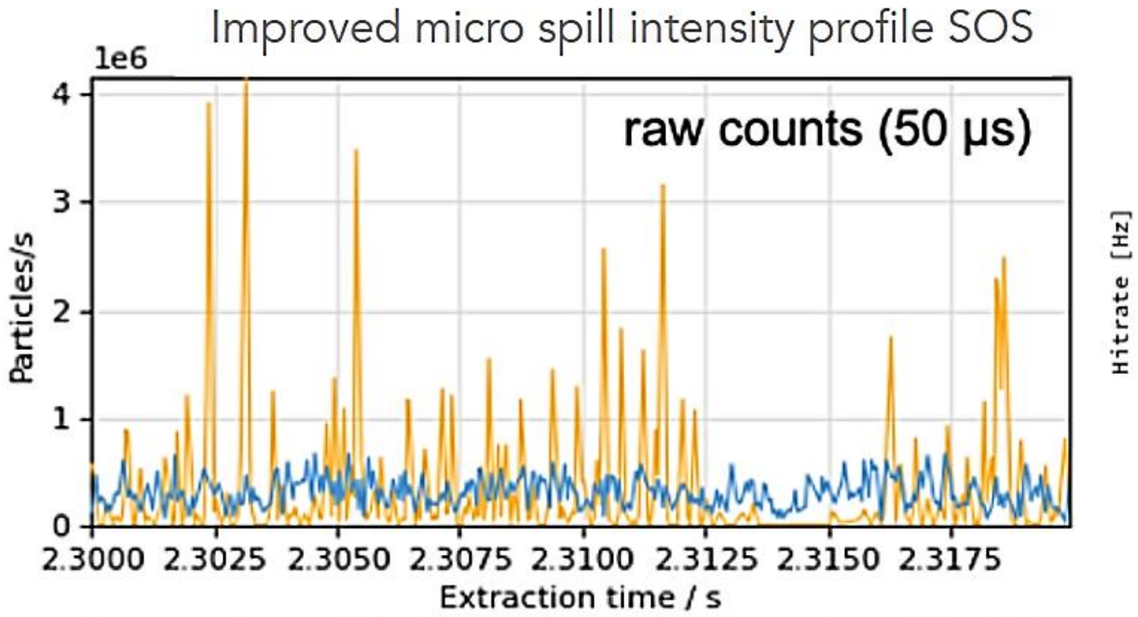
Elastic buffer in MIMOSIS

→ Peak/average >3 for 50 μs

→ Write speed 10.24 Gb/s > Read speed 2.56 Gb/s (for 8 links)







Known from SIS-18, to be implemented at SIS-100.

Challenge: Powering

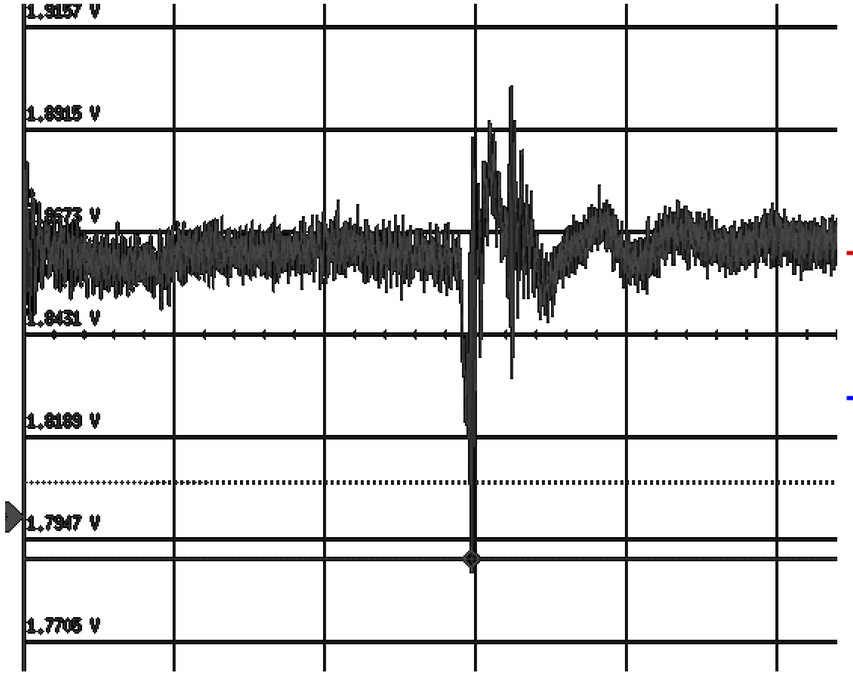
Optimize power distribution network (PDN) on-chip and in-detector

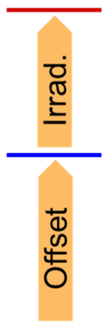
→ Static and dynamic voltage drops on all time scales

→ CMOS logic sensitivity

Validated in full system tests

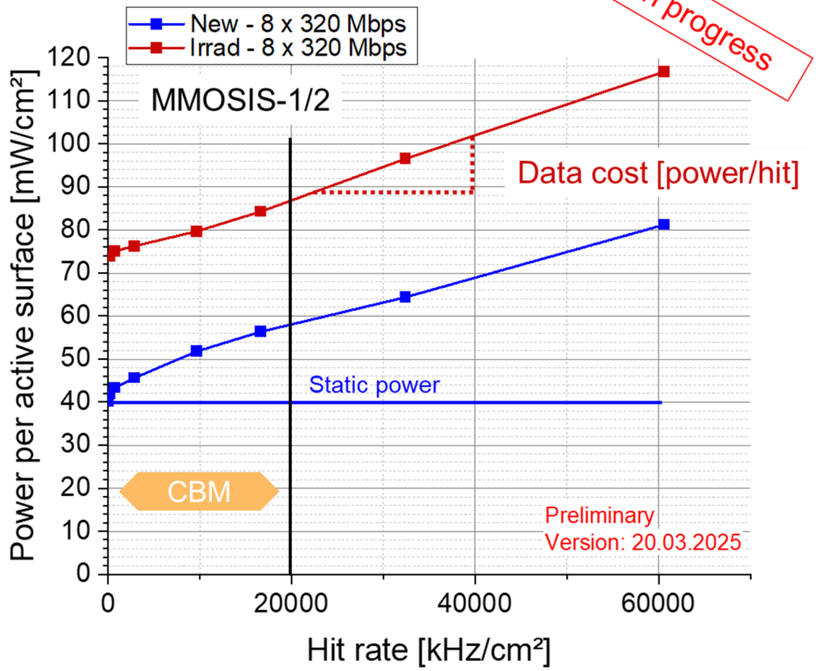
≲ 100 mV voltage fluctuations on VDD every frame (5 µs)





≲ 2x digital power increase during spills, TID effects

Work in progress

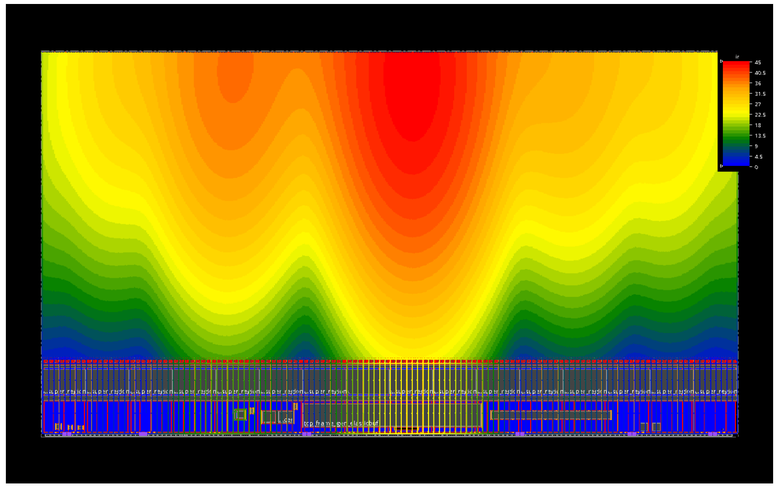


Challenge: Powering

Optimize power distribution network (PDN) on-chip and in-detector

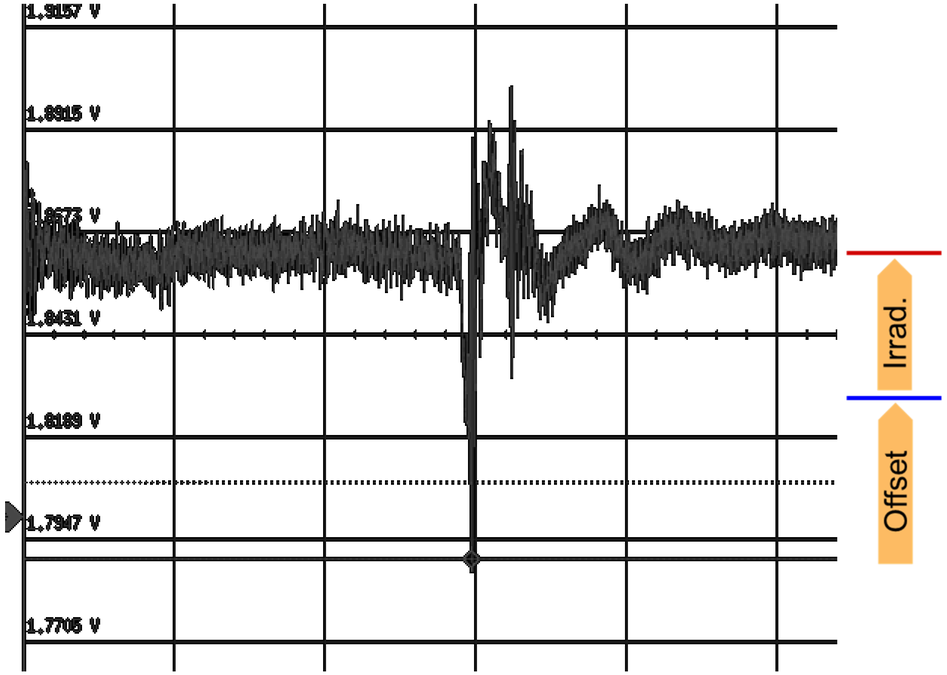
→ Static and dynamic voltage drops on all time scales

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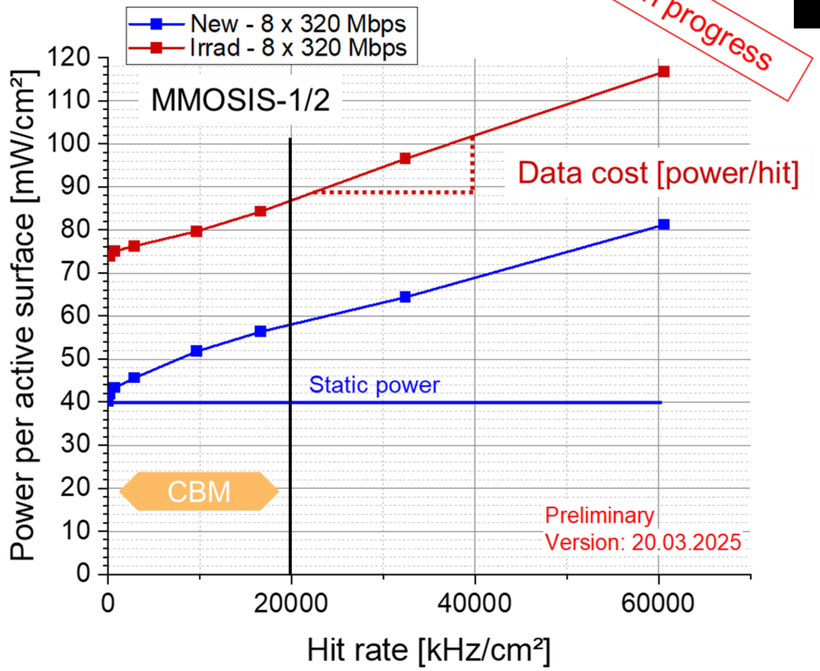
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Work in progress



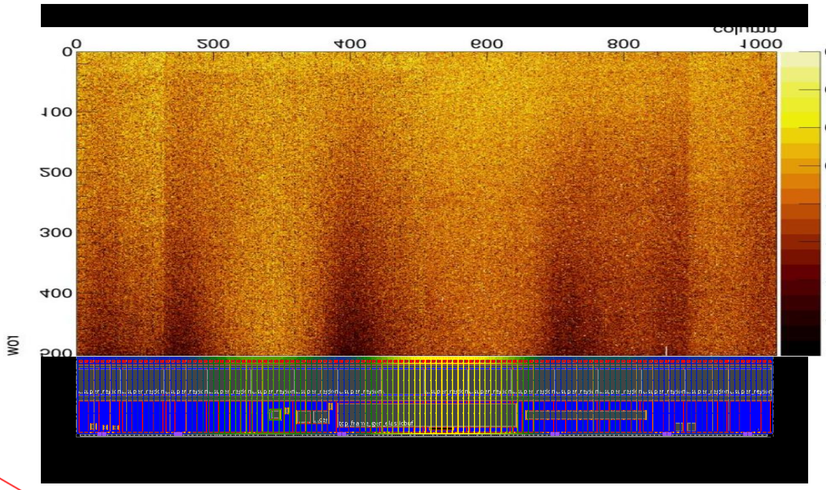
Challenge: Powering

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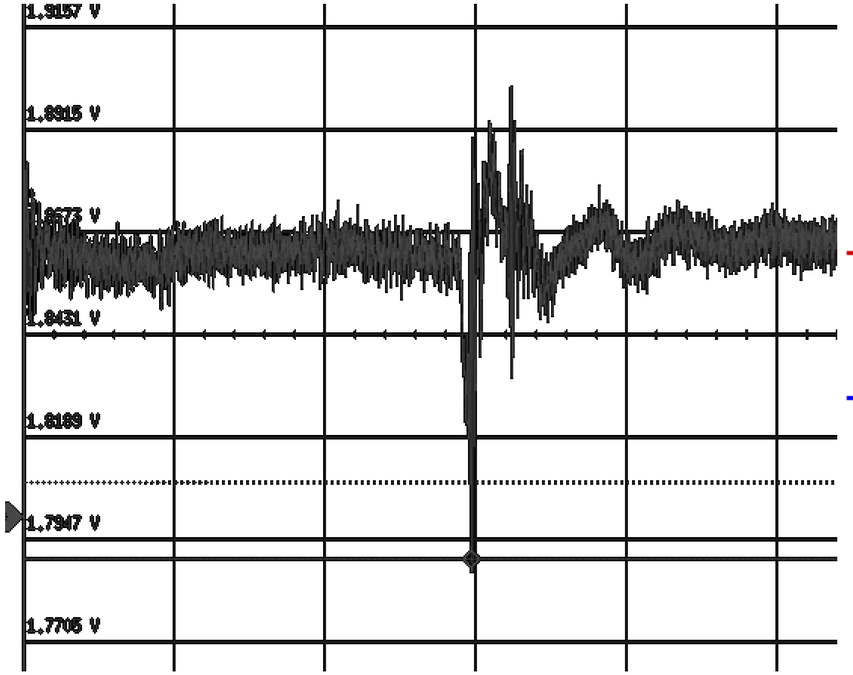
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→ CMOS logic sensitivity

Validated in full system tests

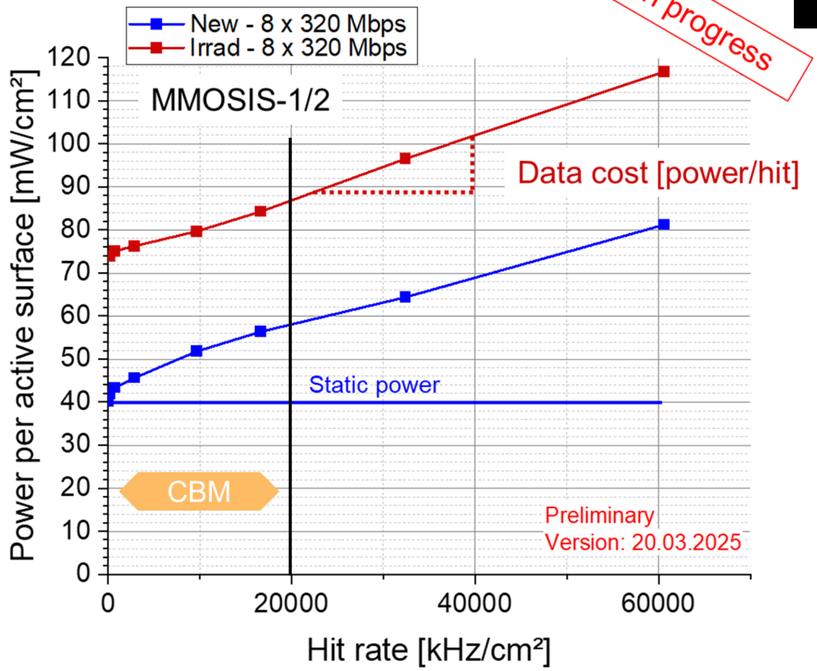


≲ 100 mV voltage fluctuations on VDD every frame (5 µs)



≲ 2x digital power increase during spills, TID effects

Work in progress



Challenge: Powering

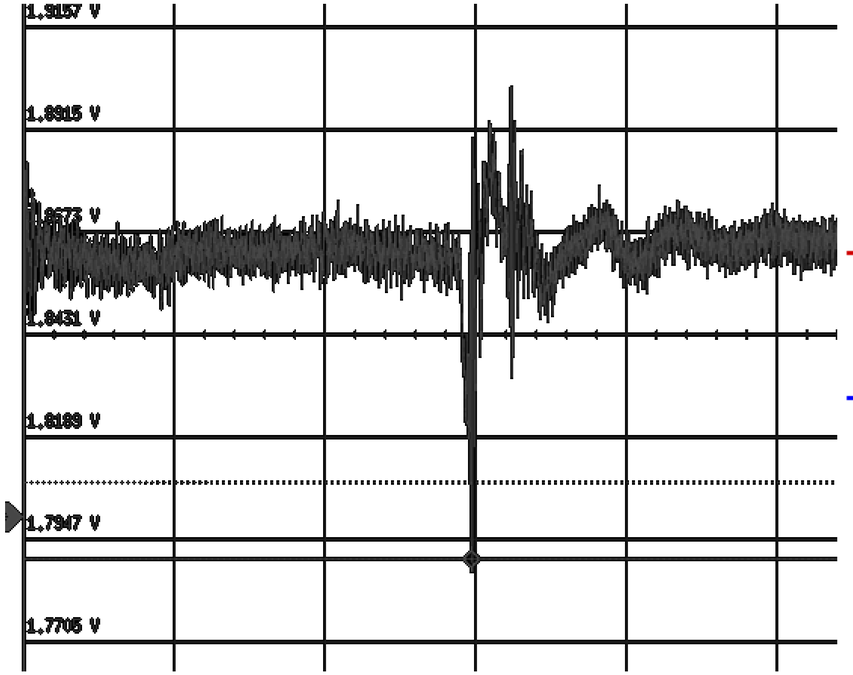
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→ Static and dynamic voltage drops on all time scales

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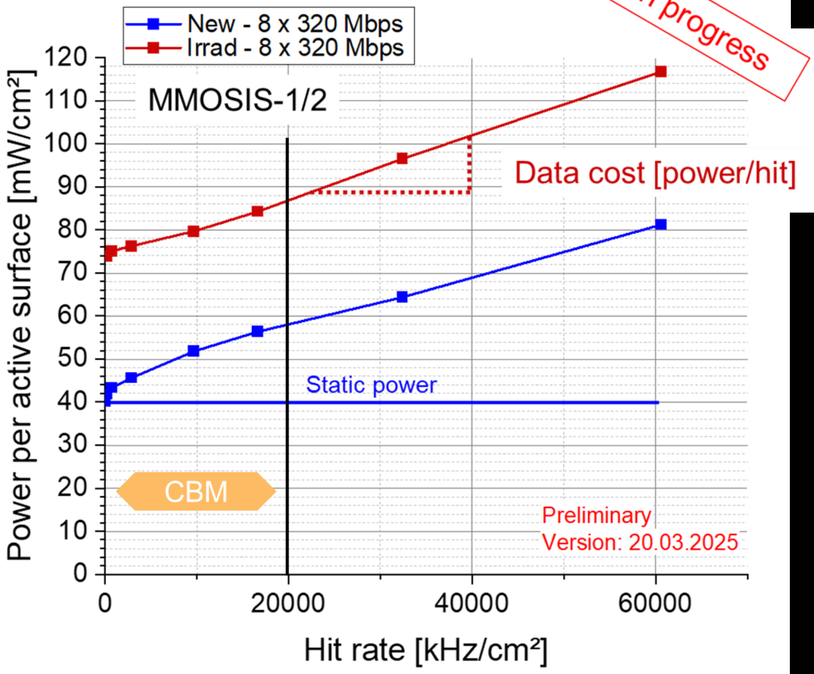
Validated in full system tests

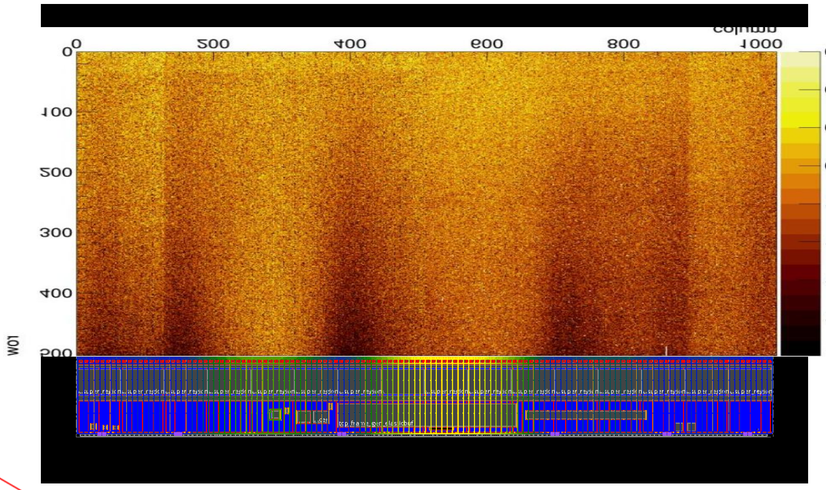
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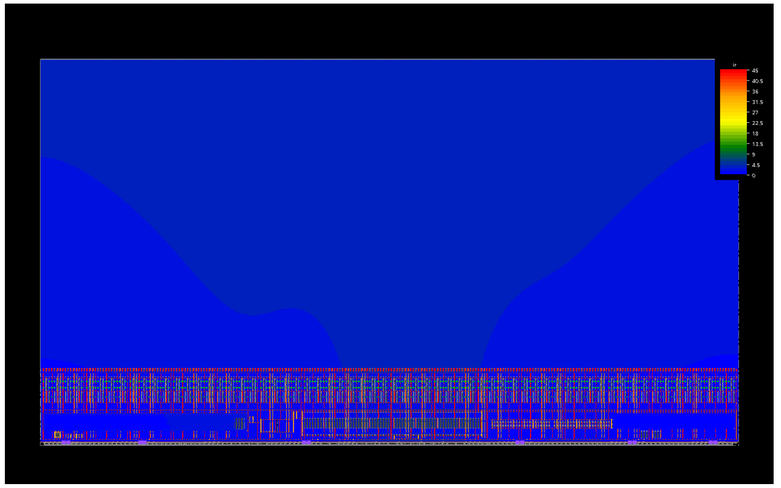
≲ 2x digital power increase during spills, TID effects

Work in progress





~4x improvements in analog power grid from M1 to M2



Powering System

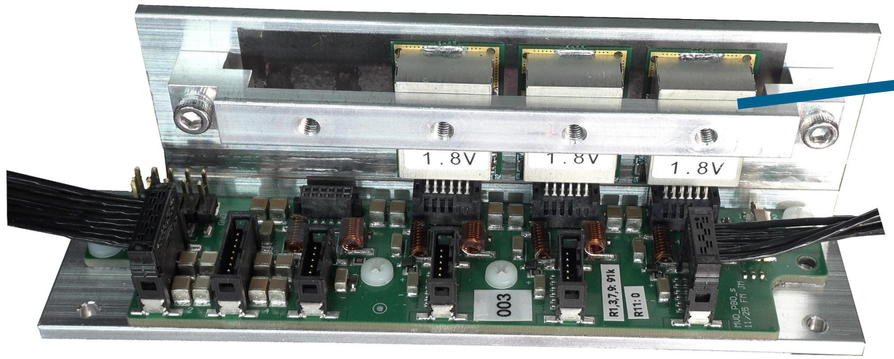
Power: FEASTMP DC/DC converters in vacuum

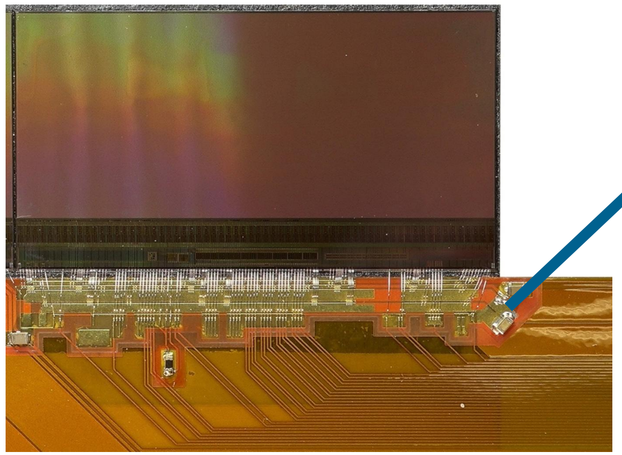
→ Main power supplies 30 m away, custom switch box for >160 rails

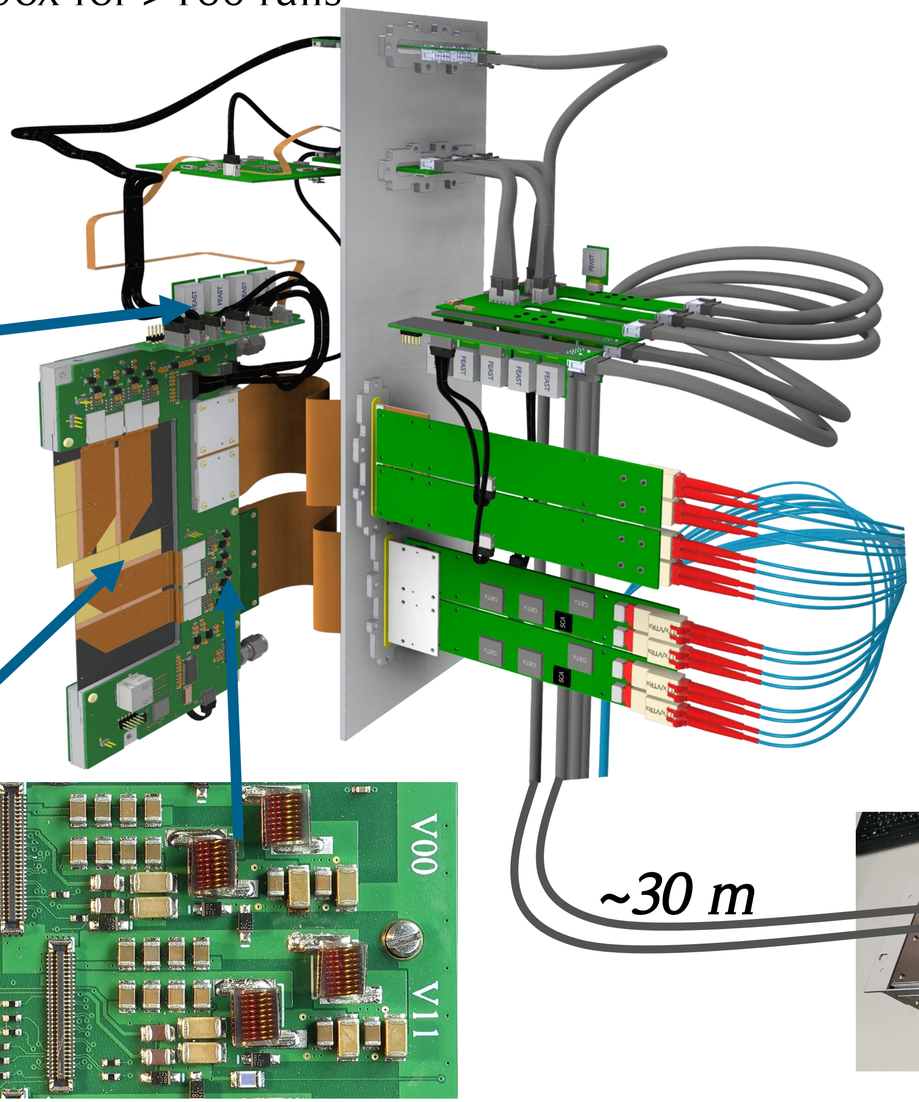
→ Analog, digital power separated

→ LC decoupling on FEBs

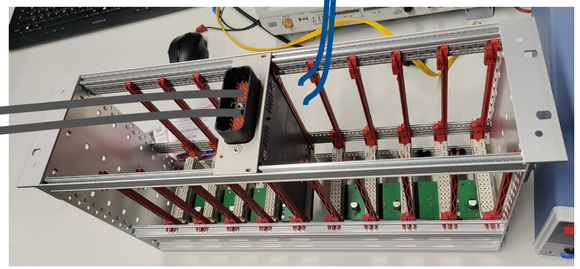
→ Capacitors close-by the sensor











Challenge: Data Integrity

High-speed signals over imperfect transmission path

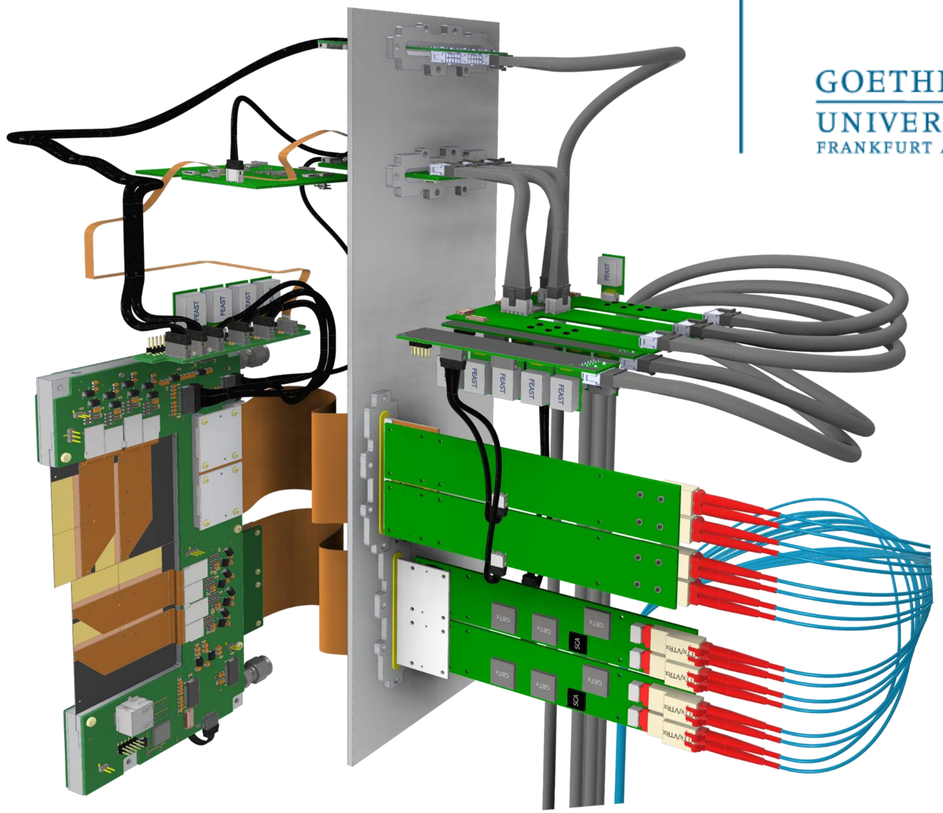
→ 320 Mb/s SLVS, up to 90 cm FPCs + PCBs

→ Three connectors (discontinuities) in data path

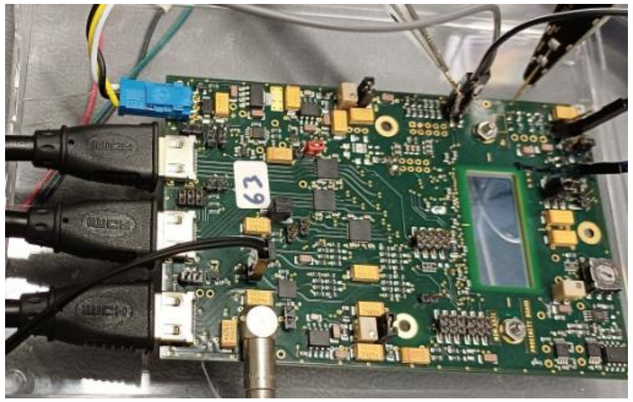
→ Single-layer, unshielded FPCs

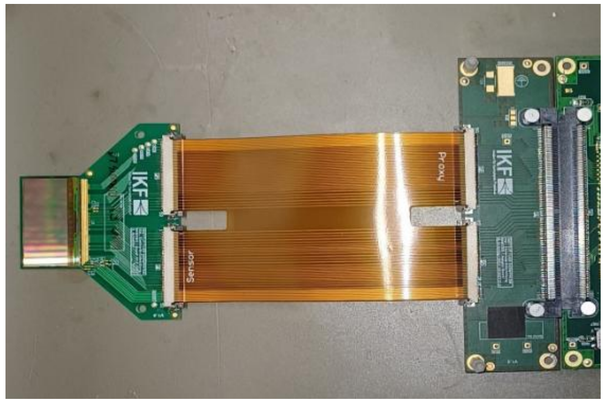
→ Static and dynamic voltage drops

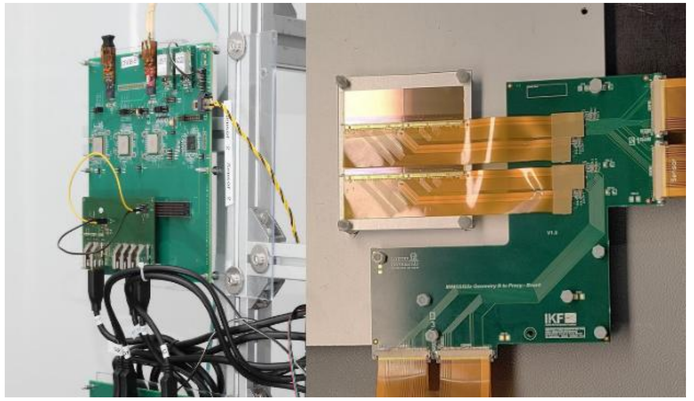
Validated in full system tests

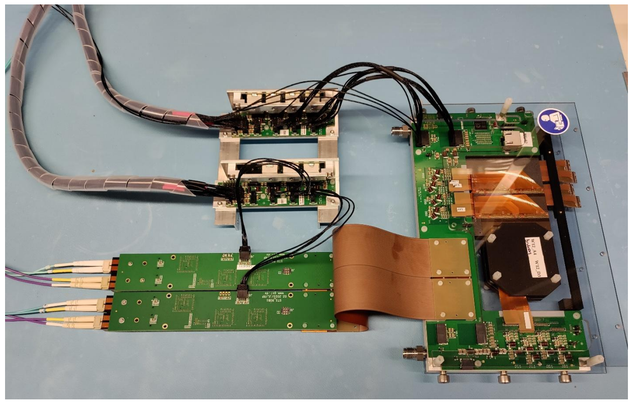


Ideal operating conditions → **MVD operating conditions**







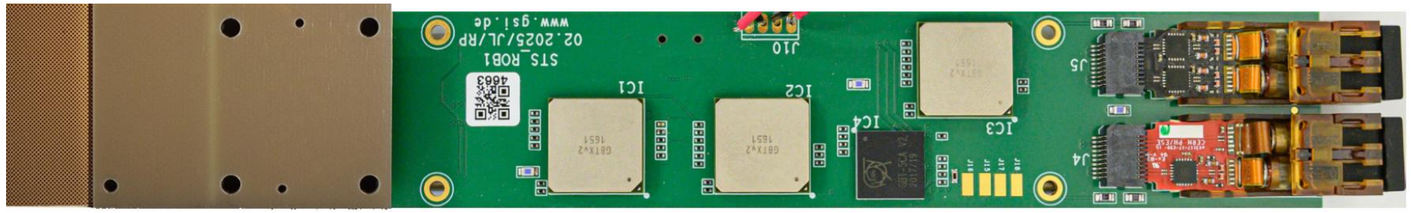


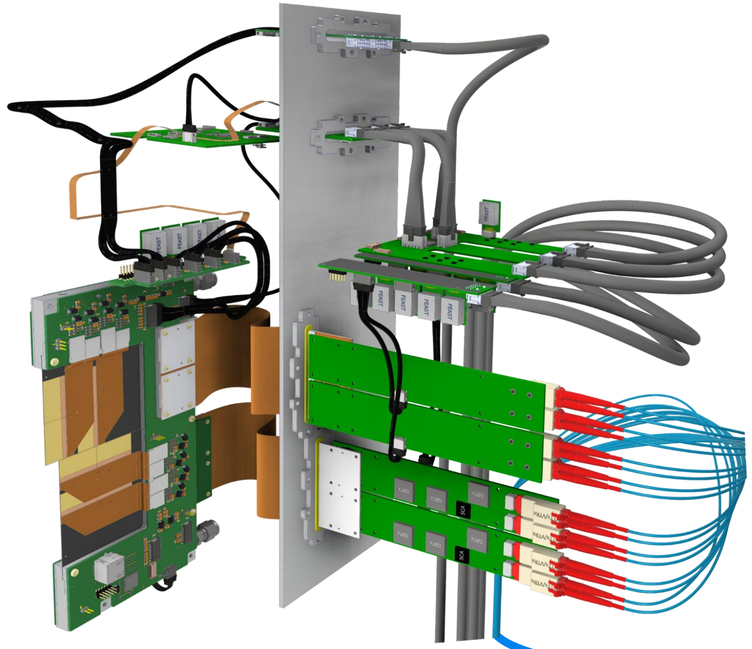
Data Path, DAQ Interface

Data aggregator/readout board based on GBTx, VTRx/VTTx

→ Bidirectional timing/control & data transport (14.4 Gbps)

→ Interfaces FEBs and Common Readout Interface (CRI)

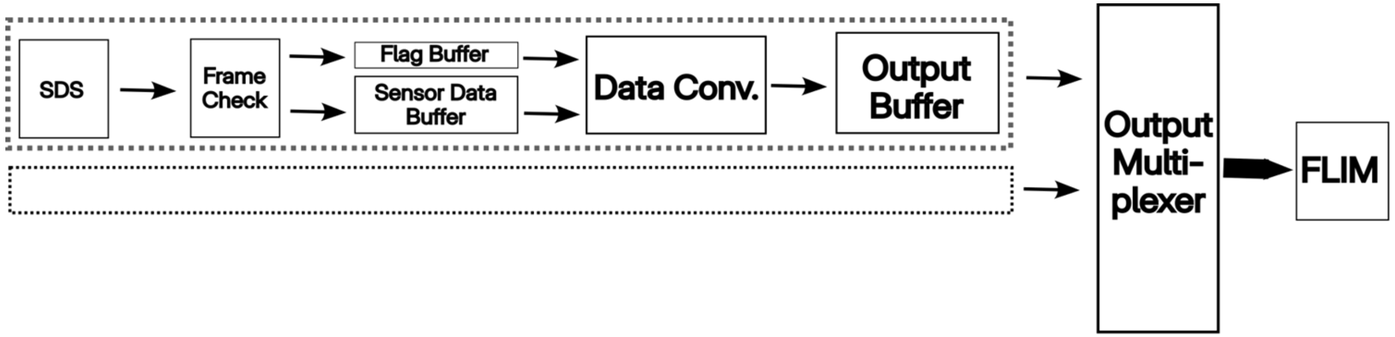


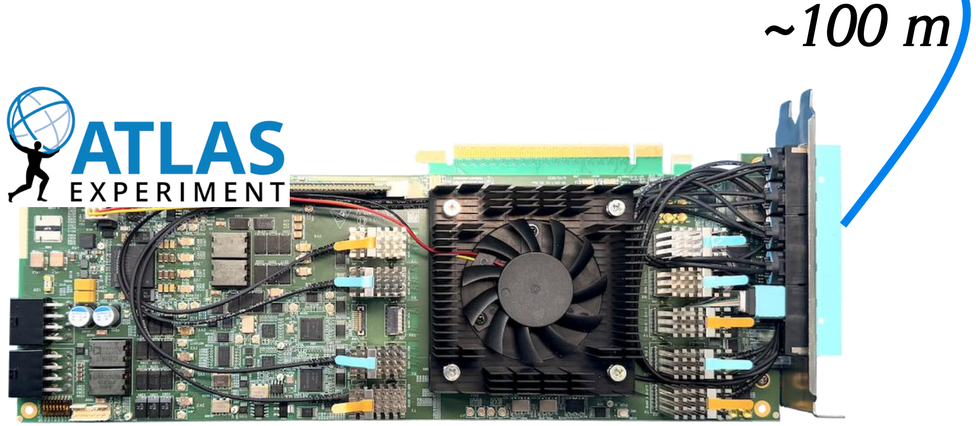


Free-streaming DAQ to FPGA-based PCIe Common Readout Interface (CRI)

→ Experimental validation in mCBM@SIS18

→ ATLAS FLX-155 (join main production)



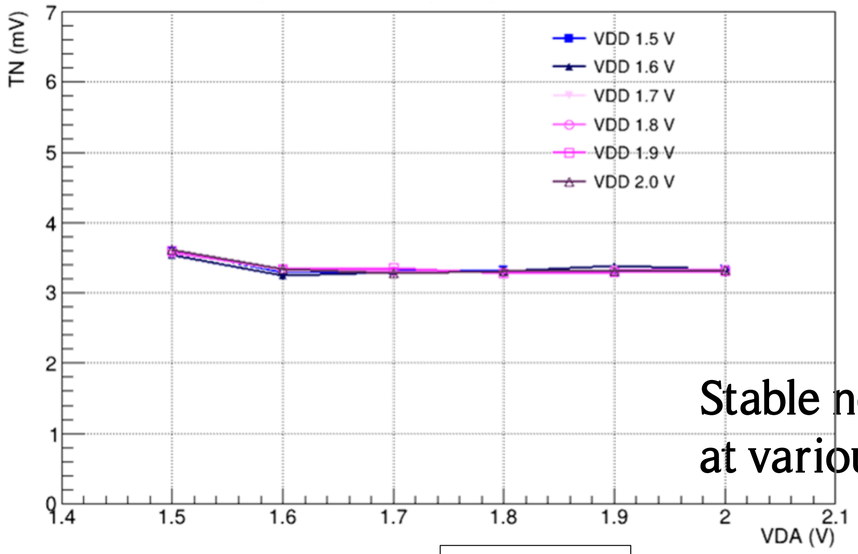


System-Level Validation

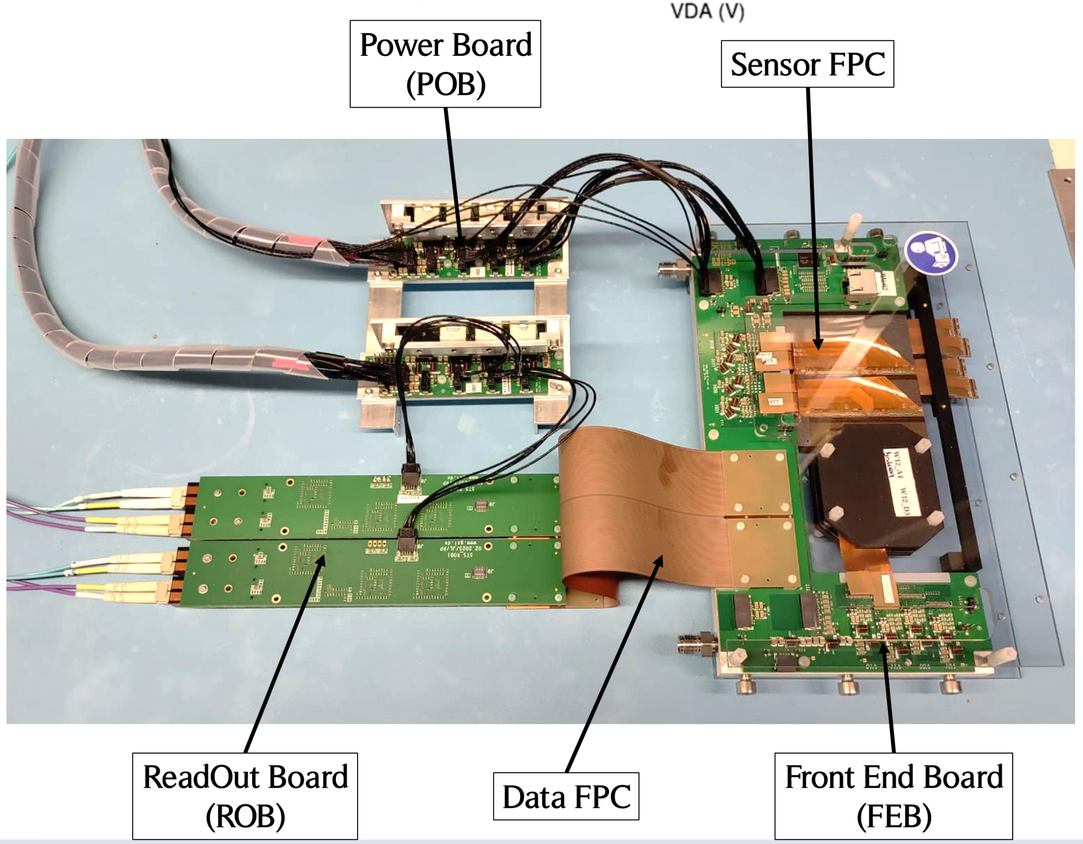
No additional noise by detector PDN

→ FEAST switching noise, PDN impedance, power decoupling

→ Stable performance for various supply voltages



Stable noise performance at various voltages



System-Level Validation

No additional noise by detector PDN

→ FEAST switching noise, PDN impedance, power decoupling

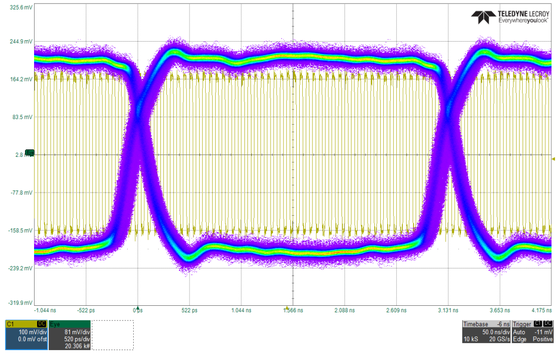
→ Stable performance for various supply voltages

Data integrity and noise performance with close-to-final FEE

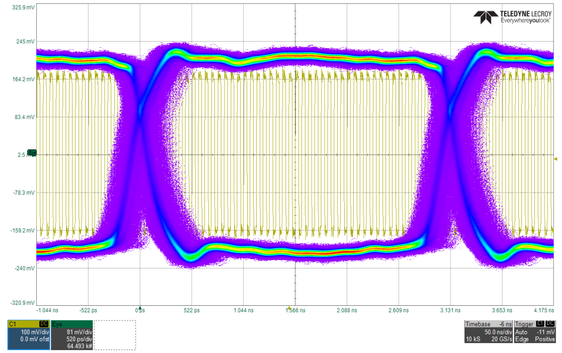
→ Eye opening ~ 75%, cross-talk visible, but negligible

→ Expected further improvements in final sensor

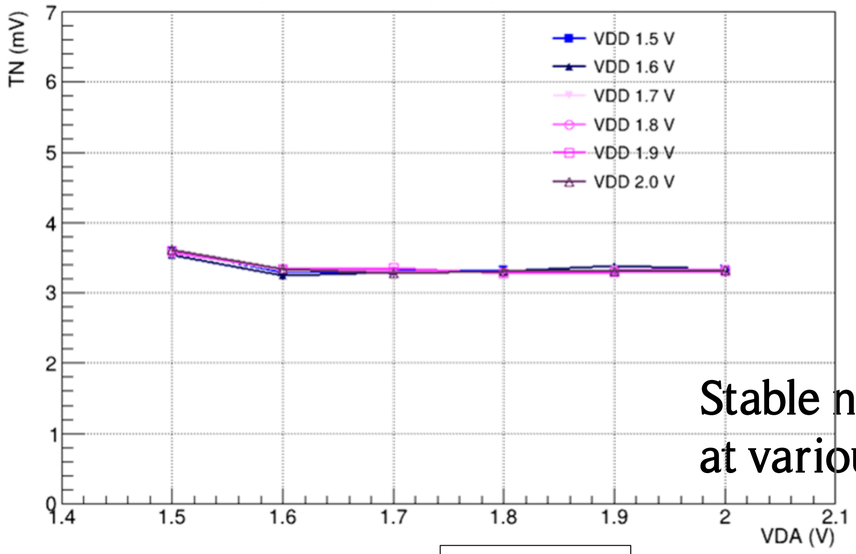
System is under control, final sensor is being submitted



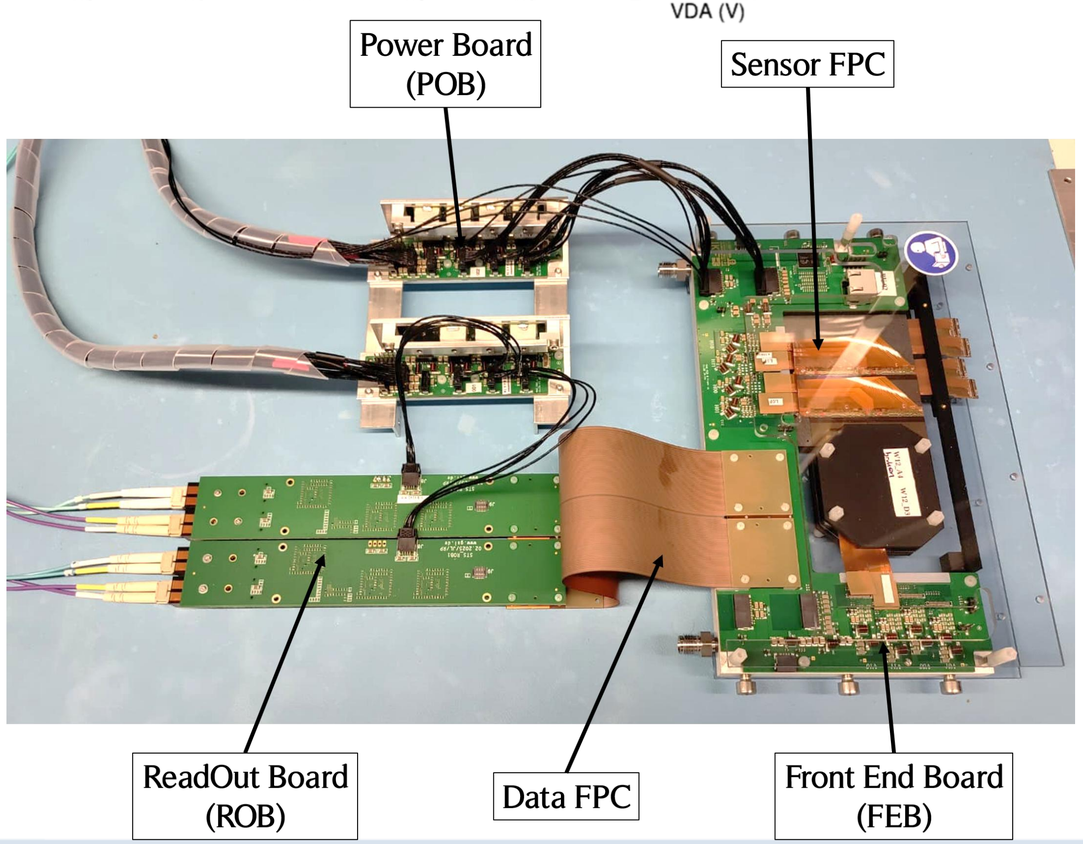
Sensor in reset



High load from pulsing



Stable noise performance at various voltages

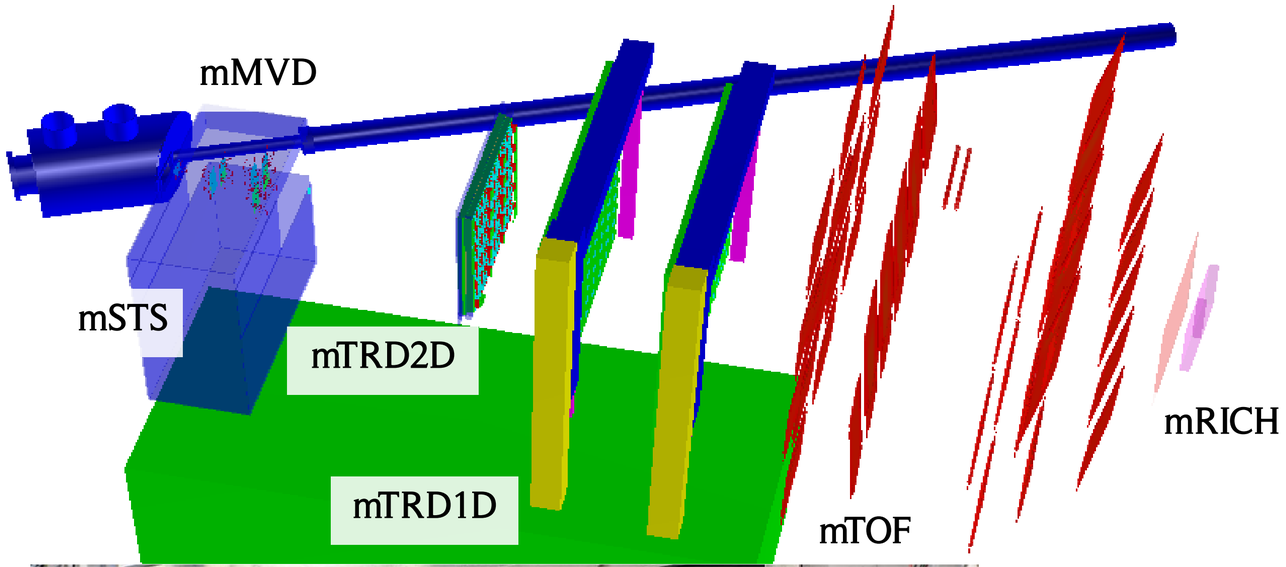


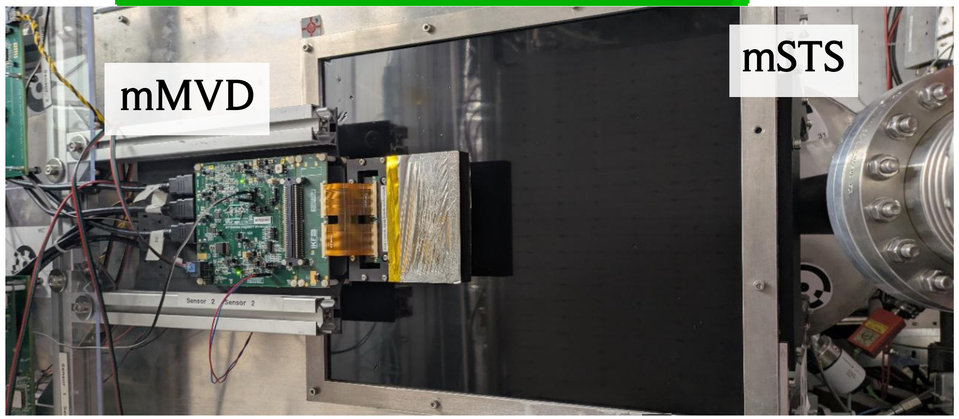
mMVD: Synchronized with mCBM DAQ

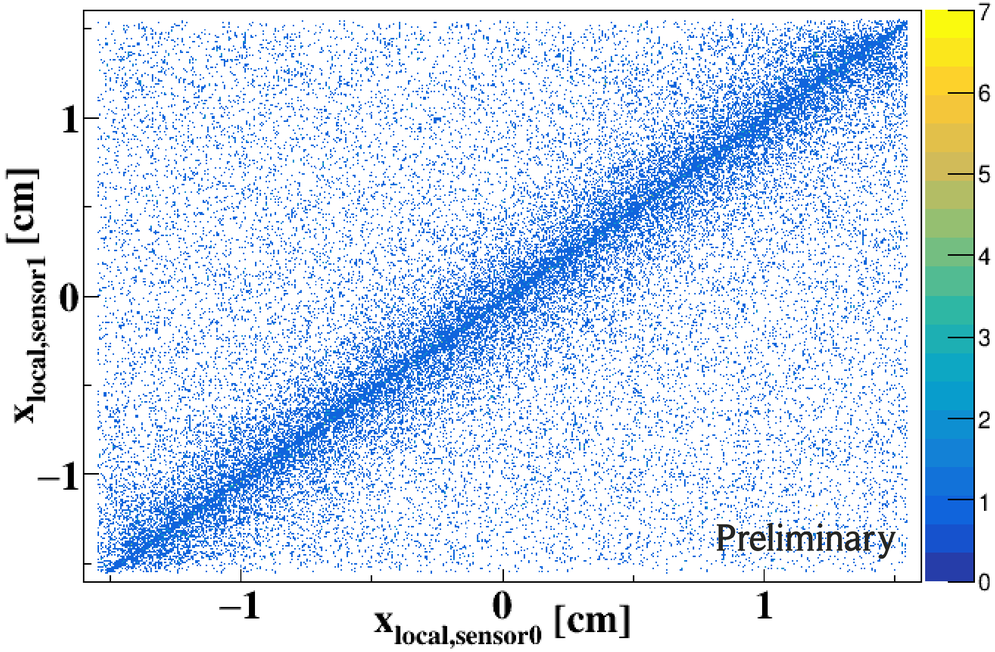
mCBM@SIS18: Demonstrator ot free-streaming DAQ

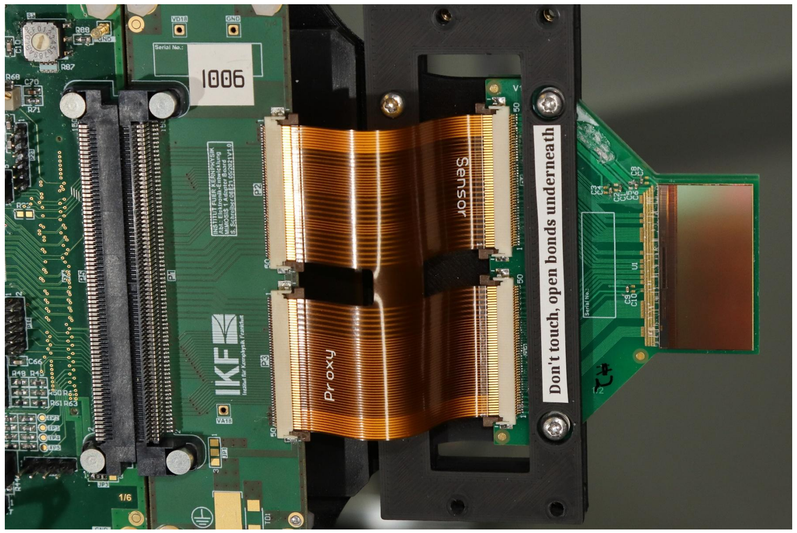
→ mMVD: 2 MIMOSIS back-to-back (μ-tracking)

→ Synchronized data readout validated









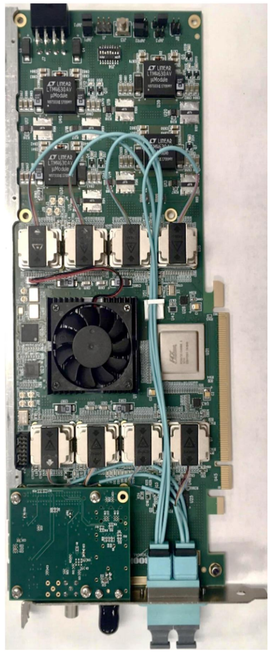
Detector Control System (DCS)

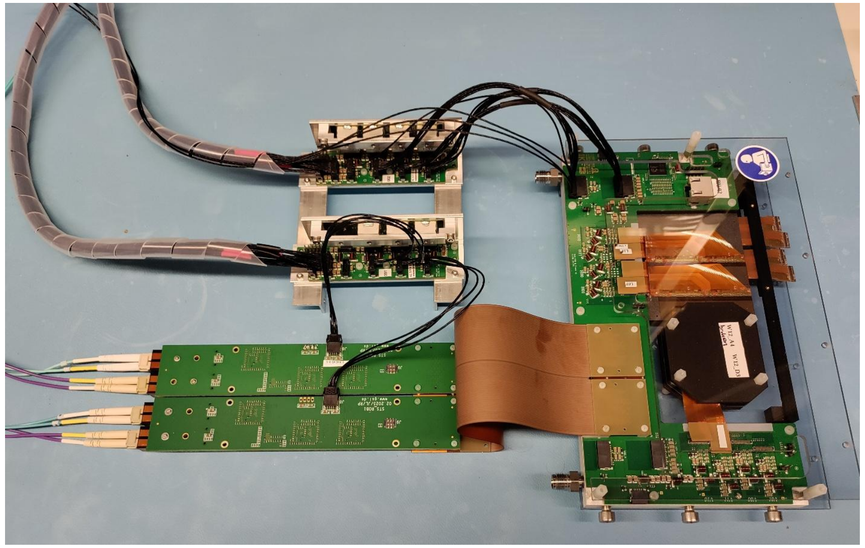
Sensor/DCS architecture implemented and running

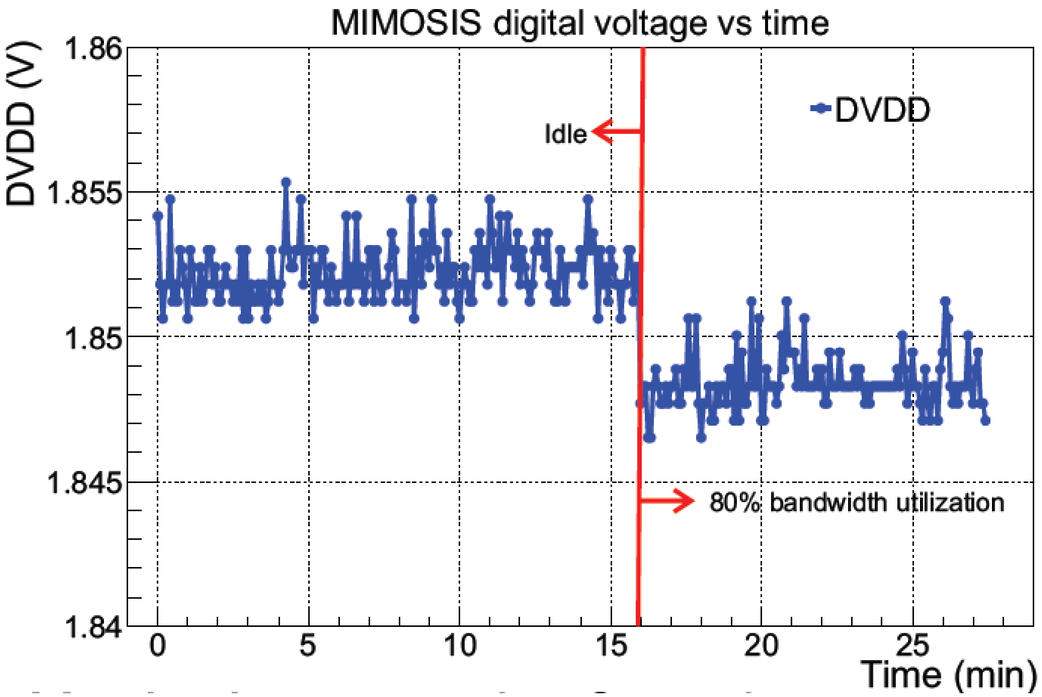
→ Python-based CRI DCA interface (GBT-SCA)

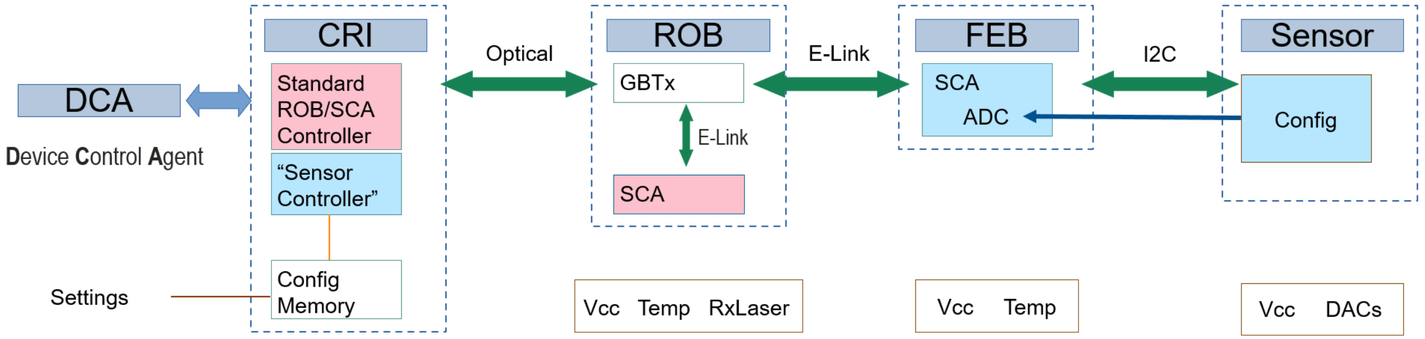
Automatic (CRI-based), EPICS interface in progress

→ Standardized components (LV, cooling, …) to be done





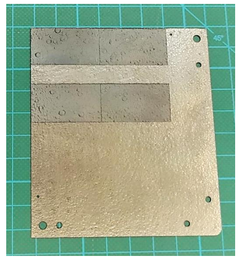




The Detector Module


Heat Sink

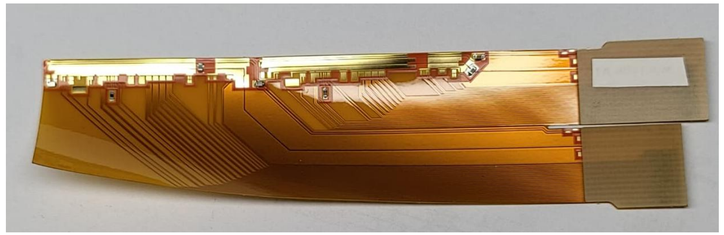
+


Carrier

+


Sensor

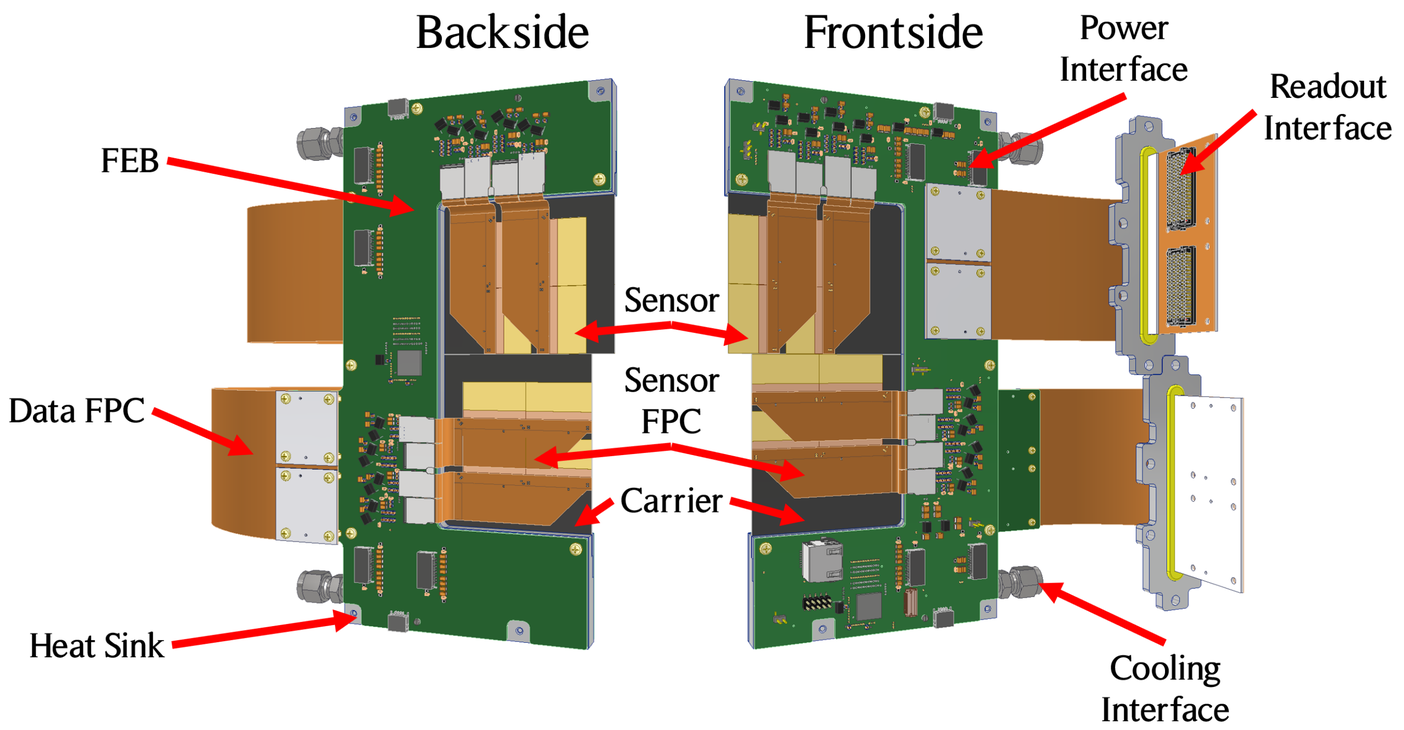
+


FPC

+

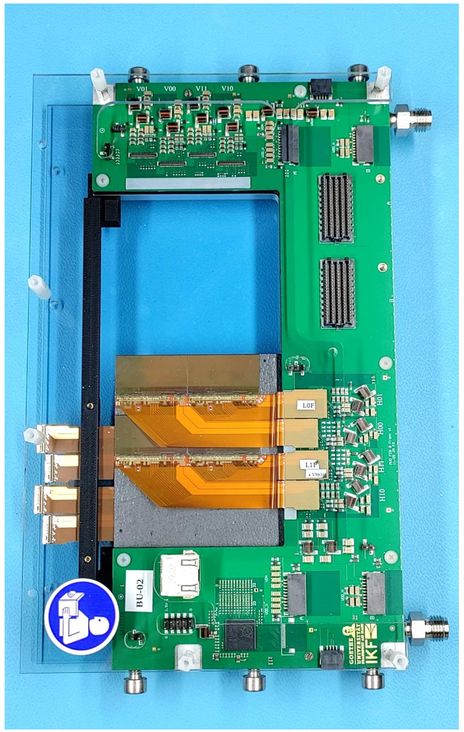

FEB

+ glues, tapes, wire-bonding. …



=





Two station geometries in the MVD. Focus today on small stations.

Cooling and Mechanics

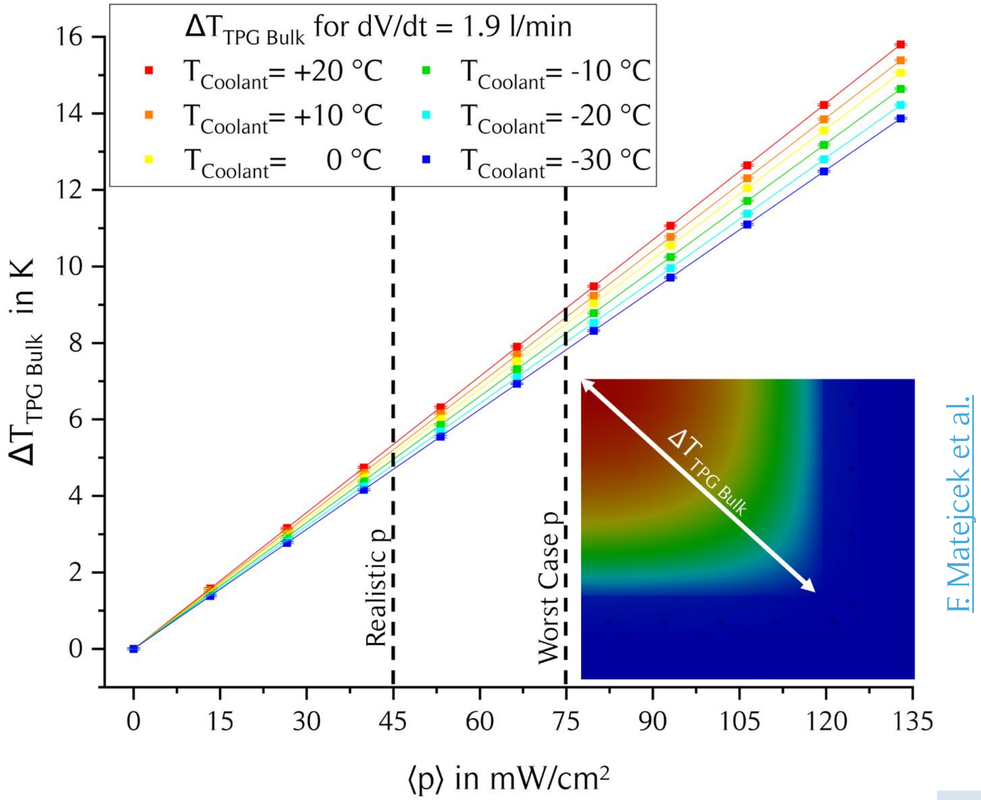
Two-stage cooling

→ Conductive (low-mass) in acceptance

380 µm Pyrolytic Graphite

→ Water-based cooling in periphery ($T_{coolant}$ ~ 5 °C)

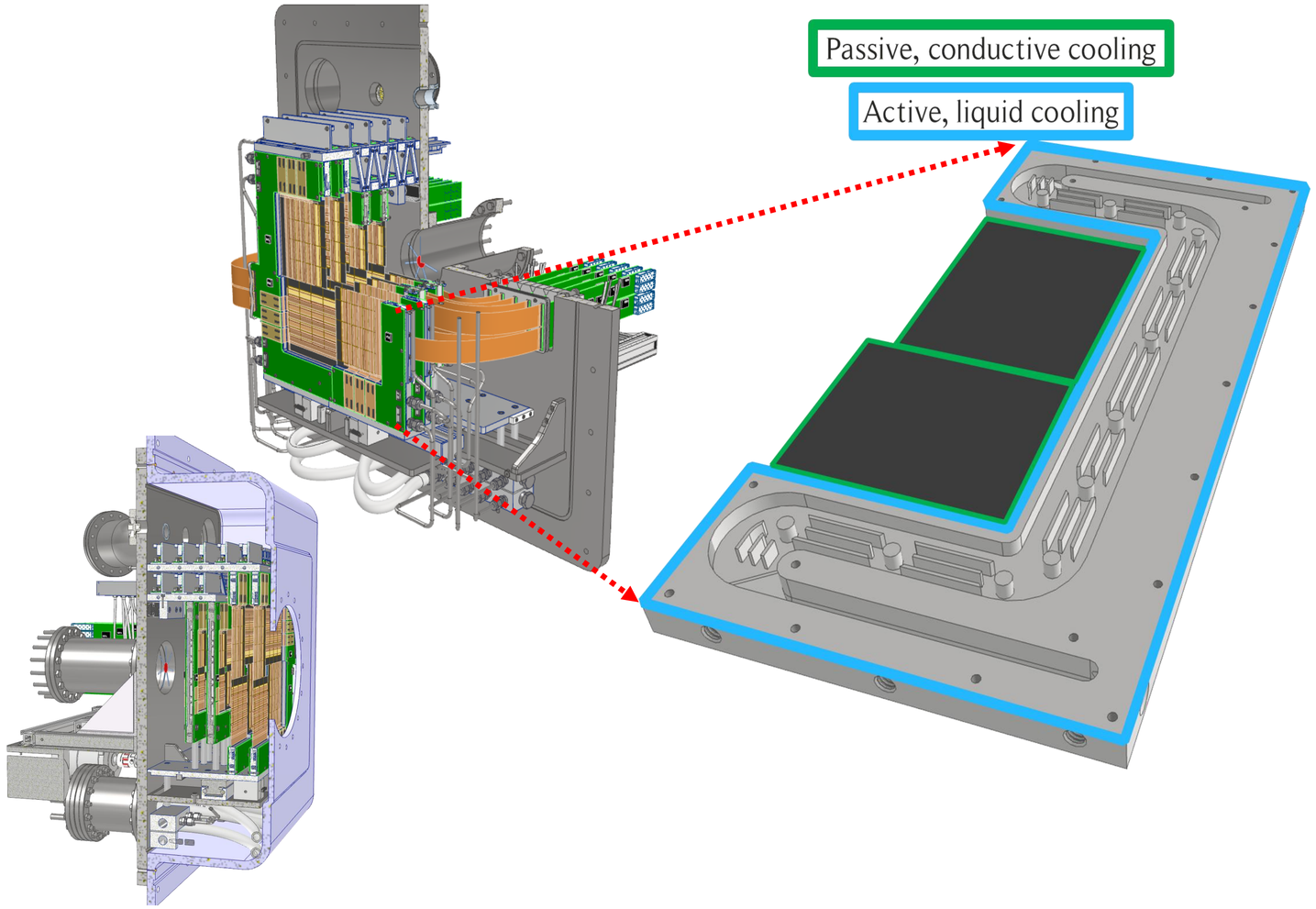
Heat sinks for heat evacuation and mechanics



C-shaped detector half-stations

→ Heat sinks as mechanical frame

→ System mounted to vacuum flange



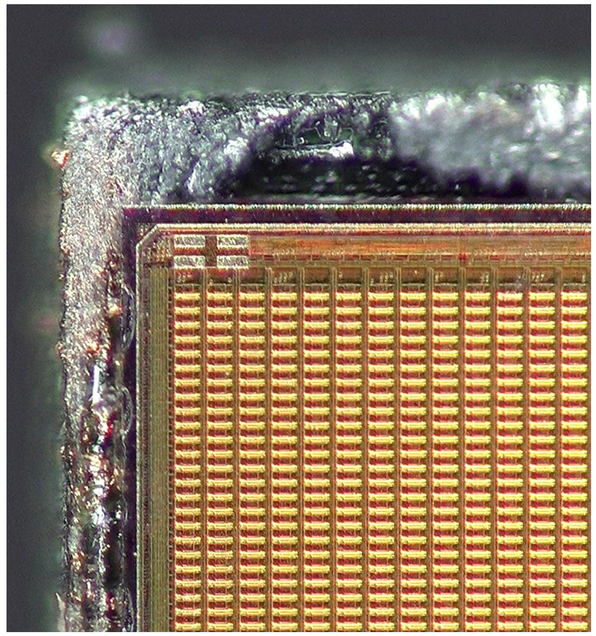
Die Bonding on TPG

CMOS MAPS glued onto carriers

→ Polished, 3D – structured, coated and activated TPG sheets

→ 35 µm Epo-Tek 301-2 (low-viscosity, room-T curing epoxy)

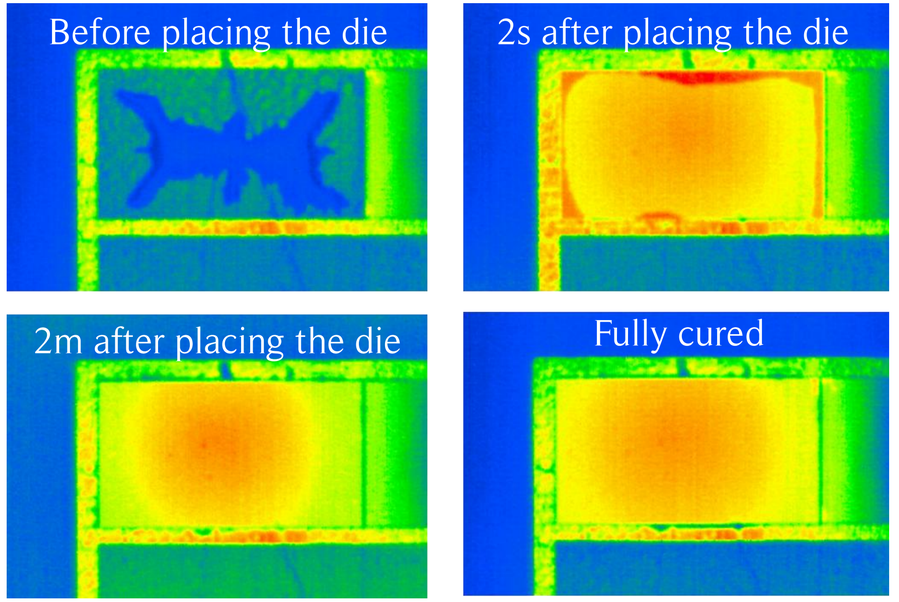
→ Star pattern for optimal glue spread



30-40 µm deep "hatches" for sensor placement, with separation bars



IR photography of optimized glue pattern on PG



Double-Sided Module Integration

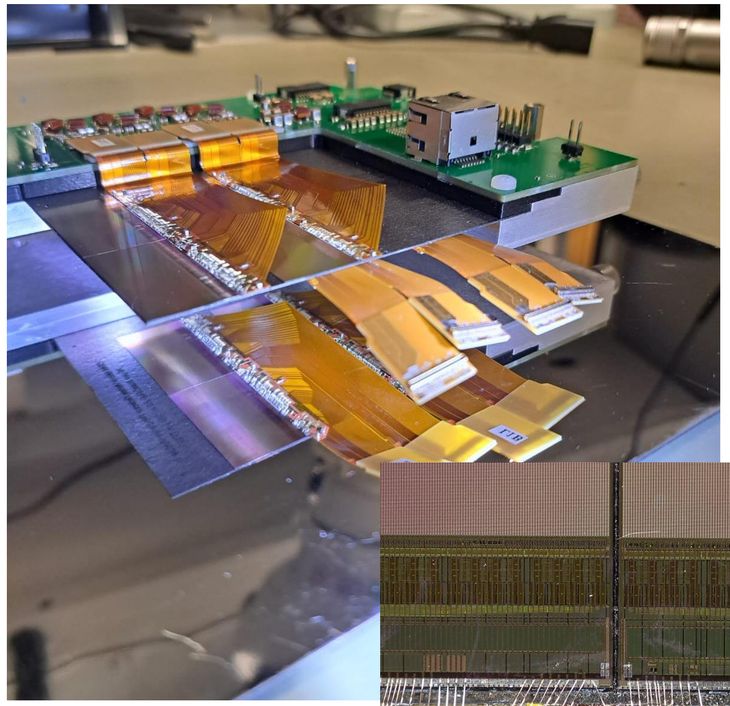
High thermal conductivity Pyrolytic Graphite carrier

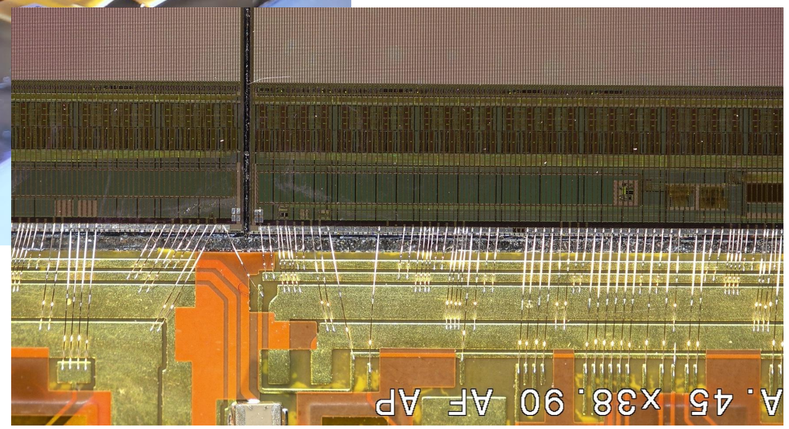
→ Jig for local mechanical support

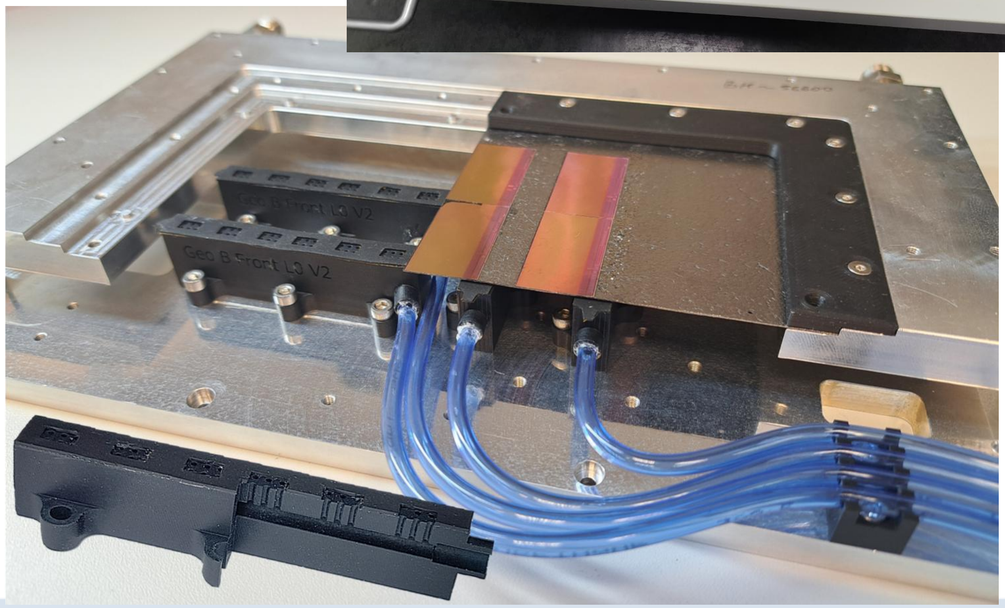
→ Full-automatic wire-bonding

PG for Day-1 MVD in house









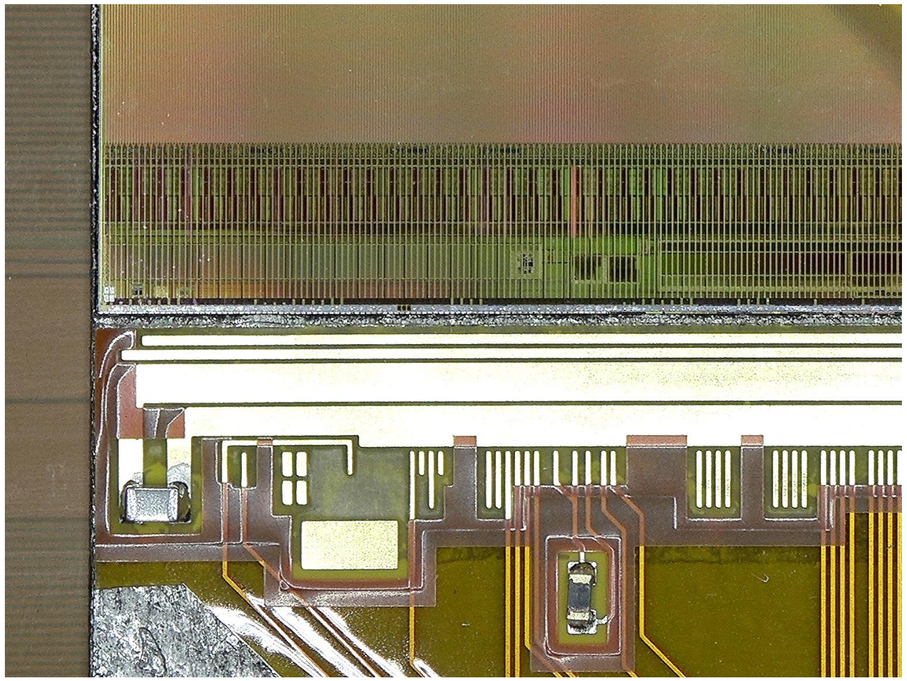
Metrology

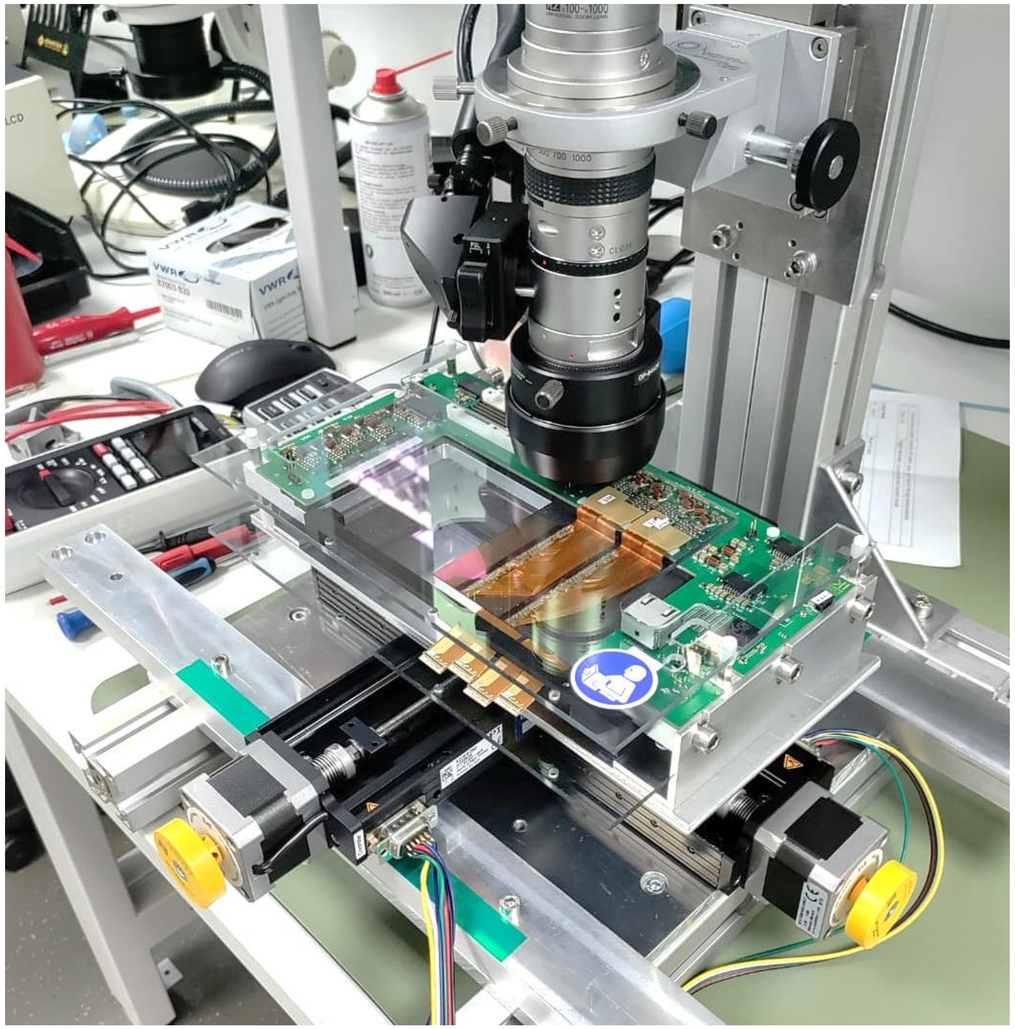
Measurement of sensor fiducials w.r.t. fiducials on carrier, heat sink

→ xy table, z-position by focus variation

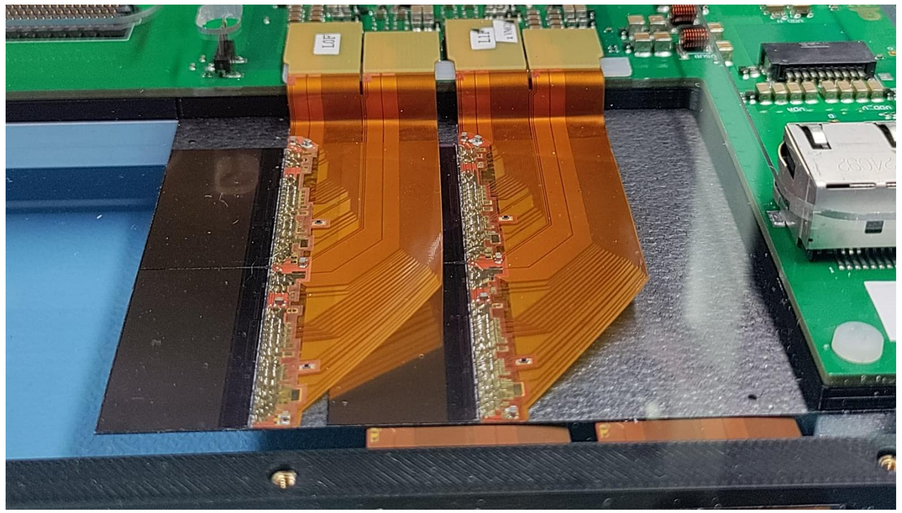
→ Half stations are functional units

→ Dedicated infrastructure is being set up

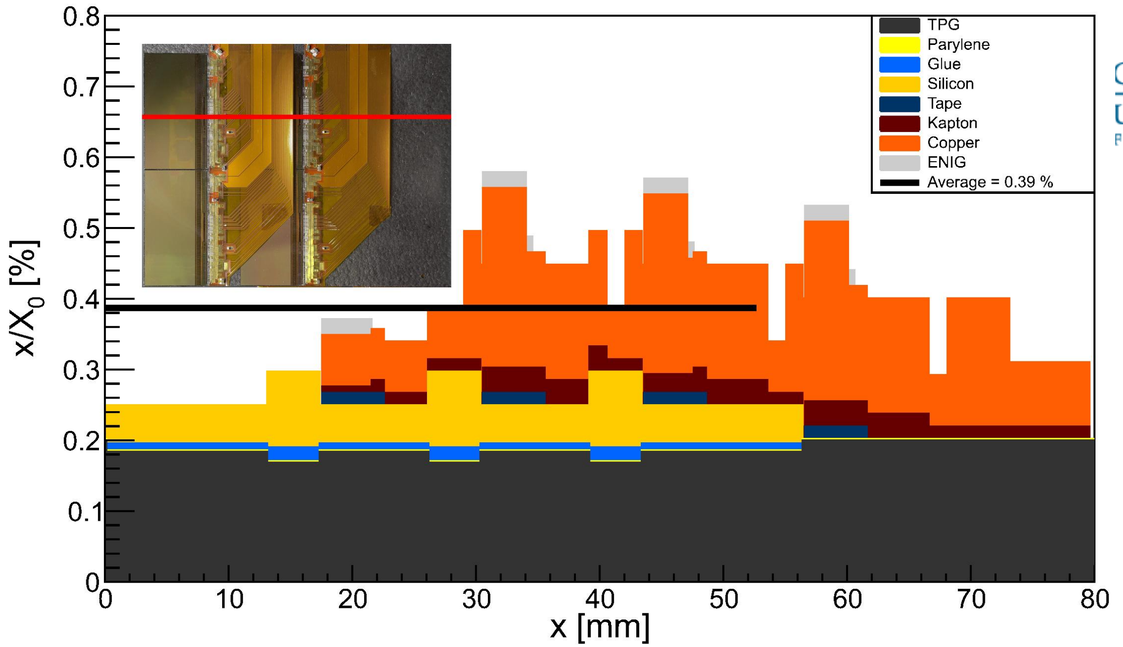




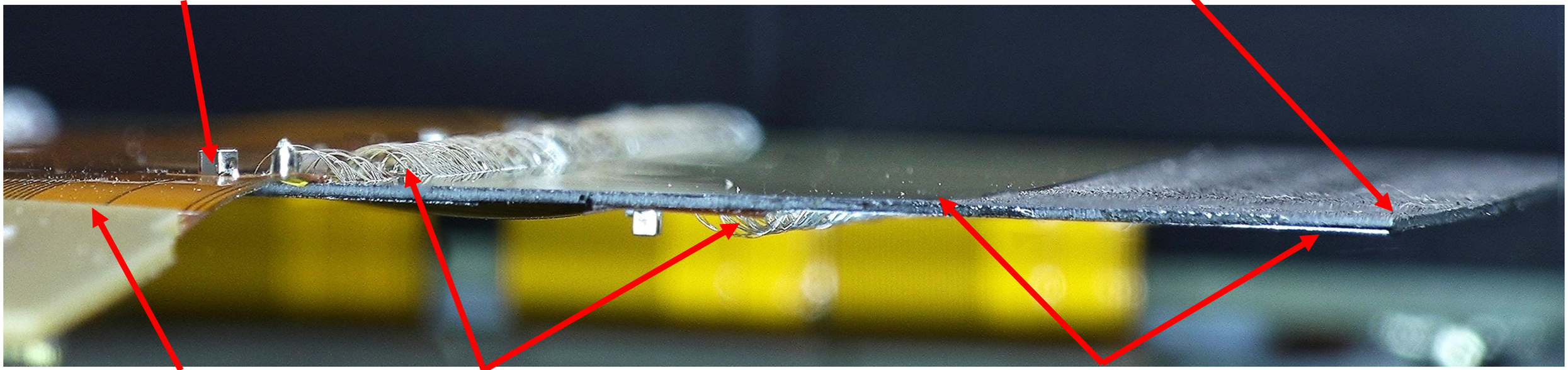
Material Budget



0402 capacitor



Pyrolytic Graphite (380 µm)



FPC (110 µm)

Wire bonds

Sensors (50 µm)

Material Budget Improvements?

To 0.3% X_0: Reduced carrier thickness 380 µm → 250 µm

→ First prototype sheets already in house, FAI passed

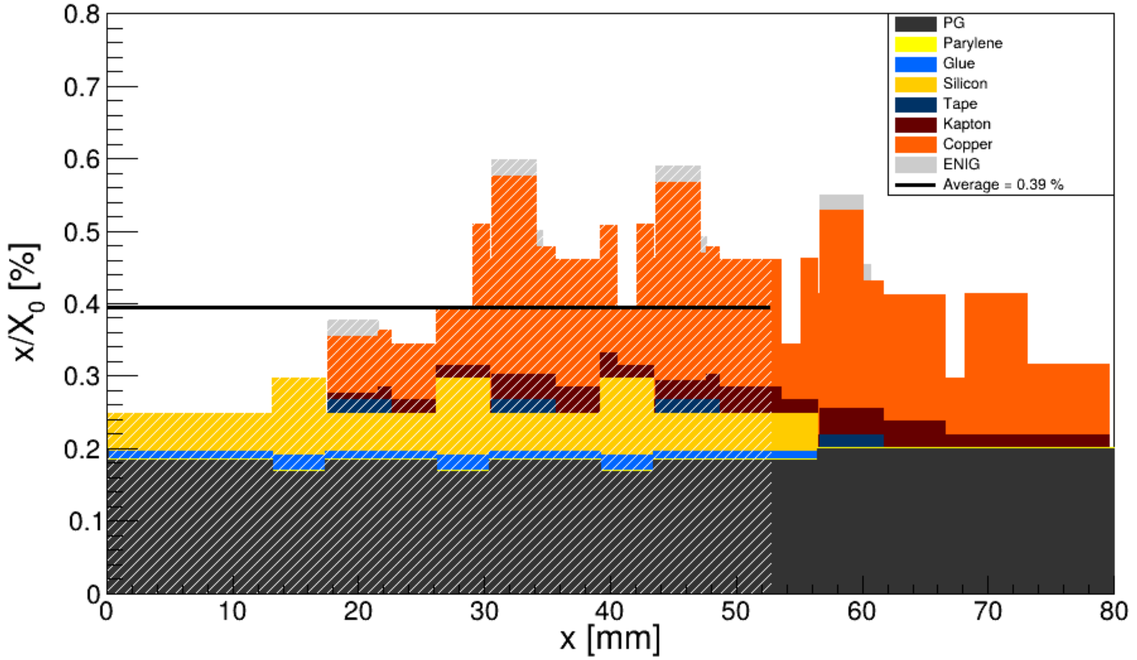
→ All standard tooling & jigs can be reused

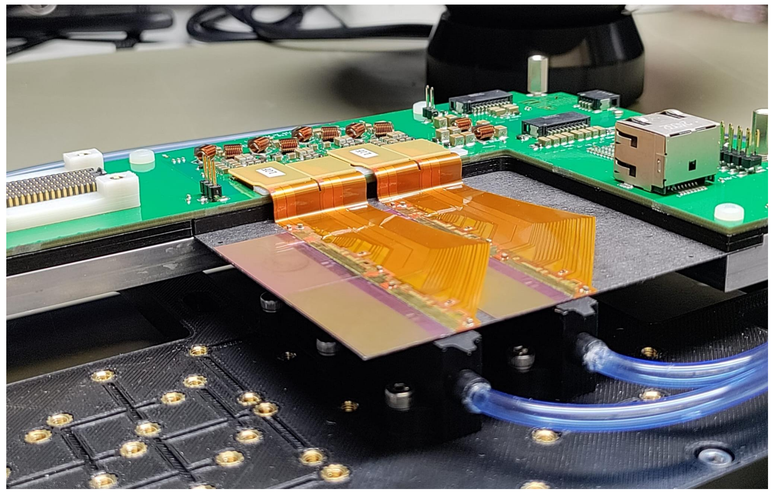
To 0.25% X_0: Al FPCs (LTU Kharkiv, FBK Trento)

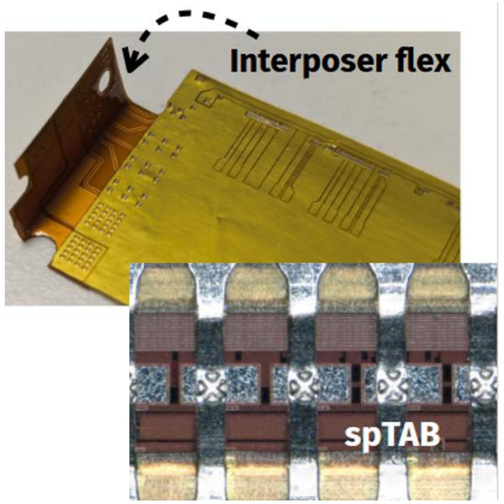
→ Technologically feasible, but some caveats

- Tight bends (Cu interposer)
- Technology choices: Single/double-layer, spTAB/wire-bonding
- Requirement: capacitors (ENIG + solder, conductive glue, …)

→ A lot of pioneering work by ITS2, Mu3e







Al FPCs at Mu3e

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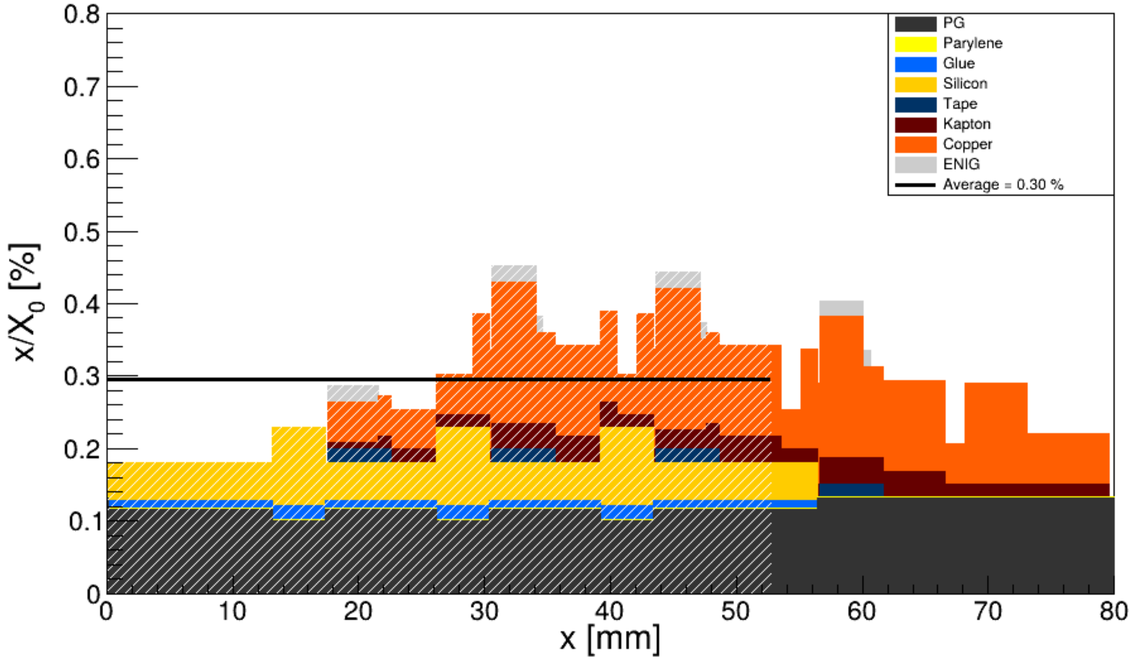
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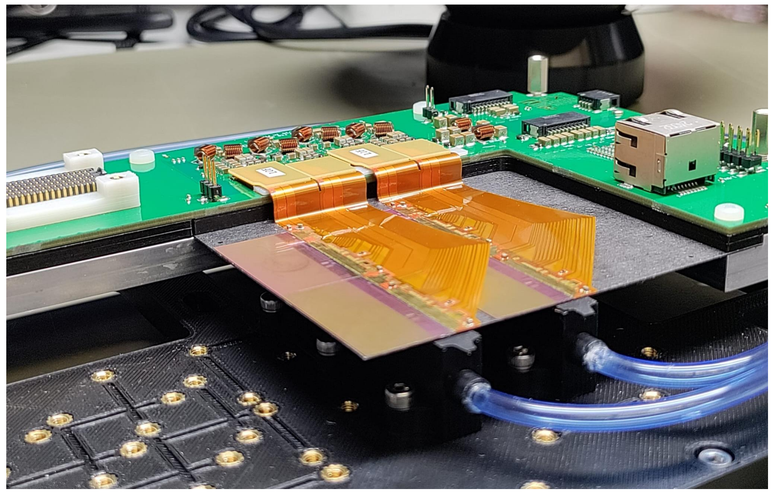
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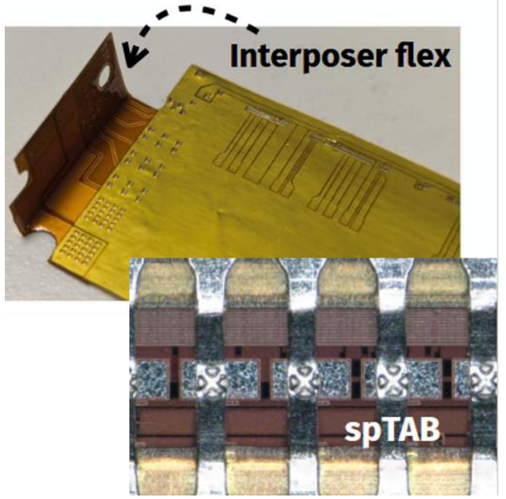
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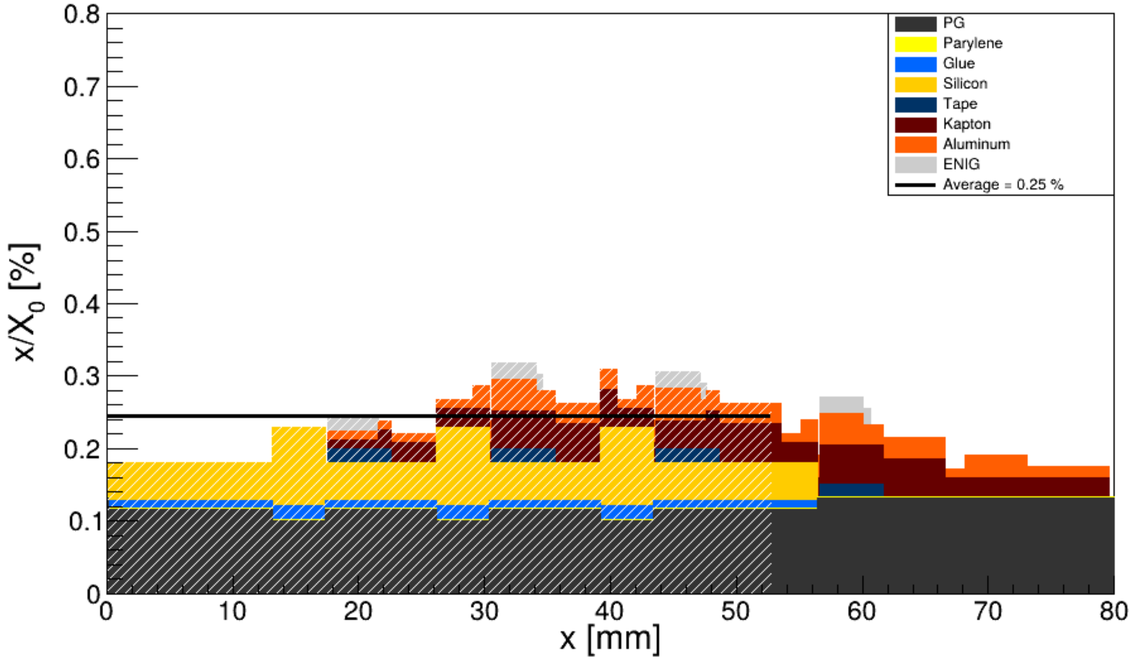
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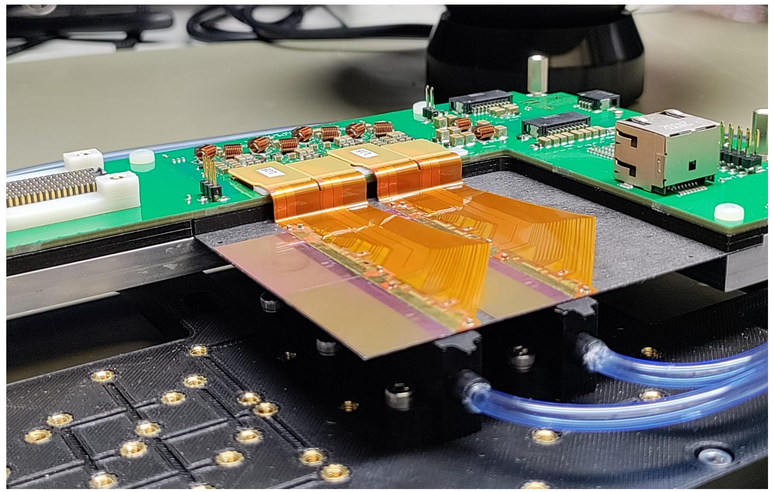
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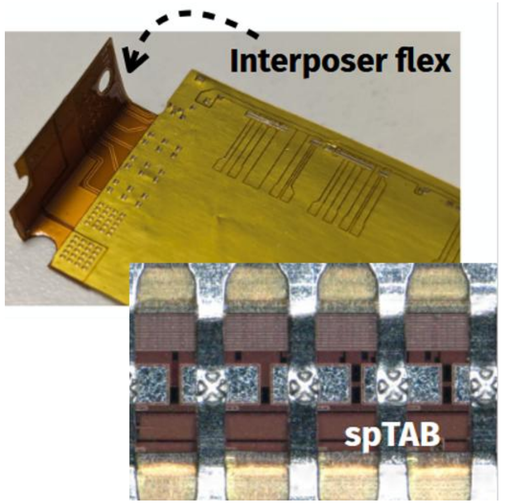
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Al FPCs at Mu3e

Summary

MVD Pre-production ongoing

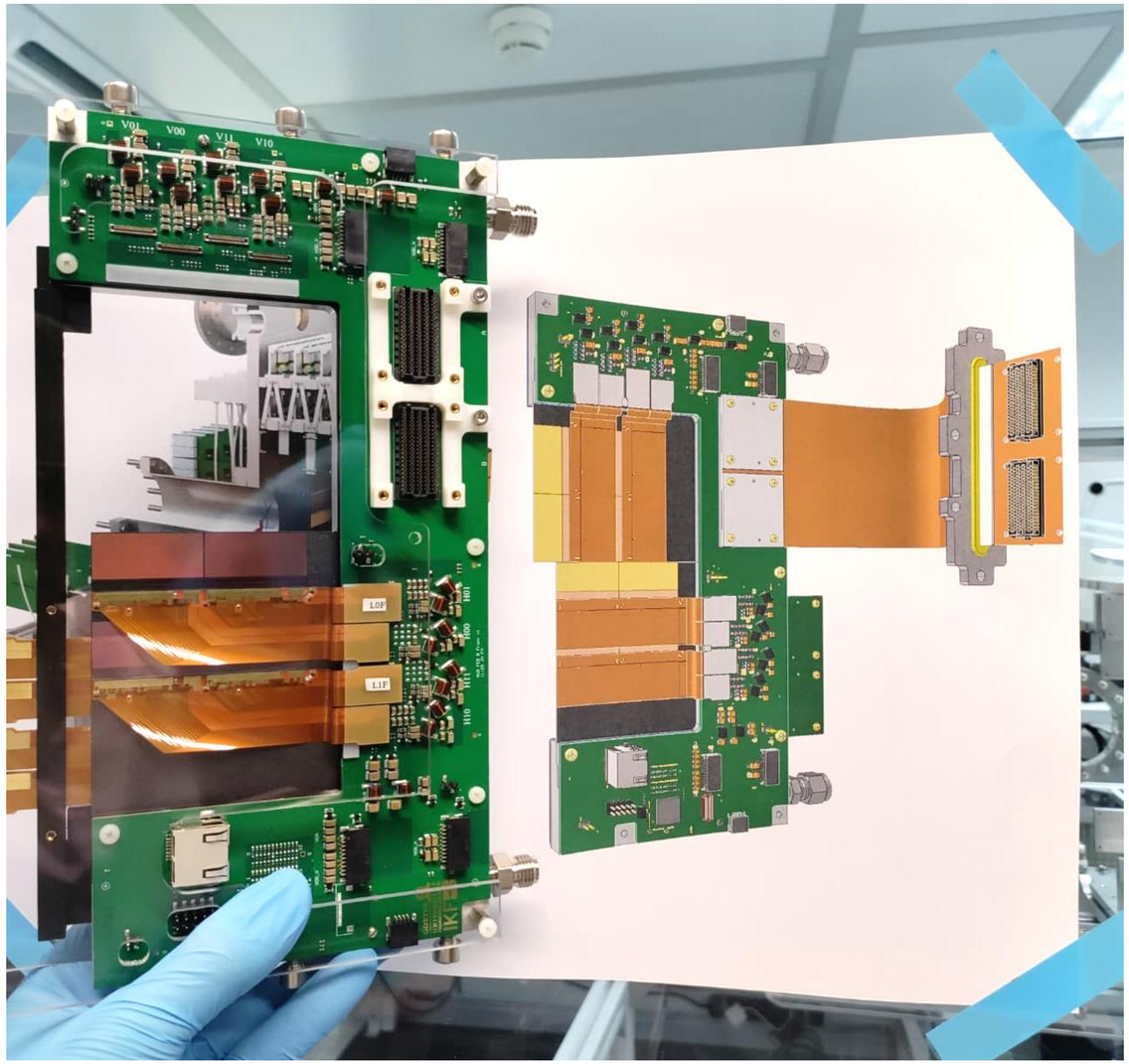
→ Successful double-sided integration

→ Final sensor Q2/2027

→ Procurement of components started

→ Full-system construction to be completed 2028

Excited for CBM 2028!



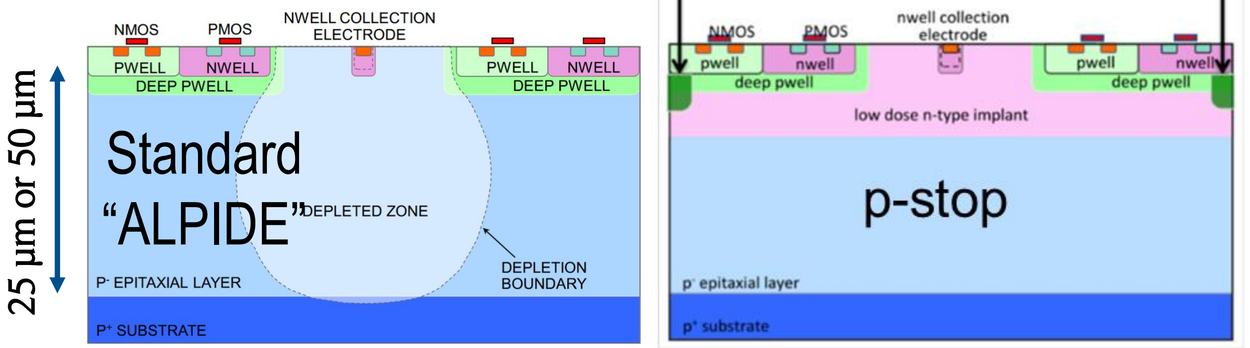
Backup

The MIMOSIS Story

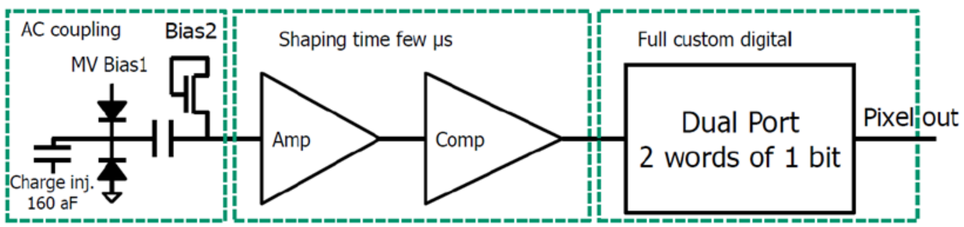
Joint venture: IPHC Strasbourg, University Frankfurt, GSI
→ Starting point: ALPIDE pixel, fully custom digital front-end

Improved radiation hardness
→ Modified epitaxial layer (“p-stop”)
→ Increased diode bias (AC-coupling)

Exploratory: Improved operation range (signal)
→ 50 µm epi thickness



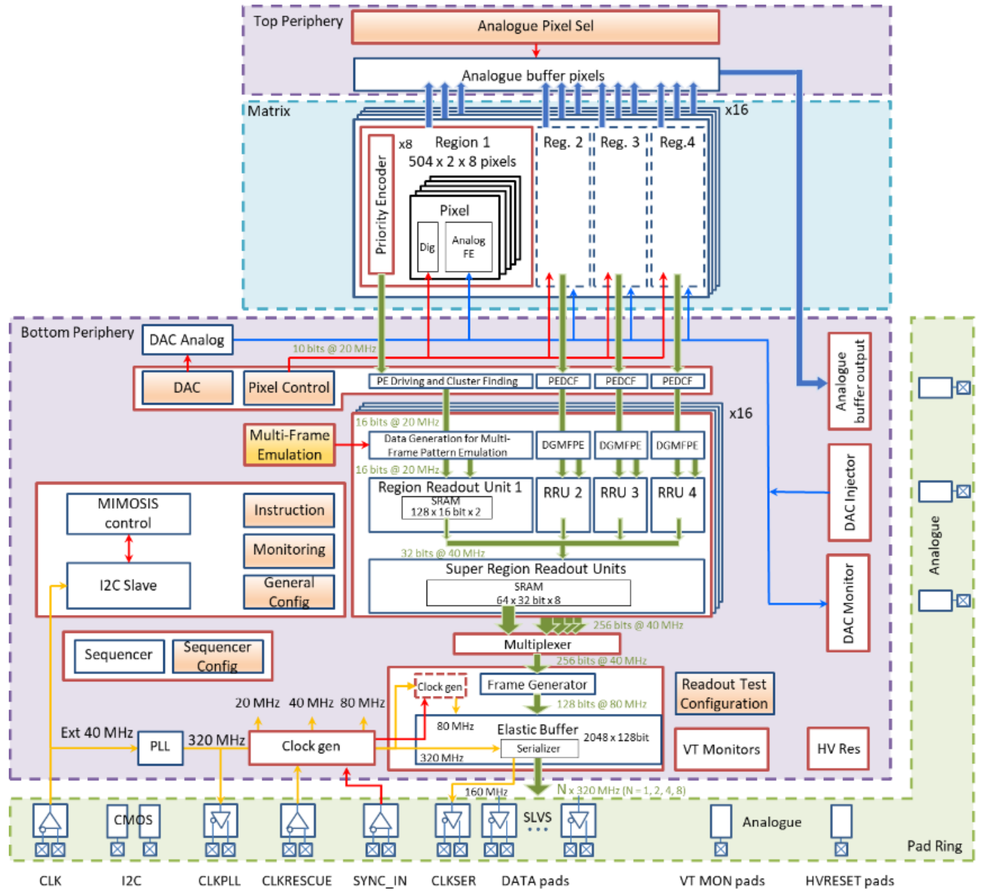
H. Darwish et al.



F. Morel

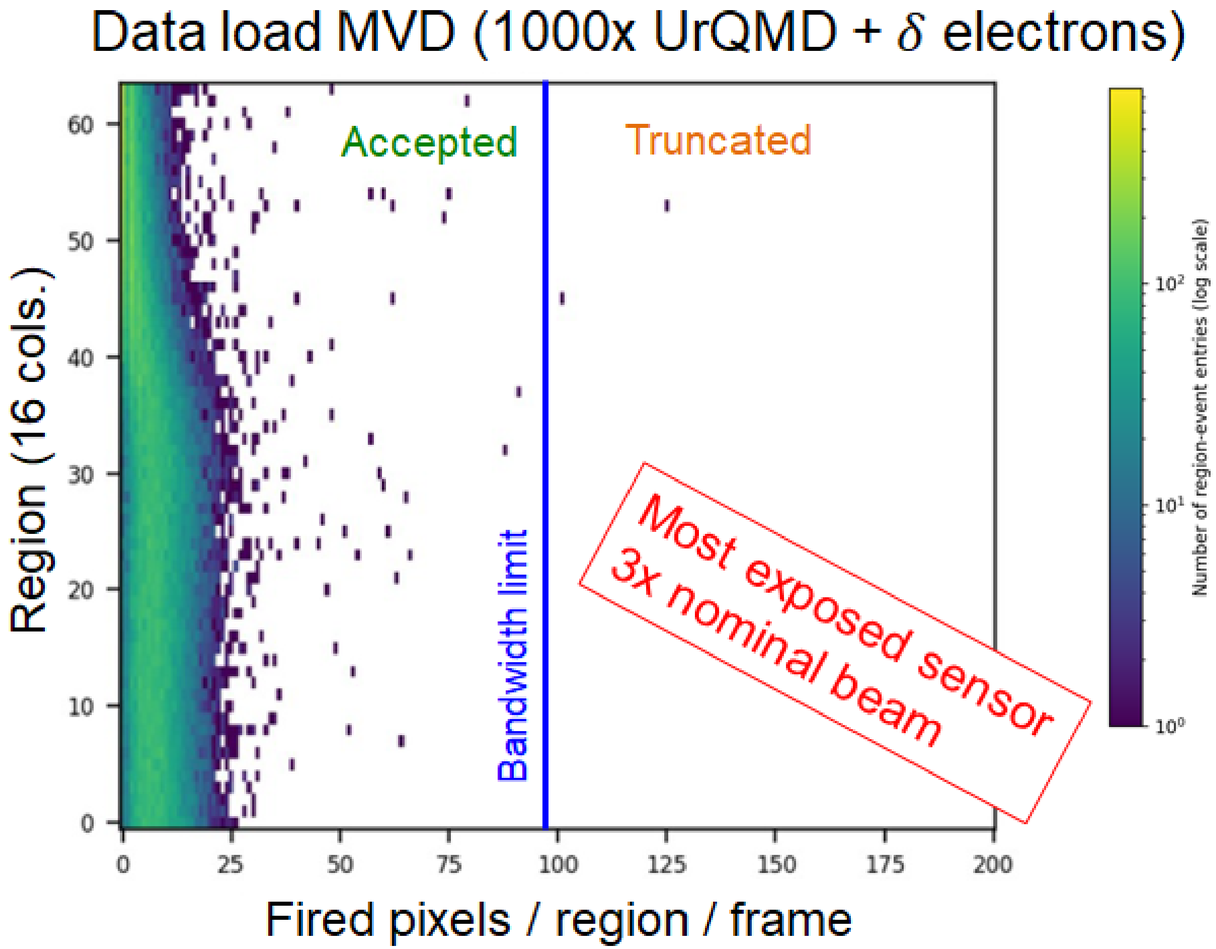
Improved readout speed
→ 8 x 320 Mbit/s

Improved SEE hardening
→ Hamming encoded DAC registers, clock triplication



Sensor Bandwith Usage

Most exposed sensor might truncate data at 3x nominal beam
→ Single regions only (region buffer overflow)
→ No bottlenecks further downstream



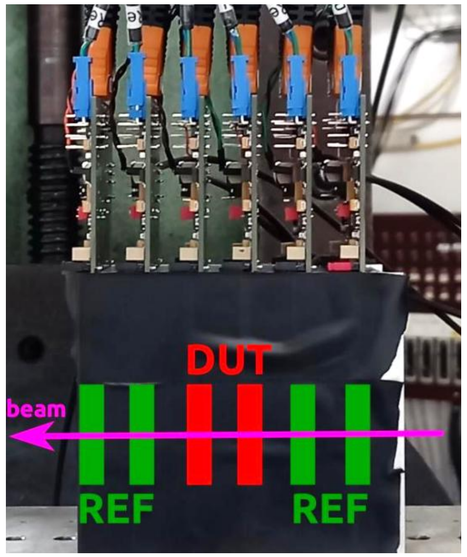
MIMOSIS-2.1 Performance

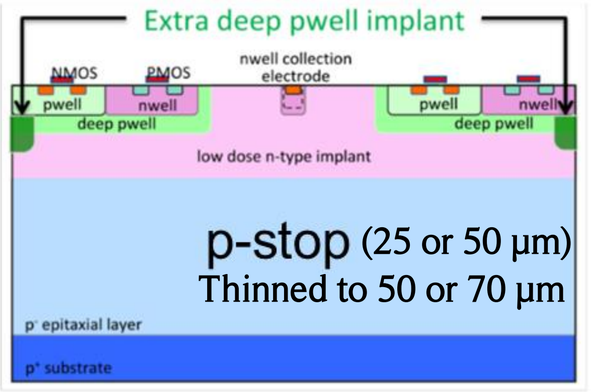
All–MIMOSIS beam telescope

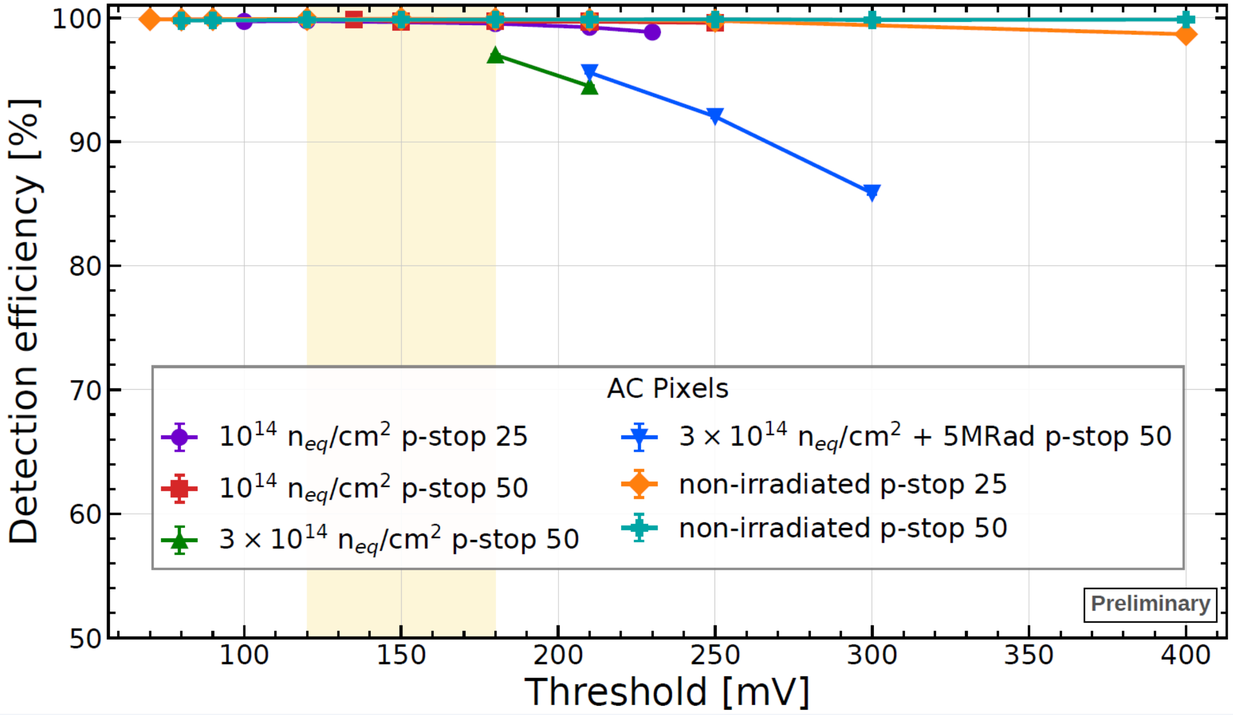
→ 4 reference sensors, 2 DUTs

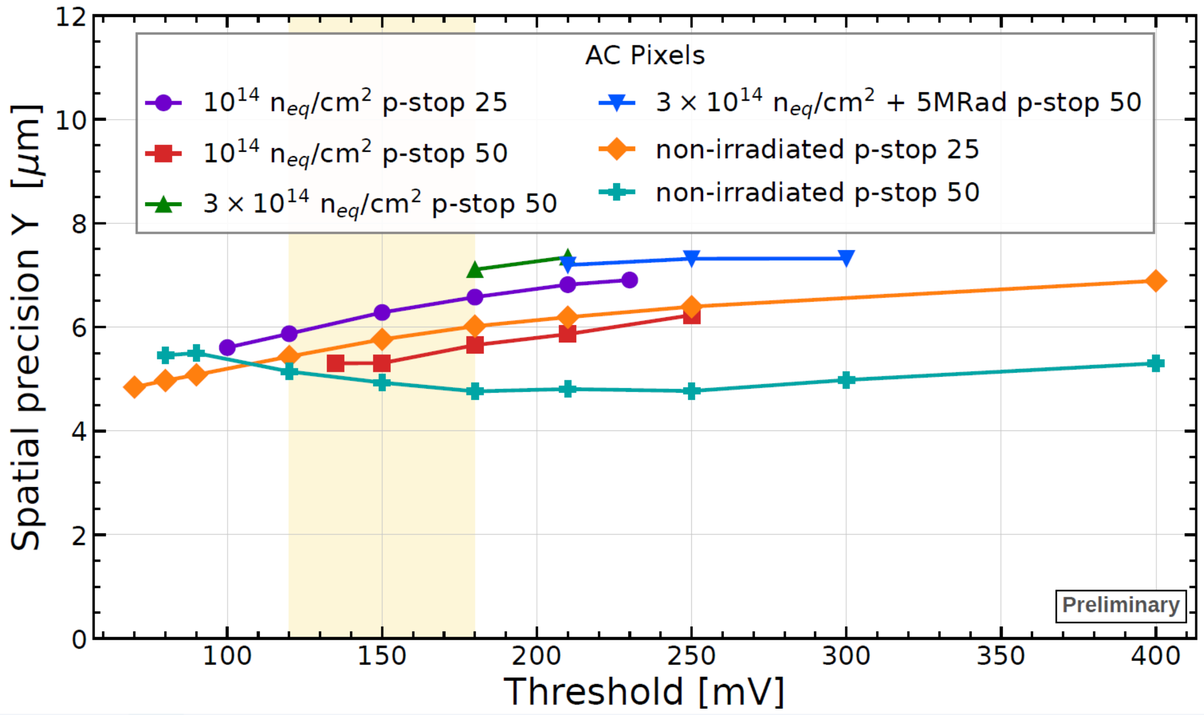
→ Controlled room temperature

→ EOL + safety margin (1 MeV reactor n, few 10 keV X-rays)









PDN-induced Problems

PDN impedance can cause digital errors

→ M2 with 320 MHz PLL fall-back clock (std: 40 MHz)

→ Desynchronization of sensor with DAQ

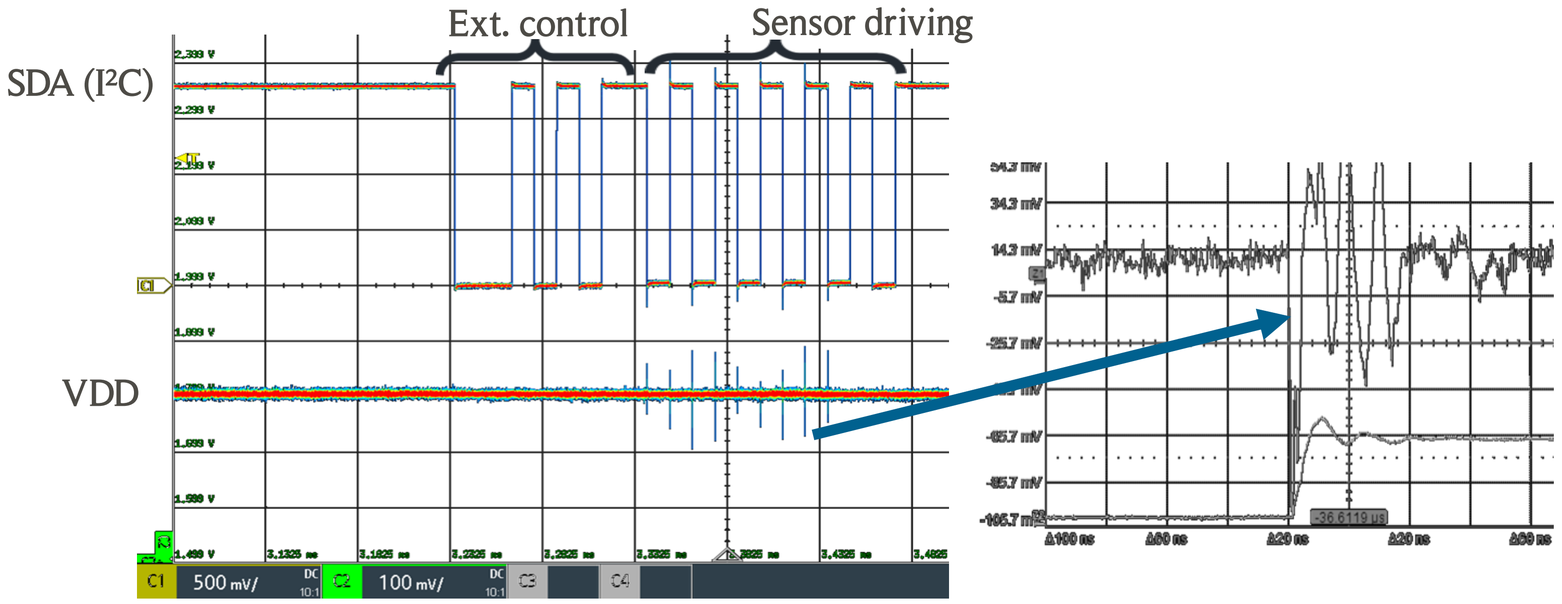
Sensor driving I²C bus (push-pull) raises local GND

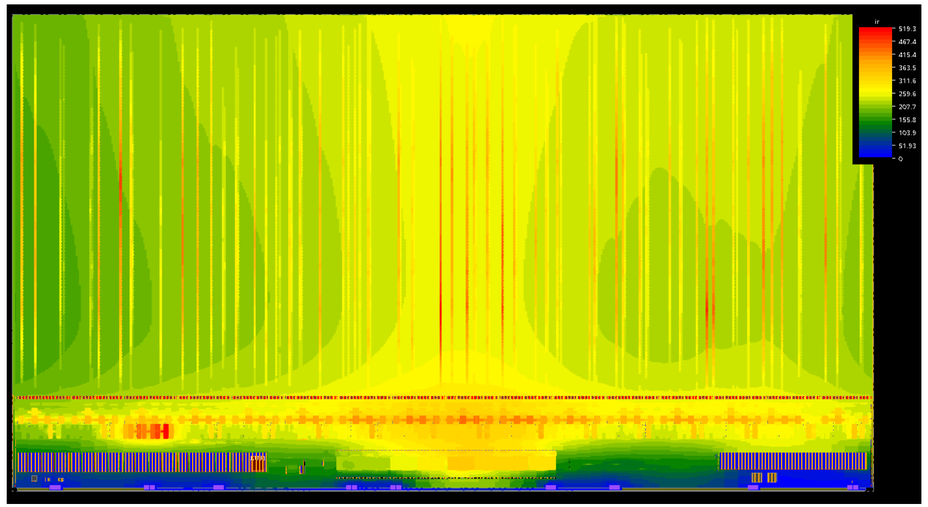
Clock edges lost

Improvements in M3

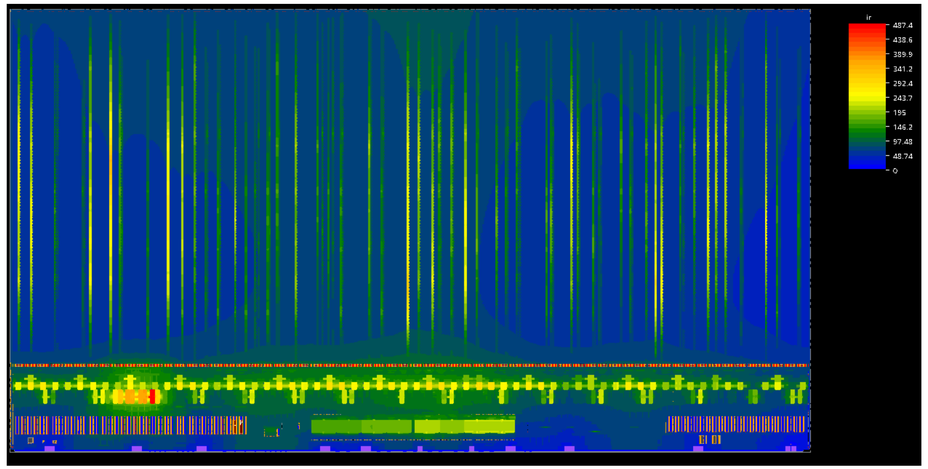
→ Thicker metal lines, addition power connections (sensor PDN)

→ Open-drain I²C pad (trade-off: speed)

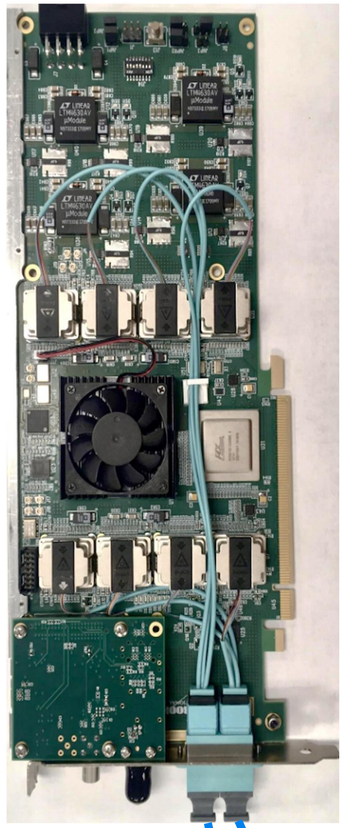




Improvements in digital power grid from M2 to M3



Front-End Electronics



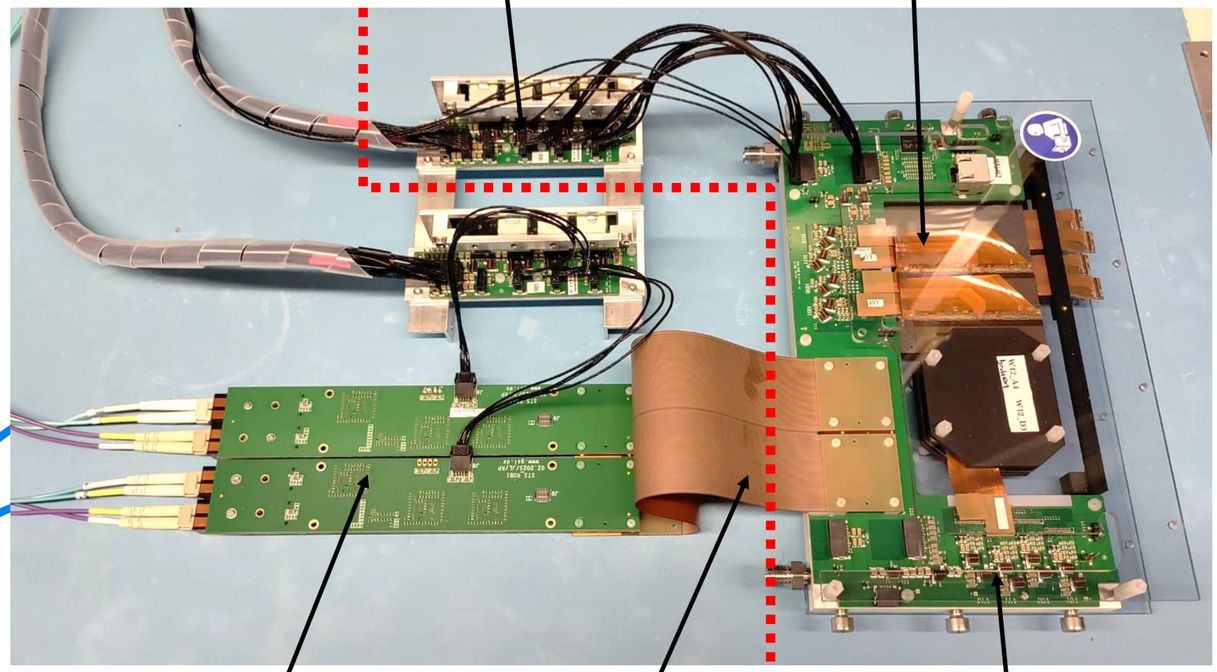
Free-streaming DAQ

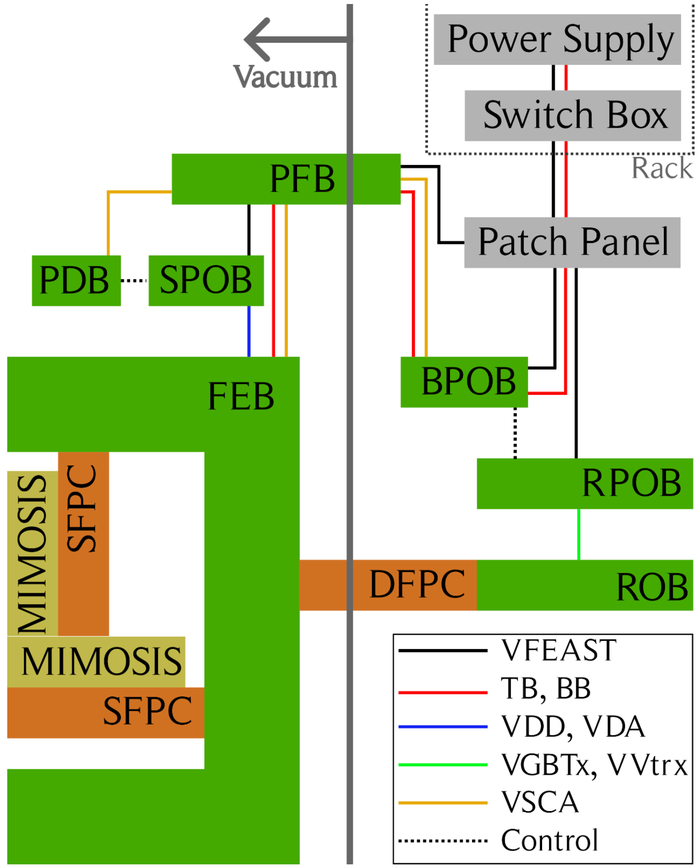
→ FPGA-based Common Readout Interface (CRI)

Prototype: ATLAS FLX-712v2

→ GBT/VTRx-based Readout, GBT-SCA for controls

→ LV: FEASTMP





Detector-level PDN

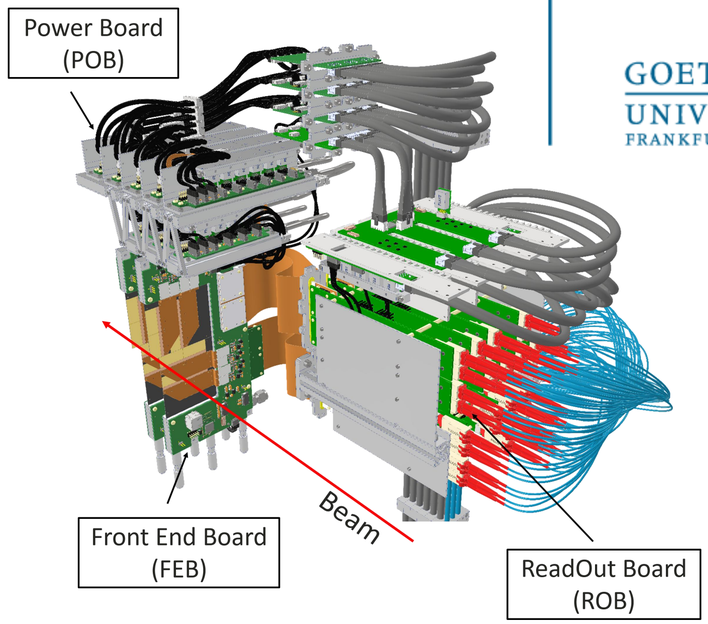
Detector PDN

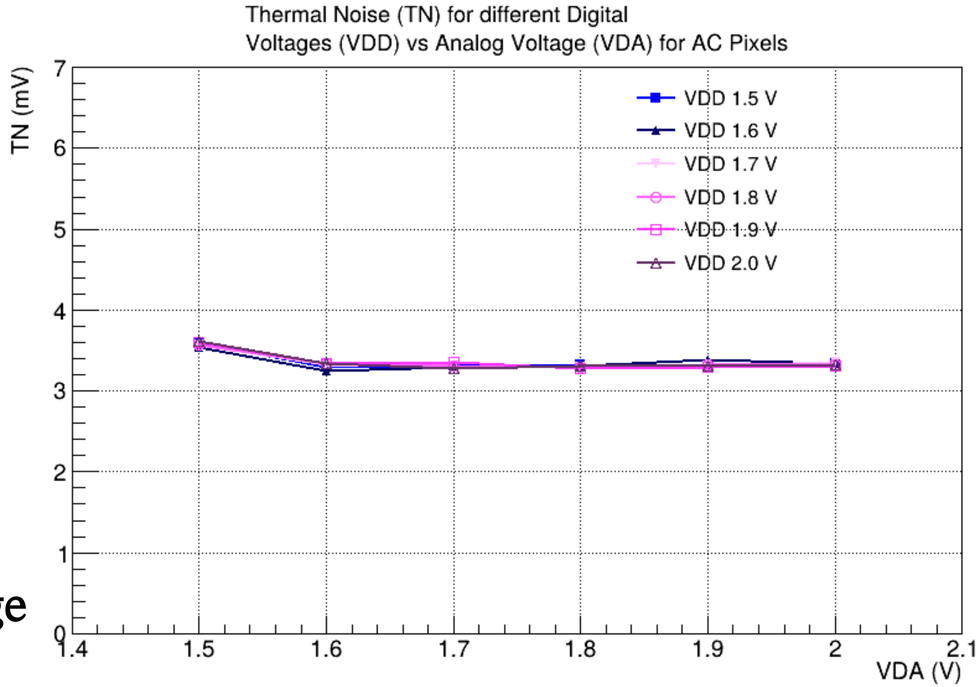
→ LV distribution in vacuum (FEAST DC/DC)
→ Low impedance power network
→ >50% of FPC area for powering
→ Separated power domains

Note: This is an "easy" system

→ Parallel powering
→ Cross-powering and latch-ups not observed
→ Sufficient stable operation voltage range

But: Capacitors in acceptance
But: Grouping of components
But: ~30 mV GND shift (biasing, SLVS)





Stable operation voltage range

Key Component: Sensor FPC

Industrial 12 µm Cu technology

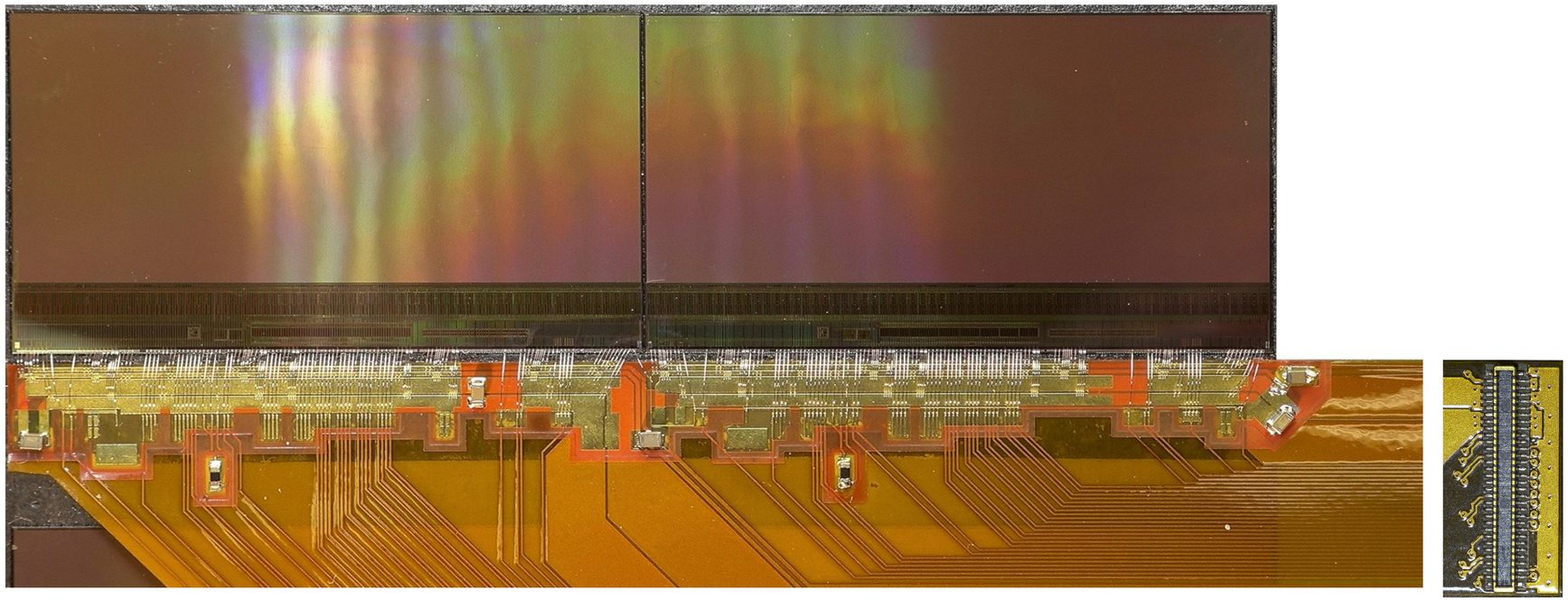
→ Partly single-layer, >50% of area for powering, rest for bias, control, data

→ 2 sensors per FPC, fine-pitch connectors to FEE

→ Integrated with 3M 9460PC transfer tape (visual QA)

Upgrade to Al FPCs planned (not day-1)

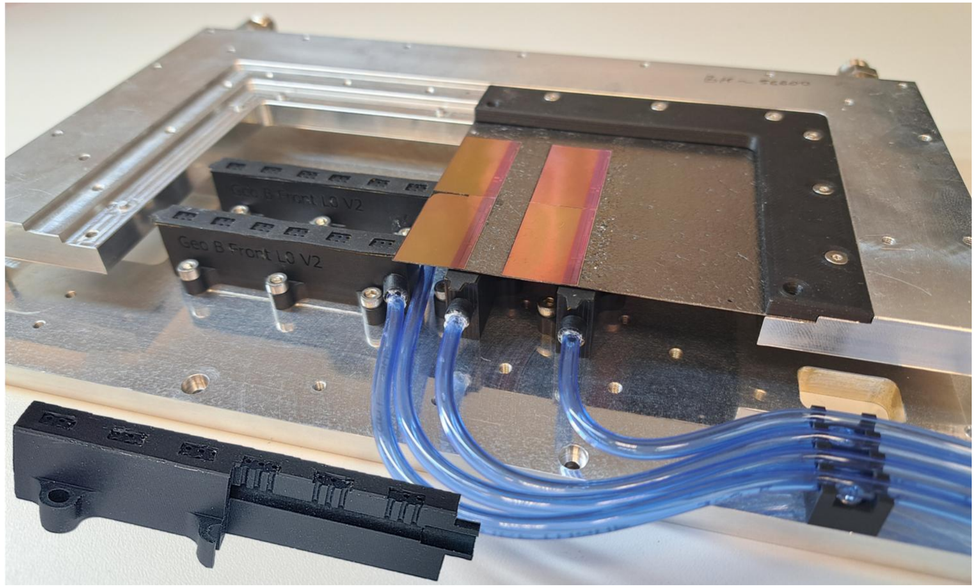
→ Requires several key design changes

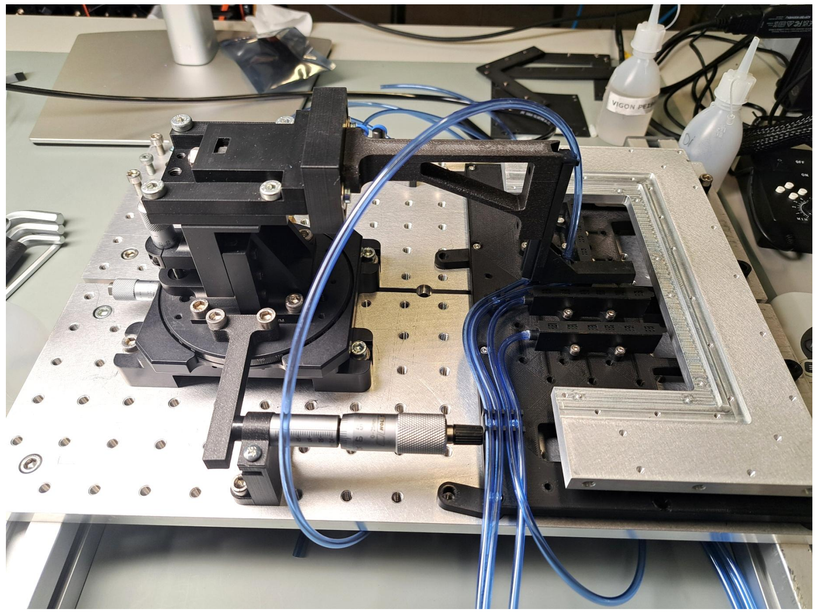


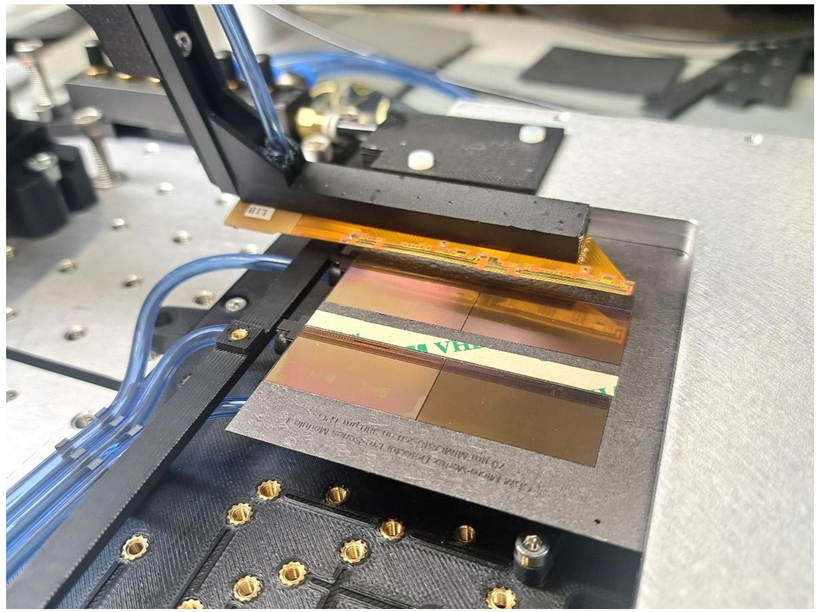
Integration Tools

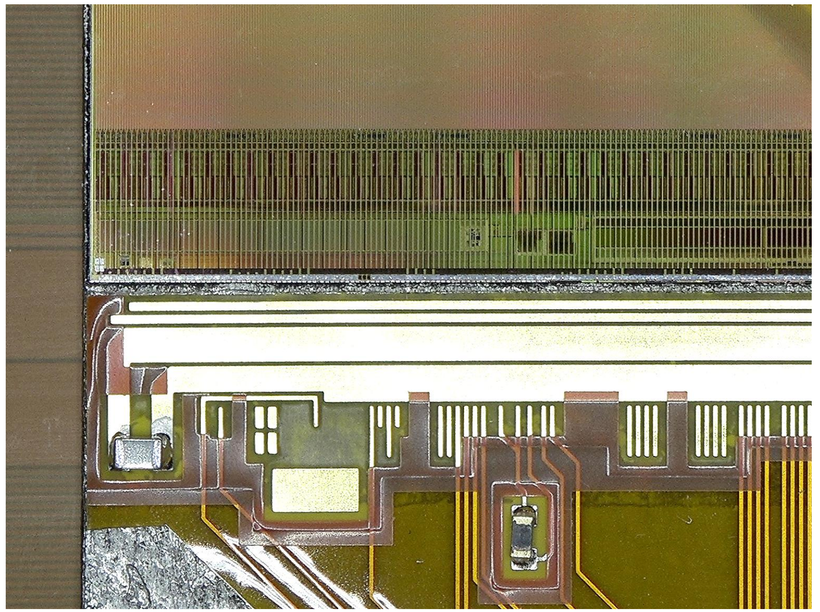
Key challenge: Double-sided modules

→ Tape and FPC placement (~50 µm precision), wire-bonding
→ Micropositioners + vacuum, camera
→ Integration jig for local mechanical support
→ 13 mm front-/back-side offset
→ SLA-printed local support structures









Wire Bonding

Full-automatic bonding (132 bonds per sensors)

→ GSI Detector lab (Delvotec 17L)

→ High quality and consistency, also with bad mechanical support

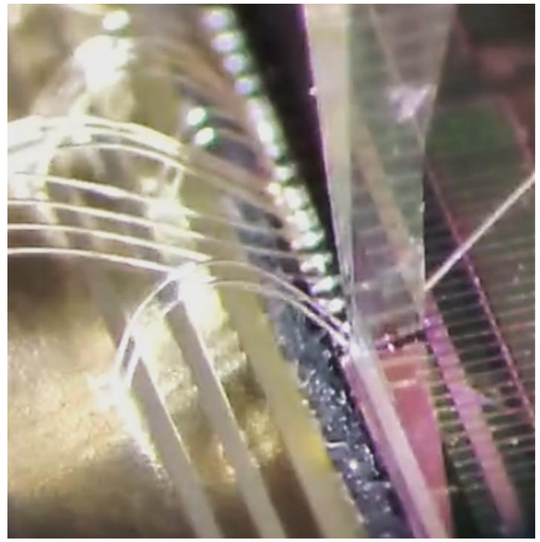
QA

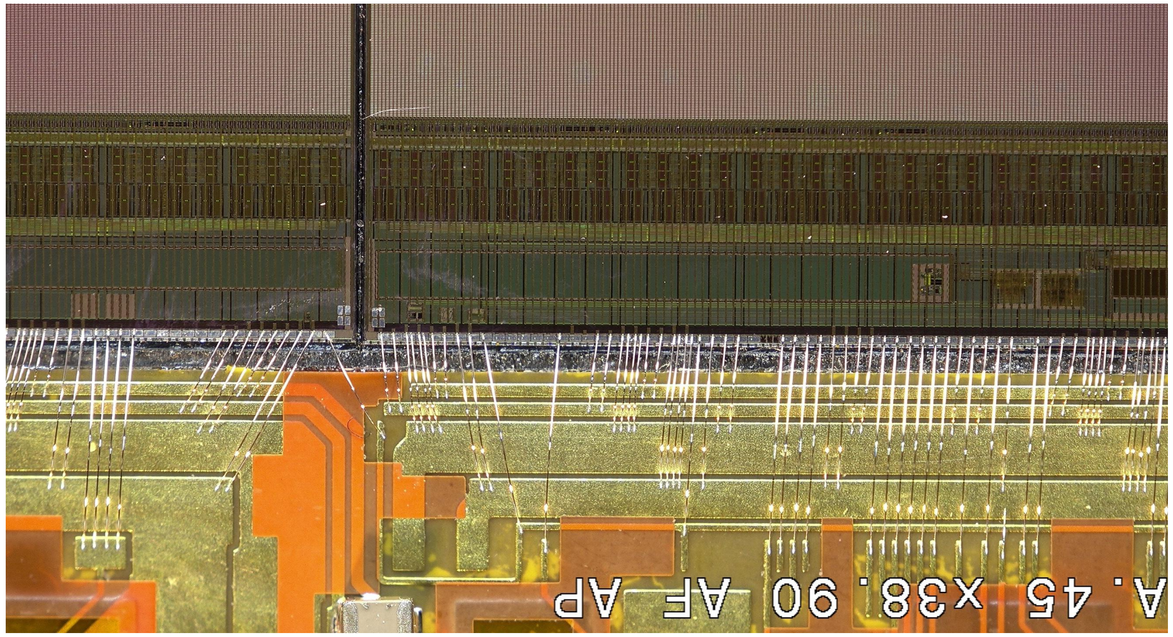
→ Visual inspection

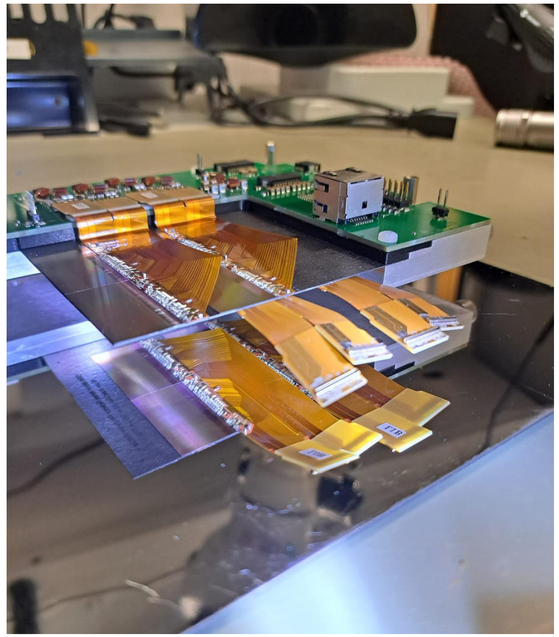
→ Electrical integrity (bench-top r/o system)

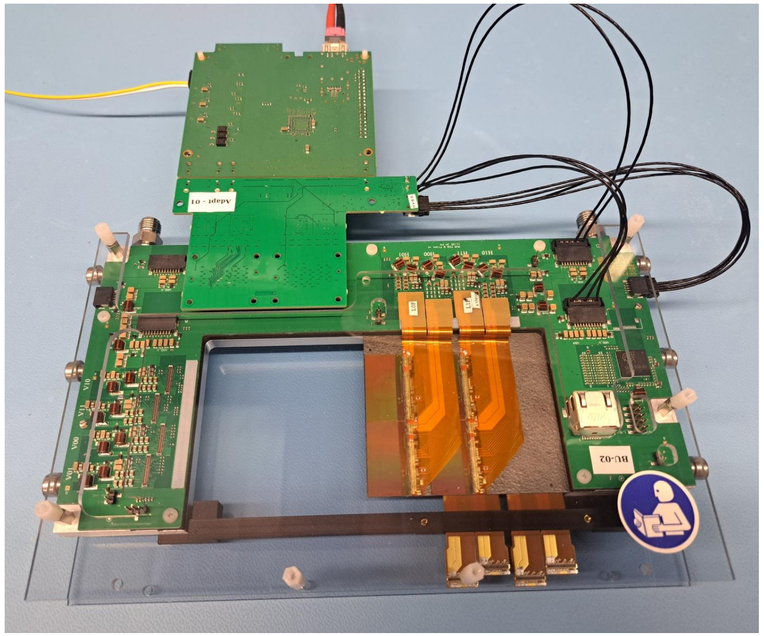
→ Metrology

Sensor bending ~15 µm during bonding due to insufficient glue fill

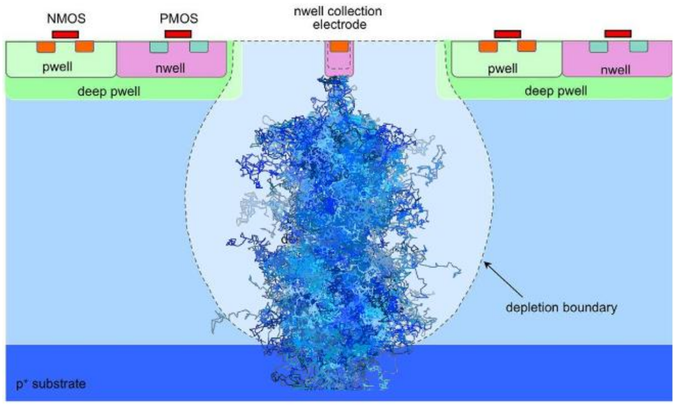


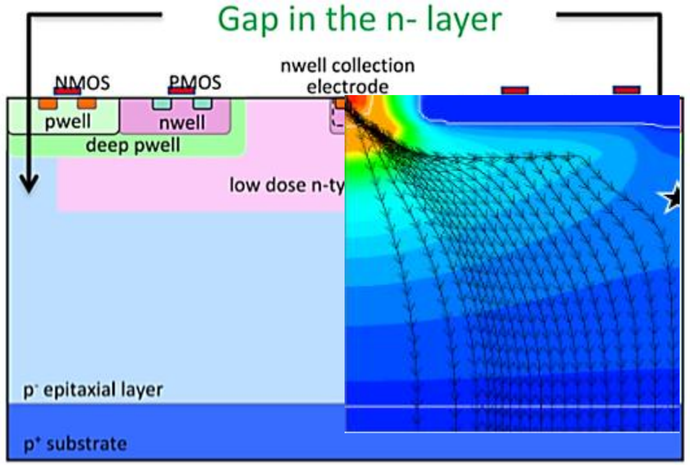


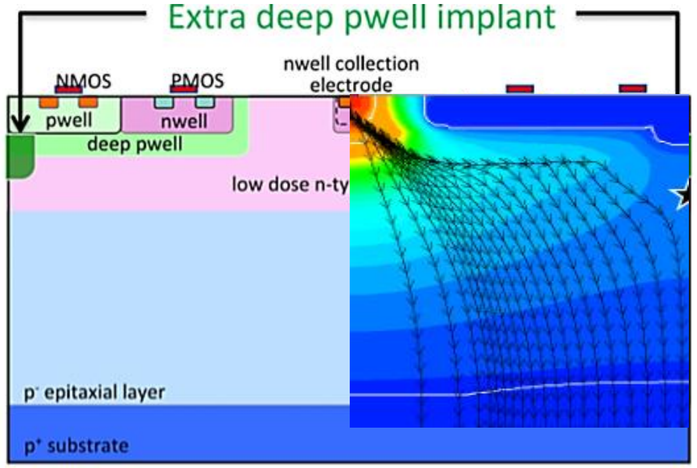




Process Modifications







https://indico.cern.ch/event/669866/contributions/3234996/attachments/1767972/2883923/slides_mmunker_pixel2018.pdf
https://iopscience.iop.org/article/10.1088/1748-0221/18/06/C06013/pdf

Fast charge collection: hardness against non-ionizing radiation (NIEL)

→ Increase depletion

→ Improved E-field in pixel corners

→ Side effect: Improve timing

First time in MIMOSIS: 50 µm for double the signal (only TJ-180)

Small nodes, fast front-ends: hardness against ionizing radiation (TID)

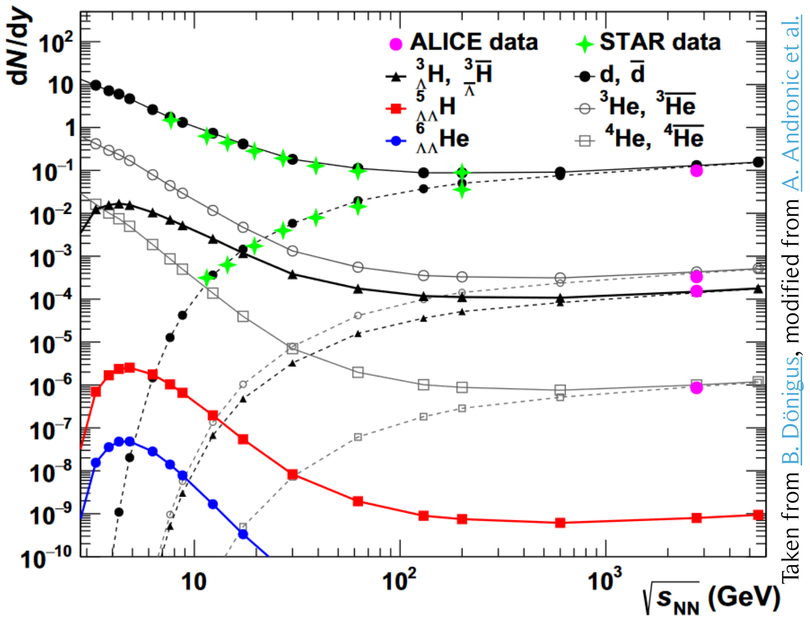
Charge trapping in SiO_2

→ More compact transistors in smaller nodes

Charge clearing through increased leakage currents

→ Faster r/o to compensate

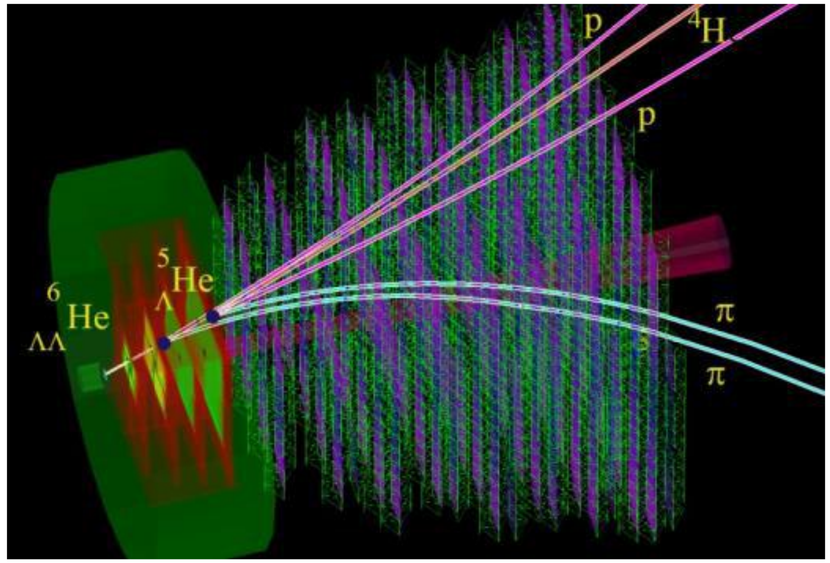
Physics with the MVD

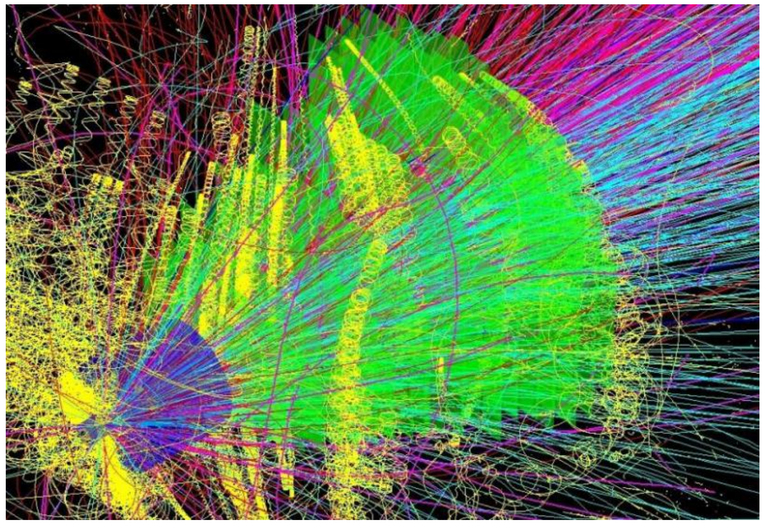


Taken from B. Dönigus, modified from A. Andronic et al.

Hypernuclei production

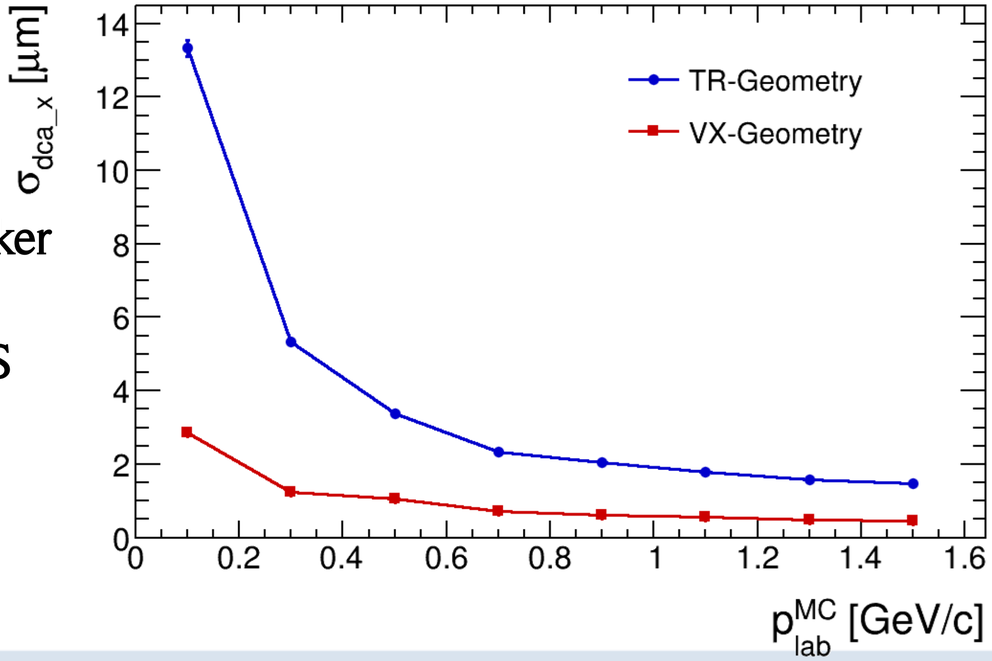
Selection w/ KFParticle Finder in CBM





High track density in the Inner Tracker

MVD track seeds minimizing STS ambiguities

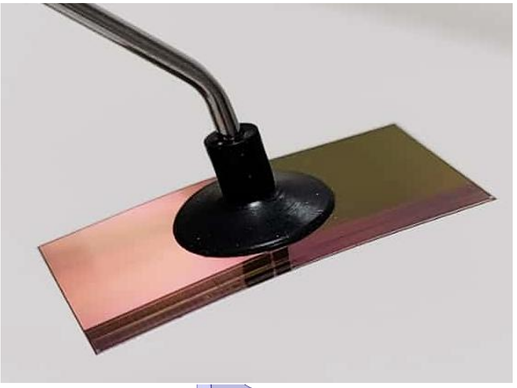


MVD Design Requirements

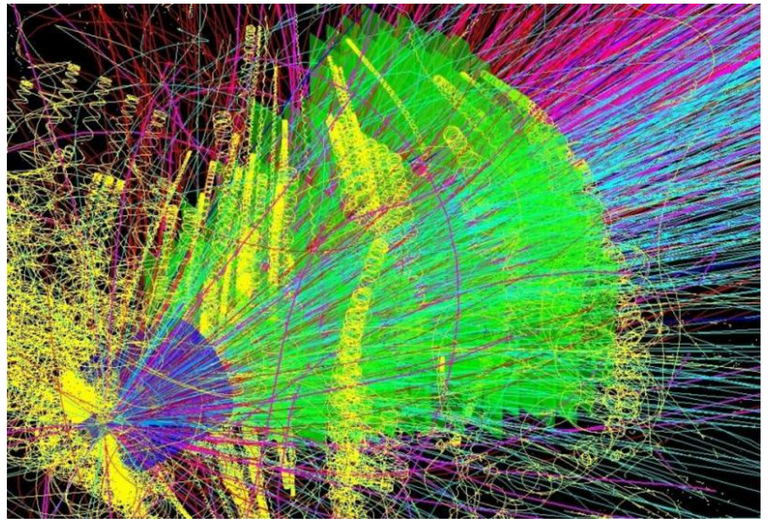
High precision tracking and vertexing
→ High track density, low momentum tracks, B-field

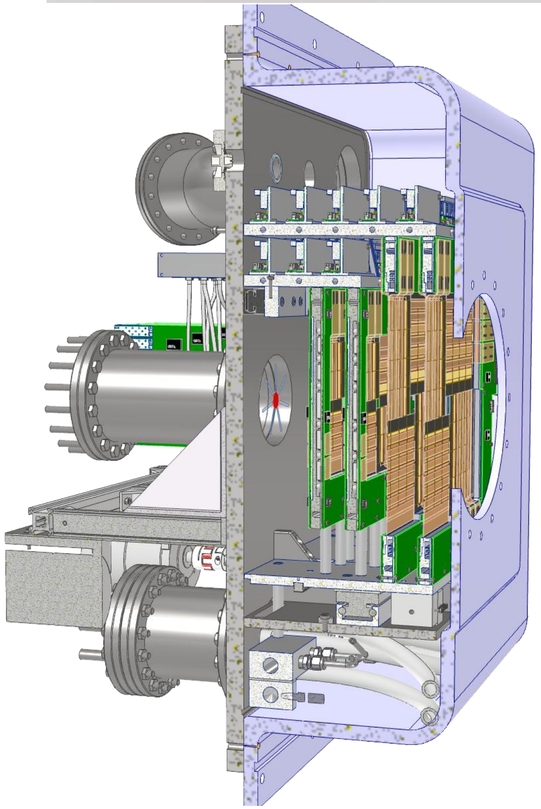
Design driven by material budget
→ Multiple Scattering dominated regime
→ Technology: (thinned) CMOS MAPS
→ Tracking **before** beam window (vacuum operation)

But: No lunch for free
→ MVD rate limited to 100 kHz Au+Au (10 MHz pp)
→ Passive cooling in acceptance
Large modules for mechanics and cooling
→ Double-sided integration



$$\sigma_{MS} \sim \frac{1}{\beta \cdot p_{lab}} \sqrt{\frac{x}{X_0}}$$





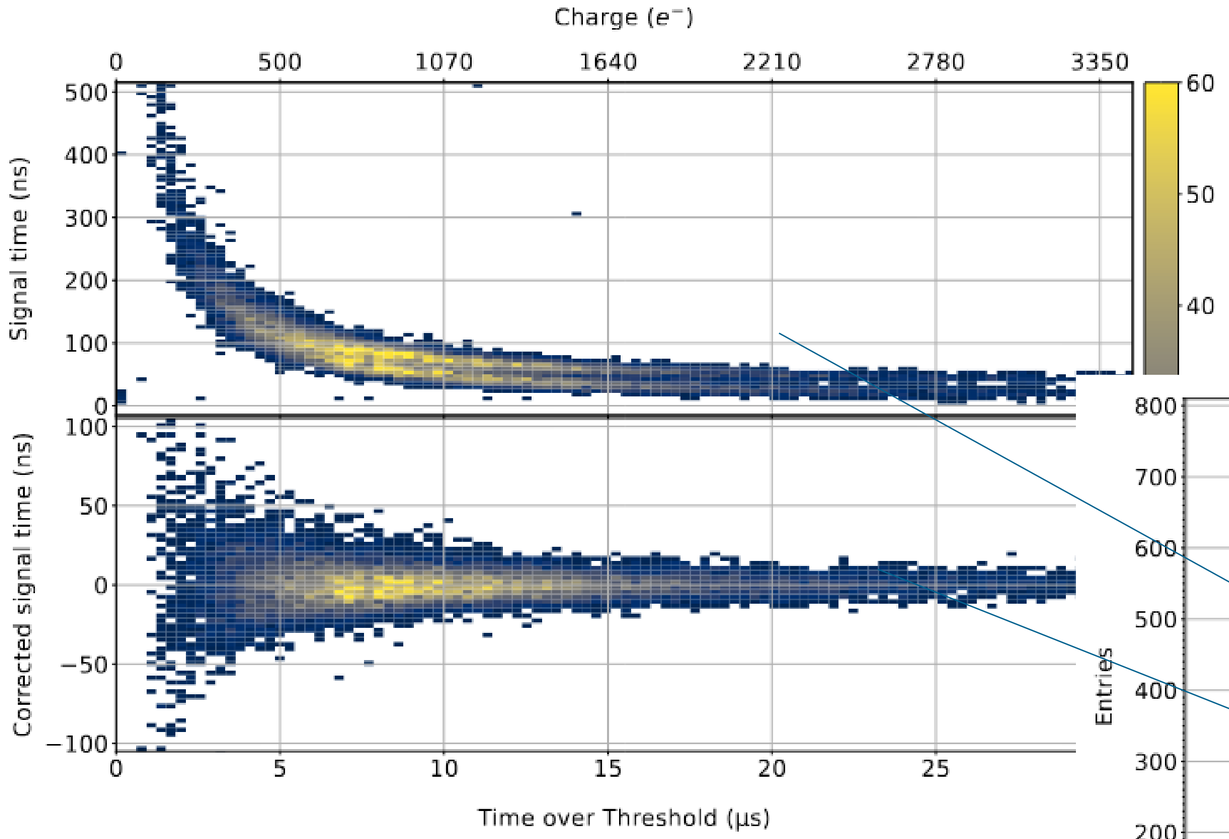
Time Walk in MAPS

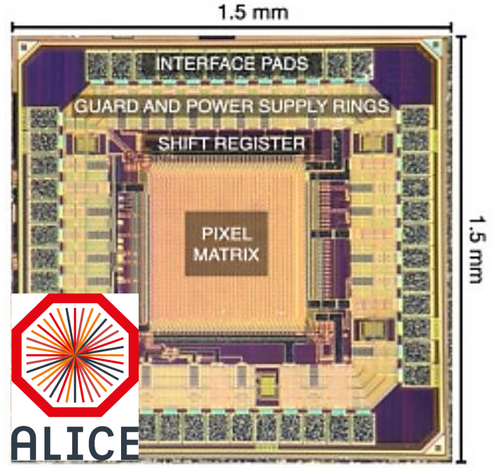
DPTS (by CERN/ALICE)

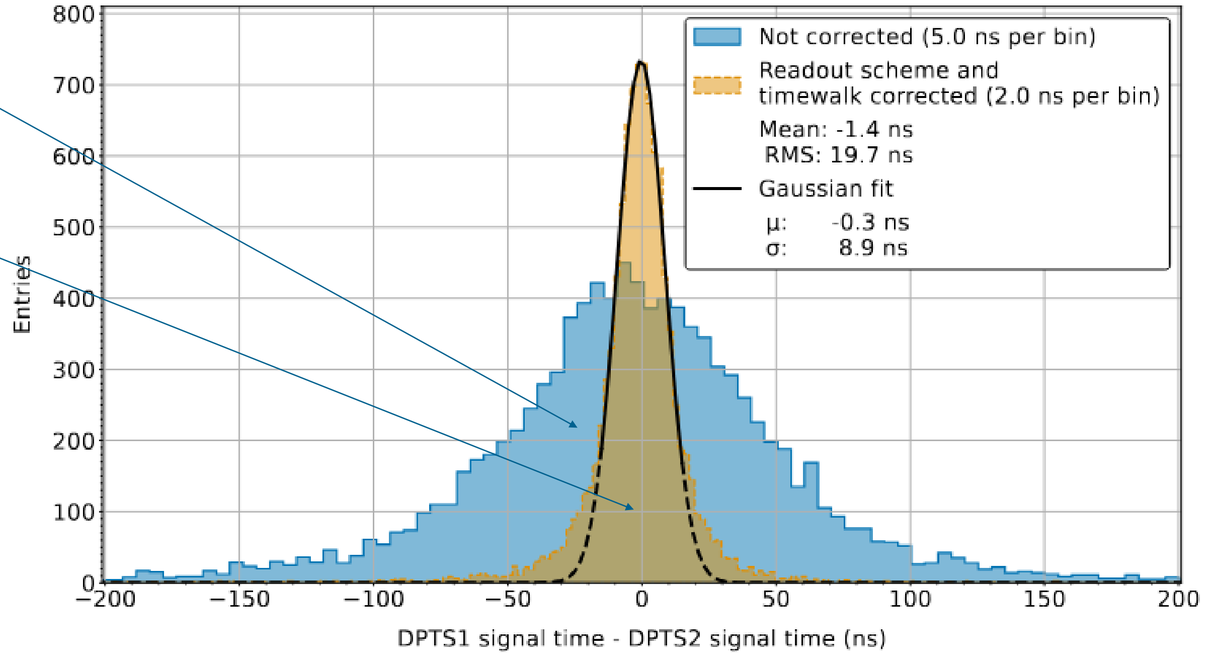
GOETHE UNIVERSITÄT FRANKFURT AM MAIN

Fast front-ends, but significant time walk

→ Charge correction







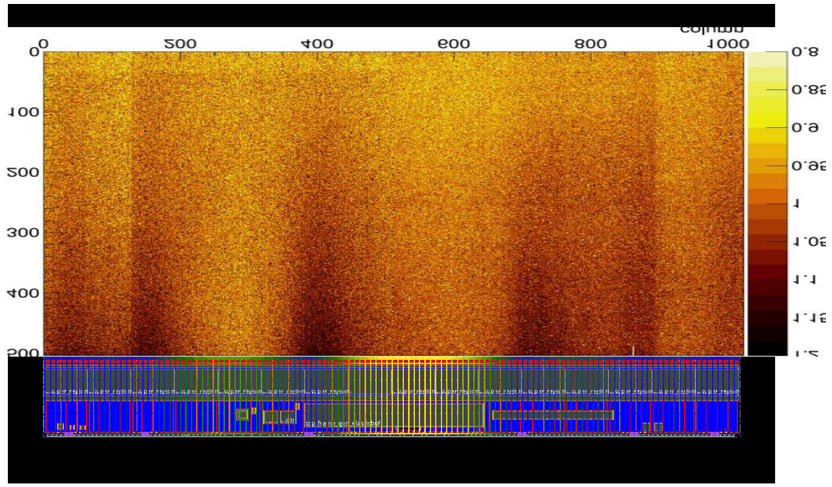
G. A. Rinella et al., arXiv:2212.08621v4

Challenge: Powering

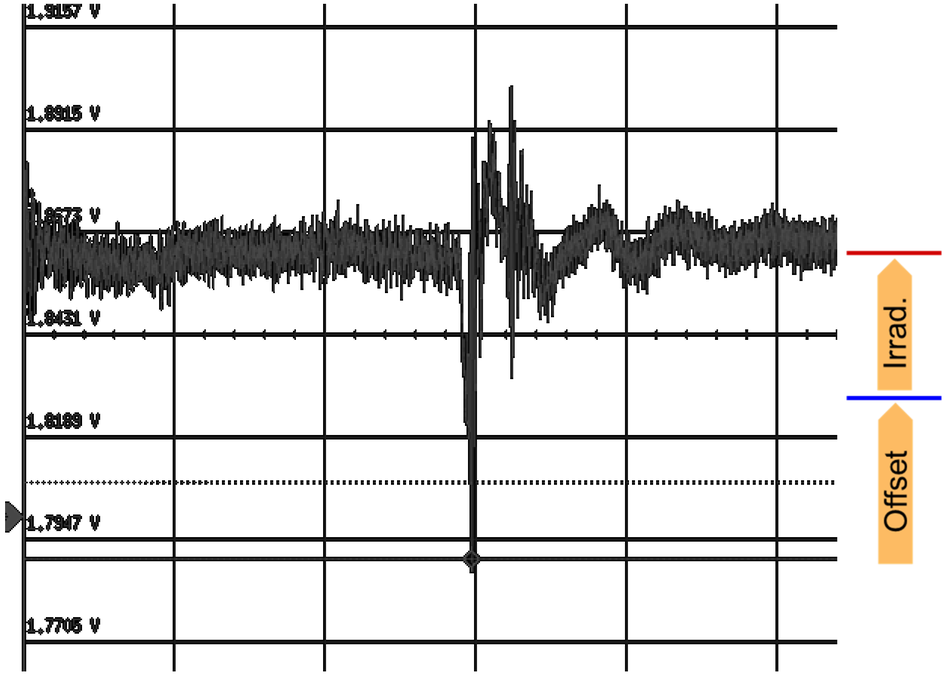
Optimize power distribution network (PDN) on-chip and in-detector

→ Static and dynamic voltage drops on all time scales

→ CMOS logic sensitivity

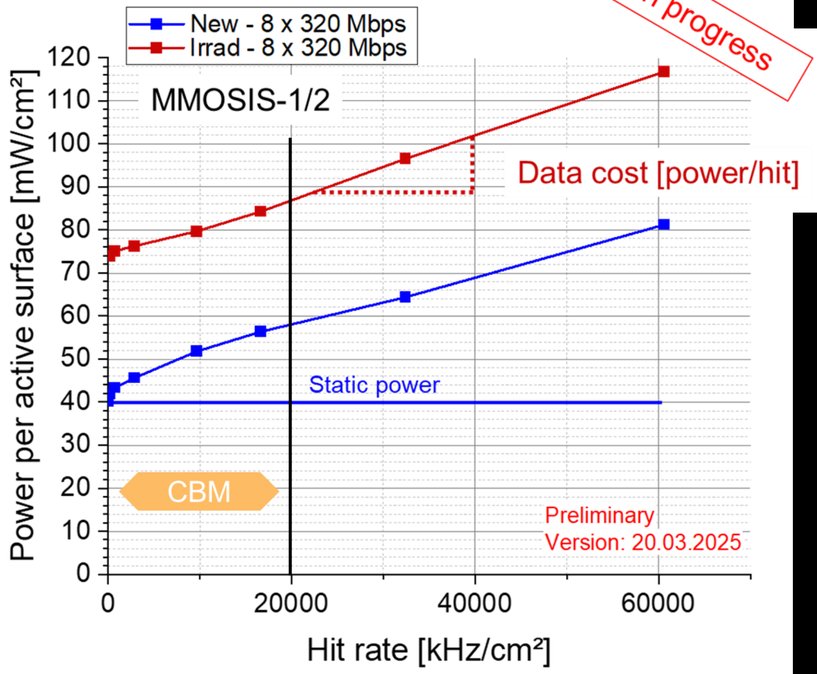


≲ 100 mV voltage fluctuations on VDD every frame (5 µs)

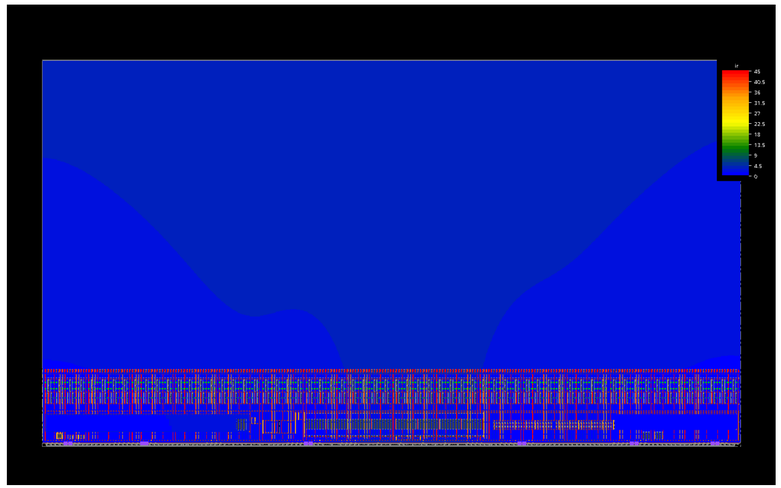


≲ 2x digital power increase during spills, TID effects

Work in progress



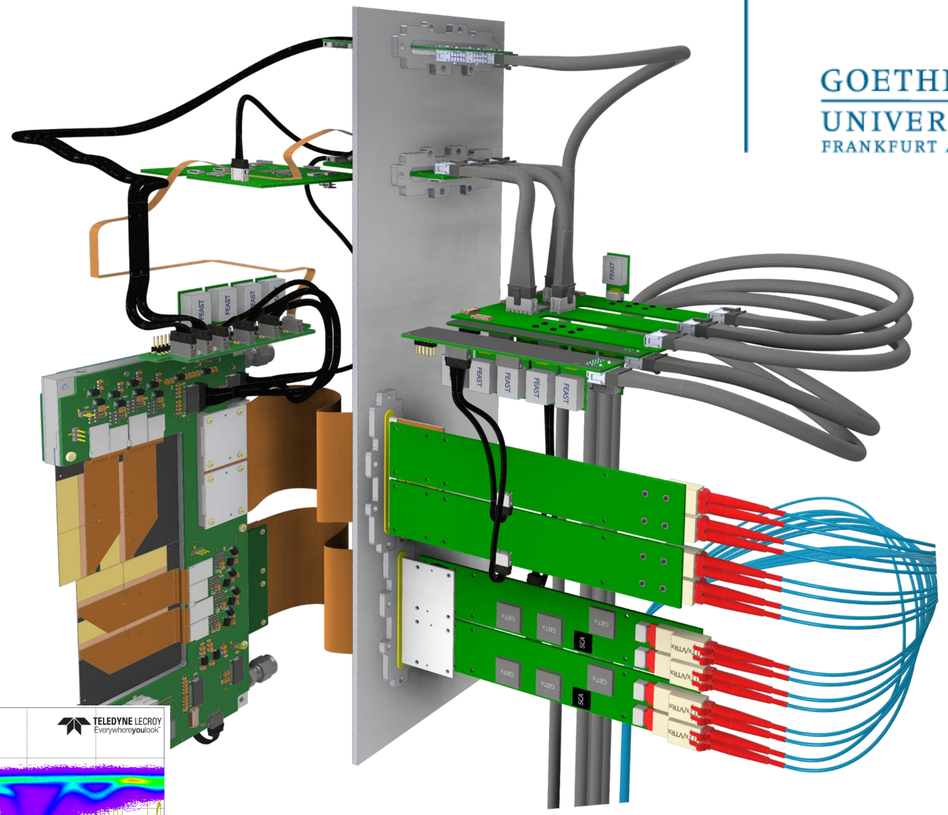
~4x improvements in analog power grid from M1 to M2



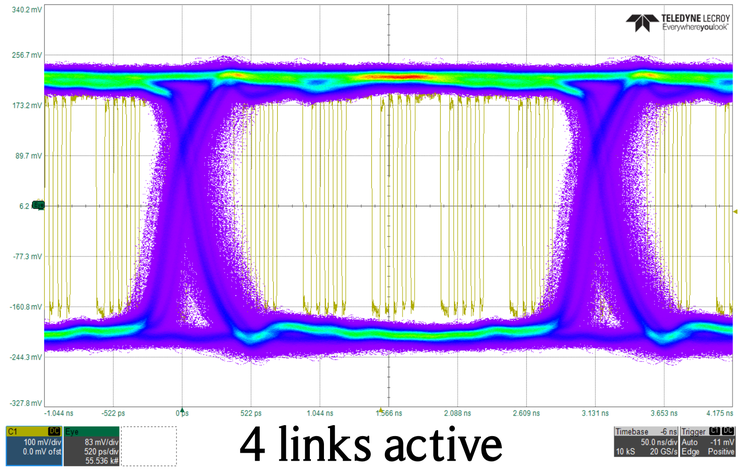
Challenge: Data Integrity

High-speed signals over imperfect transmission path

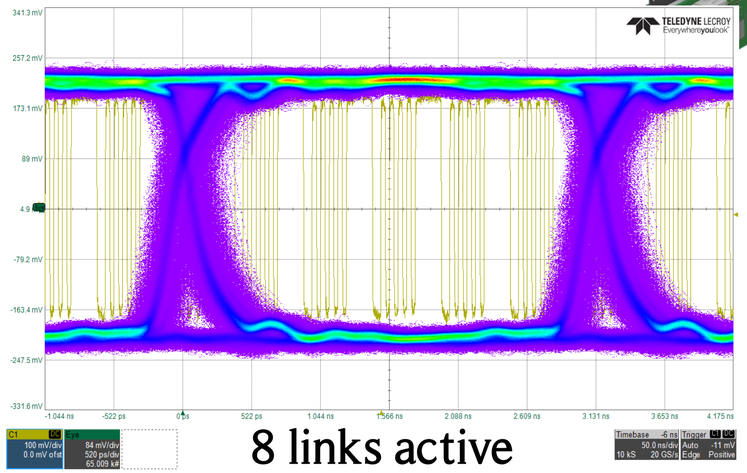
→ 320 Mb/s SLVS, up to 90 cm FPCs + PCBs
→ Three connectors (discontinuities) in data path
→ Single-layer, unshielded FPCs
→ SLVS CM (200 mV) shifts due to GND shift (30 mV)
→ Dynamic phase shifts due to power fluctuations



Validated in full system tests!



4 links active



8 links active

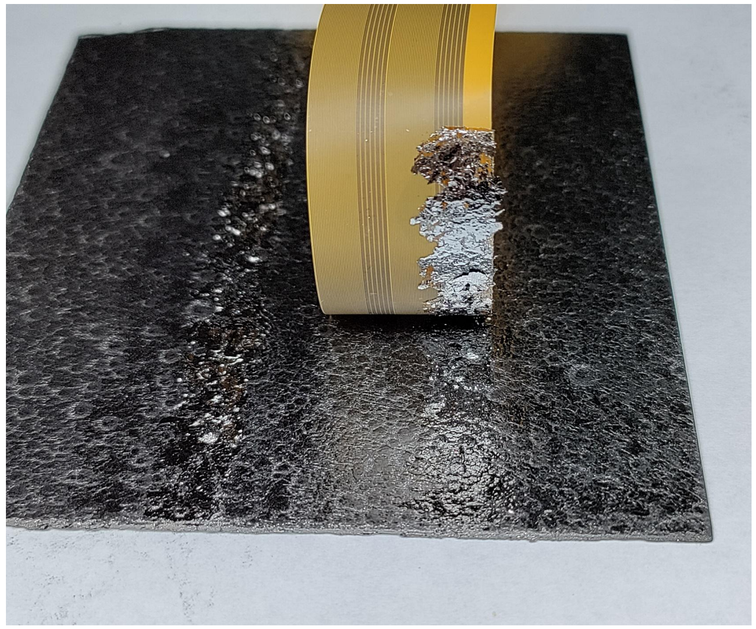
Surface Coating and Plasma Activation

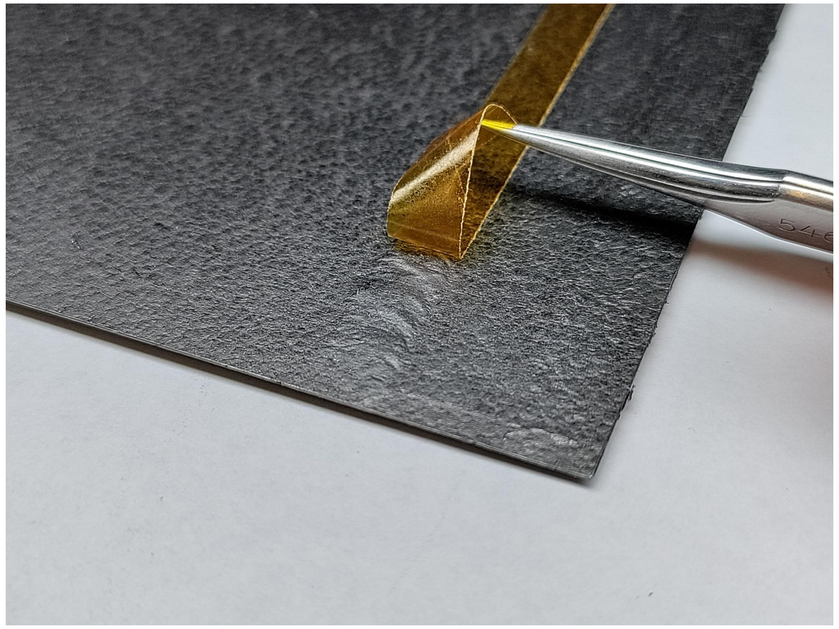
5 µm Parylene–C coating
→ Electrical insulation
→ Seal of abrasive surface

20 min O_2 plasma activation
→ Increase surface energy γ from 28 mN/m to >68 mN/m
→ ≳ 7 days time window for gluing (γ deteriotes again)

https://plasmaparylene.de/

Tape peeling: Uncoated vs coated TPG





PG for Day-1 MVD in house, FAI passed



Die Bonding Optimization

Glue amount optimization challenging

→ Glue thickness ~ surface roughness

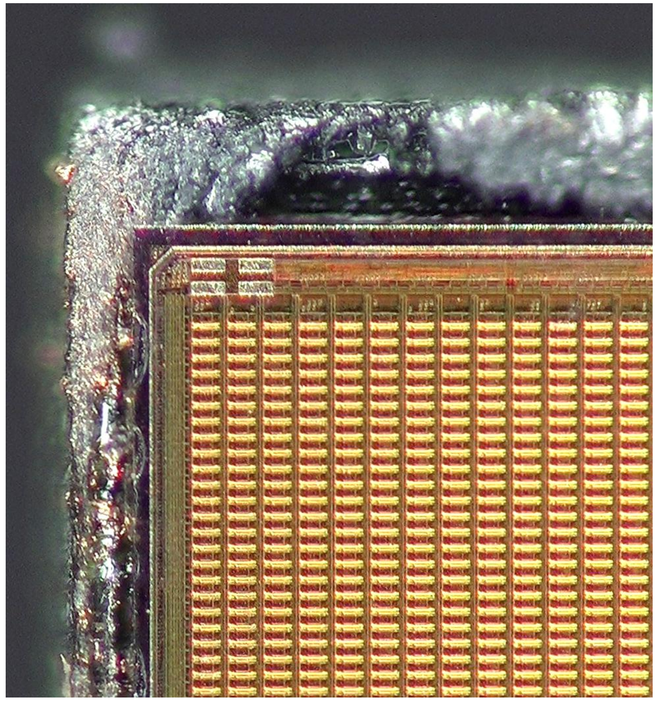
→ Bonding pads directly at the edge of the sensor

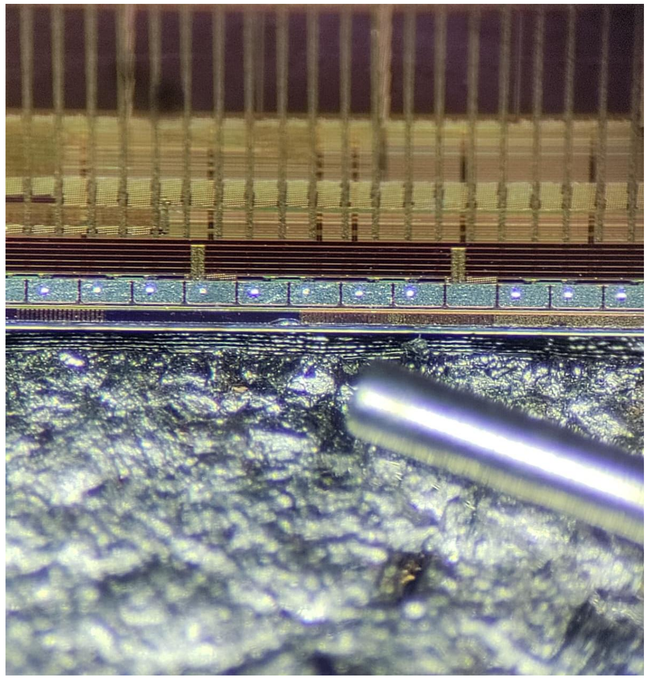
→ CH_2Cl_2 validated for reworking cured glue

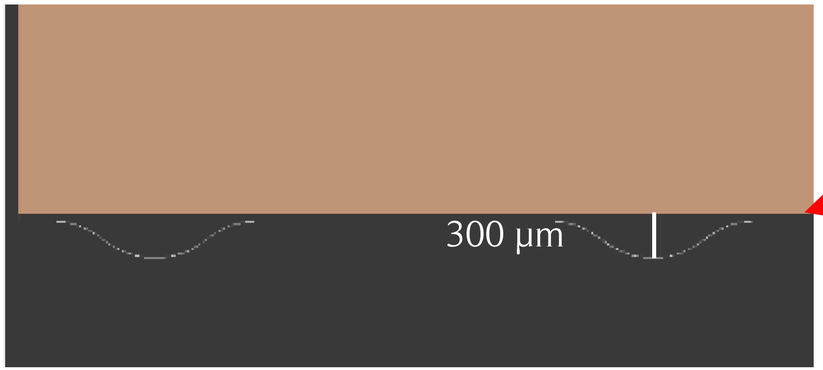
Optimized hatch layout

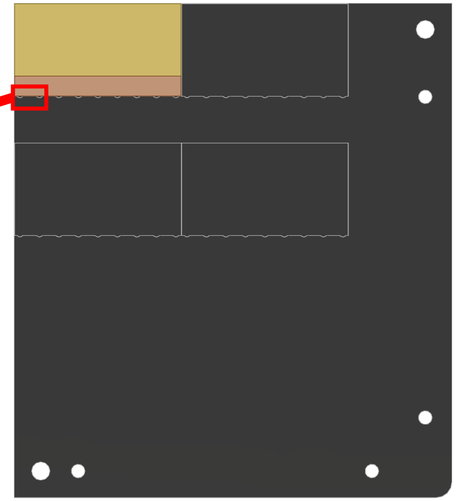
→ Improve visual inspection

→ Option for reworking insufficient glue fill









Optimized hatch layout for glue reworking
30G needle and sensor at same scale
(feature not implemented on this carrier yet)

Integration Jig

Local support structures for bonding area

→ SLA-printed

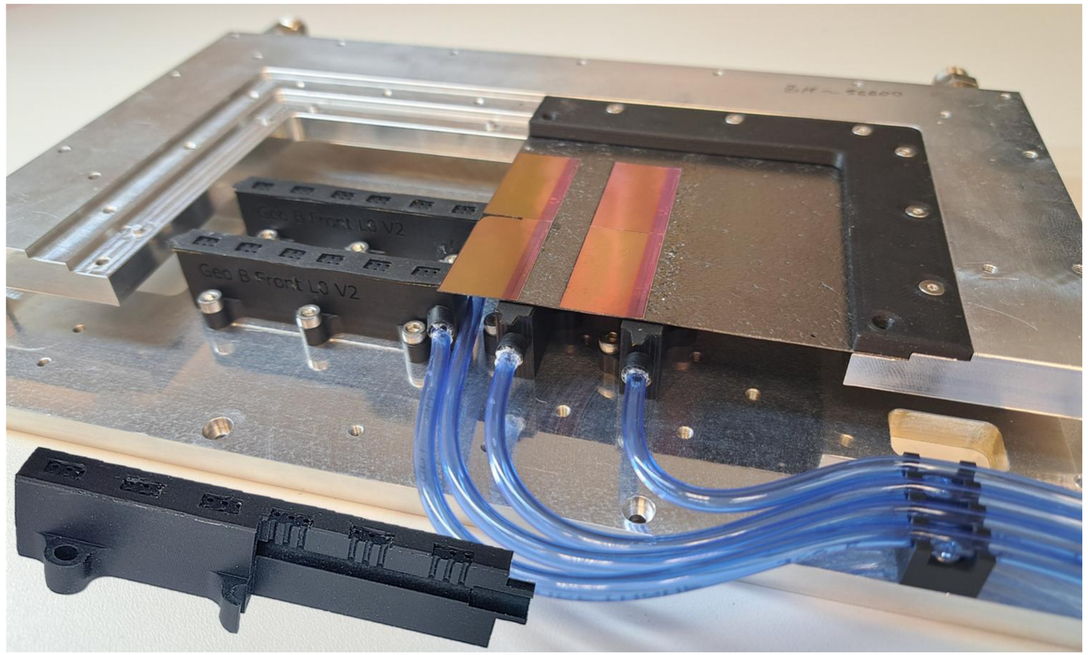
Granular internal vacuum distribution

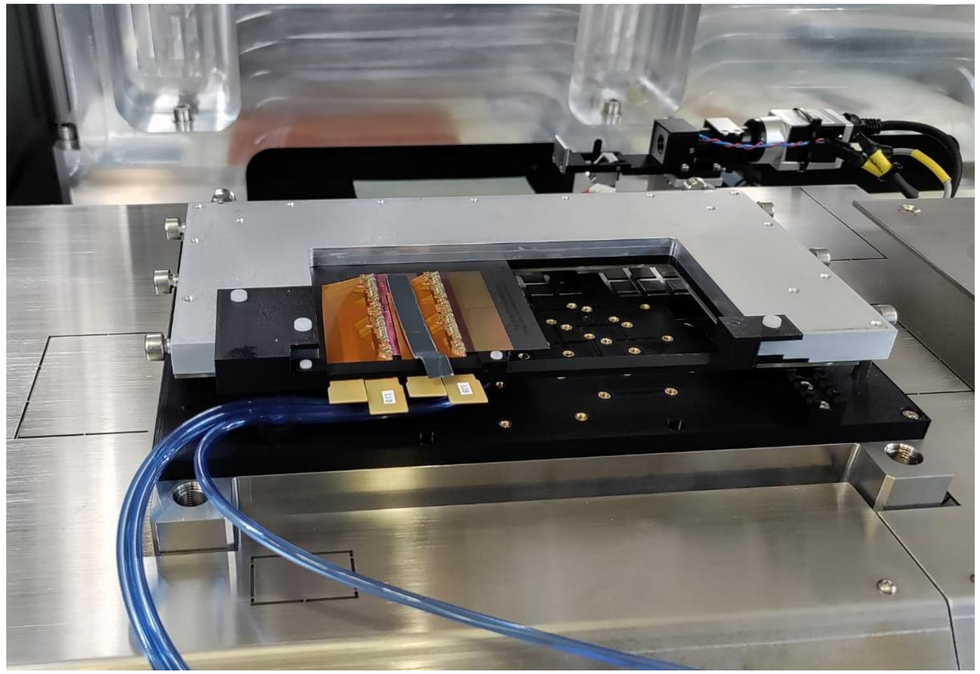
Tight tolerances, ESD-safe

Elastic surface, 500 µm conductive rubber foil (Adafruit 5464)

→ Height optimized for layer stack (TPG, sensor, FPC)

Plate can be directly mounted onto wire bonder





Data and Power Vacuum Feedthroughs

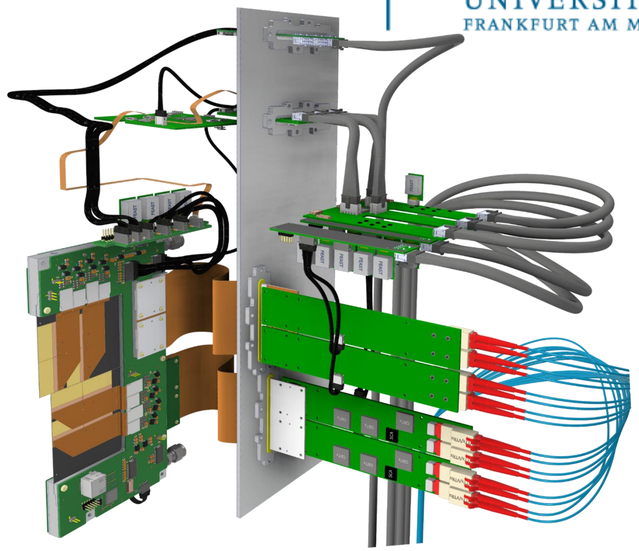
Modular feedthrough design

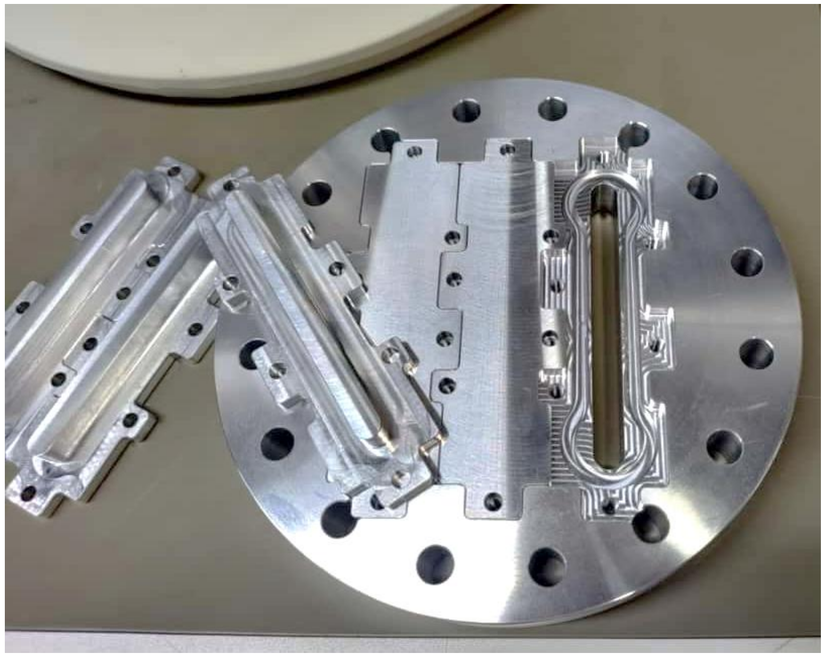
→ FPC and PCB version

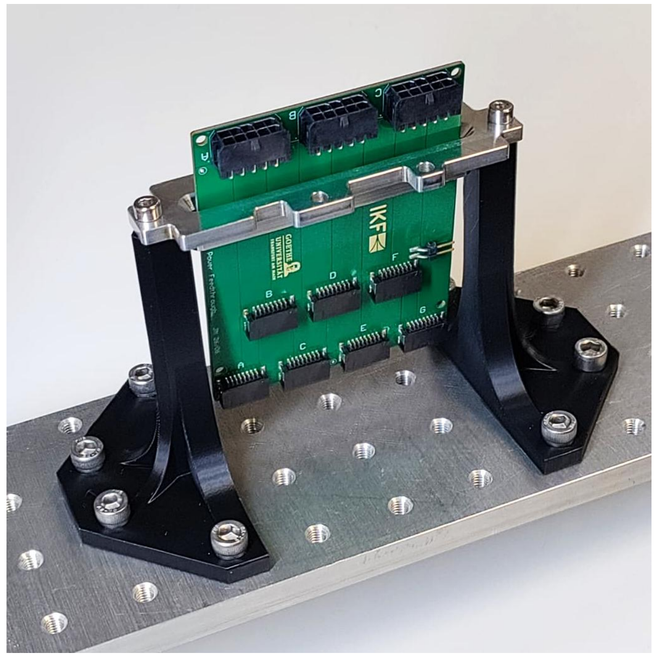
→ EPDM O-ring seal

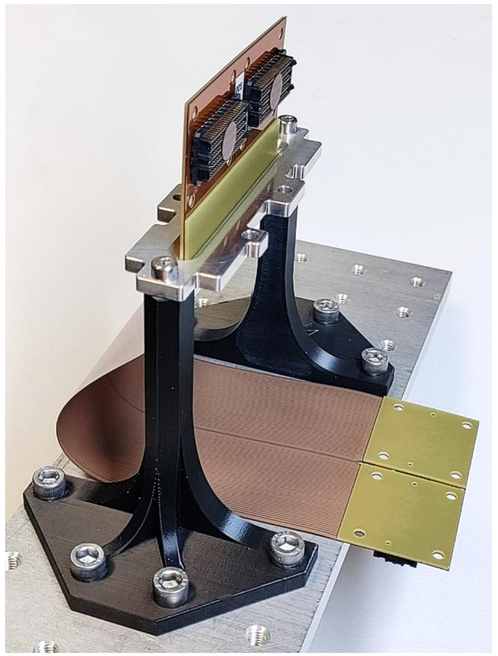
→ Al module, Araldite 2011/2020

→ Vacuum tight (3 x 10^{-6} mbar), design validated



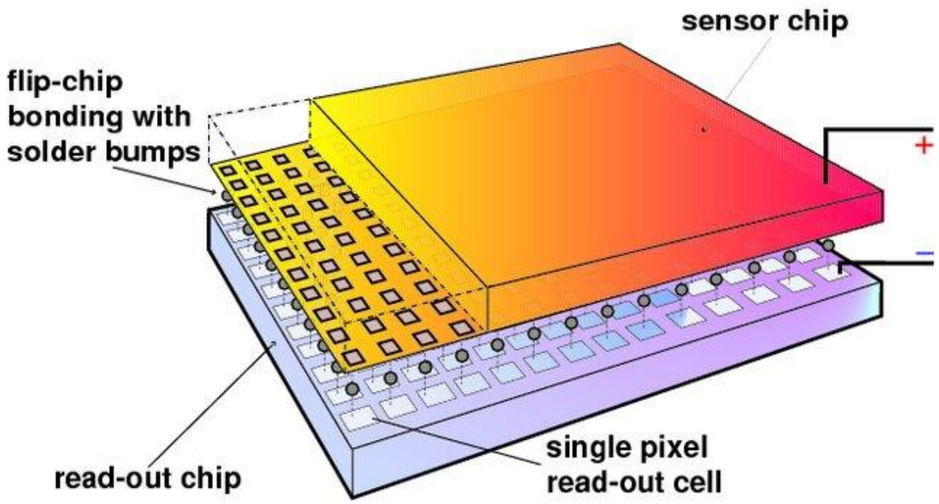




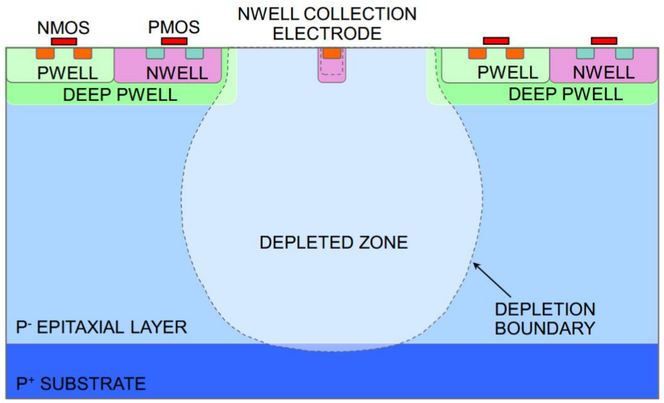




Hybrid Pixels and CMOS MAPS



https://repository.cern/records/yf32z-2ay79

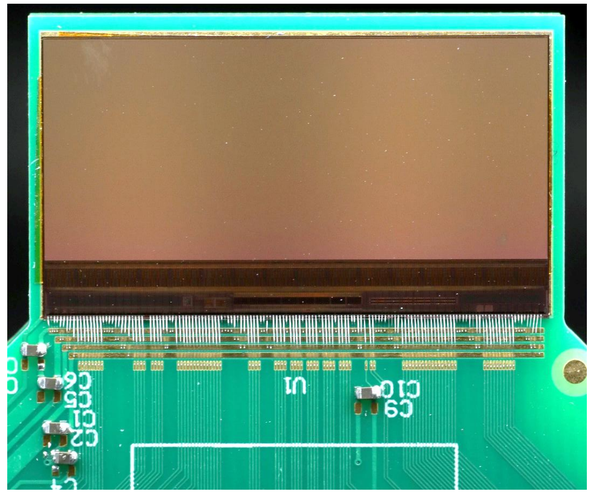


Trade-offs

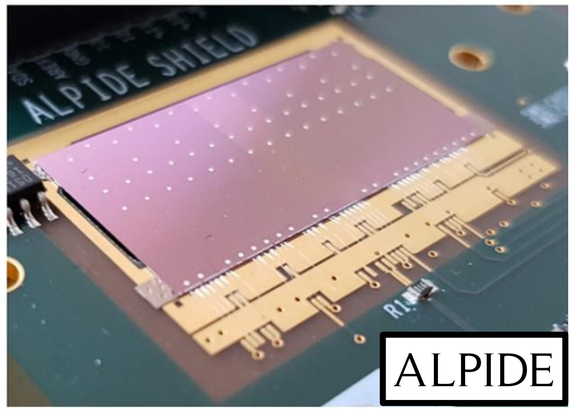
Radiation hardness
Material budget
Price
Power consumption
Speed and rate capability
Complexity
Granularity
Independence pixel/readout



https://cds.cern.ch/record/2723996/plots

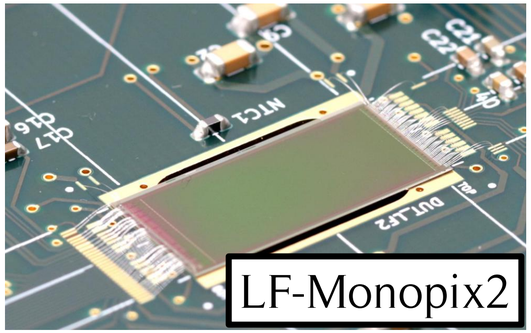


Selection of Recent MAPS Developments



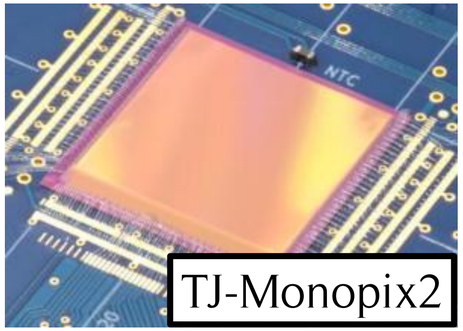
ALPIDE

https://ep-ese.web.cern.ch/project/alice-its



LF-Monopix2

https://indico.cern.ch/event/1422394/contributions/6012744/attachments/2881518/50484/26/CMOSverbund_Monopix2_LS.pdf



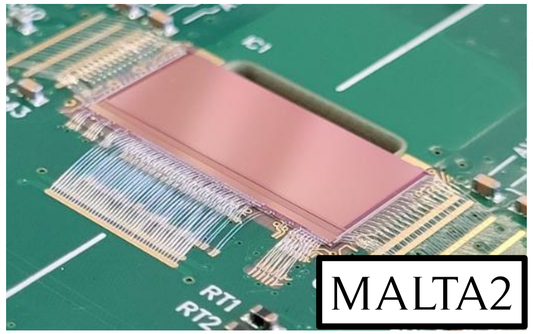
TJ-Monopix2

https://indico.cern.ch/event/1422394/contributions/6012744/attachments/2881518/50484/26/CMOSverbund_Monopix2_LS.pdf



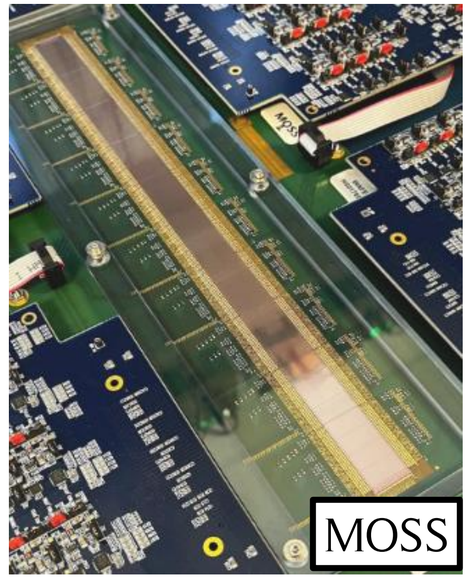
MuPix10

https://www.physi.uni-heidelberg.de/~schoning/HE/hvmaps/



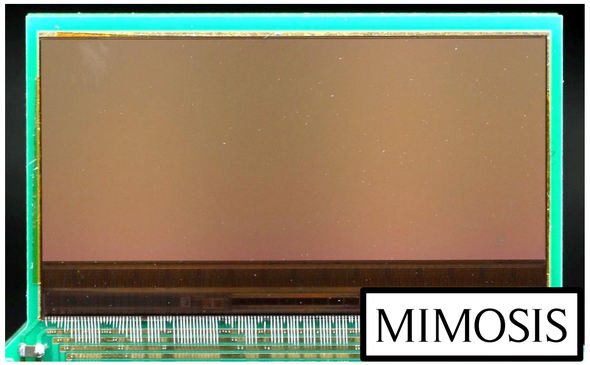
MALTA2

https://indico.ihep.ac.cn/event/17020/contributions/118942/attachments/64218/74957/CEPC_monolithic_W_Snoeys.pdf

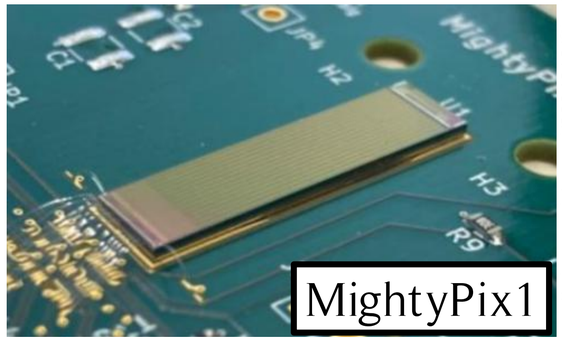


MOSS

https://indico.in2p3.fr/event/32425/contributions/142817/attachments/88980/134594/Characterization_of_MOSS_for_the_ALICE_ITS3_for_the_LHC_Run4.pdf



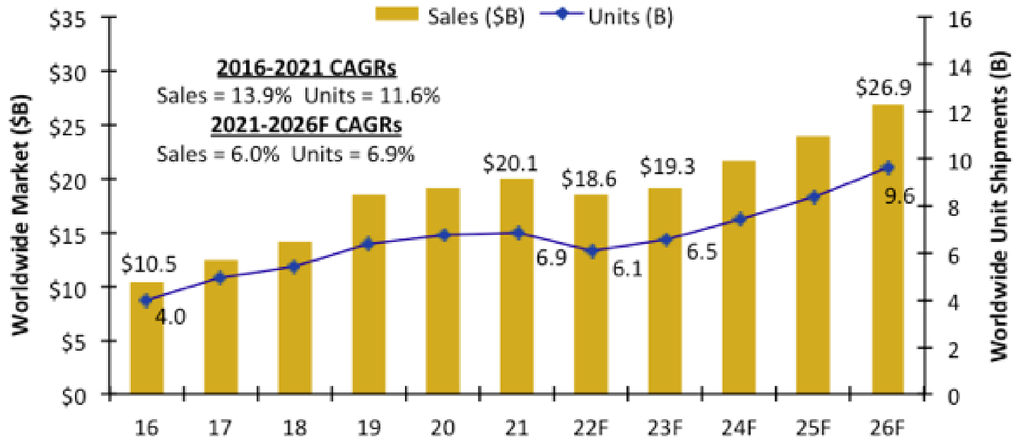
MIMOSIS



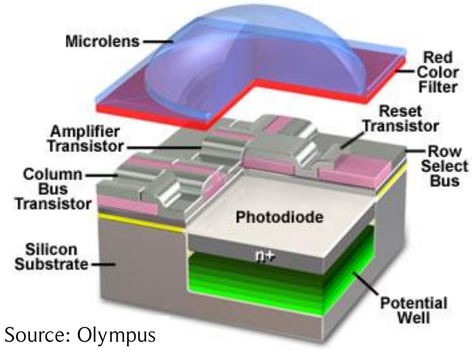
MightyPix1

https://cds.cern.ch/record/2924913/files/20220220_MightyTracker_Oscar_v3.pdf

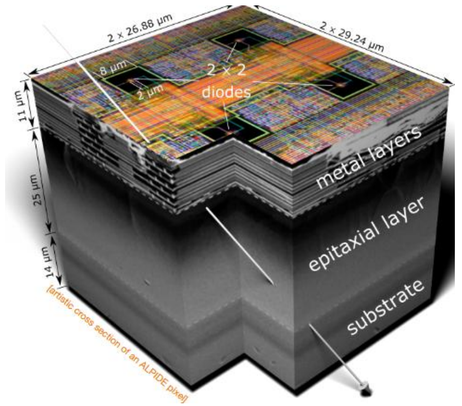
Beneficiaries from the Consumer Market



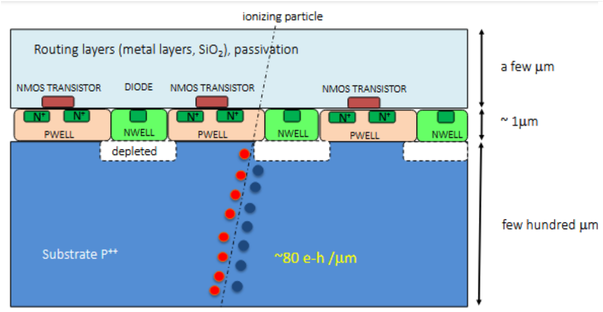
Source: IC Insights

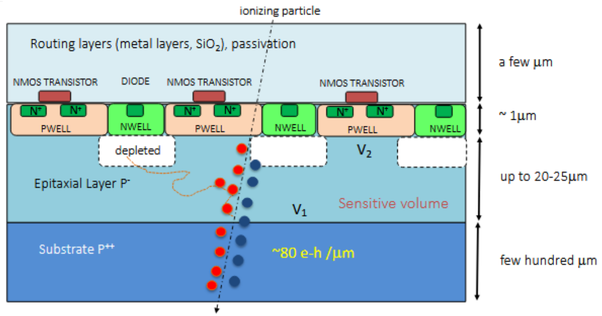


Source: Olympus



https://indico.cern.ch/event/1334113/contributions/6209778/attachments/3050762/5392236/2025-04-12_QM-static.pdf





https://indico.cern.ch/event/810687/contributions/3451968/attachments/1876305/3089703/belle_2019_musa.pdf

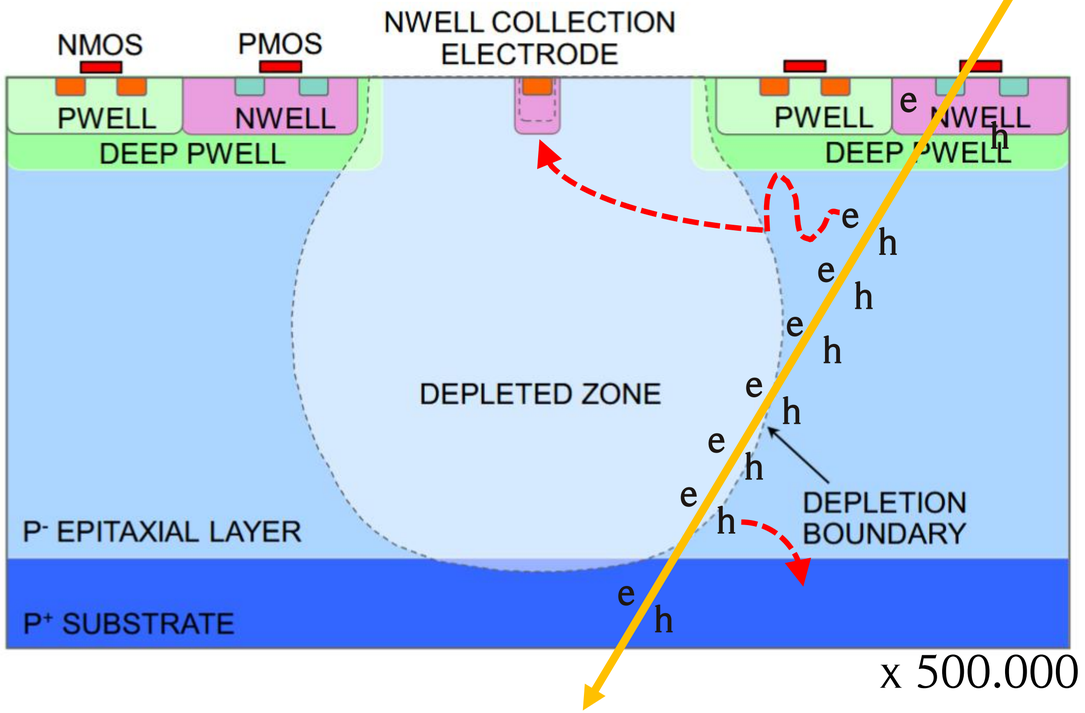
CMOS: 93% imaging sensors market share (2024)

→ Available and affordable tech, standardized tools

→ Modify optical designs for use in HEP

1. High resistivity epitaxial layer
   → Depletion, charge collection efficiency
   → 100% fill factor (no optical lense)
2. Quad-well technology
   → Full CMOS in pixel (deep-p wells)
   → Radiation hardness (p-stop, n-gap, … epi modifications)
3. Larger pixels
   → # channels, r/o speed, in-pixel logic (3T vs 100 T / pixel)
4. Sparsification (zero-suppression, on-chip clustering)
   → r/o speed, in-pixel analog and digital FE
5. Back-thinning
   → Reduced material budget

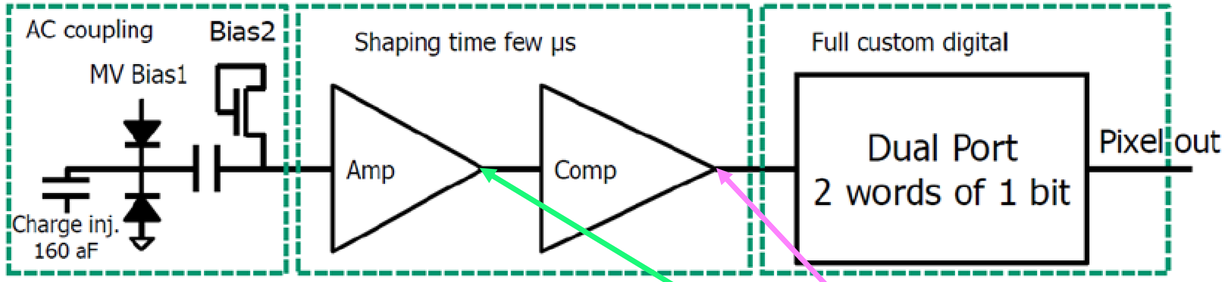
MAPS Working Principle

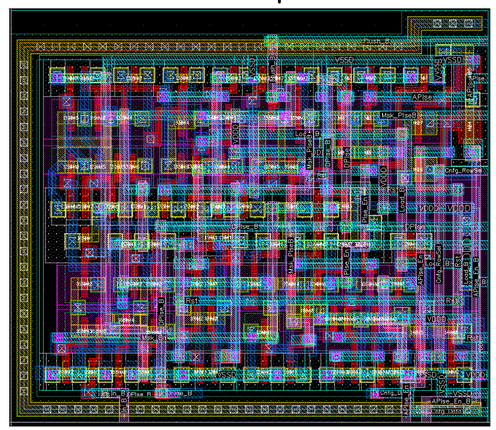


x 500.000

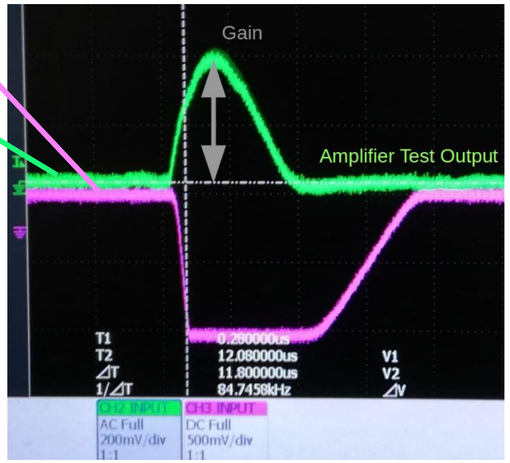
Electron-hole pairs from dE/dx
Diffusion & drift to collection diode
Induced current amplified & discriminated

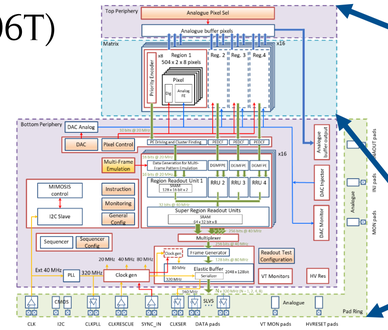
MIMOSIS: PE, buffers,
8x320 Mbit/s data output

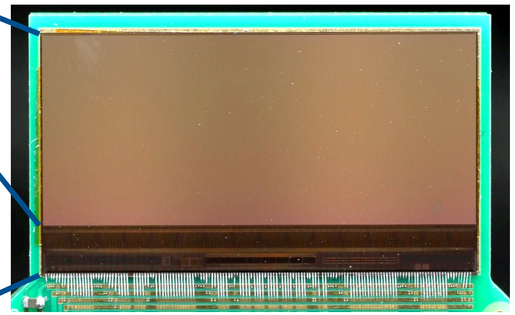




MIMOSIS Pixel Logic Layout (106T)





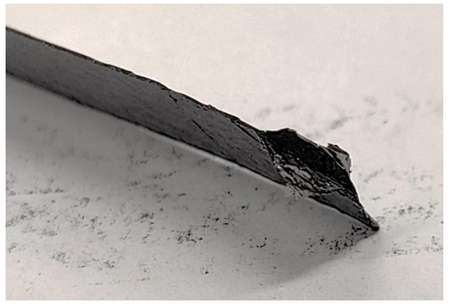


Laser Ablation of TPG

TPG is soft and delaminating

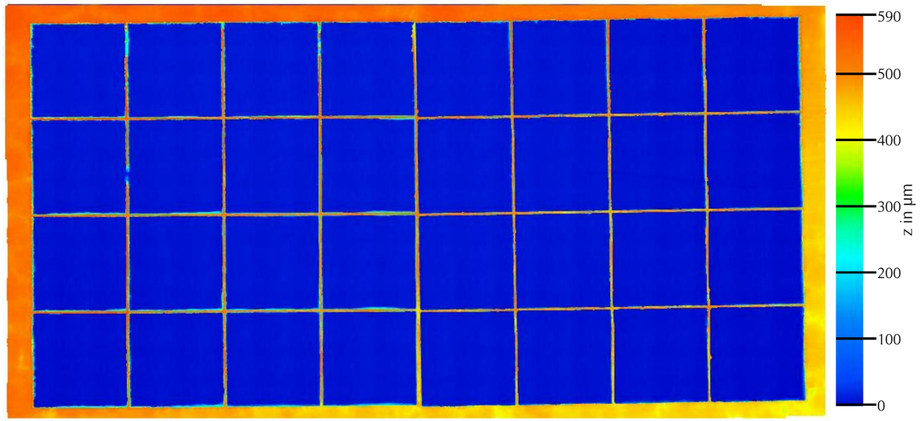
→ Mechanical machining difficult

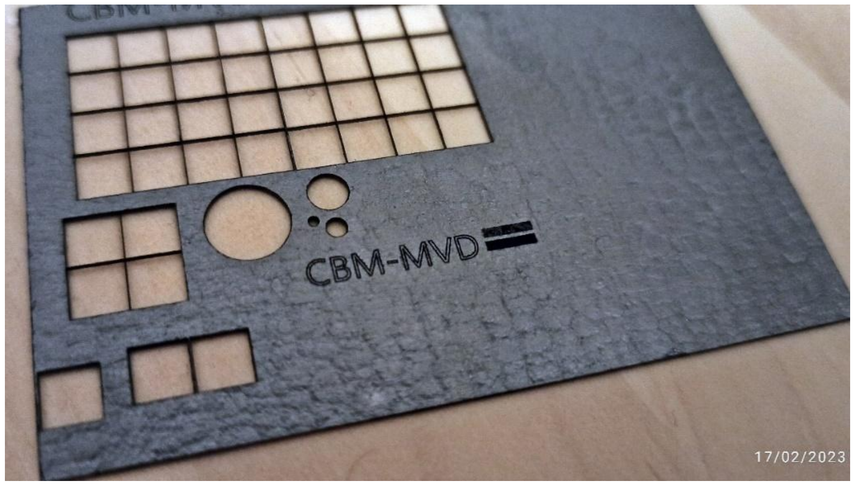
→ Laser ablation with LPKF CuttingMaster 2000

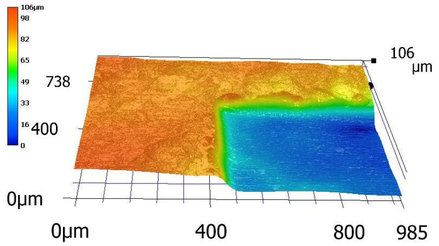




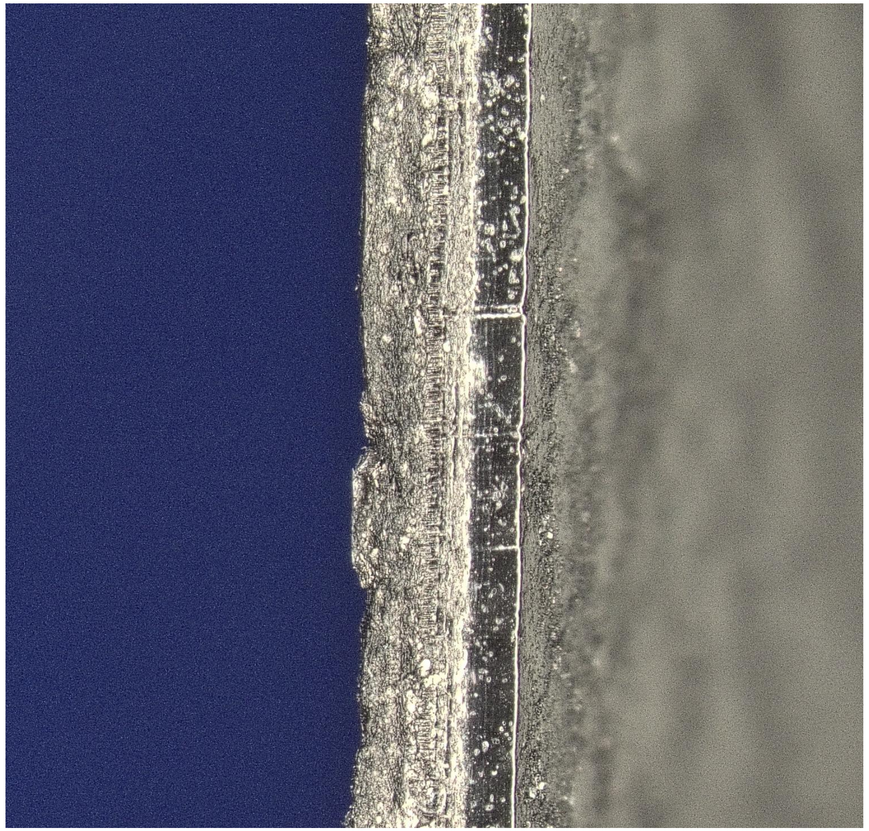
https://laser-depaneling.lpkf.com/de/products/lpkf-cuttingmaster-2000







Cross section 1mm TPG
Halfway laser cut (right),
halfway mechanically cut (left)



Mass Testing the MIMOSIS

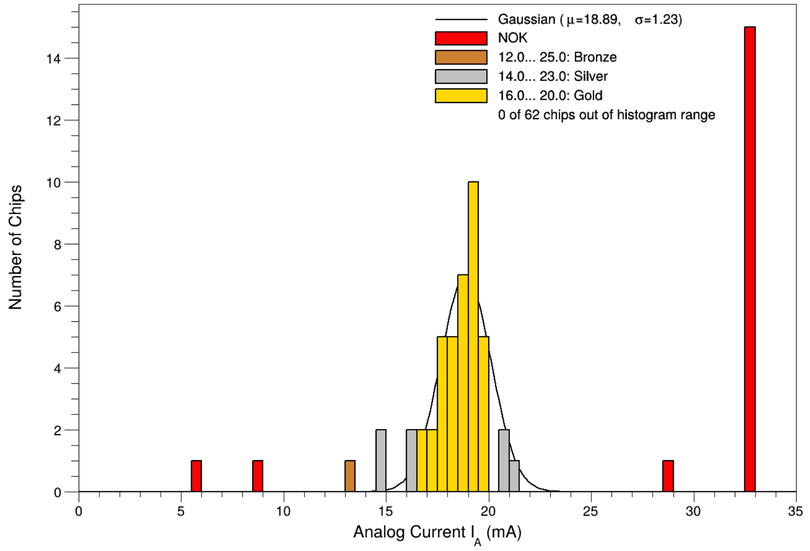
Probe tests: QA before integration

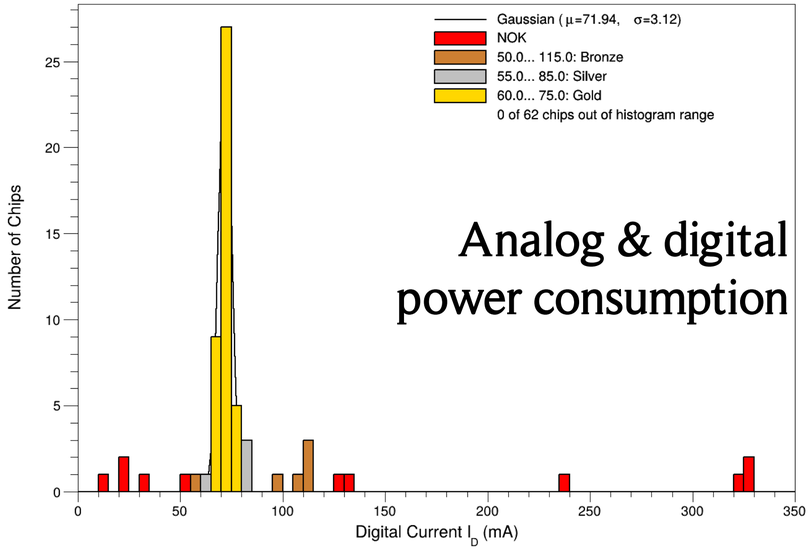
→ Thinned & diced sensors

→ 60 min per usable sensor (~2 min for unusable)

QA procedure established (ALPIDE-like)

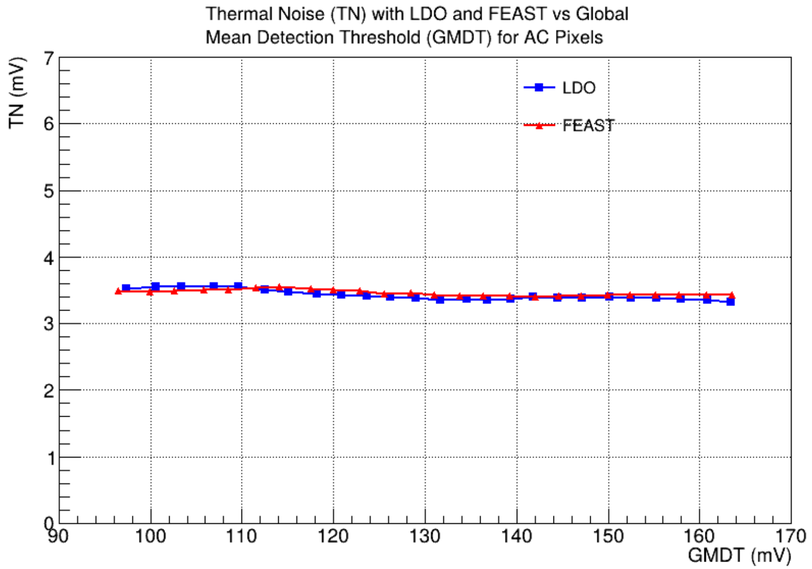
→ Yield of ~50% after thinning and dicing (based on ~60 sensors)





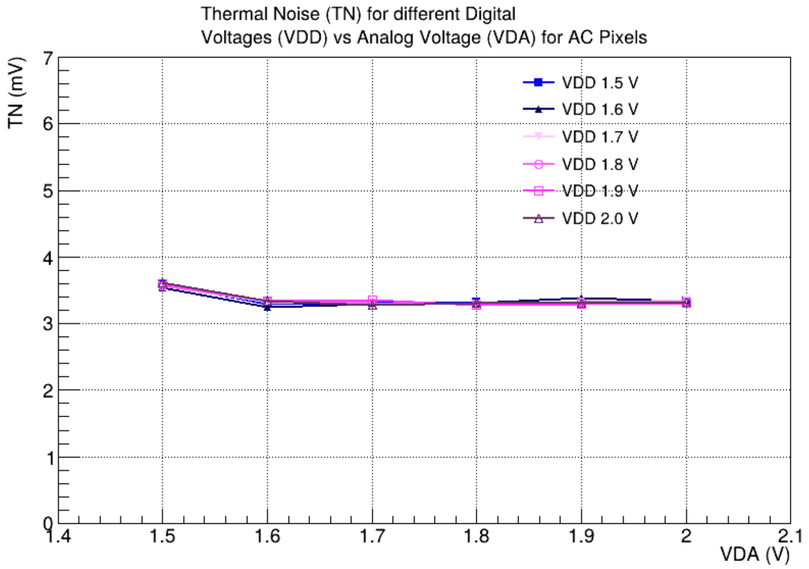


Thermal Noise – Operation Scenarios



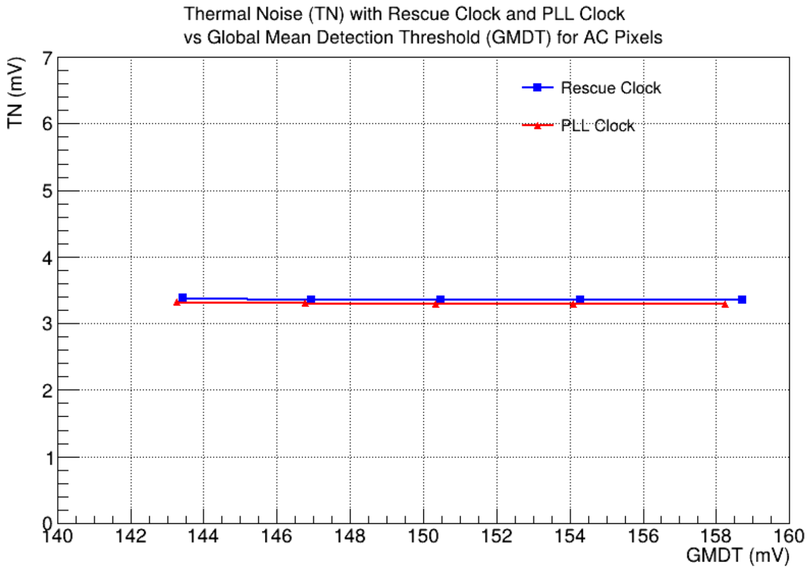
FEAST noise not picked up by sensor



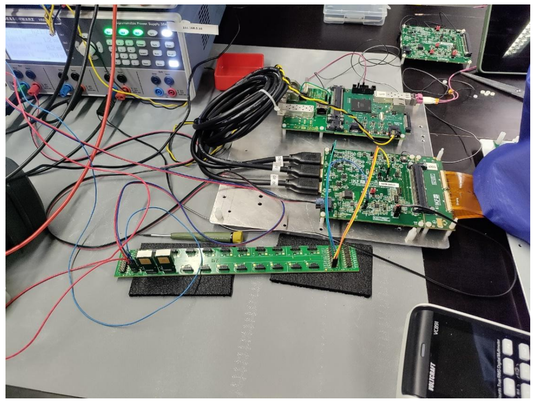


Stable over large operation voltage range

Cross powering not observed
Power supply failure scenarios tested
→ Fail-safety tested, implemented on FEB



No noise pick-up from fast clock

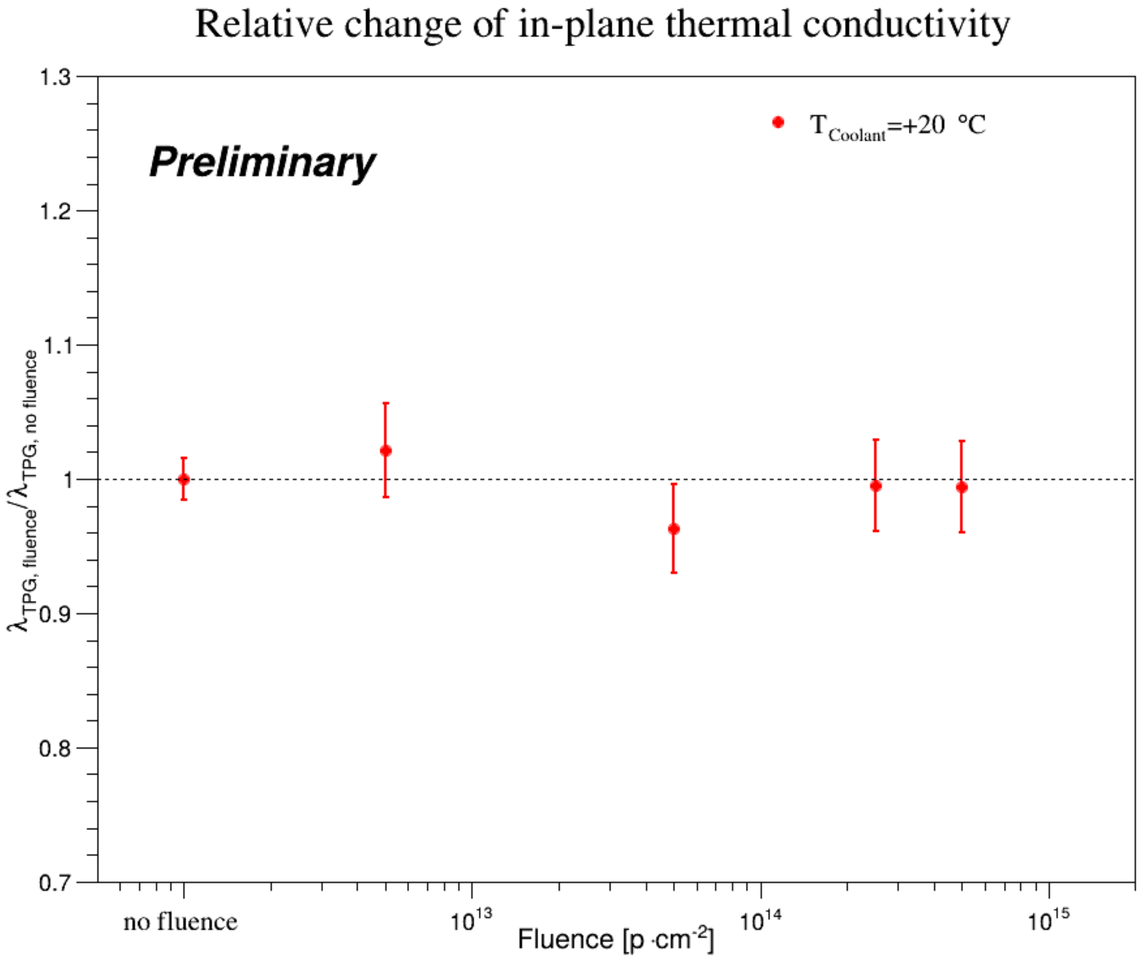


Degradation of TPG Thermal Conductivity

Measurement in collaboration with Belle II iVTX team

→ Irradiation of TPG at CYRCé (IPHC) w/ 25 MeV protons

No significant change of thermal conductivity at all coolant T



Absolute Thermal Conductivity

λ calculated from parameter a and TPG cross-sectional area

Consistent over all samples and measurements

→ Negative temperature coefficient

→ $\lambda(T) = (2084 \pm 3_{stat} \pm 260_{syst}) - (7.03 \pm 0.16_{stat} \pm 0.9_{syst}) \times T$ [W/m/K]

Global linear fit, symmetric min/max envelope

→ ATLAS: $\lambda(T) = 1870 - 7.5 \times T$ [W/m/K]

Value likely slightly overestimated

→ Here: (1940±260) W/m/K at room T

→ Vendor: 1500-1900 W/m/K at room T

→ Correction of thermal radiation from sample?

→ Coupling to supports (overestimate of heat entry)?

